Document Number: A2T07H310-24S
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RoHS

RF Power LDMOS Transistor

N-Channel Enhancement-Mode Lateral MOSFET

This 47 W asymmetrical Doherty RF power LDMOS transistor is designed for cellular base station applications covering the frequency range of 716 to 960 MHz.

870 MHz

- Typical Doherty Single-Carrier W-CDMA Performance: V_{DD} = 28 Vdc, I_{DQA} = 700 mA, V_{GSB} = 0.7 Vdc, P_{out} = 47 W Avg., Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF.

Frequency	G_{ps} (dB)	η_D (%)	Output PAR (dB)	ACPR (dBc)
851 MHz	18.9	50.5	7.7	–29.8
865 MHz	18.9	51.6	7.7	–30.1
880 MHz	18.6	51.3	7.7	–30.9

800 MHz

- Typical Doherty Single-Carrier W-CDMA Performance: V_{DD} = 28 Vdc, I_{DQA} = 700 mA, V_{GSB} = 0.7 Vdc, P_{out} = 47 W Avg., Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF.

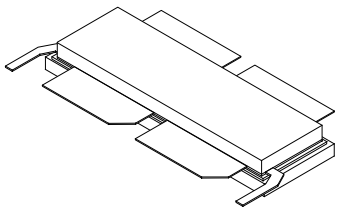
Frequency	G_{ps} (dB)	η_D (%)	Output PAR (dB)	ACPR (dBc)
790 MHz	19.5	50.7	7.7	–30.2
806 MHz	19.3	50.8	7.7	–31.2
822 MHz	18.9	50.5	7.7	–32.3

Features

- Advanced High Performance In-Package Doherty
- Greater Negative Gate-Source Voltage Range for Improved Class C Operation
- Designed for Digital Predistortion Error Correction Systems
- In Tape and Reel. R6 Suffix = 150 Units, 56 mm Tape Width, 13-inch Reel.

A2T07H310-24SR6

716–960 MHz, 47 W AVG., 28 V AIRFAST RF POWER LDMOS TRANSISTOR



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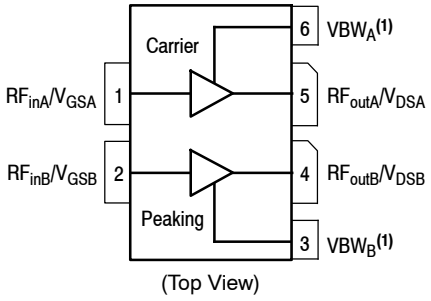


(Top View)

Figure 1. Pin Connections

1. Device cannot operate with the V_{DD} current supplied through pin 3 and pin 6.

freescale Airfast

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	–0.5, +70	Vdc
Gate-Source Voltage	V_{GS}	–6.0, +10	Vdc
Operating Voltage	V_{DD}	32, +0	Vdc
Storage Temperature Range	T_{stg}	–65 to +150	°C
Case Operating Temperature Range	T_C	–40 to +150	°C
Operating Junction Temperature Range (1,2)	T_J	–40 to +225	°C
CW Operation @ T_C = 25°C Derate above 25°C	CW	199 1.8	W W/°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value (2,3)	Unit
Thermal Resistance, Junction to Case Case Temperature 71°C, 47 W W-CDMA, 28 Vdc, I_{DQA} = 700 mA, V_{GSB} = 0.7 Vdc, 865 MHz	$R_{\theta JC}$	0.36	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22-A114)	2
Machine Model (per EIA/JESD22-A115)	B
Charge Device Model (per JESD22-C101)	IV

Table 4. Electrical Characteristics (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Off Characteristics (4)					
Zero Gate Voltage Drain Leakage Current (V_{DS} = 70 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 32 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	1	μAdc
Gate-Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
On Characteristics - Side A (4) (Carrier)					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 174 μAdc)	$V_{GS(th)}$	1.0	1.5	2.0	Vdc
Gate Quiescent Voltage (V_{DD} = 28 Vdc, I_{DA} = 700 mAdc, Measured in Functional Test)	$V_{GS(Q)}$	1.5	2.0	2.5	Vdc
Drain-Source On-Voltage (V_{GS} = 10 Vdc, I_D = 1.74 Adc)	$V_{DS(on)}$	0.1	0.2	0.3	Vdc
On Characteristics - Side B (4) (Peaking)					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 224 μAdc)	$V_{GS(th)}$	1.0	1.5	2.0	Vdc
Drain-Source On-Voltage (V_{GS} = 10 Vdc, I_D = 2.24 Adc)	$V_{DS(on)}$	0.05	0.1	0.3	Vdc

1. Continuous use at maximum temperature will affect MTTF.
2. MTTF calculator available at http://www.freescale.com/rf. Select Software & Tools/Development Tools/Calculators to access MTTF calculators by product.
3. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers.* Go to http://www.freescale.com/rf. Select Documentation/Application Notes - AN1955.
4. Each side of device measured separately.

(continued)

Table 4. Electrical Characteristics (T_A = 25°C unless otherwise noted) **(continued)**

Characteristic	Symbol	Min	Typ	Max	Unit
Functional Tests (1,2) (In Freescale Doherty Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQA} = 700 mA, V_{GSB} = 0.7 Vdc, P_{out} = 47 W Avg., f = 880 MHz, Single-Carrier W-CDMA, IQ Magnitude Clipping, Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @ ±5 MHz Offset.					
Power Gain	G_{ps}	17.7	18.6	20.7	dB
Drain Efficiency	η_D	48.0	51.3	—	%
Output Peak-to-Average Ratio @ 0.01% Probability on CCDF	PAR	7.2	7.7	—	dB
Adjacent Channel Power Ratio	ACPR	—	–30.9	–26.9	dBc
Load Mismatch (2) (In Freescale Doherty Test Fixture, 50 ohm system) I_{DQA} = 700 mA, V_{GSB} = 0.7 Vdc, f = 865 MHz					
VSWR 10:1 at 32 Vdc, 316 W CW (4) Output Power (3 dB Input Overdrive from 126 W CW Rated Power)	No Device Degradation				
Typical Performance (2) (In Freescale Doherty Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQA} = 700 mA, V_{GSB} = 0.7 Vdc, 851–880 MHz Bandwidth					
P_{out} @ 1 dB Compression Point, CW	P1dB	—	126	—	W
P_{out} @ 3 dB Compression Point (3)	P3dB	—	330	—	W
AM/PM (Maximum value measured at the P3dB compression point across the 851–880 MHz frequency range)	Φ	—	–21	—	°
VBW Resonance Point (IMD Third Order Intermodulation Inflection Point)	VBW_{res}	—	180	—	MHz
Gain Flatness in 29 MHz Bandwidth @ P_{out} = 47 W Avg.	G_F	—	0.4	—	dB
Gain Variation over Temperature (–30°C to +85°C)	ΔG	—	0.01	—	dB/°C
Output Power Variation over Temperature (–30°C to +85°C) (4)	ΔP1dB	—	0.2	—	dB/°C

1. Part internally matched both on input and output.
2. Measurement made with device in an asymmetrical Doherty configuration.
3. P3dB = P_{avg} + 7.0 dB where P_{avg} is the average output power measured using an unclipped W-CDMA single-carrier input signal where output PAR is compressed to 7.0 dB @ 0.01% probability on CCDF.
4. Exceeds recommended operating conditions. See CW operation data in Maximum Ratings table.

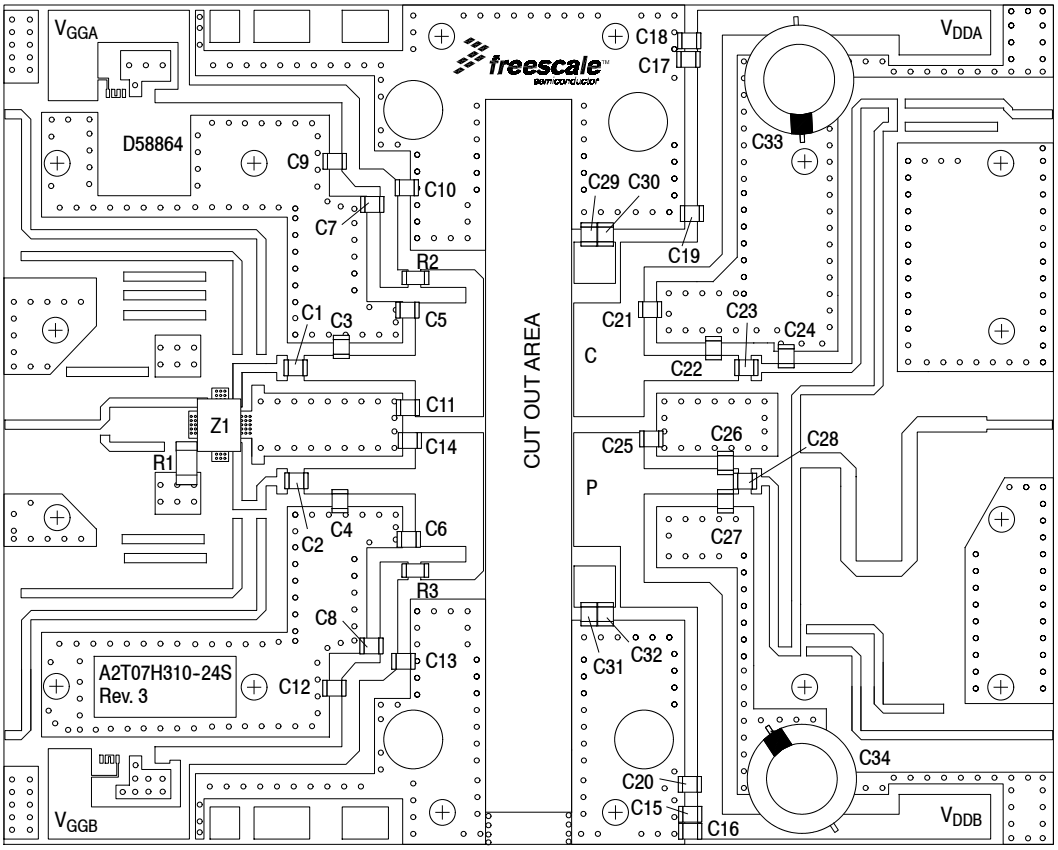


Figure 2. A2T07H310-24SR6 Test Circuit Component Layout — 851–880 MHz

Table 5. A2T07H310-24SR6 Test Circuit Component Designations and Values — 851–880 MHz

Part	Description	Part Number	Manufacturer
C1, C2, C7, C8, C19, C20, C23, C28	43 pF Chip Capacitors	ATC100B430JT500XT	ATC
C3, C4, C5, C6, C21, C22, C25	6.8 pF Chip Capacitors	ATC100B6R8CT500XT	ATC
C9, C10, C12, C13	10 μF Chip Capacitors	GRM31CR61H106KA12	Muruta
C11, C14, C26	5.6 pF Chip Capacitors	ATC100B5R6CT500XT	ATC
C15, C16, C17, C18, C29, C30, C31, C32	10 μF Chip Capacitors	C5750X7S2A106M230KB	TDK
C24	2.7 pF Chip Capacitor	ATC100B2R7BT500XT	ATC
C27	4.7 pF Chip Capacitor	ATC100B4R7CT500XT	ATC
C33, C34	330 μF Electrolytic Capacitors	MCRH63V337M13X21–RH	Multicomp
R1	50 Ω, 10 W Termination	81A7031–50–5F	Florida RF Labs
R2, R3	2.2 Ω, 1/4 W Chip Resistors	CRCW12062R20JNEA	Vishay
Z1	800–1000 MHz Band, 90°, 3 dB Hybrid Coupler	X3C09P1–03S	Anaren
PCB	Rogers RO4350B, 0.020″, ε_r = 3.66	D58864	MTL

TYPICAL CHARACTERISTICS — 851–880 MHz

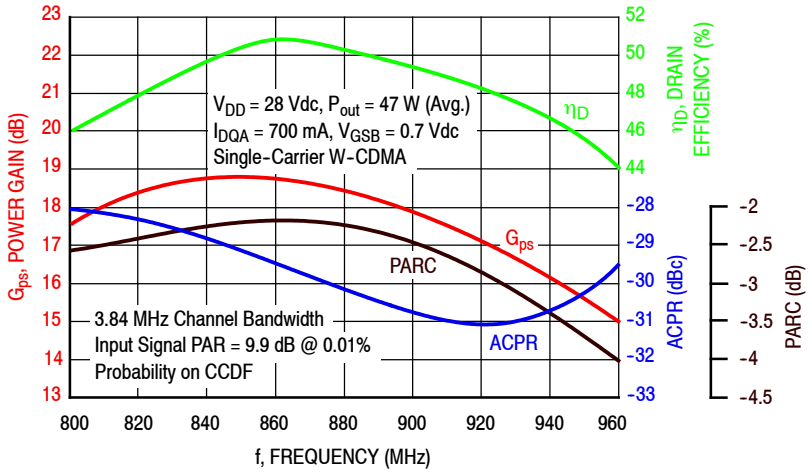


Figure 3. Single-Carrier Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @ P_{out} = 47 Watts Avg.

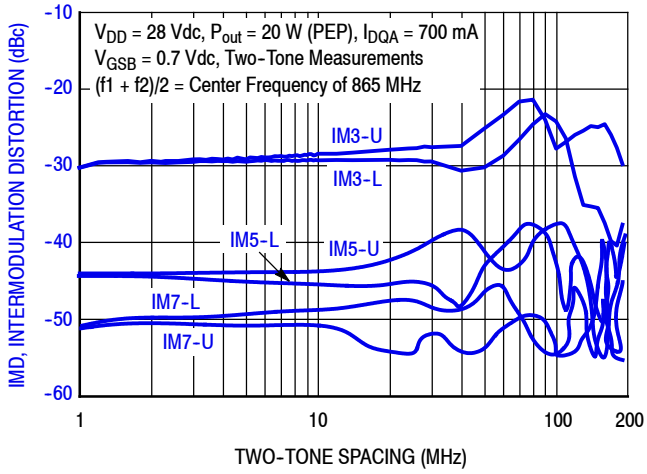


Figure 4. Intermodulation Distortion Products versus Two-Tone Spacing

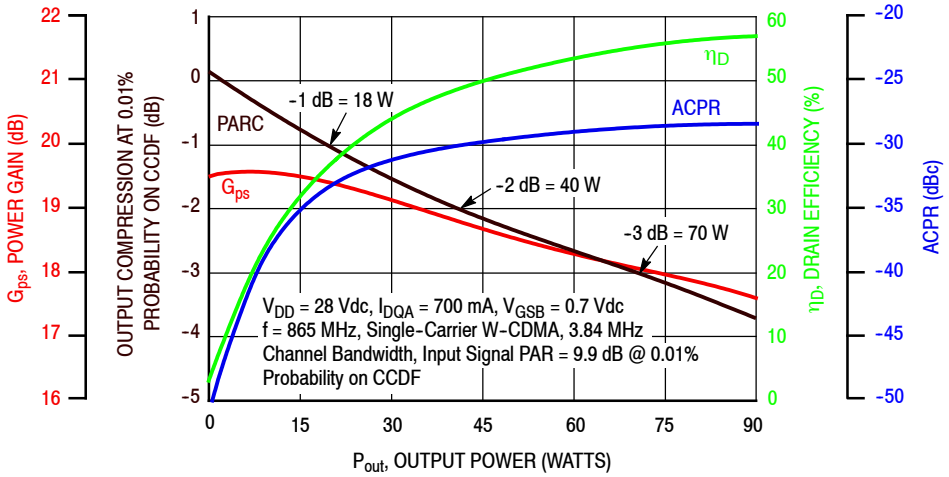


Figure 5. Output Peak-to-Average Ratio Compression (PARC) versus Output Power

TYPICAL CHARACTERISTICS — 851–880 MHz

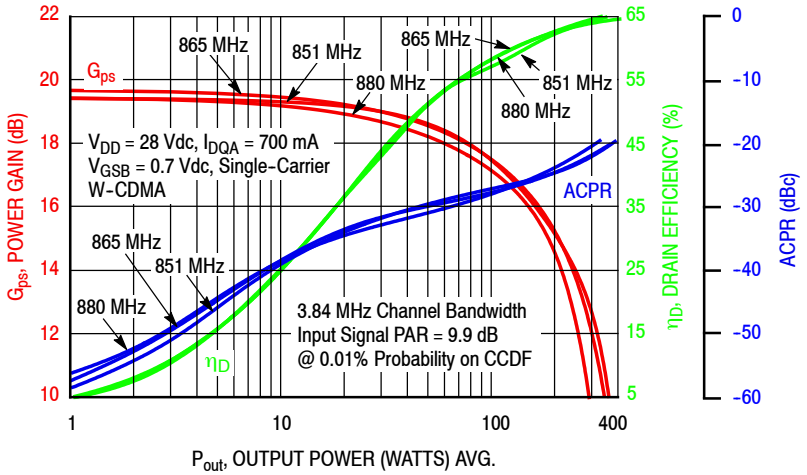


Figure 6. Single-Carrier W-CDMA Power Gain, Drain Efficiency and ACPR versus Output Power

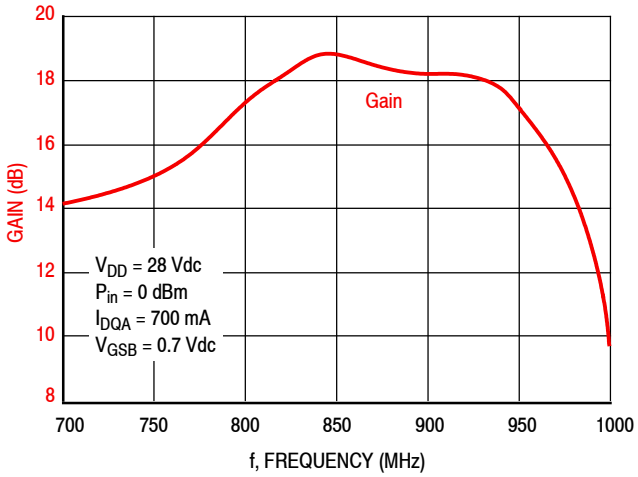


Figure 7. Broadband Frequency Response

Table 6. Carrier Side Load Pull Performance — Maximum Power Tuning

V_{DD} = 28 Vdc, I_{DQA} = 661 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Output Power P1dB Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
851	1.12 – j2.70	1.13 + j2.77	1.30 – j2.73	19.7	53.1	204	56.2	–8
865	1.16 – j2.79	1.21 + j2.89	1.24 – j2.80	19.5	53.2	210	56.8	–8
880	1.16 – j2.89	1.30 + j3.03	1.19 – j2.87	19.3	53.3	215	57.4	–8

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Output Power P3dB Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
851	1.12 – j2.70	1.12 + j2.86	1.29 – j3.01	17.5	54.1	258	59.8	–11
865	1.16 – j2.79	1.20 + j2.98	1.22 – j3.06	17.3	54.2	263	59.2	–11
880	1.16 – j2.89	1.29 + j3.11	1.12 – j3.12	16.9	54.3	268	58.6	–12

(1) Load impedance for optimum P1dB power.
(2) Load impedance for optimum P3dB power.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

Table 7. Carrier Side Load Pull Performance — Maximum Drain Efficiency Tuning

V_{DD} = 28 Vdc, I_{DQA} = 661 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Drain Efficiency P1dB Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
851	1.12 – j2.70	1.08 + j2.78	3.72 – j0.98	23.1	50.5	113	73.7	–16
865	1.16 – j2.79	1.16 + j2.91	3.74 – j0.62	23.2	50.1	101	74.2	–19
880	1.16 – j2.89	1.24 + j3.02	3.23 – j1.04	22.8	50.4	110	72.8	–18

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Drain Efficiency P3dB Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
851	1.12 – j2.70	1.09 + j2.86	4.40 – j1.30	21.3	50.9	124	75.8	–23
865	1.16 – j2.79	1.17 + j2.97	3.50 – j1.76	20.7	51.7	147	76.1	–21
880	1.16 – j2.89	1.25 + j3.10	3.36 – j1.39	20.7	51.3	135	75.8	–24

(1) Load impedance for optimum P1dB efficiency.
(2) Load impedance for optimum P3dB efficiency.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

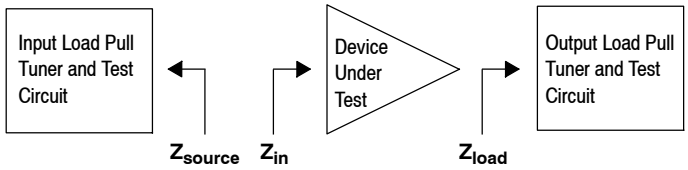


Table 8. Peaking Side Load Pull Performance — Maximum Power Tuning

V_{DD} = 28 Vdc, V_{GSB} = 0.7 Vdc, Pulsed CW, 10 μsec(on), 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Output Power P1dB Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
851	1.12 – j2.70	1.29 + j2.85	0.92 – j3.03	15.1	53.7	237	53.2	–15
865	1.16 – j2.79	1.38 + j2.99	0.94 – j3.06	15.2	53.9	245	55.4	–15
880	1.16 – j2.89	1.48 + j3.15	0.88 – j3.16	14.9	54.0	251	55.0	–15

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Output Power P3dB Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
851	1.12 – j2.70	1.28 + j2.95	0.92 – j3.10	13.0	54.8	302	56.8	–19
865	1.16 – j2.79	1.38 + j3.10	0.90 – j3.25	12.8	54.9	310	57.4	–18
880	1.16 – j2.89	1.48 + j3.26	0.88 – j3.26	12.8	55.1	320	58.9	–19

(1) Load impedance for optimum P1dB power.
(2) Load impedance for optimum P3dB power.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

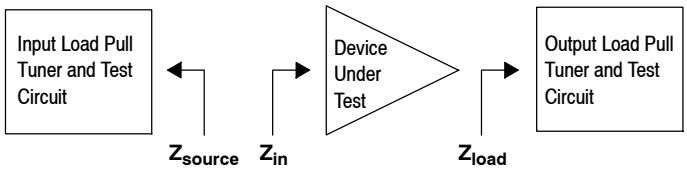
Table 9. Peaking Side Load Pull Performance — Maximum Drain Efficiency Tuning

V_{DD} = 28 Vdc, V_{GSB} = 0.7 Vdc, Pulsed CW, 10 μsec(on), 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Drain Efficiency P1dB Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
851	1.12 – j2.70	1.19 + j2.73	2.88 – j1.01	16.7	50.7	117	76.2	–26
865	1.16 – j2.79	1.28 + j2.87	2.60 – j1.20	16.6	50.8	121	76.0	–25
880	1.16 – j2.89	1.35 + j3.01	2.49 – j0.76	16.2	50.0	100	76.0	–29

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Drain Efficiency P3dB Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
851	1.12 – j2.70	1.20 + j2.84	3.23 – j1.20	14.6	51.3	134	77.1	–32
865	1.16 – j2.79	1.30 + j3.01	2.60 – j1.80	14.6	52.1	162	76.6	–29
880	1.16 – j2.89	1.41 + j3.18	2.28 – j2.21	14.4	52.6	183	77.0	–28

(1) Load impedance for optimum P1dB efficiency.
(2) Load impedance for optimum P3dB efficiency.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.



P1dB - TYPICAL CARRIER SIDE LOAD PULL CONTOURS — 865 MHz

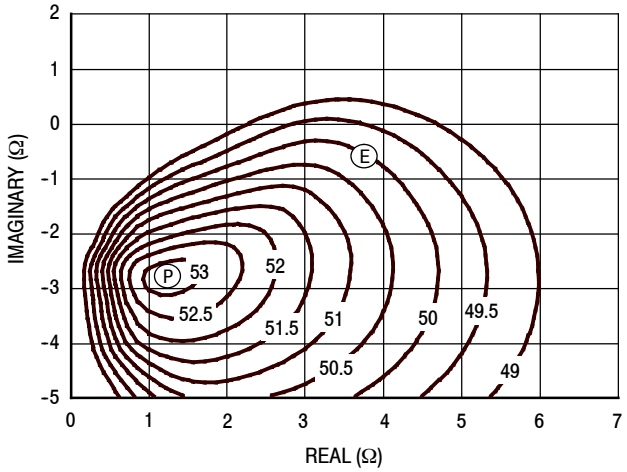


Figure 8. P1dB Load Pull Output Power Contours (dBm)

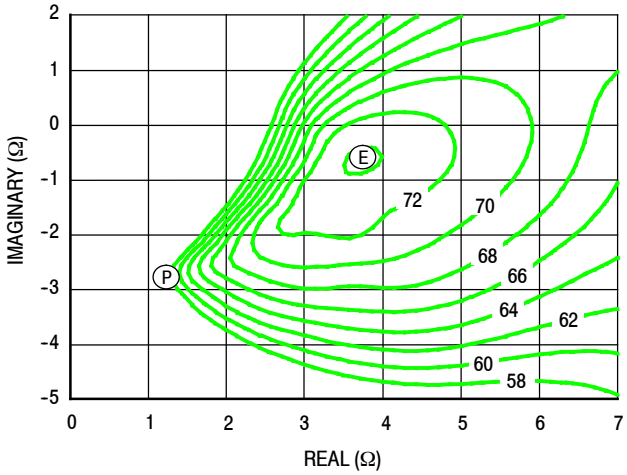


Figure 9. P1dB Load Pull Efficiency Contours (%)

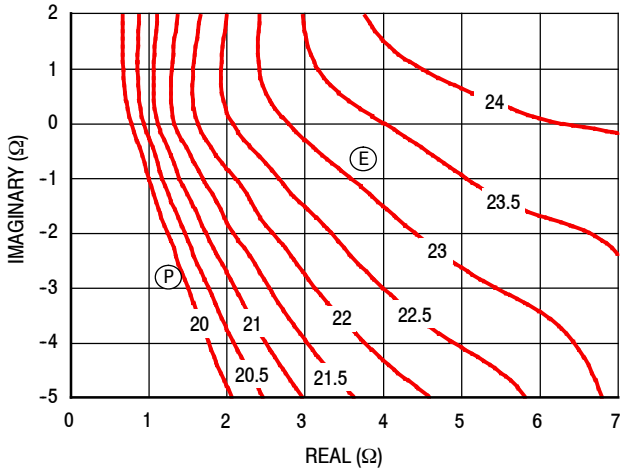


Figure 10. P1dB Load Pull Gain Contours (dB)

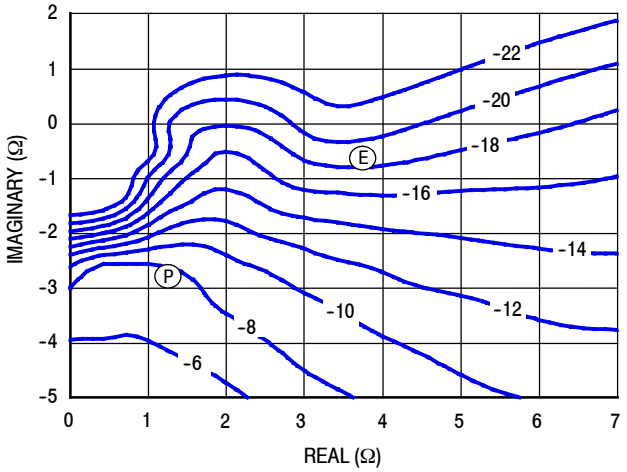


Figure 11. P1dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power

Ⓔ = Maximum Drain Efficiency

Gain

Drain Efficiency

Linearity

Output Power

P3dB - TYPICAL CARRIER SIDE LOAD PULL CONTOURS — 865 MHz

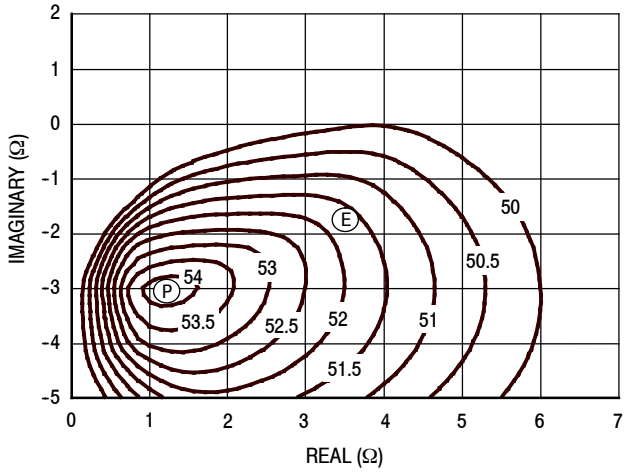


Figure 13. P3dB Load Pull Output Power Contours (dBm)

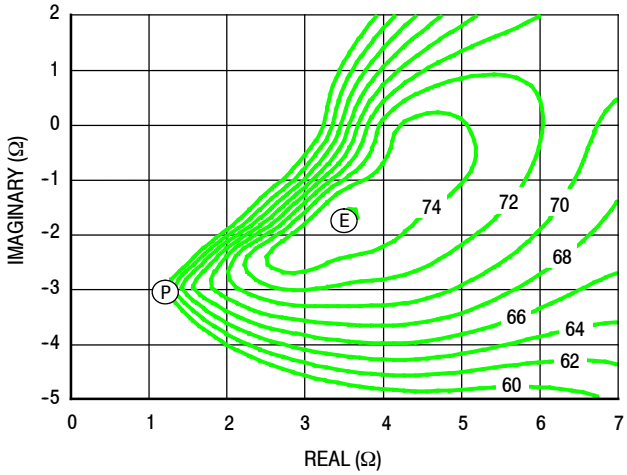


Figure 14. P3dB Load Pull Efficiency Contours (%)

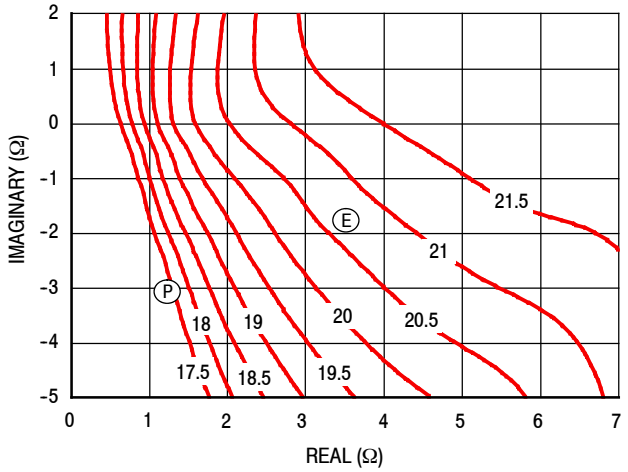


Figure 15. P3dB Load Pull Gain Contours (dB)

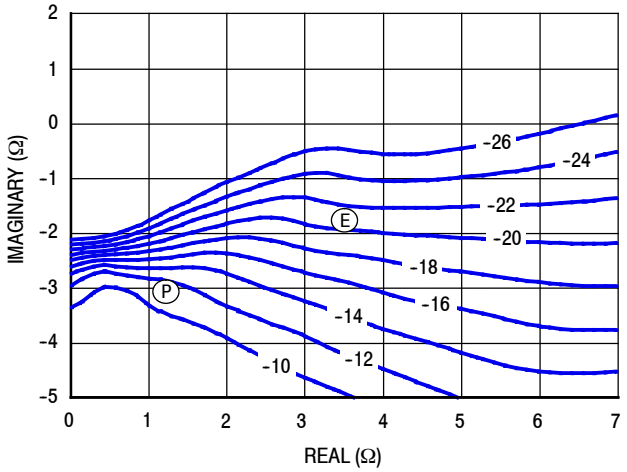


Figure 12. P3dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power

Ⓔ = Maximum Drain Efficiency

Gain

Drain Efficiency

Linearity

Output Power

P1dB - TYPICAL PEAKING SIDE LOAD PULL CONTOURS — 865 MHz

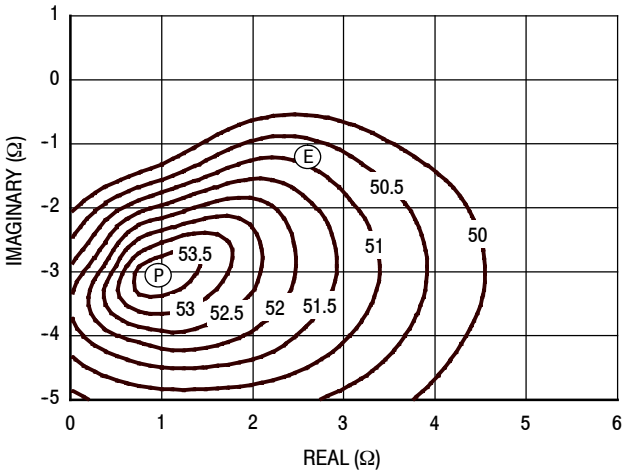


Figure 16. P1dB Load Pull Output Power Contours (dBm)

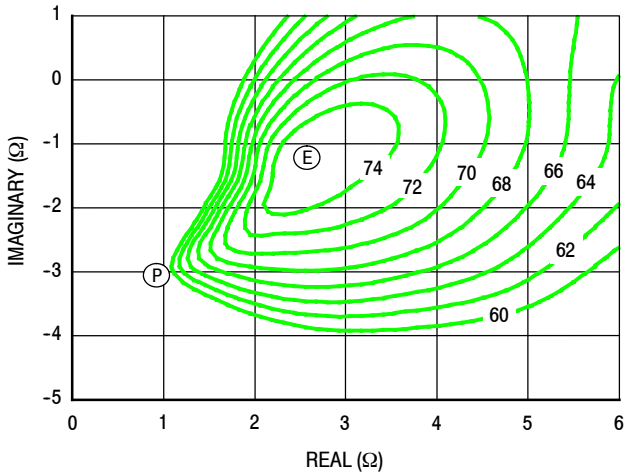


Figure 17. P1dB Load Pull Efficiency Contours (%)

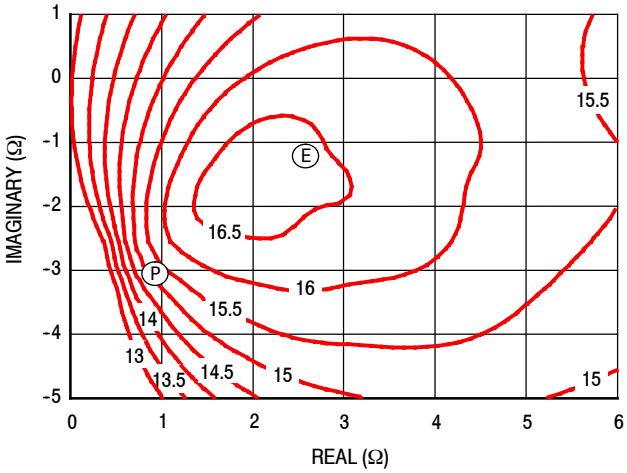


Figure 18. P1dB Load Pull Gain Contours (dB)

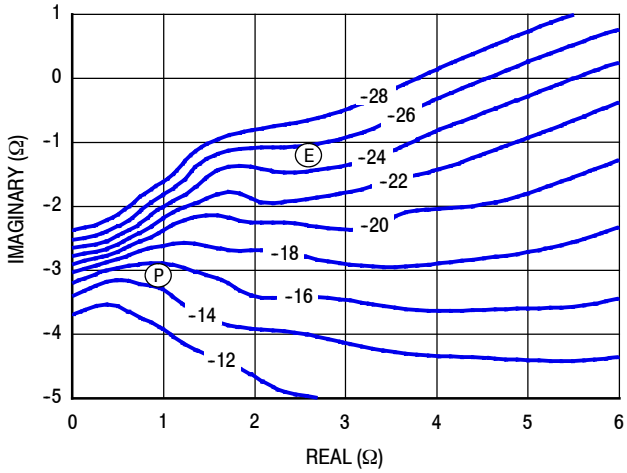


Figure 19. P1dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power

Ⓔ = Maximum Drain Efficiency

Gain

Drain Efficiency

Linearity

Output Power

P3dB - TYPICAL PEAKING SIDE LOAD PULL CONTOURS — 865 MHz

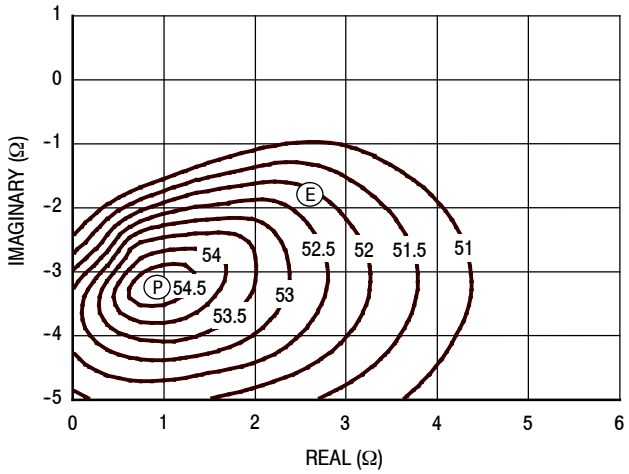


Figure 20. P3dB Load Pull Output Power Contours (dBm)

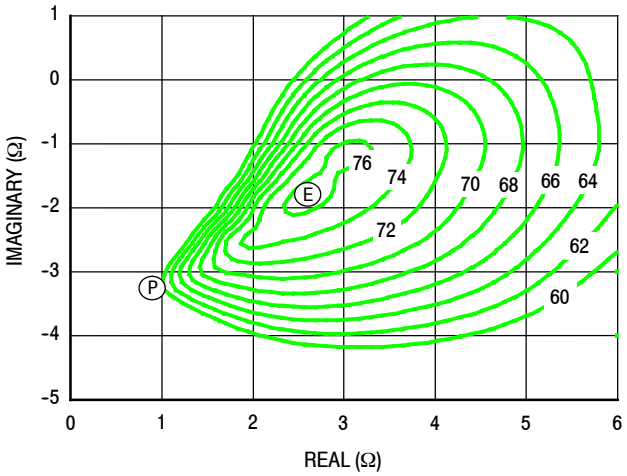


Figure 21. P3dB Load Pull Efficiency Contours (%)

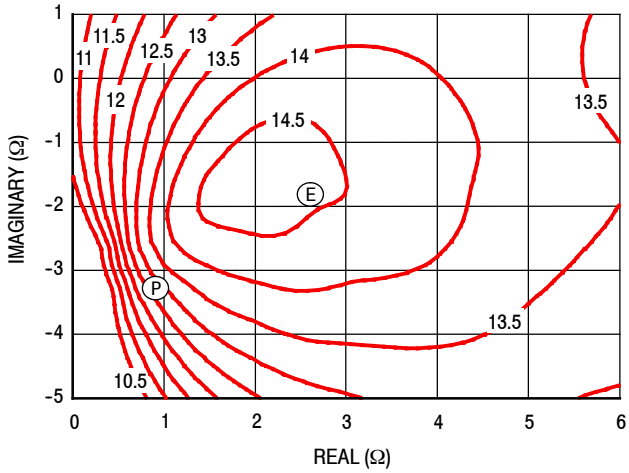


Figure 22. P3dB Load Pull Gain Contours (dB)

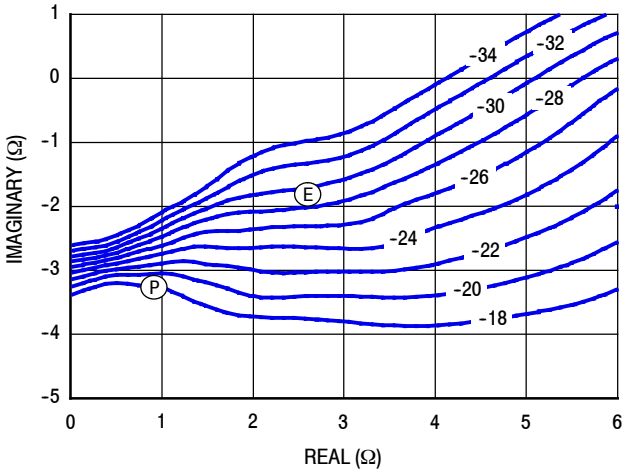


Figure 23. P3dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power

Ⓔ = Maximum Drain Efficiency

Gain

Drain Efficiency

Linearity

Output Power

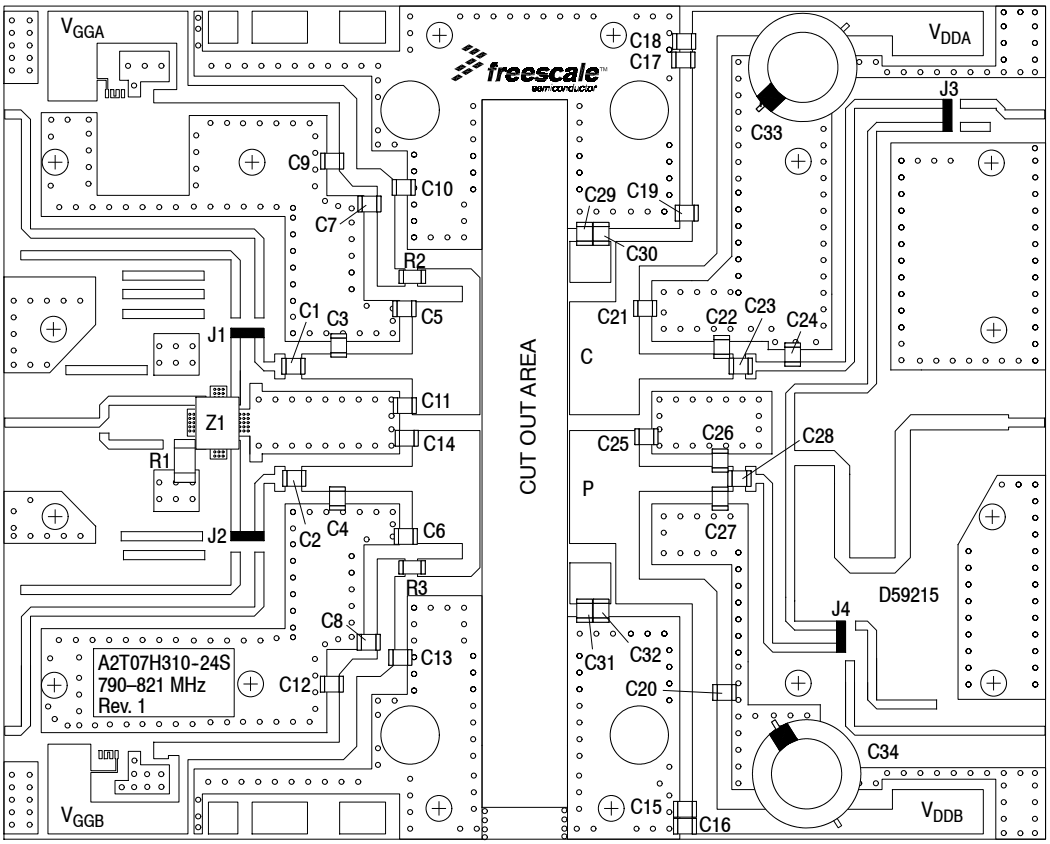


Figure 24. A2T07H310-24SR6 Test Circuit Component Layout — 790–822 MHz

Table 10. A2T07H310-24SR6 Test Circuit Component Designations and Values — 790–822 MHz

Part	Description	Part Number	Manufacturer
C1, C2, C7, C8, C19, C20, C23, C28	43 pF Chip Capacitors	ATC100B430JT500XT	ATC
C3, C4, C5, C6, C21, C22, C25	9.1 pF Chip Capacitors	ATC100B9R1CT500XT	ATC
C9, C10, C12, C13	10 μF Chip Capacitors	GRM31CR61H106KA12	Muruta
C11, C14	7.5 pF Chip Capacitors	ATC100B7R5CT500XT	ATC
C15, C16, C17, C18, C29, C30, C31, C32	10 μF Chip Capacitors	C5750X7S2A106M230KB	TDK
C24	2.7 pF Chip Capacitor	ATC100B2R7BT500XT	ATC
C26	6.8 pF Chip Capacitor	ATC100B6R8CT500XT	ATC
C27	4.7 pF Chip Capacitor	ATC100B4R7CT500XT	ATC
C33, C34	330 μF Electrolytic Capacitors	MCRH63V337M13X21–RH	Multicomp
J1, J2, J3, J4	Copper Foil		
R1	50 Ω, 10 W Termination	81A7031–50–5F	Florida RF Labs
R2, R3	2.2 Ω, 1/4 W Chip Resistors	CRCW12062R20JNEA	Vishay
Z1	800–1000 MHz Band, 90°, 3 dB Hybrid Coupler	X3C09P1–03S	Anaren
PCB	Rogers RO4350B, 0.020″, ε_r = 3.66	D59215	MTL

TYPICAL CHARACTERISTICS — 790–822 MHz

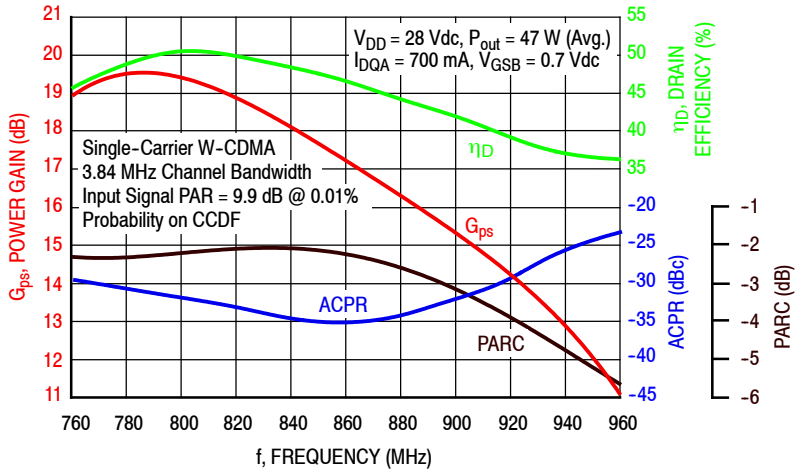


Figure 25. Single-Carrier Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @ P_{out} = 47 Watts Avg.

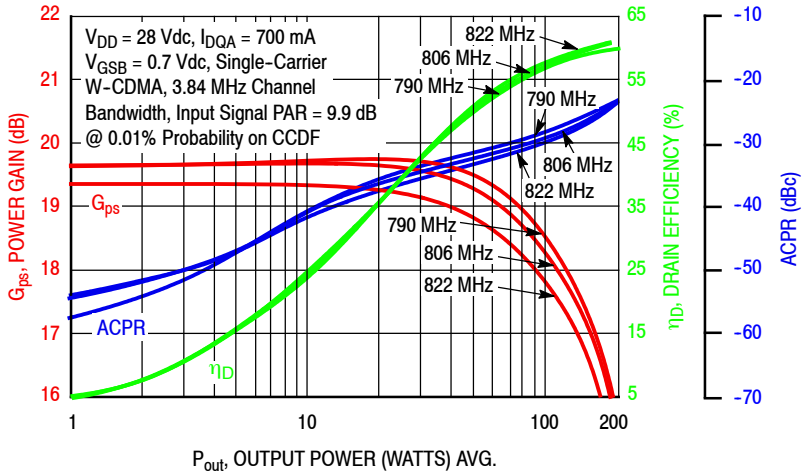


Figure 26. Single-Carrier W-CDMA Power Gain, Drain Efficiency and ACPR versus Output Power

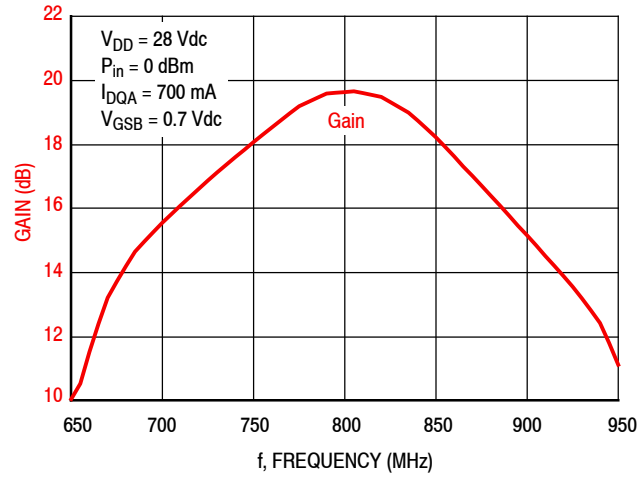


Figure 27. Broadband Frequency Response

Table 11. Carrier Side Load Pull Performance — Maximum Power Tuning

V_{DD} = 28 Vdc, I_{DQA} = 680 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Output Power P1dB Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
790	0.96 – j2.26	0.93 + j2.40	1.46 – j2.24	20.4	52.8	192	54.3	–9
806	0.95 – j2.37	0.97 + j2.49	1.43 – j2.35	20.2	52.3	171	50.8	–9
822	1.07 – j2.57	1.02 + j2.60	1.42 – j2.59	19.9	52.3	168	50.3	–8

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Output Power P3dB Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
790	0.96 – j2.26	0.90 + j2.48	1.32 – j2.47	18.0	53.8	240	55.5	–12
806	0.95 – j2.37	0.95 + j2.57	1.30 – j2.74	17.7	53.4	218	52.6	–13
822	1.07 – j2.57	1.00 + j2.68	1.36 – j2.90	17.7	53.4	220	53.9	–11

(1) Load impedance for optimum P1dB power.
(2) Load impedance for optimum P3dB power.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

Table 12. Carrier Side Load Pull Performance — Maximum Drain Efficiency Tuning

V_{DD} = 28 Vdc, I_{DQA} = 680 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Drain Efficiency P1dB Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
790	0.96 – j2.26	0.88 + j2.41	4.00 – j0.94	23.4	50.6	114	67.8	–17
806	0.95 – j2.37	0.93 + j2.49	3.65 – j1.48	23.0	50.5	111	63.5	–14
822	1.07 – j2.57	0.99 + j2.61	4.49 – j1.29	23.2	49.9	99	65.5	–13

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Drain Efficiency P3dB Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
790	0.96 – j2.26	0.87 + j2.49	4.15 – j1.31	21.4	51.3	135	70.7	–23
806	0.95 – j2.37	0.92 + j2.57	3.82 – j1.72	21.0	51.3	136	67.1	–20
822	1.07 – j2.57	0.99 + j2.70	4.56 – j1.89	21.2	51.0	127	69.4	–18

(1) Load impedance for optimum P1dB efficiency.
(2) Load impedance for optimum P3dB efficiency.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

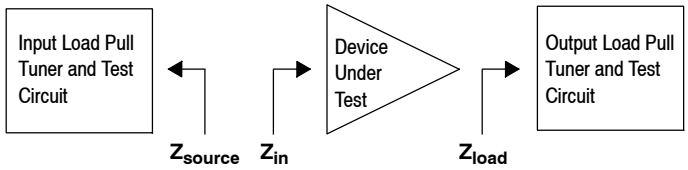


Table 13. Peaking Side Load Pull Performance — Maximum Power Tuning

V_{DD} = 28 Vdc, V_{GSB} = 0.7 Vdc, Pulsed CW, 10 μsec(on), 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Output Power P1dB Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
790	1.21 – j2.23	1.06 + j2.38	1.11 – j2.38	15.6	53.4	218	54.0	–16
806	1.18 – j2.27	1.11 + j2.50	1.15 – j2.52	15.2	53.1	202	52.6	–16
822	1.32 – j2.41	1.17 + j2.66	1.06 – j2.79	14.8	53.1	203	50.5	–13

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Output Power P3dB Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
790	1.21 – j2.23	1.05 + j2.48	1.04 – j2.59	13.3	54.4	275	55.2	–19
806	1.18 – j2.27	1.10 + j2.61	1.00 – j2.78	12.7	54.2	262	52.5	–19
822	1.32 – j2.41	1.16 + j2.76	1.01 – j2.97	12.5	54.2	263	52.5	–16

(1) Load impedance for optimum P1dB power.
(2) Load impedance for optimum P3dB power.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

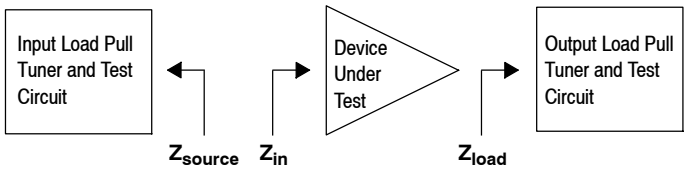
Table 14. Peaking Side Load Pull Performance — Maximum Drain Efficiency Tuning

V_{DD} = 28 Vdc, V_{GSB} = 0.7 Vdc, Pulsed CW, 10 μsec(on), 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Drain Efficiency P1dB Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
790	1.21 – j2.23	0.98 + j2.27	3.32 – j0.43	17.0	50.5	113	73.5	–28
806	1.18 – j2.27	1.04 + j2.41	3.04 – j0.87	16.6	50.6	114	69.7	–25
822	1.32 – j2.41	1.10 + j2.55	3.34 – j1.03	16.4	50.5	113	70.8	–21

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Drain Efficiency P3dB Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
790	1.21 – j2.23	0.99 + j2.39	3.41 – j0.81	15.0	51.3	135	73.9	–32
806	1.18 – j2.27	1.05 + j2.52	3.05 – j1.36	14.6	51.7	147	70.9	–29
822	1.32 – j2.41	1.10 + j2.67	3.46 – j1.34	14.3	51.4	138	72.2	–26

(1) Load impedance for optimum P1dB efficiency.
(2) Load impedance for optimum P3dB efficiency.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.



P1dB - TYPICAL CARRIER SIDE LOAD PULL CONTOURS — 806 MHz

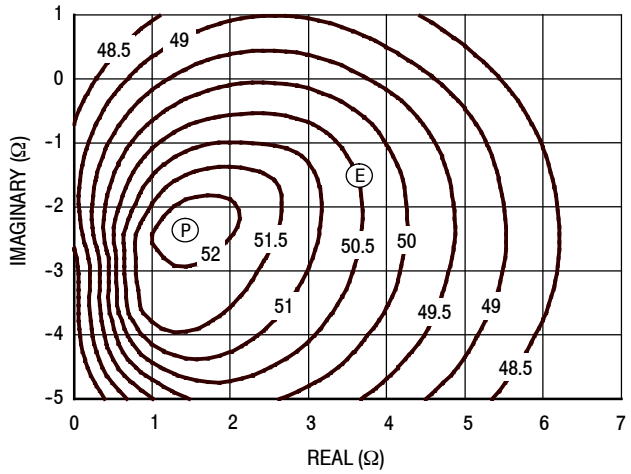


Figure 28. P1dB Load Pull Output Power Contours (dBm)

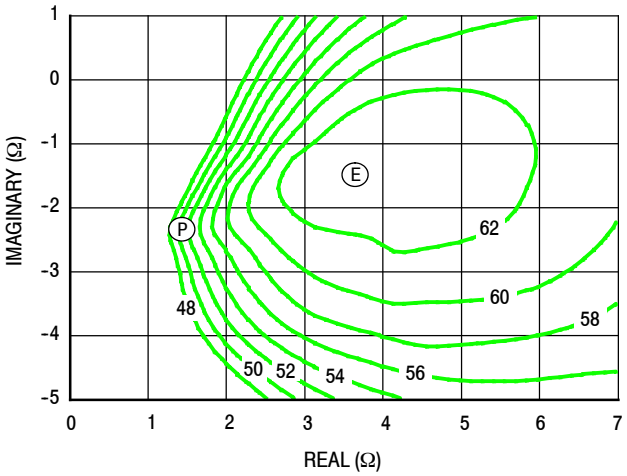


Figure 29. P1dB Load Pull Efficiency Contours (%)

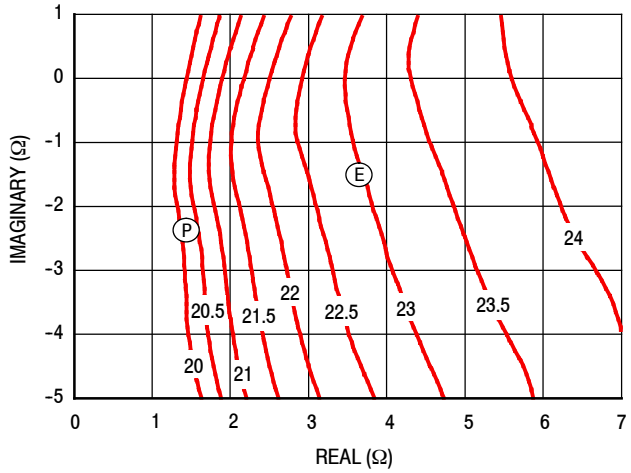


Figure 30. P1dB Load Pull Gain Contours (dB)

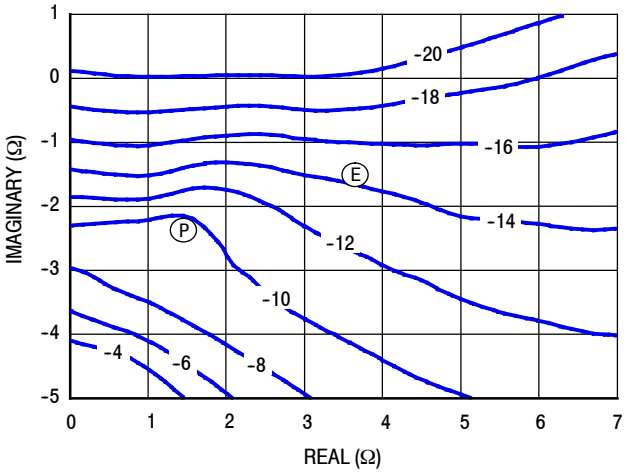


Figure 31. P1dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power

Ⓔ = Maximum Drain Efficiency

Gain

Drain Efficiency

Linearity

Output Power

P3dB - TYPICAL CARRIER SIDE LOAD PULL CONTOURS — 806 MHz

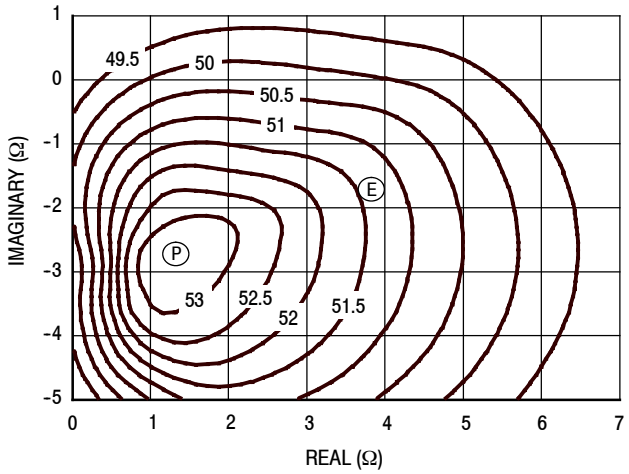


Figure 32. P3dB Load Pull Output Power Contours (dBm)

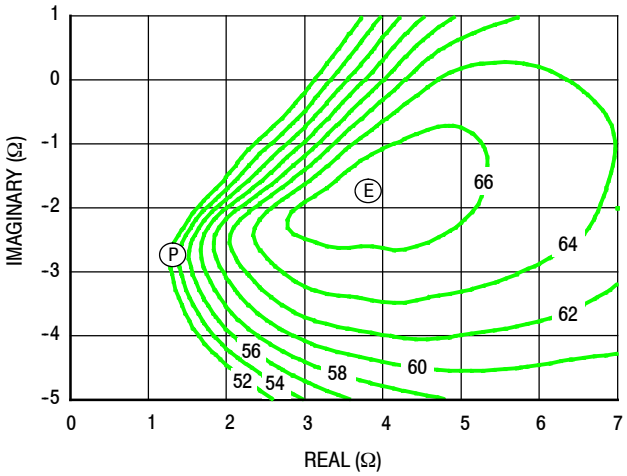


Figure 33. P3dB Load Pull Efficiency Contours (%)

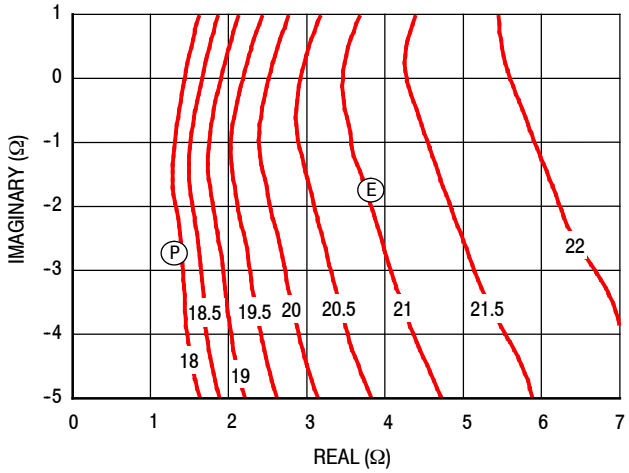


Figure 34. P3dB Load Pull Gain Contours (dB)

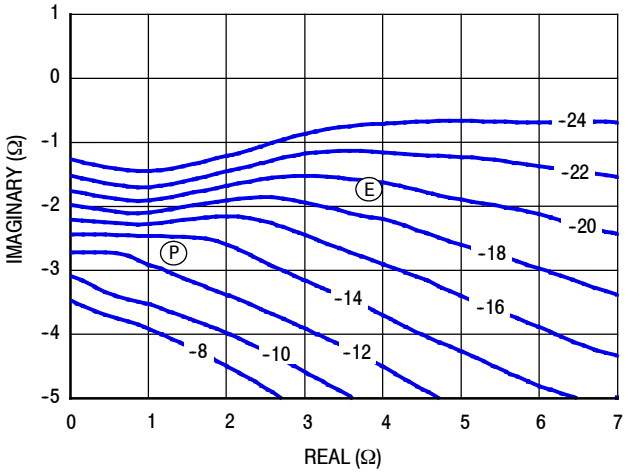


Figure 35. P3dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power

Ⓔ = Maximum Drain Efficiency

Gain

Drain Efficiency

Linearity

Output Power

P1dB - TYPICAL PEAKING SIDE LOAD PULL CONTOURS — 806 MHz

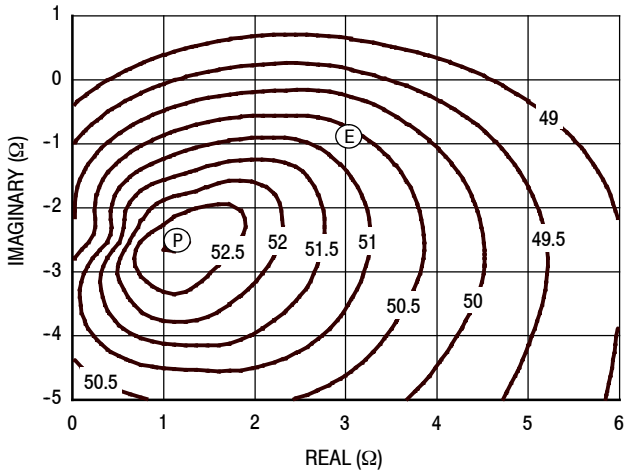


Figure 36. P1dB Load Pull Output Power Contours (dBm)

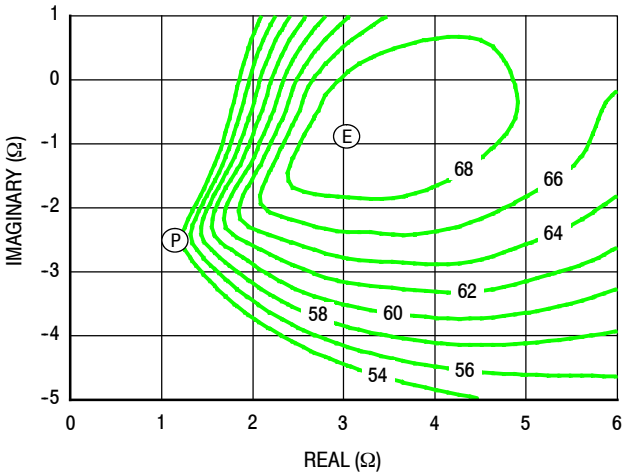


Figure 37. P1dB Load Pull Efficiency Contours (%)

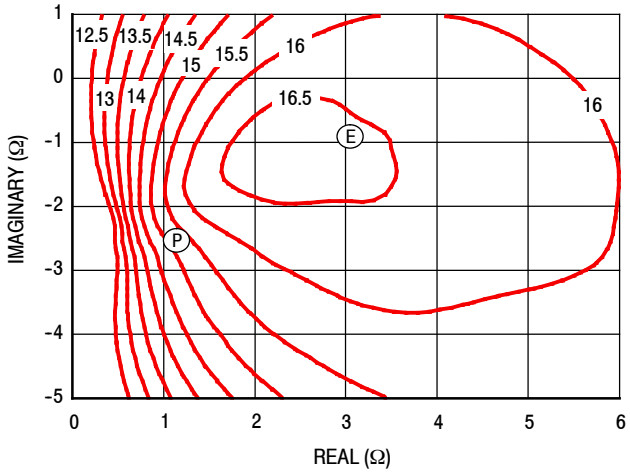


Figure 38. P1dB Load Pull Gain Contours (dB)

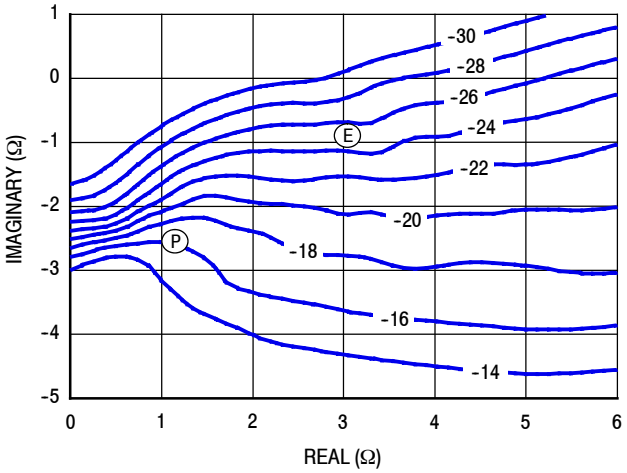


Figure 39. P1dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power

Ⓔ = Maximum Drain Efficiency

Gain

Drain Efficiency

Linearity

Output Power

P3dB - TYPICAL PEAKING SIDE LOAD PULL CONTOURS — 806 MHz

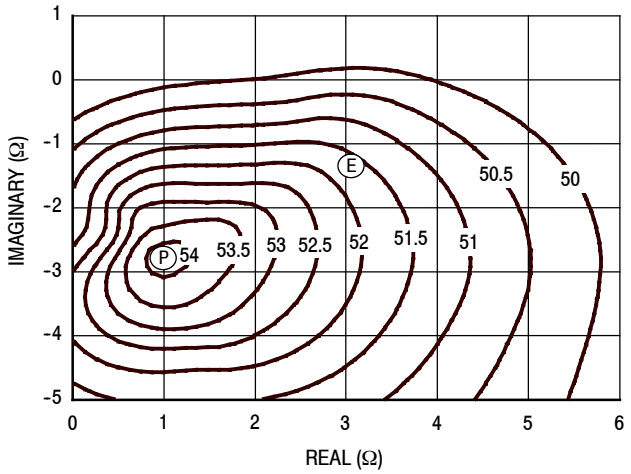


Figure 40. P3dB Load Pull Output Power Contours (dBm)

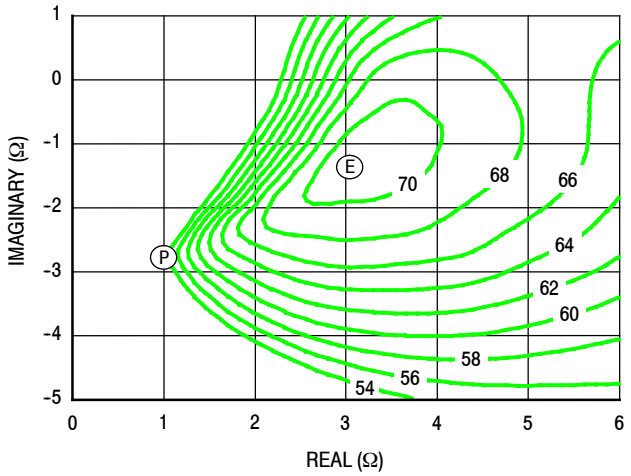


Figure 41. P3dB Load Pull Efficiency Contours (%)

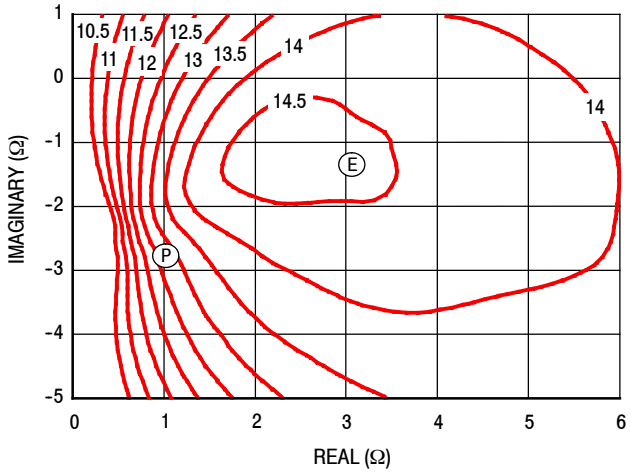


Figure 42. P3dB Load Pull Gain Contours (dB)

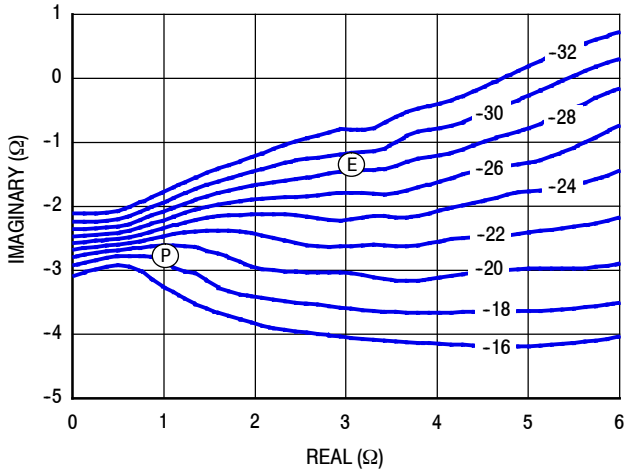


Figure 43. P3dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power

Ⓔ = Maximum Drain Efficiency

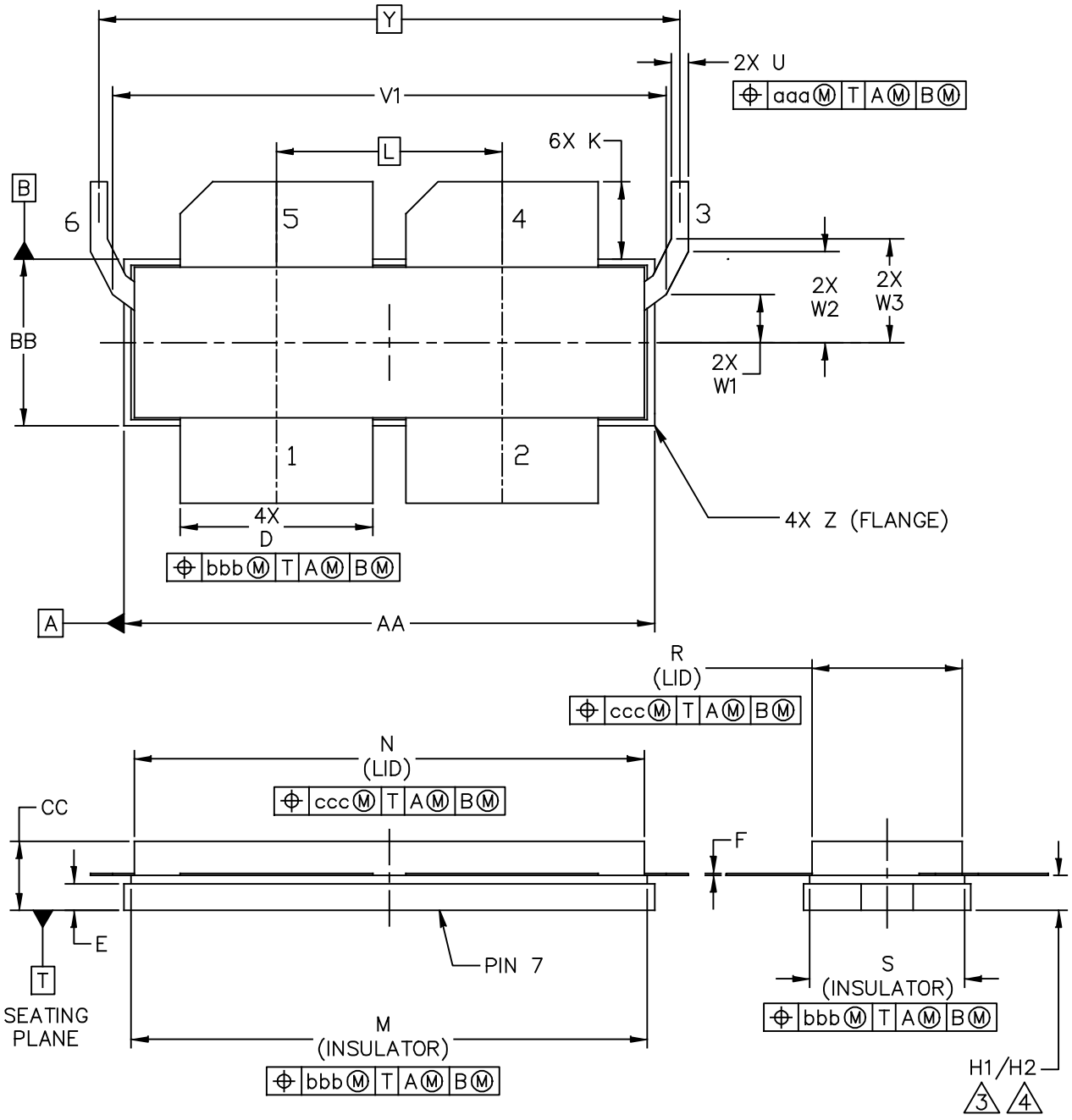
Gain

Drain Efficiency

Linearity

Output Power

PACKAGE DIMENSIONS



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	STANDARD: NON-JEDEC	
	08 MAR 2013	

NOTES:

1. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.

2. CONTROLLING DIMENSION: INCH

3. DIMENSIONS H1 AND H2 ARE MEASURED .030 INCH (0.762 MM) AWAY FROM FLANGE PARALLEL TO DATUM B. H1 APPLIES TO PINS 1, 2, 4 & 5. H2 APPLIES TO PINS 3 & 6.

4. TOLERANCE OF DIMENSION H2 IS TENTATIVE AND COULD CHANGE ONCE SUFFICIENT MANUFACTURING DATA IS AVAILABLE.

DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX	DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX
AA	1.265	1.275	32.13	32.39	N	1.218	1.242	30.94	31.55
BB	.395	.405	10.03	10.29	R	.365	.375	9.27	9.53
CC	.170	.190	4.32	4.83	S	.365	.375	9.27	9.53
D	.455	.465	11.56	11.81	U	.035	.045	0.89	1.14
E	.062	.066	1.57	1.68	V1	1.320	1.330	33.53	33.78
F	.004	.007	0.10	0.18	W1	.110	.120	2.79	3.05
H1	.082	.090	2.08	2.29	W2	.213	.223	5.41	5.66
H2	.078	.094	1.98	2.39	W3	.243	.253	6.17	6.43
K	.175	.195	4.45	4.95	Y	1.390 BSC		35.31 BSC	
L	.540 BSC		13.72 BSC		Z	R.000	R.040	R0.00	R1.02
M	1.219	1.241	30.96	31.52	aaa	.015		0.38	
					bbb	.010		0.25	
					ccc	.020		0.51	

MECHANICAL OUTLINE | PRINT VERSION NOT TO SCALE

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PRODUCT DOCUMENTATION, SOFTWARE AND TOOLS

Refer to the following resources to aid your design process.

Application Notes

- AN1955: Thermal Measurement Methodology of RF Power Amplifiers

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

Software

- Electromigration MTTF Calculator
- RF High Power Model
- .s2p File

Development Tools

- Printed Circuit Boards

For Software and Tools, do a Part Number search at http://www.freescale.com, and select the “Part Number” link. Go to the Software & Tools tab on the part’s Product Summary page to download the respective tool.

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	June 2014	• Initial Release of Data Sheet

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