

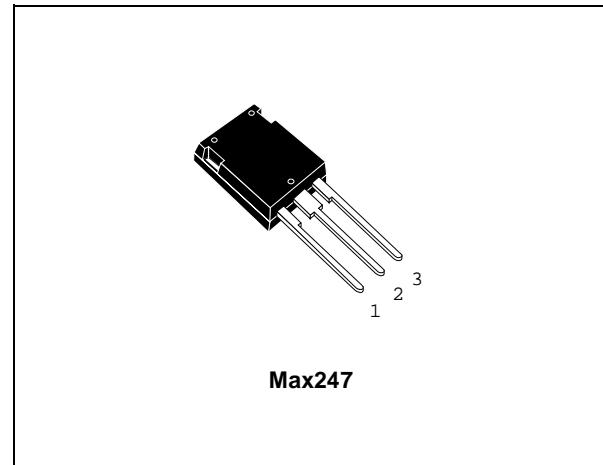


STY60NK30Z

N-CHANNEL 300V - 0.033Ω - 60A Max247
Zener-Protected SuperMESH™ Power MOSFET

TYPE	V _{DSS}	R _{DS(on)}	I _D	P _W
STY60NK30Z	300 V	< 0.045 Ω	60 A	450 W

- TYPICAL R_{DS(on)} = 0.033 Ω
- EXTREMELY HIGH dv/dt CAPABILITY
- 100% AVALANCHE TESTED
- GATE CHARGE MINIMIZED
- VERY LOW INTRINSIC CAPACITANCES
- VERY GOOD MANUFACTURING REPEATABILITY



Max247

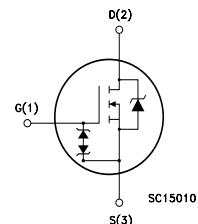
DESCRIPTION

The SuperMESH™ series is obtained through an extreme optimization of ST's well established strip-based PowerMESH™ layout. In addition to pushing on-resistance significantly down, special care is taken to ensure a very good dv/dt capability for the most demanding applications. Such series complements ST full range of high voltage MOSFETs including revolutionary MDmesh™ products.

APPLICATIONS

- HIGH CURRENT, HIGH EFFICIENCY SWITCHING DC/DC CONVERTERS FOR PLASMA TV's
- IDEAL FOR OFF-LINE POWER SUPPLIES, ADAPTORS AND PFC

INTERNAL SCHEMATIC DIAGRAM



ORDERING INFORMATION

SALES TYPE	MARKING	PACKAGE	PACKAGING
STY60NK30Z	Y60NK30Z	Max247	TUBE

STY60NK30Z

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source Voltage ($V_{GS} = 0$)	300	V
V_{DGR}	Drain-gate Voltage ($R_{GS} = 20 \text{ k}\Omega$)	300	V
V_{GS}	Gate- source Voltage	± 30	V
I_D	Drain Current (continuous) at $T_C = 25^\circ\text{C}$	60	A
I_D	Drain Current (continuous) at $T_C = 100^\circ\text{C}$	37.5	A
$I_{DM} (\bullet)$	Drain Current (pulsed)	240	A
P_{TOT}	Total Dissipation at $T_C = 25^\circ\text{C}$	450	W
	Derating Factor	3.57	W/ $^\circ\text{C}$
$V_{ESD(G-S)}$	Gate source ESD(HBM-C=100 pF, $R=1.5 \text{ k}\Omega$)	6000	V
$dv/dt (1)$	Peak Diode Recovery voltage slope	4.5	V/ns
T_j T_{stg}	Operating Junction Temperature Storage Temperature	-55 to 150	$^\circ\text{C}$

(•) Pulse width limited by safe operating area

(1) $I_{SD} \leq 60\text{A}$, $di/dt \leq 200\text{A}/\mu\text{s}$, $V_{DD} \leq V_{(BR)DSS}$, $T_j \leq T_{JMAX}$.

THERMAL DATA

Rthj-case	Thermal Resistance Junction-case Max	0.28	$^\circ\text{C/W}$
Rthj-amb	Thermal Resistance Junction-ambient Max	30	$^\circ\text{C/W}$
T_I	Maximum Lead Temperature For Soldering Purpose	300	$^\circ\text{C}$

AVALANCHE CHARACTERISTICS

Symbol	Parameter	Max Value	Unit
I_{AR}	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T_j max)	60	A
E_{AS}	Single Pulse Avalanche Energy (starting $T_j = 25^\circ\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50 \text{ V}$)	0.7	J

GATE-SOURCE ZENER DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
BV_{GSO}	Gate-Source Breakdown Voltage	$I_{GS} = \pm 1\text{mA}$ (Open Drain)	30			V

PROTECTION FEATURES OF GATE-TO-SOURCE ZENER DIODES

The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

ELECTRICAL CHARACTERISTICS (T_{CASE} =25°C UNLESS OTHERWISE SPECIFIED)
ON/OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V(BR)DSS	Drain-source Breakdown Voltage	I _D = 1 mA, V _{GS} = 0	300			V
I _{DSS}	Zero Gate Voltage Drain Current (V _{GS} = 0)	V _{DS} = Max Rating V _{DS} = Max Rating, T _C = 125 °C			1 50	μA μA
I _{GSS}	Gate-body Leakage Current (V _{DS} = 0)	V _{GS} = ± 20 V			±10	μA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 100 μA	3	3.75	4.5	V
R _{DS(on)}	Static Drain-source On Resistance	V _{GS} = 10V, I _D = 30 A		0.033	0.045	Ω

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g _f (1)	Forward Transconductance	V _{DS} = 15 V, I _D = 30 A		29		S
C _{iss} C _{oss} C _{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	V _{DS} = 25V, f = 1 MHz, V _{GS} = 0		7200 1070 250		pF pF pF
C _{oss} eq. (3)	Equivalent Output Capacitance	V _{GS} = 0V, V _{DS} = 0V to 240V		880		pF

SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
t _{d(on)} t _r	Turn-on Delay Time Rise Time	V _{DD} = 150 V, I _D = 30 A R _G = 4.7Ω, V _{GS} = 10 V (Resistive Load see, Figure 3)		50 90		ns ns
Q _g Q _{gs} Q _{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	V _{DD} = 240 V, I _D = 60 A, V _{GS} = 10 V		220 46 123		nC nC nC

SWITCHING OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
t _{d(off)} t _f	Turn-off Delay Time Fall Time	V _{DD} = 150 V, I _D = 30 A R _G = 4.7Ω, V _{GS} = 10 V (Resistive Load see, Figure 3)		150 60		ns ns
t _{r(Voff)} t _f t _c	Off-voltage Rise Time Fall Time Cross-over Time	V _{DD} = 240 V, I _D = 60 A, R _G = 4.7Ω, V _{GS} = 10V (Inductive Load see, Figure 5)		40 65 110		ns ns ns

SOURCE DRAIN DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I _{SD} I _{SDM} (2)	Source-drain Current Source-drain Current (pulsed)				60 240	A A
V _{SD} (1)	Forward On Voltage	I _{SD} = 60 A, V _{GS} = 0			1.6	V
t _{rr} Q _{rr} I _{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	I _{SD} = 60 A, di/dt = 100 A/μs V _R = 100 V, T _j = 150°C (see test circuit, Figure 5)		475 6.4 27		ns μC A

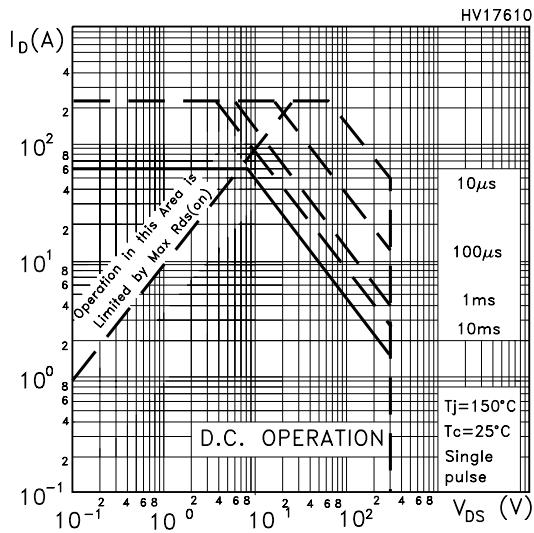
Note: 1. Pulsed: Pulse duration = 300 μs, duty cycle 1.5 %.

2. Pulse width limited by safe operating area.

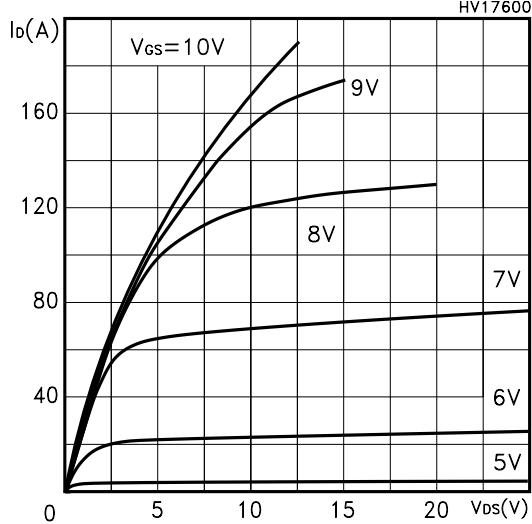
3. C_{oss} eq. is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}.

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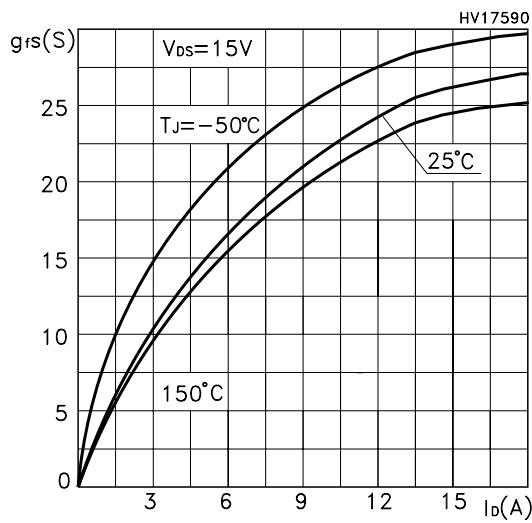
Safe Operating Area



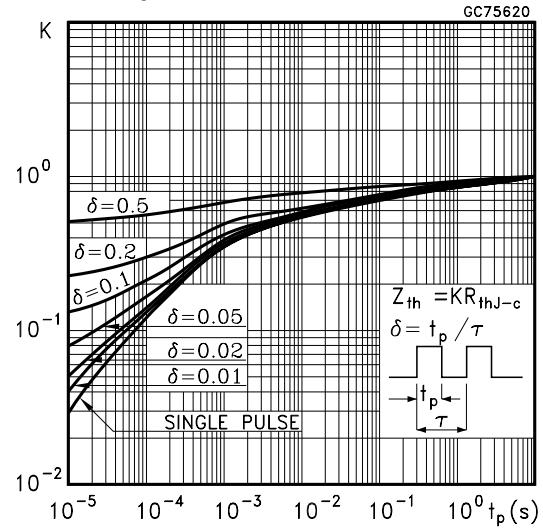
Output Characteristics



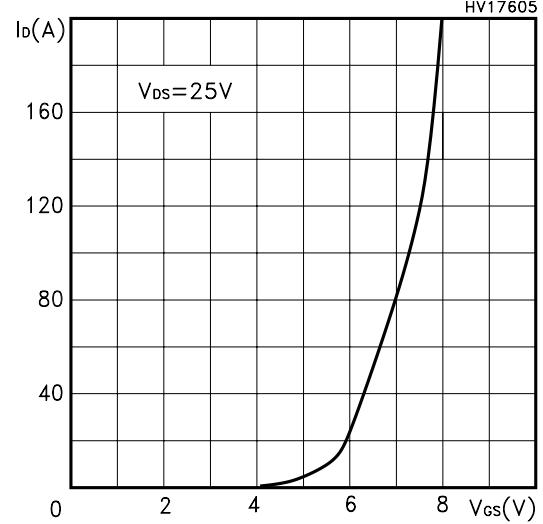
Transconductance



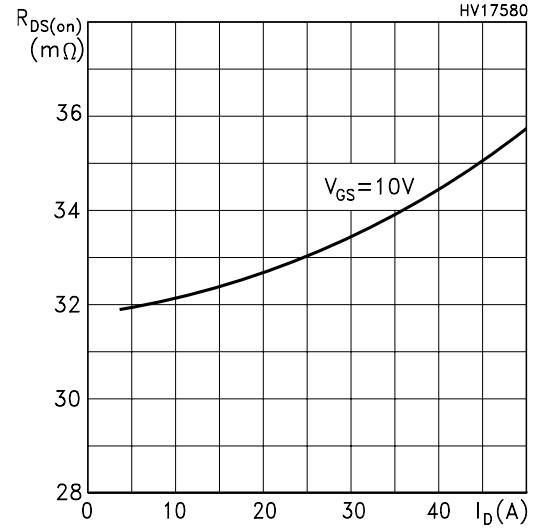
Thermal Impedance

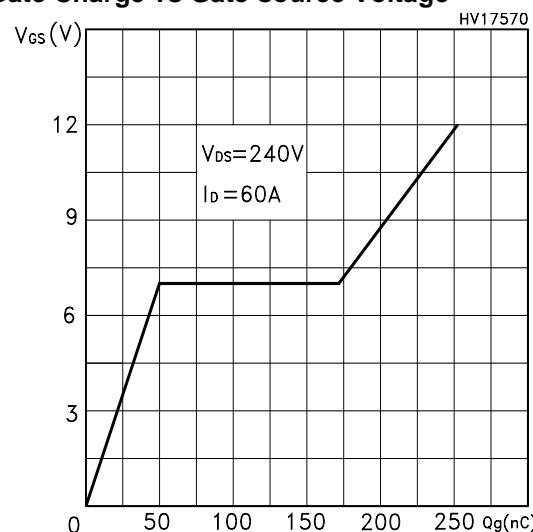
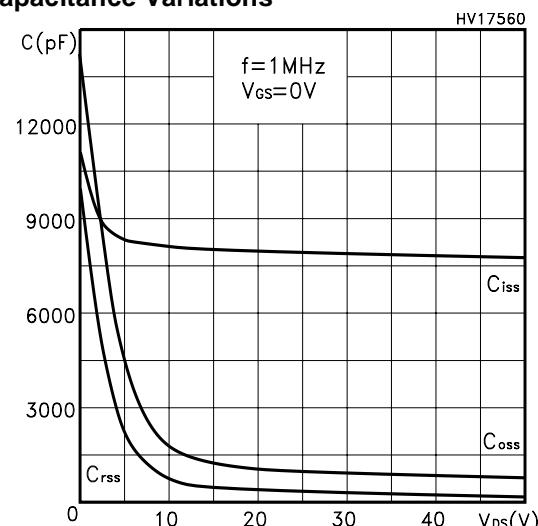
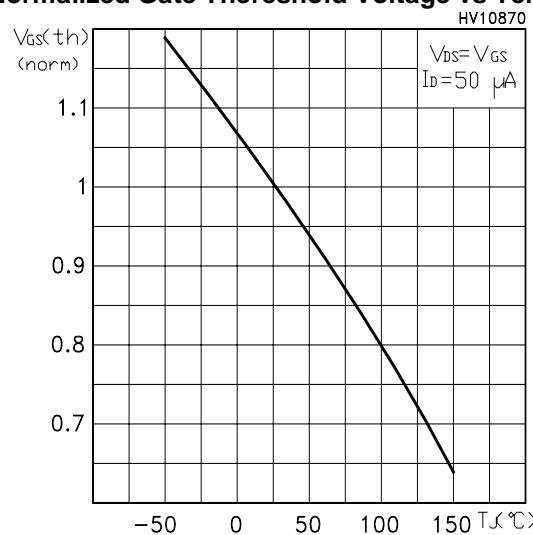
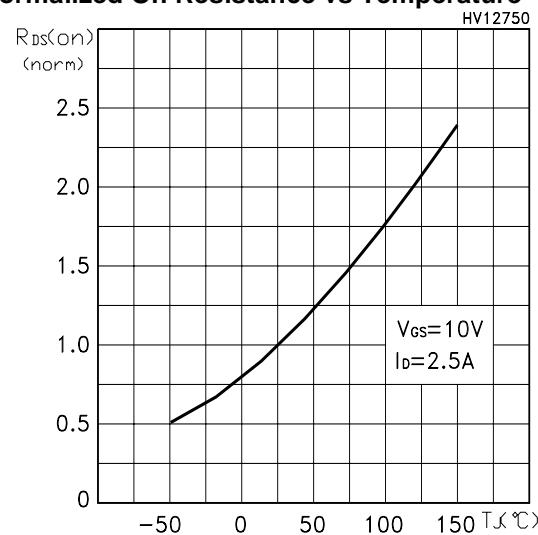
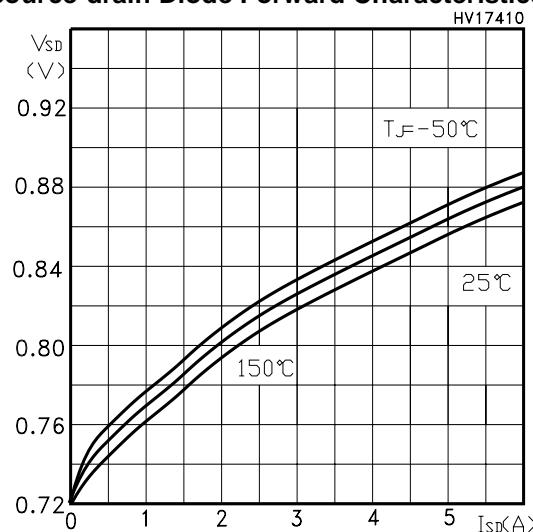


Transfer Characteristics



Static Drain-source On Resistance



Gate Charge vs Gate-source Voltage**Capacitance Variations****Normalized Gate Threshold Voltage vs Temp.****Normalized On Resistance vs Temperature****Source-drain Diode Forward Characteristics**

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Fig. 1: Unclamped Inductive Load Test Circuit

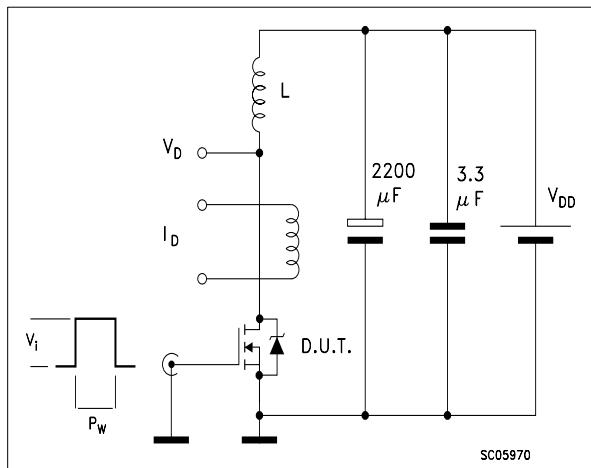


Fig. 2: Unclamped Inductive Waveform

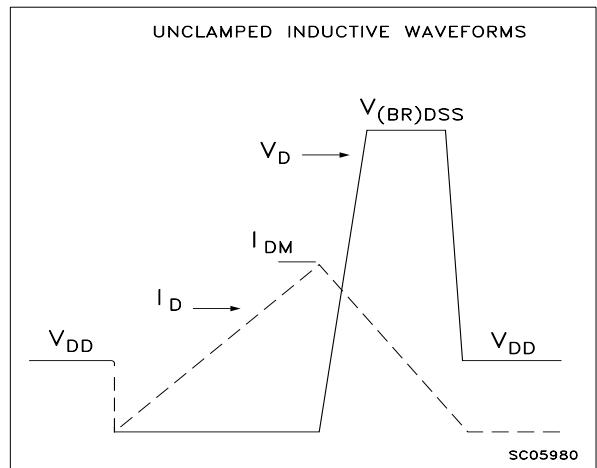


Fig. 3: Switching Times Test Circuit For Resistive Load

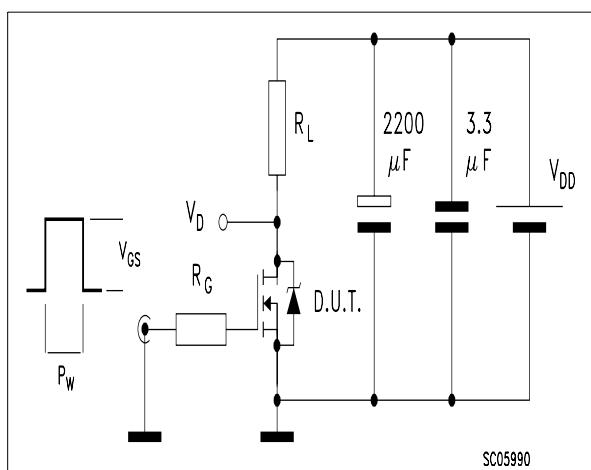


Fig. 4: Gate Charge test Circuit

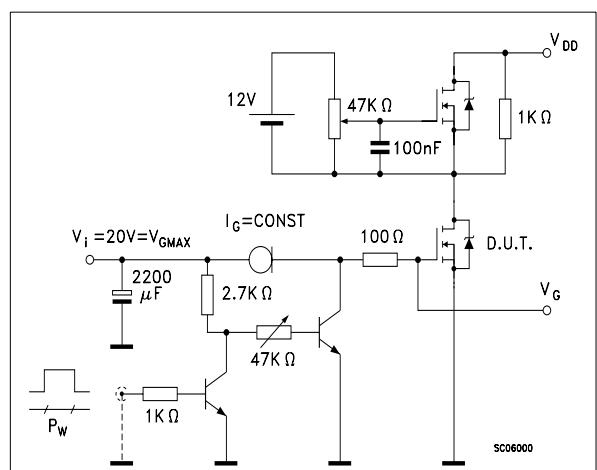
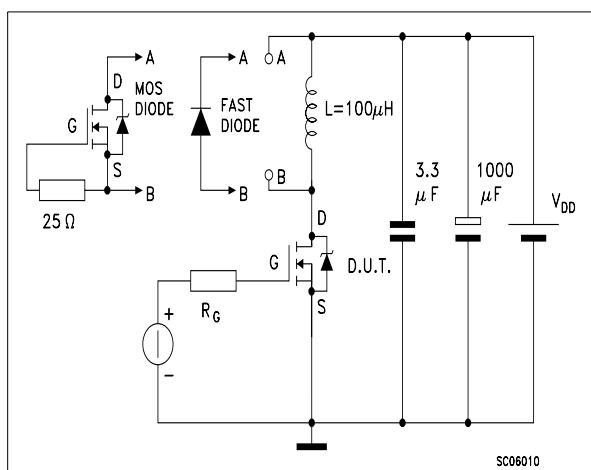
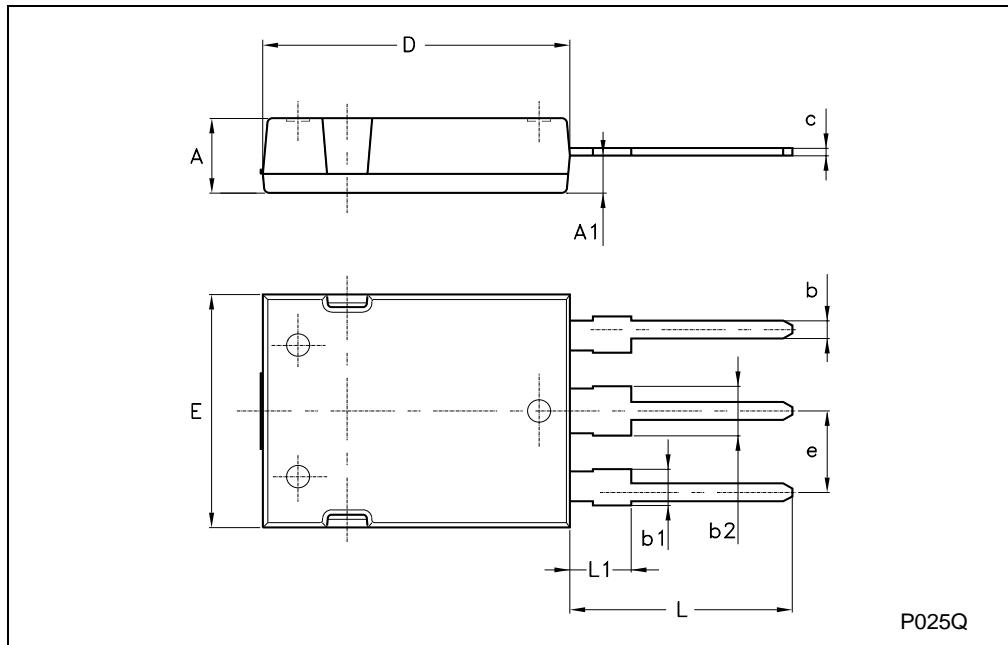


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times



Max247 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.70		5.30			
A1	2.20		2.60			
b	1.00		1.40			
b1	2.00		2.40			
b2	3.00		3.40			
c	0.40		0.80			
D	19.70		20.30			
e	5.35		5.55			
E	15.30		15.90			
L	14.20		15.20			
L1	3.70		4.30			



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