Synchronous DRAM Module

MT36LSDT12872 – 1GB
MT36LSDT25672 – 2GB

For the latest data sheet, refer to Micron's Web site: www.micron.com/products/modules

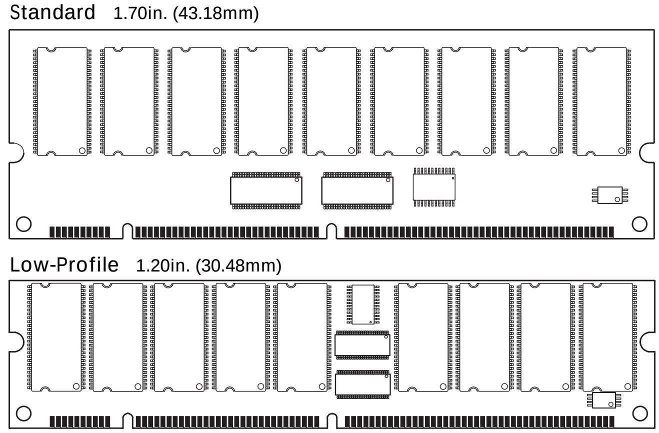
Features

- 168-pin, dual in-line memory module (DIMM)
- PC100- and PC133-compliant
- Registered inputs with one-clock delay
- Phase-lock loop (PLL) clock driver to reduce loading
- Utilizes 125 MHz and 133 MHz SDRAM components
- Supports ECC error detection and correction
- 1GB (128 Meg x 72) and 2GB (256 Meg x 72)
- Single +3.3V power supply
- Fully synchronous; all signals registered on positive edge of PLL clock
- Internal pipelined operation; column address can be changed every clock cycle
- Internal SDRAM banks for hiding row access/ precharge
- Programmable burst lengths: 1, 2, 4, 8, or full page
- Auto precharge, includes concurrent auto precharge
- Auto refresh mode
- Self refresh mode: 64ms, 4,096-cycle refresh
- LVTTL-compatible inputs and outputs
- Serial presence-detect (SPD)
- Gold edge contacts

Table 1: Timing Parameters
CL = CAS (READ) latency

Module Marking	Clock	Access Time CL = 2	Access Time CL = 3	Setup Time	Hold Time
-13E	133 MHz	5.4ns	–	1.5	0.8
-133	133 MHz	–	5.4ns	1.5	0.8

Figure 1: 168-Pin DIMM (MO-161)



Options / Marking

Options	Marking
• Package	
168-pin DIMM (standard)	G
168-pin DIMM (lead-free)	Y[1]
• Frequency/CAS Latency[2]	
133 MHz/CL = 2	-13E
133 MHz/CL = 3	-133
• PCB	
Standard 1.70in (43.18mm)	See note on page 2
Low-Profile 1.20in. (30.48mm)	See note on page 2

Notes: 1. Contact Micron for product availability.
2. Registered mode adds one clock cycle to CL.

Table 2: Address Table

Parameter	1GB	2GB
Refresh Count	8K	8K
Device Banks	4 (BA0, BA1)	4 (BA0, BA1)
Device Configuration	256Mb (64 Meg x 4)	512Mb (128 Meg x 4)
Row Addressing	8K (A0–A12)	8K (A0–A12)
Column Addressing	2K (A0–A9, A11)	4K (A0–A9, A11, A12)
Module Ranks	2 (S0#, S2#; S1#, S3#)	2 (S0#, S2#; S1#, S3#)

Table 3: Part Numbers

Part Number	Module Density	Configuration	System Bus Speed
MT36LSDT12872G-13E__	1GB	128 Meg x 72	133 MHz
MT36LSDT12872Y-13E__	1GB	128 Meg x 72	133 MHz
MT36LSDT12872G-133__	1GB	128 Meg x 72	133 MHz
MT36LSDT12872Y-133__	1GB	128 Meg x 72	133 MHz
MT36LSDT25672G-13E__	2GB	256 Meg x 72	133 MHz
MT36LSDT25672Y-13E__	2GB	256 Meg x 72	133 MHz
MT36LSDT25672G-133__	2GB	256 Meg x 72	133 MHz
MT36LSDT25672Y-133__	2GB	256 Meg x 72	133 MHz

Note: The designators for component and PCB revision are the last two characters of each part number. Consult factory for current revision codes. Example: MT36LSDT12872G-133B1.

Pin Assignments and Descriptions

Table 4: Pin Assignment

168-Pin DIMM Front								168-Pin DIMM Back							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	VSS	22	CB1	43	VSS	64	VSS	85	VSS	106	CB5	127	VSS	148	VSS
2	DQ0	23	VSS	44	NC	65	DQ21	86	DQ32	107	VSS	128	CKE0	149	DQ53
3	DQ1	24	NC	45	S2#	66	DQ22	87	DQ33	108	NC	129	S3#	150	DQ54
4	DQ2	25	NC	46	DQMB2	67	DQ23	88	DQ34	109	NC	130	DQMB6	151	DQ55
5	DQ3	26	VDD	47	DQMB3	68	VSS	89	DQ35	110	VDD	131	DQMB7	152	VSS
6	VDD	27	WE#	48	NC	69	DQ24	90	VDD	111	CAS#	132	NC	153	DQ56
7	DQ4	28	DQMB0	49	VDD	70	DQ25	91	DQ36	112	DQMB4	133	VDD	154	DQ57
8	DQ5	29	DQMB1	50	NC	71	DQ26	92	DQ37	113	DQMB5	134	NC	155	DQ58
9	DQ6	30	S0#	51	NC	72	DQ27	93	DQ38	114	S1#	135	NC	156	DQ59
10	DQ7	31	NC	52	CB2	73	VDD	94	DQ39	115	RAS#	136	CB6	157	VDD
11	DQ8	32	VSS	53	CB3	74	DQ28	95	DQ40	116	VSS	137	CB7	158	DQ60
12	VSS	33	A0	54	VSS	75	DQ29	96	VSS	117	A1	138	VSS	159	DQ61
13	DQ9	34	A2	55	DQ16	76	DQ30	97	DQ41	118	A3	139	DQ48	160	DQ62
14	DQ10	35	A4	56	DQ17	77	DQ31	98	DQ42	119	A5	140	DQ49	161	DQ63
15	DQ11	36	A6	57	DQ18	78	VSS	99	DQ43	120	A7	141	DQ50	162	VSS
16	DQ12	37	A8	58	DQ19	79	CK2	100	DQ44	121	A9	142	DQ51	163	CK3
17	DQ13	38	A10	59	VDD	80	NC	101	DQ45	122	BA0	143	VDD	164	NC
18	VDD	39	BA1	60	DQ20	81	NC	102	VDD	123	A11	144	DQ52	165	SA0
19	DQ14	40	VDD	61	NC	82	SDA	103	DQ46	124	VDD	145	NC	166	SA1
20	DQ15	41	VDD	62	NC	83	SCL	104	DQ47	125	CK1	146	NC	167	SA2
21	CB0	42	CK0	63	CKE1	84	VDD	105	CB4	126	A12	147	REGE	168	VDD

Figure 2: 168-Pin DIMM Pin Locations

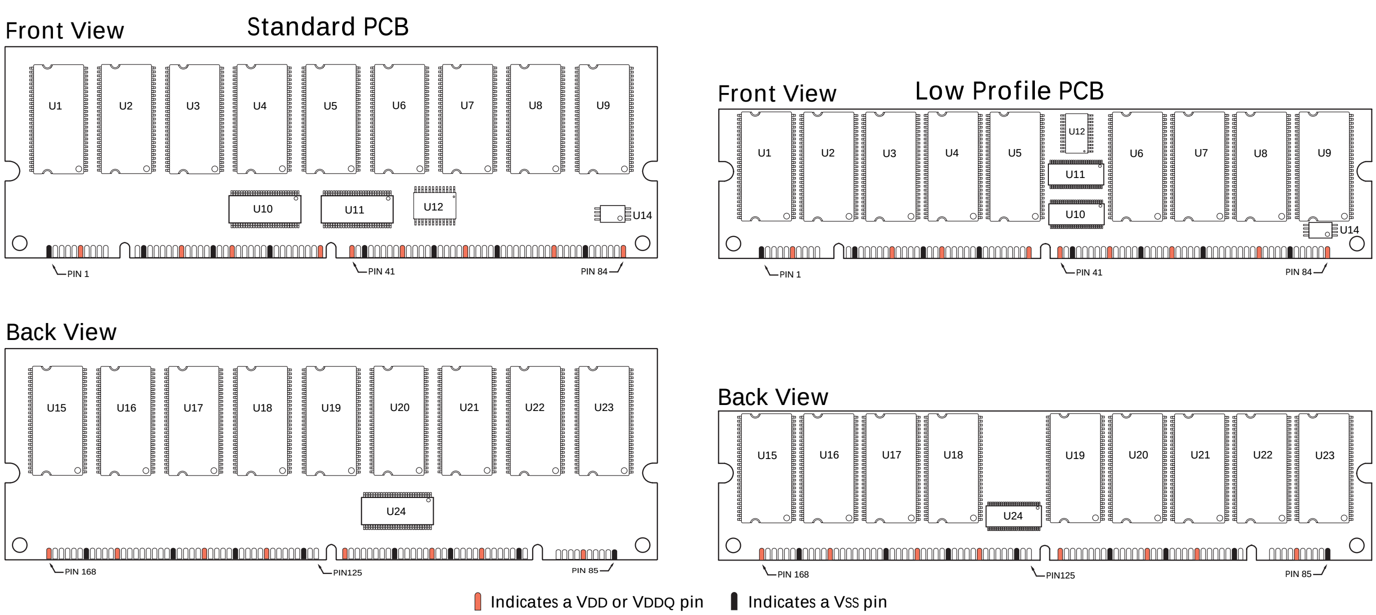


Table 5: Pin Descriptions

Pin numbers may not correlate with symbol order; refer to Table 4 on page 3 for more information

Pin Numbers	Symbol	Type	Description
27, 111, 115	RAS#, CAS#, WE#	Input	Command inputs: RAS#, CAS#, and WE# (along with S#) define the command being entered.
42, 79, 125, 163	CK0–CK3	Input	Clock: CK0 is distributed through an on-board PLL to all devices. CK1–CK3 are terminated.
128	CKE0	Input	Clock enable: CKE activates (HIGH) and deactivates (LOW) the CK0 signal. Deactivating the clock provides POWER-DOWN and SELF REFRESH operation (all device banks idle) or CLOCK SUSPEND operation (burst access in progress). CKE is synchronous except after the device enters power-down and self refresh modes, where CKE becomes asynchronous until after exiting the same mode. The input buffers, including CK, are disabled during power-down and self refresh modes, providing low standby power.
30, 45, 114, 129	S0#–S3#	Input	Chip select: S# enable (registered LOW) and disable (registered HIGH) the command decoder. All commands are masked when S# are registered HIGH. S# are considered part of the command code.
28, 29, 46, 47, 112, 113, 130, 131	DQMB0–DQMB7	Input	Input/Output mask: DQMB is an input mask signal for write accesses and an output enable signal for read accesses. Input data is masked when DQMB is sampled HIGH during a WRITE cycle. The output buffers are placed in a High-Z state (two-clock latency) when DQMB is sampled HIGH during a READ cycle.
39, 122	BA0, BA1	Input	Bank address: BA0 and BA1 define to which device bank the ACTIVE, READ, WRITE, or PRECHARGE command is being applied.
33–38, 117–121, 123, 126	A0–A12	Input	Address inputs: Provide the row address for ACTIVE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective device bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one device bank (A10 LOW, device bank selected by BA0, BA1) or all device banks (A10 HIGH). The address inputs also provide the op-code during a MODE REGISTER SET command.
83	SCL	Input	Serial clock for presence-detect: SCL is used to synchronize the presence-detect data transfer to and from the module.
165–167	SA0–SA2	Input	Presence-Detect address inputs: These pins are used to configure the presence-detect device.
147	REGE	Input	Register enable: REGE permits the DIMM to operate in “buffered” mode (LOW) or “registered” mode (HIGH).
2–5, 7–11, 13–17, 19–20, 55–58, 60, 65–67, 69–72, 74–77, 86–89, 91–95, 97–101, 103–104, 139–142, 144, 149–151, 153–156, 158–161	DQ0–DQ63	Input/ Output	Data I/Os: Data bus.
21, 22, 52, 53, 105, 106, 136, 137	CB0–CB7	Input/ Output	Check bits.
82	SDA	Input/ Output	Serial presence-detect data: SDA is a bidirectional pin used to transfer addresses and data into and data out of the presence-detect portion of the module.

Table 5: Pin Descriptions (Continued)
Pin numbers may not correlate with symbol order; refer to Table 4 on page 3 for more information

Pin Numbers	Symbol	Type	Description
6, 18, 26, 40, 41, 49, 59, 73, 84, 90, 102, 110, 124, 133, 143, 157, 168	V_{DD}	Supply	Power supply: +3.3V ±0.3V.
1, 12, 23, 32, 43, 54, 64, 68, 78, 85, 96, 107, 116, 127, 138, 148, 152, 162	V_{SS}	Supply	Ground.
24, 25, 31, 44, 48 50, 51 61, 62, 63, 80, 81, 108, 109, 132, 134, 135, 145, 146, 164	NC	–	Not connected: Listed pins are not connected on these modules.

Functional Block Diagram

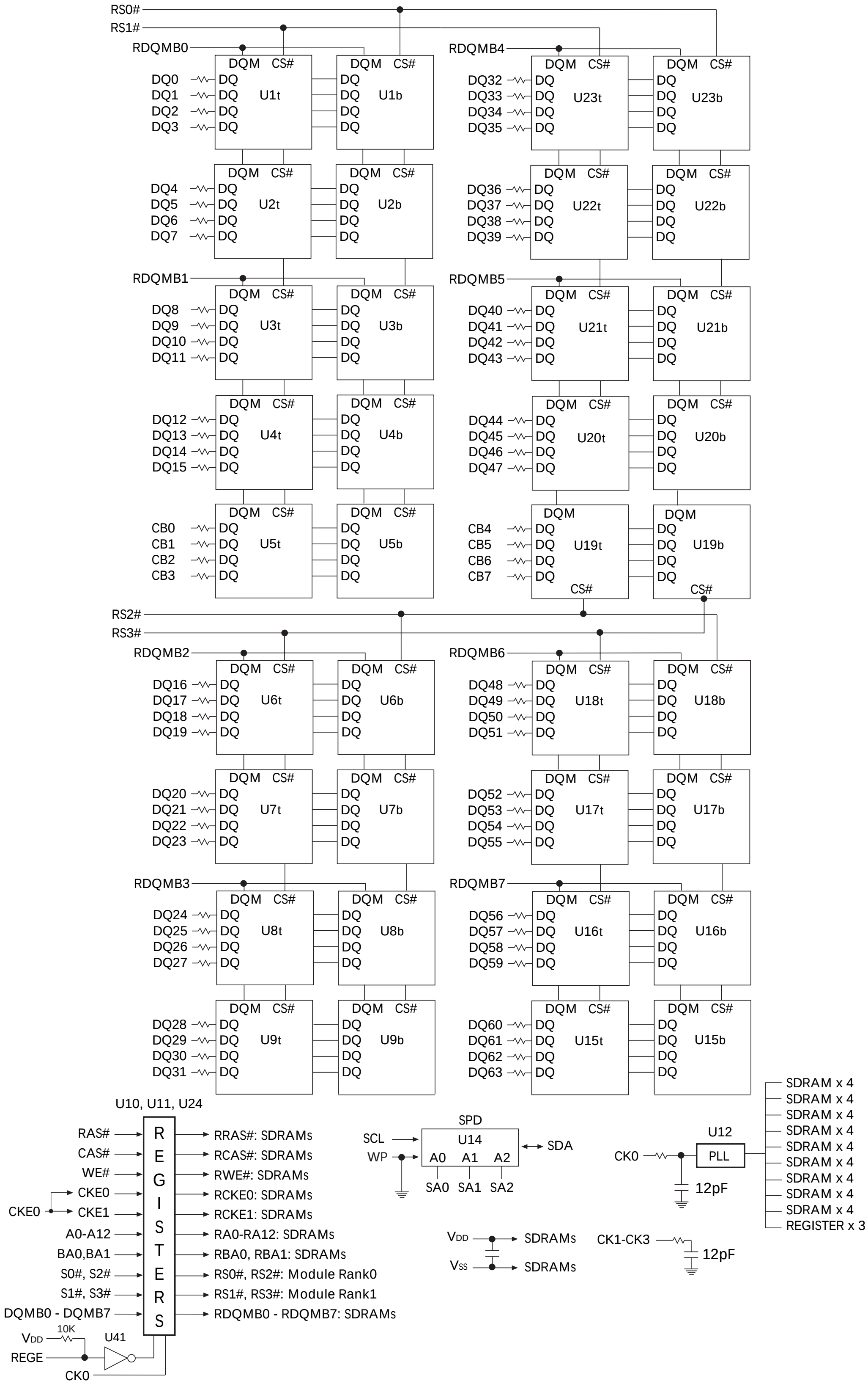
All resistor values are 10Ω unless otherwise specified.

‘t’ indicates top portion of stacked SDRAM. ‘b’ indicates bottom portion of stacked SDRAM.

Per industry standard, Micron modules utilize various component speed grades, as referenced in the module part number guide at www.micron.com/support/numbering.html.

Standard modules use the following SDRAM devices: MT48LC64M4A2TG (1GB); MT48LC128M4A2TG (2GB). Lead-free modules use the following SDRAM devices: MT48LC64M4A2P (1GB); MT48LC128M4A2P (2GB).

Figure 3: Functional Block Diagram



General Description

The MT36LSDT12872 and MT36LSDT25672 are high-speed CMOS, dynamic random-access, 1GB and 2GB memory modules organized in x72 (ECC) configurations. SDRAM modules use internally configured quad-bank SDRAM devices with a synchronous interface (all signals are registered on the positive edge of clock signal CK).

Read and write accesses to SDRAM modules are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the device bank and row to be accessed (BA0, BA1 select the device bank; A0–A12, select the device row). The address bits registered coincident with the READ or WRITE command are used to select the starting column location for the burst access.

SDRAM modules provide for programmable read or write burst lengths of 1, 2, 4, or 8 locations, or full page, with a burst terminate option. An auto precharge function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst sequence.

SDRAM modules use an internal pipelined architecture to achieve high-speed operation. Precharging one device bank while accessing one of the other three device banks will hide the PRECHARGE cycles and provide seamless, high-speed, random-access operation.

SDRAM modules are designed to operate in 3.3V, low-power memory systems. An auto refresh mode is provided, along with a power-saving, power-down mode. All inputs and outputs are LVTTL-compatible.

SDRAM modules offer substantial advances in DRAM operating performance, including the ability to synchronously burst data at a high data rate with automatic column-address generation, the ability to interleave between device banks in order to hide precharge time, and the capability to randomly change column addresses on each clock cycle during a burst access. For more information regarding SDRAM operation, refer to the 256Mb or 512Mb SDRAM component data sheets.

PLL and Register Operation

These modules can be operated in either registered mode (REGE pin HIGH), where the control/address input signals are latched in the register on one rising clock edge and sent to the SDRAM devices on the following rising clock edge (data access is delayed by one clock), or in buffered mode (REGE pin LOW) where the input signals pass through the register/buffer to the SDRAM devices on the same clock.

A phase-lock loop (PLL) on the modules is used to redrive the clock to the SDRAM devices to minimize system clock loading. (CK0 is connected to the PLL, and CK1, CK2, and CK3 are terminated.)

Serial Presence-Detect Operation

These modules incorporate serial presence-detect (SPD). The SPD function is implemented using a 2,048-bit EEPROM. This nonvolatile storage device contains 256 bytes. The first 128 bytes can be programmed by Micron to identify the module type and various SDRAM organizations and timing parameters. The remaining 128 bytes of storage are available for use by the customer. System READ/WRITE operations between the master (system logic) and the slave EEPROM device (DIMM) occur via a standard I^2C bus using the DIMM's SCL (clock) and SDA (data) signals, together with SA (2:0), which provide eight unique DIMM/EEPROM addresses. Write protect (WP) is tied to ground on the module, permanently disabling hardware write protect.

Initialization

SDRAMs must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation. Once power is applied to VDD and VDDQ (simultaneously) and the clock is stable (stable clock is defined as a signal cycling within timing constraints specified for the clock pin), the SDRAM requires a 100µs delay prior to issuing any command other than a COMMAND INHIBIT or NOP. Starting at some point during this 100µs period and continuing at least through the end of this period, COMMAND INHIBIT or NOP commands should be applied.

Once the 100µs delay has been satisfied with at least one COMMAND INHIBIT or NOP command having been applied, a PRECHARGE command should be applied. All device banks must then be precharged, thereby placing the device in the all device banks idle state.

Once in the idle state, two auto refresh cycles must be performed. After the auto refresh cycles are complete, the SDRAM is ready for mode register programming. Because the mode register will power up in an unknown state, it should be loaded prior to applying any operational command.

Mode Register Definition

The mode register is used to define the specific mode of operation of the SDRAM. This definition includes the selection of a burst length, a burst type, a CAS latency, an operating mode and a write burst mode, as shown in Figure 4 on page 9. The mode register is programmed via the LOAD MODE REGISTER command and will retain the stored information until it is programmed again or the device loses power.

Mode register bits M0–M2 specify the burst length, M3 specifies the type of burst (sequential or interleaved), M4–M6 specify the CAS latency, M7 and M8 specify the operating mode, M9 specifies the write burst mode, and M10 and M11 are reserved for future use. Address A12 (M12) is undefined but should be driven LOW during loading of the mode register.

The mode register must be loaded when all device banks are idle, and the controller must wait the specified time before initiating the subsequent operation. Violating either of these requirements will result in unspecified operation.

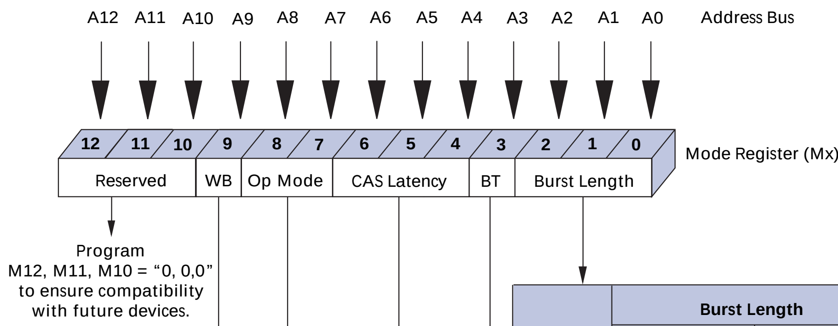
Burst Length

Read and write accesses to the SDRAM are burst oriented, with the burst length being programmable, as shown in Figure 4 on page 9. The burst length determines the maximum number of column locations that can be accessed for a given READ or WRITE command. Burst lengths of 1, 2, 4, or 8 locations are available for both the sequential and the interleaved burst types, and a full-page burst is available for the sequential type. The full-page burst is used in conjunction with the BURST TERMINATE command to generate arbitrary burst lengths.

Reserved states should not be used, as unknown operation or incompatibility with future versions may result.

When a READ or WRITE command is issued, a block of columns equal to the burst length is effectively selected. All accesses for that burst take place within this block, meaning that the burst will wrap within the block if a boundary is reached, as shown in Table 6 on page 10. The block is uniquely selected by A1–A*i* when BL = 2; A2–A*i* when BL = 4; and by A3–A*i* when BL = 8. See Note 8 of Table 6 on page 10 for A*i* values. The remaining (least significant) address bit(s) is (are) used to select the starting location within the block. Full-page bursts wrap within the page if the boundary is reached, as shown in Table 6 on page 10.

Figure 4: Mode Register Definition Diagram



M2 M1 M0	Burst Length M3 = 0	Burst Length M3 = 1
0 0 0	1	1
0 0 1	2	2
0 1 0	4	4
0 1 1	8	8
1 0 0	Reserved	Reserved
1 0 1	Reserved	Reserved
1 1 0	Reserved	Reserved
1 1 1	Full Page	Reserved

M3	Burst Type
0	Sequential
1	Interleaved

M6 M5 M4	CAS Latency
0 0 0	Reserved
0 0 1	Reserved
0 1 0	2
0 1 1	3
1 0 0	Reserved
1 0 1	Reserved
1 1 0	Reserved
1 1 1	Reserved

M8	M7	M6-M0	Operating Mode
0	0	Defined	Standard Operation
-	-	-	All other states reserved

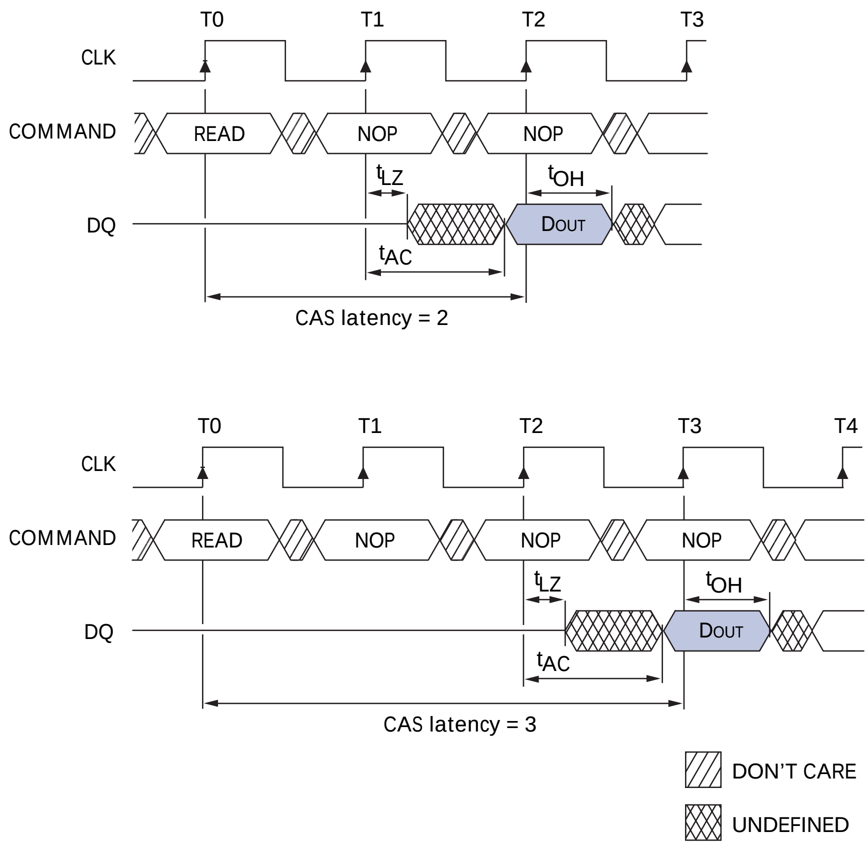
M9	Write Burst Mode
0	Programmed Burst Length
1	Single Location Access

Table 6: Burst Definition Table

Burst Length	Starting Column Address			Order of Accesses Within a Burst	
				Type = Sequential	Type = Interleaved
2			**A0**		
			0	0-1	0-1
			1	1-0	1-0
4		**A1**	**A0**		
		0	0	0-1-2-3	0-1-2-3
		0	1	1-2-3-0	1-0-3-2
		1	0	2-3-0-1	2-3-0-1
		1	1	3-0-1-2	3-2-1-0
8	**A2**	**A1**	**A0**		
	0	0	0	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7
	0	0	1	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6
	0	1	0	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5
	0	1	1	3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4
	1	0	0	4-5-6-7-0-1-2-3	4-5-6-7-0-1-2-3
	1	0	1	5-6-7-0-1-2-3-4	5-4-7-6-1-0-3-2
	1	1	0	6-7-0-1-2-3-4-5	6-7-4-5-2-3-0-1
	1	1	1	7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0
Full Page (y)	n = *i* (location 0-y)			Cn, Cn+1, Cn+2, Cn+3, Cn+4..., ...Cn-1, Cn...	Not supported

Notes:
1. For full-page accesses: y = 2,048 (1GB); y= 4,096 (2GB).
2. For BL = 2, *i* will select the block of two burst; A0 selects the starting column within the block.
3. For BL = 4, *i* will select the block of four burst; A0–A1 select the starting column within the block.
4. For BL = 8, *i* will select the block of eight burst; A0–A2 select the starting column within the block.
5. For a full-page burst, the full row is selected and i will select the starting column.
6. Whenever a boundary of the block is reached within a given sequence above, the following access wraps within the block.
7. For BL = 1, *i* will select the unique column to be accessed, and mode register bit M3 is ignored.
8. A*i* = A0–A9, A11 for 1GB;
   A*i* = A0–A9, A11, A12 for 2GB.

Figure 5: CAS Latency Diagram



Burst Type

Accesses within a given burst may be programmed to be either sequential or interleaved; this is referred to as the burst type and is selected via bit M3.

The ordering of accesses within a burst is determined by the burst length, the burst type and the starting column address, as shown in Table 6 on page 10.

CAS Latency

The CAS latency is the delay, in clock cycles, between the registration of a READ command and the availability of the first piece of output data. The latency can be set to two or three clocks.

If a READ command is registered at clock edge n, and the latency is m clocks, the data will be available by clock edge $n + m$. The DQ will start driving as a result of the clock edge one cycle earlier ($n + m - 1$), and provided that the relevant access times are met, the data will be valid by clock edge $n + m$. For example, assuming that the clock cycle time is such that all relevant access times are met, if a read command is registered at T0 and the latency is programmed to two clocks, the DQ will start driving after T1 and the data will be valid by T2, as shown in the Figure 5 on page 11. Table 7 on page 12, indicates the operating frequencies at which each CAS latency setting can be used.

Reserved states should not be used as unknown operation or incompatibility with future versions may result.

Operating Mode

The normal operating mode is selected by setting M7 and M8 to zero; the other combinations of values for M7 and M8 are reserved for future use and/or test modes. The programmed burst length applies to both read and write bursts.

Test modes and reserved states should not be used because unknown operation or incompatibility with future versions may result.

Write Burst Mode

When M9 = 0, the burst length programmed via M0–M2 applies to both read and write bursts; when M9 = 1, the programmed burst length applies to read bursts, but write accesses are single-location (non burst) accesses.

Table 7: CAS Latency Table

Registered mode adds one clock cycle to CAS latency

Speed	Allowable Operating Clock Frequency (MHz)	
	CAS Latency = 2	CAS Latency = 3
-13E	≤ 133	≤ 143
-133	≤ 100	≤ 133

Commands

Table 8 provides a quick reference of available commands. This is followed by a written description of each command. For a more detailed description of commands and operations refer to the 256Mb or 512Mb SDRAM component data sheets.

Table 8: SDRAM Command and DQMB Operation Truth Table
CKE is HIGH for all commands shown except Self Refresh

Name (Function)	CS#	RAS#	CAS#	WE#	DQMB	ADDR	DQs	Notes
COMMAND INHIBIT (NOP)	H	X	X	X	X	X	X	
NO OPERATION (NOP)	L	H	H	H	X	X	X	
ACTIVE (Select bank and activate row)	L	L	H	H	X	Bank/Row	X	1
READ (Select bank and column, and start READ burst)	L	H	L	H	L/H[7]	Bank/Col	X	2
WRITE (Select bank and column, and start WRITE burst)	L	H	L	L	L/H[7]	Bank/Col	Valid	2
BURST TERMINATE	L	H	H	L	X	X	Active	
PRECHARGE (Deactivate row in bank or banks)	L	L	H	L	X	Code	X	3
AUTO REFRESH or SELF REFRESH (Enter self refresh mode)	L	L	L	H	X	X	X	4, 5
LOAD MODE REGISTER	L	L	L	L	X	Op-Code	X	6
Write Enable/Output Enable	–	–	–	–	L	–	Active	7
Write Inhibit/Output High-Z	–	–	–	–	H	–	High-Z	7

Notes:
1. A0–A12 provide device row address. BA0, BA1 determine which device bank is made active.
2. A0–A9, A11 (1GB) or 0–A9, A11, A12 (2GB) provide device column address; A10 HIGH enables the auto precharge feature (nonpersistent), while A10 LOW disables the auto precharge feature; BA0, BA1 determine which device bank is being read from or written to.
3. A10 LOW: BA0, BA1 determine which device bank is being precharged. A10 HIGH: both device banks are precharged and BA0, BA1 are "Don't Care."
4. This command is Auto Refresh if CKE is HIGH, Self Refresh if CKE is LOW.
5. Internal refresh counter controls row addressing; all inputs and I/Os are "Don't Care" except for CKE.
6. A0–A12 define the op-code written to the Mode Register, and should be driven low.
7. Activates or deactivates the DQs during WRITEs (zero-clock delay) and READs (two-clock delay).

Absolute Maximum Ratings

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Figure 6: Absolute Maximum DC Ratings

Parameter	Min	Max	Units
Voltage on V_{DD} supply relative to V_{SS}	-1	+4.6	V
Voltage on inputs, NC or I/O pins relative to V_{SS}	-1	+4.6	V
Operating temperature T_{OPR} (commercial - ambient)	0	+65	°C
Storage temperature (plastic)	-55	+150	°C

DC Operating Specifications

Table 9: DC Electrical Characteristics and Operating Conditions
Notes: 1, 5, 6; notes appear on page 19; V_{DD} = V_{DDQ} = +3.3V ±0.3V

Parameter/Condition		Symbol	Min	Max	Units	Notes
Supply voltage		V_{DD}, V_{DDQ}	3	3.6	V	
Input high voltage: Logic 1; All inputs		V_{IH}	2	V_{DD} + 0.3	V	22
Input low voltage: Logic 0; All inputs		V_{IL}	-0.3	0.8	V	22
Input leakage current: Any input: 0V ≤ V_{IN} ≤ V_{DD} (All other pins not under test = 0V)	Command and address, CKE	I_I	-20	20	µA	33
	CK, DQMB, S#		-10	10		
Output leakage current: DQs are disabled; 0V ≤ V_{IN} ≤ V_{DD}	DQ	I_{OZ}	-5	5	µA	33
Output levels: Output high voltage (I_{OUT} = -4mA)		V_{OH}	2.4	–	V	
Output low voltage (I_{OUT} = 4mA)		V_{OL}	–	0.4	V	

Table 10: I_{DD} Specifications and Conditions – 1GB
SDRAM components only; Notes: 1, 5, 6, 11, 13; notes appear on page 19; V_{DD} = $V_{DD}Q$ = +3.3V ±0.3V

Parameter/Condition		Symbol	Max -13E	Max -133	Units	Notes
Operating current: Active mode; Burst = 2; READ or WRITE; ^{t}RC = ^{t}RC (MIN)		I_{DD1}[a]	2,466	2,286	mA	3, 18, 19, 30
Standby current: Power-Down mode; All device banks idle; CKE = LOW		I_{DD2}[b]	72	72	mA	30
Standby current: Active mode; CKE = HIGH; CS# = HIGH; All device banks active after ^{t}RCD met; No accesses in progress		I_{DD3}[a]	756	756	mA	3, 12, 19, 30
Operating current: Burst mode; Continuous burst; READ or WRITE; All device banks active		I_{DD4}[a]	2,466	2,466	mA	3, 18, 19, 30
Auto refresh current	^{t}RFC = ^{t}RFC (MIN)	I_{DD5}[b]	10,260	9,720	mA	3, 12
CS# = HIGH; CKE = HIGH	^{t}RFC = 7.8125µs	I_{DD6}[b]	126	126	mA	18, 19, 30, 31
Self refresh current: CKE ≤ 0.2V		I_{DD7}[b]	90	90	mA	4

Note: a - Value calculated as one module rank in this operating condition, and all other module ranks in power-down mode.
b - Value calculated reflects all module ranks in this operating condition.

Table 11: I_{DD} Specifications and Conditions – 2GB
SDRAM components only; Notes: 1, 5, 6, 11, 13; notes appear on page 19; V_{DD} = $V_{DD}Q$ = +3.3V ±0.3V

Parameter/Condition		Symbol	Max -13E	Max -133	Units	Notes
Operating current: Active mode; Burst = 2; READ or WRITE; ^{t}RC = ^{t}RC (MIN)		I_{DD1}[a]	3,906	3,636	mA	3, 18, 19, 30
Standby current: Power-Down Mode; All device banks idle; CKE = LOW		I_{DD2}[b]	72	72	mA	30
Standby current: Active Mode; CKE = HIGH; CS# = HIGH; All device banks active after ^{t}RCD met; No accesses in progress		I_{DD3}[a]	1,476	1,476	mA	3, 12, 19, 30
Operating current: Burst mode; Continuous burst; READ or WRITE; All device banks active		I_{DD4}[a]	3,276	3,276	mA	3, 18, 19, 30
Auto refresh current	^{t}RFC = ^{t}RFC (MIN)	I_{DD5}[b]	14,400	13,320	mA	3, 12
CS# = HIGH; CKE = HIGH	^{t}RFC = 7.8125µs	I_{DD6}[b]	360	360	mA	18, 19, 30, 31
Self refresh current: CKE ≤ 0.2V		I_{DD7}[b]	216	216	mA	4

Note: a - Value calculated as one module rank in this operating condition, and all other module ranks in power-down mode.
b - Value calculated reflects all module ranks in this operating condition.

Capacitance

Table 12: Capacitance
Note: 2; notes appear on page 19

Parameter	Symbol	Min	Typ	Max	Units
Input capacitance: Address and command	C_{I1}	–	8	–	pF
Input capacitance: CKE	C_{I2}	–	16	–	pF
Input capacitance: CK	C_{I2}	–	14	–	pF
Input capacitance: S#, DQMB	C_{I4}	–	5		pF
Input/Output capacitance: DQ	C_{IO}	8	–	12	pF

AC Operating Specifications

Table 13: SDRAM Component Electrical Characteristics and Recommended AC Operating Conditions

Notes: 5, 6, 8, 9, 11, 31; notes appear on page 19

AC Characteristic			-13E		-133			
Parameter		Sym	Min	Max	Min	Max	Units	Notes
Access time from CLK (pos. edge)	CL= 3	$^tAC(3)$		5.4		5.4	ns	27
	CL= 2	$^tAC(2)$		5.4		6	ns	
Address hold time		^tAH	0.8		0.8		ns	
Address setup time		^tAS	1.5		1.5		ns	
CLK high-level width		^tCH	2.5		2.5		ns	
CLK low-level width		^tCL	2.5		2.5		ns	
Clock cycle time	CL= 3	$^tCK(3)$	7		7.5		ns	23
	CL = 2	$^tCK(2)$	7.5		10		ns	23
CKE hold time		^tCKH	0.8		0.8		ns	
CKE setup time		^tCKS	1.5		1.5		ns	
CS#, RAS#, CAS#, WE#, DQM hold time		^tCMH	0.8		0.8		ns	
CS#, RAS#, CAS#, WE#, DQM setup time		^tCMS	1.5		1.5		ns	
Data-in hold time		^tDH	0.8		0.8		ns	
Data-in setup time		^tDS	1.5		1.5		ns	
Data-out High-Z time	CL = 3	$^tHZ(3)$		5.4		5.4	ns	10
	CL = 2	$^tHZ(2)$		5.4		6	ns	10
Data-out Low-Z time		^tLZ	1		1		ns	
Data-out hold time (load)		^tOH	3		3		ns	
Data-out hold time (no load)		^tOH_N	1.8		1.8		ns	28
ACTIVE-to-PRECHARGE command		^tRAS	37	120,000	44	120,000	ns	29
ACTIVE-to-ACTIVE command period		^tRC	60		66		ns	
ACTIVE-to-READ or WRITE delay		^tRCD	15		20		ns	
Refresh period		^tREF		64		64	ms	
Auto refresh period		^tRFC	66		66		ns	
PRECHARGE command period		^tRP	15		20		ns	
ACTIVE bank *a* to ACTIVE bank *b* command		^tRRD	14		15		ns	
Transition time		^tT	0.3	1.2	0.3	1.2	ns	7
WRITE recovery time		^tWR	1 CLK + 7ns		1 CLK + 7.5ns		ns	24
			14		15		ns	25
Exit SELF REFRESH-to-ACTIVE command		^tXSR	67		75		ns	20

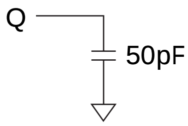
Table 14: AC Functional Characteristics

Notes: 5, 6, 7, 8, 9, 11, 31; notes appear on page 19

Parameter		Symbol	-13E	-133	Units	Notes
READ/WRITE command to READ/WRITE command		^{t}CCD	1	1	^{t}CK	17
CKE to clock disable or power-down entry mode		^{t}CKED	1	1	^{t}CK	14, 34
CKE to clock enable or power-down exit setup mode		^{t}PED	1	1	^{t}CK	14, 34
DQM to input data delay		^{t}DQD	0	0	^{t}CK	17, 34
DQM to data mask during WRITEs		^{t}DQM	0	0	^{t}CK	17, 34
DQM to data High-Z during READs		^{t}DQZ	2	2	^{t}CK	17, 34
WRITE command to input data delay		^{t}DWD	0	0	^{t}CK	17, 34
Data-in to ACTIVE command		^{t}DAL	4	5	^{t}CK	15, 21, 34
Data-in to PRECHARGE command		^{t}DPL	2	2	^{t}CK	16, 21, 34
Last data-in to burst STOP command		^{t}BDL	1	1	^{t}CK	17, 34
Last data-in to new READ/WRITE command		^{t}CDL	1	1	^{t}CK	17, 34
Last data-in to PRECHARGE command		^{t}RDL	2	2	^{t}CK	16, 21, 34
LOAD MODE REGISTER command to ACTIVE or REFRESH command		^{t}MRD	2	2	^{t}CK	26
Data-out to High-Z from PRECHARGE command	CL= 3	^{t}ROH(3)	3	3	^{t}CK	17, 34
	CL = 2	^{t}ROH(2)	2	2	^{t}CK	17, 34

Notes

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. V_{DD} = $V_{DD}Q$ = +3.3V ±0.3V; f = 1 MHz, T_A = 25°C; pin under test biased at 1.4V.
3. I_{DD} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
4. Enables on-chip refresh and address counters.
5. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is ensured; (0°C ≤ T_A ≤ 55°C).
6. An initial pause of 100µs is required after power-up, followed by two AUTO REFRESH commands, before proper device operation is ensured. (V_{DD} and $V_{DD}Q$ must be powered up simultaneously. Vss and $V_{SS}Q$ must be at same potential.) The two AUTO REFRESH command wake-ups should be repeated any time the ^{t}REF refresh requirement is exceeded.
7. AC characteristics assume ^{t}T = 1ns.
8. In addition to meeting the transition rate specification, the clock and CKE must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
9. Outputs measured at 1.5V with equivalent load:



10. ^{t}HZ defines the time at which the output achieves the open circuit condition; it is not a reference to V_{OH} or V_{OL}. The last valid data element will meet ^{t}OH before going High-Z.
11. AC timing and I_{DD} tests have V_{IL} = 0V and V_{IH} = 3.0V, using a measurement reference level of 1.5V. If the input transition time is longer than 1ns, then the timing is measured from V_{IL} (MAX) and V_{IH} (MIN) and no longer at the 1.5V midpoint. CLK should always be referenced to crossover. Refer to Micron Technical Note TN-48-09.
12. Other input signals are allowed to transition no more than once every two clocks and are otherwise at valid V_{IH} or V_{IL} levels.
13. I_{DD} specifications are tested after the device is properly initialized.
14. Timing actually specified by ^{t}CKS; clock(s) specified as a reference only at minimum cycle rate.
15. Timing actually specified by ^{t}WR + ^{t}RP; clock(s) specified as a reference only at minimum cycle rate.
16. Timing actually specified by ^{t}WR.
17. Required clocks are specified by JEDEC functionality and are not dependent on any timing parameter.
18. The I_{DD} current will increase or decrease proportionally according to the amount of frequency alteration for the test condition.
19. Address transitions average one transition every two clocks.
20. CLK must be toggled a minimum of two times during this period.
21. Based on ^{t}CK = 7.5ns for -133 and -13E.

22. V_{IH} overshoot: V_{IH} (MAX) = V_{DDQ} + 2V for a pulse width ≤ 3ns, and the pulse width cannot be greater than one third of the cycle rate. V_{IL} undershoot: V_{IL} (MIN) = -2V for a pulse width ≤ 3ns for all inputs except A12. V_{IH} overshoot for pin A12 is limited to V_{DDQ} + 1V for a pulse width ≤ 3ns, and the pulse width cannot be greater than one third of the cycle rate.
23. The clock frequency must remain constant (stable clock is defined as a signal cycling within timing constraints specified for the clock pin) during access or precharge states (READ, WRITE, including ^tWR, and PRECHARGE commands). CKE may be used to reduce the data rate.
24. Auto precharge mode only. The precharge timing budget (^tRP) begins 7ns for -13E; and 7.5ns for -133 after the first clock delay, after the last WRITE is executed.
25. Precharge mode only.
26. JEDEC and PC100 specify three clocks.
27. ^tAC for -133/-13E at CL = 3 with no load is 4.6ns and is guaranteed by design.
28. Parameter guaranteed by design.
29. For -133, CL = 3 and ^tCK = 7.5ns; for -13E, CL = 2 and ^tCK = 7.5ns.
30. CKE is HIGH during refresh command period ^tRFC (MIN) else CKE is LOW. The I_{DD6} limit is actually a nominal value and does not result in a fail value.
31. Refer to component data sheet for timing waveforms.
32. The value for ^tRAS used in -13E speed grade modules is calculated from ^tRC - ^tRP = 45ns.
33. Leakage number reflects the worst case leakage possible through the module pin, not what each memory device contributes.
34. This AC timing function will show an extra clock cycle when in registered mode.

Timing Requirements and Switching Characteristics

Table 15: Register Timing Requirements and Switching Characteristics

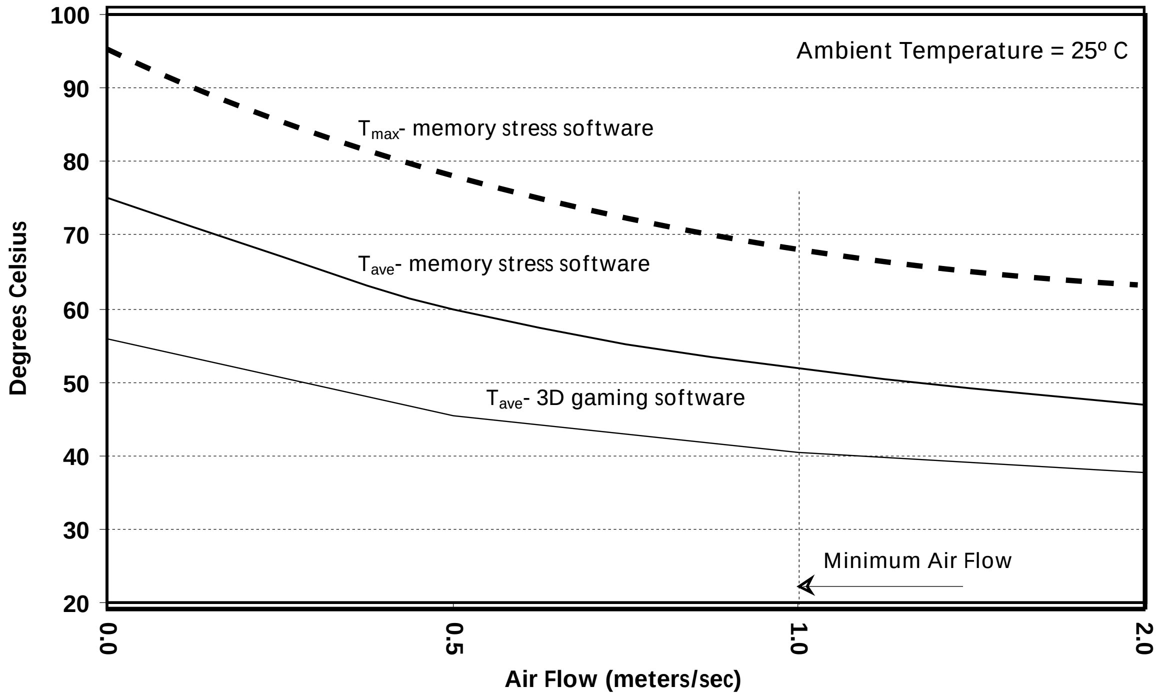
Register	Symbol	Parameter	Condition	$0°C \le T_A \le 55°C$ VDD = +3.3V ±0.3V		Units
				Min	Max	
SSTL bit pattern by JESD82-2	f_{clock}	Clock frequency		150	240	MHz
	t_{pd1}	Propagation delay, single rank (CK to Output)	50pF to GND and 50 Ohms to Vtt	1.4	3.5	ns
	t_{pd2}	propagation delay, dual rank (CK to output)	30pF to GND and 50Ω to VTT	0.7	2.4	ns
	t_w	Pulse duration	CK, HIGH or LOW	3.3	–	ns
	t_{su}	Setup time	Data before CK HIGH	.75	–	ns
	t_h	Hold time	Data after CK HIGH	.75	–	ns

Table 16: PLL Clock Driver Timing Requirements And Switching Characteristics

Parameter	Symbol	$0°C \le T_A \le 55°C$ VDD = +3.3V ±0.3V		Units	Notes
		Min	Max		
Operating clock frequency	^{f}CK	50	140	MHz	
Input duty cycle	^{t}DC	44	55	%	
Cycle to cycle jitter	$^{t}JIT_{CC}$	-75	75	ps	
Static phase offset	$^{t}\varnothing$	-150	150	ps	
SSC induced skew	^{t}SSC	–	150	ps	1, 2
Output to output skew	$^{t}SK_O$	–	150	ps	

Notes: 1. SSC = Spread Spectrum Clock. the use of SSC synthesizers on the system motherboard will reduce EMI.
2. Skew is defined as the total clock skew between any two outputs and is therefore specified as a maximum only.

Figure 7: Component Case Temperature vs. Airflow



Notes:
1. Micron Technology, Inc. recommends a minimum air flow of 1 meter/second (~197 LFM) across all modules when installed in a system.
2. The component case temperature measurements shown above are obtained experimentally. The system used for experimental purposes is a dual-processor 600 MHz work station, fully loaded with four MT36LSDT12872G modules. Case temperatures charted represent worst-case component locations on modules installed in the internal slots of the system.
3. Temperature versus air speed data is obtained by performing experiments with the system motherboard removed from its case and mounted in a Eiffel-type low air speed wind tunnel. Peripheral devices installed on the system motherboard for testing are the processor(s) and video card, all other peripheral devices are mounted outside of the wind tunnel test chamber.
4. The memory diagnostic software used for determining worst-case component temperatures is a memory diagnostic software application developed for internal use by Micron Technology, Inc.

Serial Presence Detect

SPD Clock and Data Conventions

Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions (as shown in Figure 8, and Figure 9 on page 24).

SPD Start Condition

All commands are preceded by the start condition, which is a HIGH-to-LOW transition of SDA when SCL is HIGH. The SPD device continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met.

SPD Stop Condition

All communications are terminated by a stop condition, which is a LOW-to-HIGH transition of SDA when SCL is HIGH. The stop condition is also used to place the SPD device into standby power mode.

SPD Acknowledge

Acknowledge is a software convention used to indicate successful data transfers. The transmitting device, either master or slave, will release the bus after transmitting eight bits. During the ninth clock cycle, the receiver will pull the SDA line LOW to acknowledge that it received the eight bits of data (as shown in Figure 10 on page 24).

The SPD device will always respond with an acknowledge after recognition of a start condition and its slave address. If both the device and a WRITE operation have been selected, the SPD device will respond with an acknowledge after the receipt of each subsequent eight bit word. In the read mode the SPD device will transmit eight bits of data, release the SDA line and monitor the line for an acknowledge. If an acknowledge is detected and no stop condition is generated by the master, the slave will continue to transmit data. If an acknowledge is not detected, the slave will terminate further data transmissions and await the stop condition to return to standby power mode.

Figure 8: Data Validity

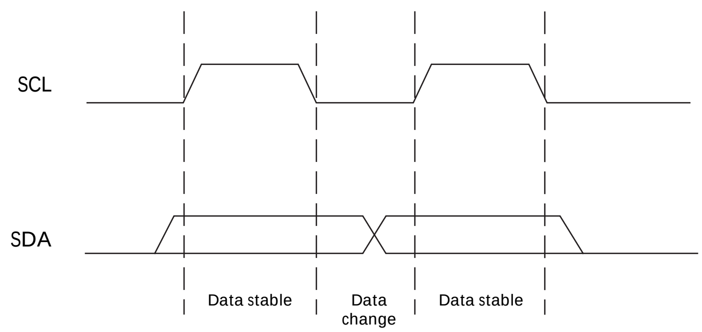


Figure 9: Definition of Start and Stop

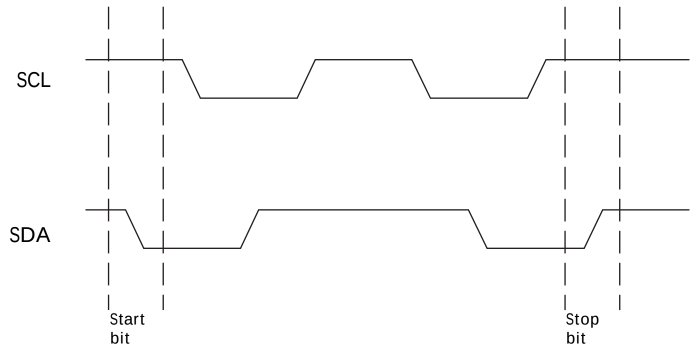


Figure 10: Acknowledge Response From Receiver

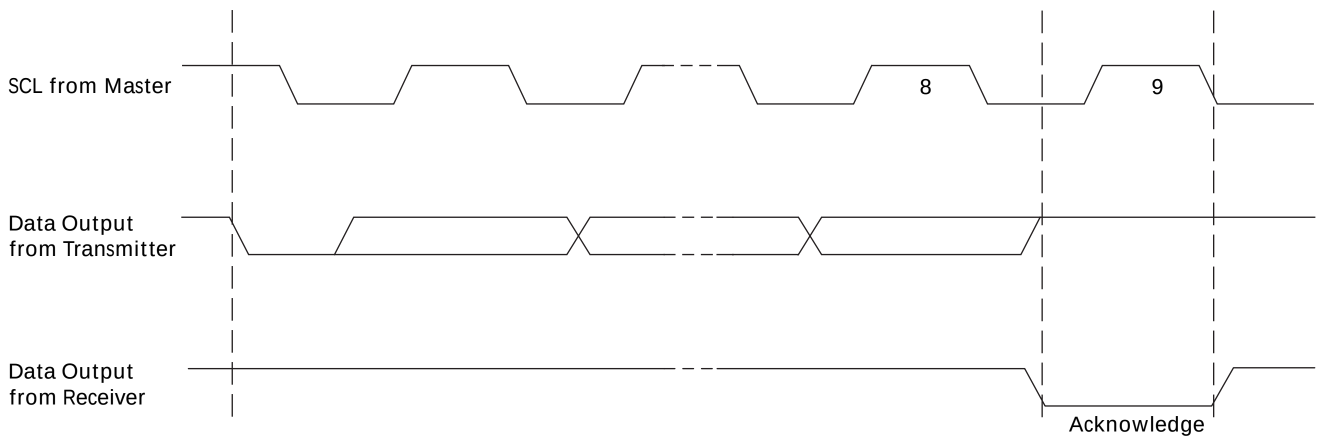


Table 17: EEPROM Device Select Code
The most significant bit (b7) is sent first

Select Code	Device Type Identifier				Chip Enable			$R\overline{W}$
	b7	b6	b5	b4	b3	b2	b1	b0
Memory area select code (two arrays)	1	0	1	0	SA2	SA1	SA0	$R\overline{W}$
Protection register select code	0	1	1	0	SA2	SA1	SA0	$R\overline{W}$

Table 18: EEPROM Operating Modes

Mode	$R\overline{W}$ Bit	$\overline{WC}$	BYTES	Initial Sequence
Current address read	1	V_{IH} or V_{IL}	1	Start, device select, $R\overline{W}$ = 1
Random address read	0	V_{IH} or V_{IL}	1	Start, device select, $R\overline{W}$ = 0, address
	1	V_{IH} or V_{IL}		Restart, device select, $R\overline{W}$ = 1
Sequential read	1	V_{IH} or V_{IL}	≥ 1	Similar to current or random address read
Byte write	0	V_{IL}	1	Start, device select, $R\overline{W}$ = 0
Page write	0	V_{IL}	≤ 16	Start, device select, $R\overline{W}$ = 0

Figure 11: SPD EEPROM Timing Diagram

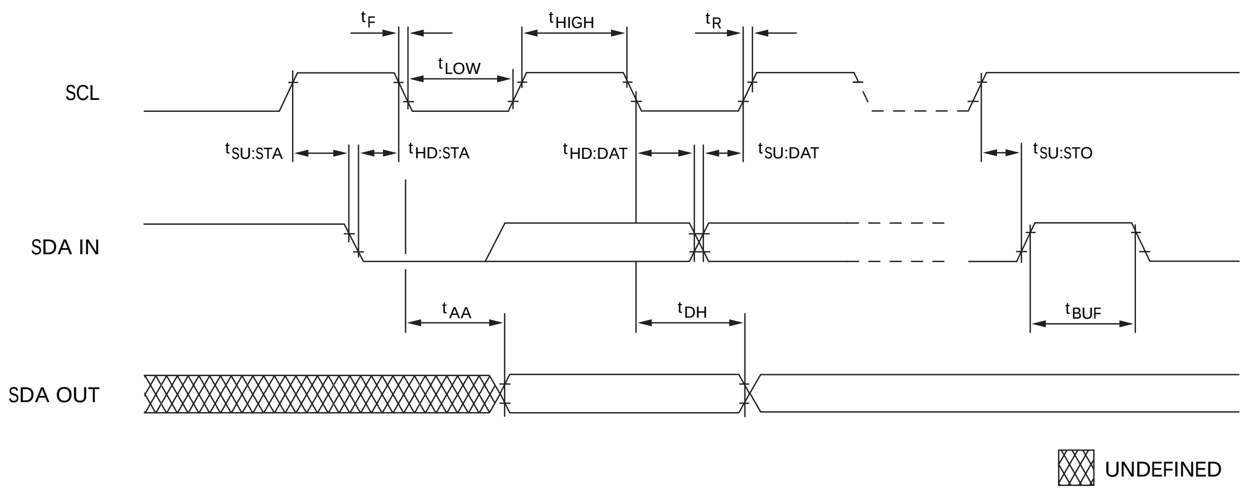


Table 19: Serial Presence-Detect EEPROM DC Operating Conditions

All voltages referenced to V_{SS}; V_{DDSPD} = +2.3V to +3.6V

Parameter/Condition	Symbol	Min	Max	Units
Supply voltage	V_{DD}	3	3.6	V
Input high voltage: Logic 1; All inputs	V_{IH}	V_{DD} x 0.7	V_{DD} + 0.5	V
Input low voltage: Logic 0; All inputs	V_{IL}	-1	V_{DD} x 0.3	V
Output low voltage: I_{OUT} = 3mA	V_{OL}	–	0.4	V
Input leakage current: V_{IN} = GND to V_{DD}	I_{LI}	-10	10	µA
Output leakage current: V_{OUT} = GND to V_{DD}	I_{LO}	-10	10	µA
Standby current: SCL = SDA = V_{DD} - 0.3V; All other inputs = V_{SS} or V_{DD}	I_{CCS}	–	30	µA
Power supply current: SCL clock frequency = 100 KHz	I_{CC} Write	–	3	mA
	I_{CC} Read	–	1	mA

Table 20: Serial Presence-Detect EEPROM AC Operating Conditions

All voltages referenced to V_{SS}; V_{DDSPD} = +2.3V to +3.6V

Parameter/Condition	Symbol	Min	Max	Units	Notes
SCL LOW to SDA data-out valid	^{t}AA	0.2	0.9	µs	1
Time the bus must be free before a new transition can start	^{t}BUF	1.3		µs	
Data-out hold time	^{t}DH	200		ns	
SDA and SCL fall time	^{t}F		300	ns	2
Data-in hold time	$^{t}HD:DAT$	0		µs	
Start condition hold time	$^{t}HD:STA$	0.6		µs	
Clock HIGH period	$^{t}HIGH$	0.6		µs	
Noise suppression time constant at SCL, SDA inputs	^{t}I		50	ns	
Clock LOW period	^{t}LOW	1.3		µs	
SDA and SCL rise time	^{t}R		0.3	µs	2
SCL clock frequency	^{f}SCL		400	KHz	
Data-in setup time	$^{t}SU:DAT$	100		ns	
Start condition setup time	$^{t}SU:STA$	0.6		µs	3

Table 20: Serial Presence-Detect EEPROM AC Operating Conditions
All voltages referenced to V_{SS}; V_{DDSPD} = +2.3V to +3.6V

Parameter/Condition	Symbol	Min	Max	Units	Notes
Stop condition setup time	$^tSU:STO$	0.6		µs	
WRITE cycle time	^tWRC		10	ms	4

Notes:
1. To avoid spurious START and STOP conditions, a minimum delay is placed between SCL=1 and the falling or rising edge of SDA.
2. This parameter is sampled.
3. For a reSTART condition, or following a WRITE cycle.
4. The SPD EEPROM WRITE cycle time (^tWRC) is the time from a valid stop condition of a write sequence to the end of the EEPROM internal erase/program cycle. During the WRITE cycle, the EEPROM bus interface circuit is disabled, SDA remains HIGH due to pull-up resistor, and the EEPROM does not respond to its slave address.

Table 21: Serial Presence-Detect Matrix
"1"/"0": Serial data, "driven to HIGH"/"driven to LOW"; VDD = +3.3V ±0.3V

Byte	Description	Entry (Version)	MT36LSDT12872	MT36LSDT25672
0	Number of bytes used by Micron	128	80	80
1	Total number of SPD memory bytes	256	08	08
2	Memory type	SDRAM	04	04
3	Number of row addresses	13	0D	0D
4	Number of column addresses	11 or 12	0B	0C
5	Number of module ranks	2	02	02
6	Module data width	72	48	48
7	Module data width (continued)	0	00	00
8	Module voltage interface levels	LVTTL	01	01
9	SDRAM cycle time, ^{t}CK (CAS latency = 3)	7ns (-13E) 7.5ns (-133)	70 75	70 75
10	SDRAM access from clock, ^{t}AC (CAS latency = 3)	5.4ns (-13E/-133)	54	54
11	Module configuration type	ECC	02	02
12	Refresh rate/type	7.81µs/SELF	82	82
13	SDRAM width (primary SDRAM)	4	04	04
14	Error-checking SDRAM data width	4	04	04
15	Minimum clock delay from back-to-back random column addresses,^{t}CCD	1	01	01
16	Burst lengths supported	1, 2, 4, 8, PAGE	8F	8F
17	Number of banks on SDRAM device	4	04	04
18	CAS latencies supported	2, 3	06	06
19	CS latency	0	01	01
20	WE latency	0	01	01
21	SDRAM module attributes	-13E/-133	1F	1F
22	SDRAM device attributes: General	0E	0E	0E
23	SDRAM cycle time, ^{t}CK (CAS latency = 2)	7.5ns (-13E)	75	75
24	SDRAM access from clock, ^{t}AC (CAS latency = 2)	5.4ns (-13E)	54	54
25	SDRAM cycle time, ^{t}CK (CAS latency = 1)	–	00	00
26	SDRAM access from clock, ^{t}AC (CAS latency = 1)	–	00	00
27	Minimum row precharge time, ^{t}RP	15ns (-13E) 20ns (-133)	0F 14	0F 14
28	Minimum row active to row active, ^{t}RRD	14ns (-13E) 15ns (-133)	0E 0F	0E 0F
29	Minimum RAS# to CAS# delay, ^{t}RCD	15ns (-13E) 20ns (-133)	0F 14	0F 14
30	Minimum RAS# pulse width, ^{t}RAS (See note 1)	45ns (-13E) 44ns (-133)	2D 2C	2D 2C
31	Module rank density	512MB / 1GB	80	01
32	Command and address setup time, ^{t}AS, ^{t}CMS	1.5ns (-13E/-133)	15	15
33	Command and address hold time, ^{t}AH, ^{t}CMH	0.8ns (-13E/-133)	08	08
34	Data signal input setup time, ^{t}DS	1.5ns (-13E/-133)	15	15

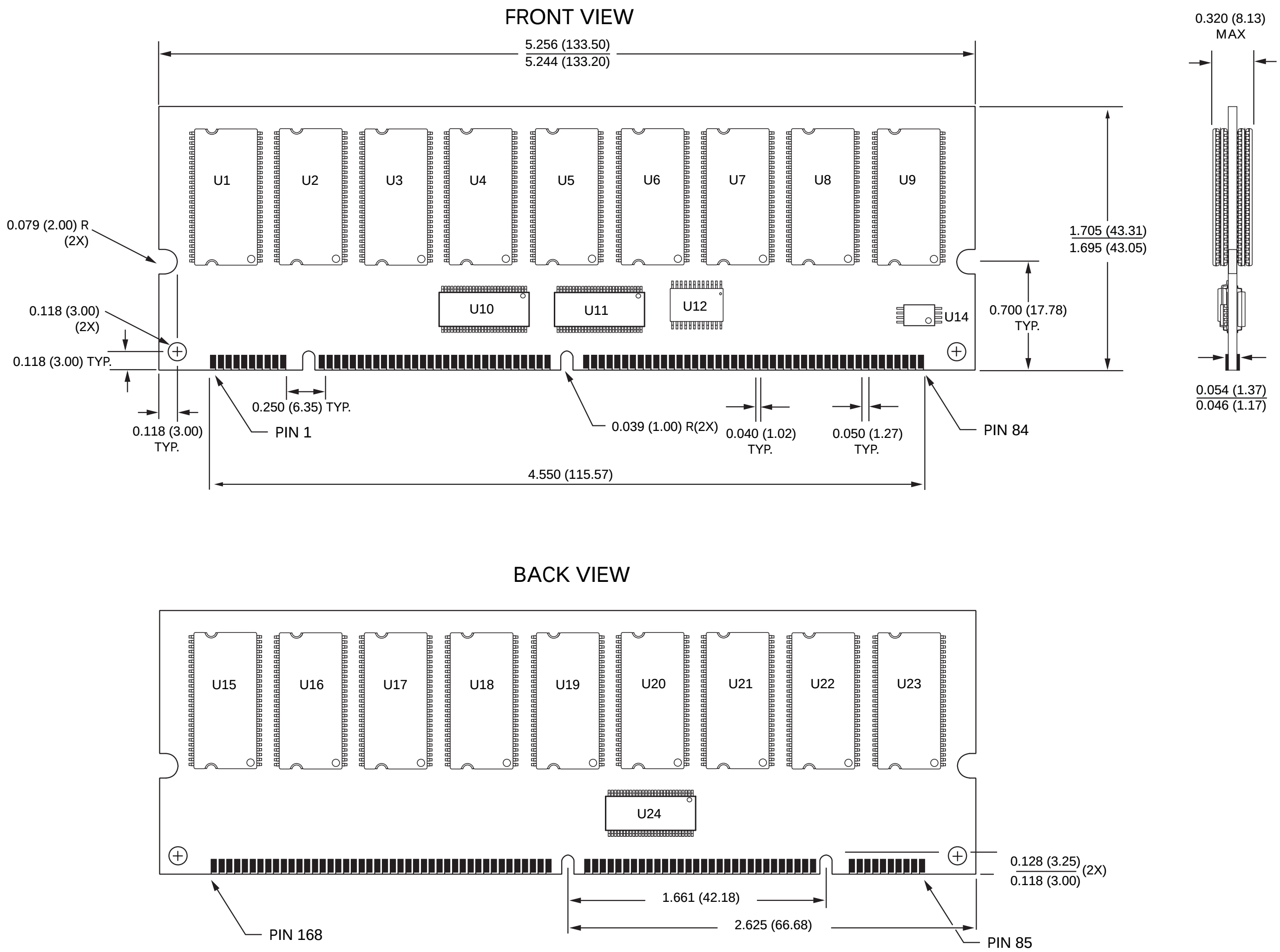
Table 21: Serial Presence-Detect Matrix (Continued)
"1"/"0": Serial data, "driven to HIGH"/"driven to LOW"; V_{DD} = +3.3V ±0.3V

Byte	Description	Entry (Version)	MT36LSDT12872	MT36LSDT25672
35	Data signal input hold time, ^{t}DH	0.8ns (-13E/-133)	08	08
36–40	Reserved		00	00
41	Device minimum active/auto-refresh time, ^{t}RC	66ns (-13E) 71ns (-133)	3C 42	3C 42
42–61	Reserved		00	00
62	SPD revision	REV. 2.0	02	02
63	Checksum for bytes 0–62	-13E -133	22 6E	A4 F0
64	Manufacturer's JEDEC ID code	MICRON	2C	2C
65–71	Manufacturer's JEDEC ID code (continued)		FF	FF
72	Manufacturing location	1–9	01–09	01–09
73–90	Module part number (ASCII)		Variable Data	Variable Data
91	PCB identification code	1–12	01–0C	01–0C
92	Identification code (continued)	0	00	00
93	Year of manufacture in BCD		Variable Data	Variable Data
94	Week of manufacture in BCD		Variable Data	Variable Data
95–98	Module serial number		Variable Data	Variable Data
99–125	Manufacturer-Specific data (RSVD)		–	–
126	System frequency	100 MHz (-13E/-133)	64	64
127	SDRAM component and clock detail		8F	8F

Notes: 1. The value of ^{t}RAS used for the -13E module is calculated from ^{t}RC - ^{t}RP. Actual device specification value is 37ns.

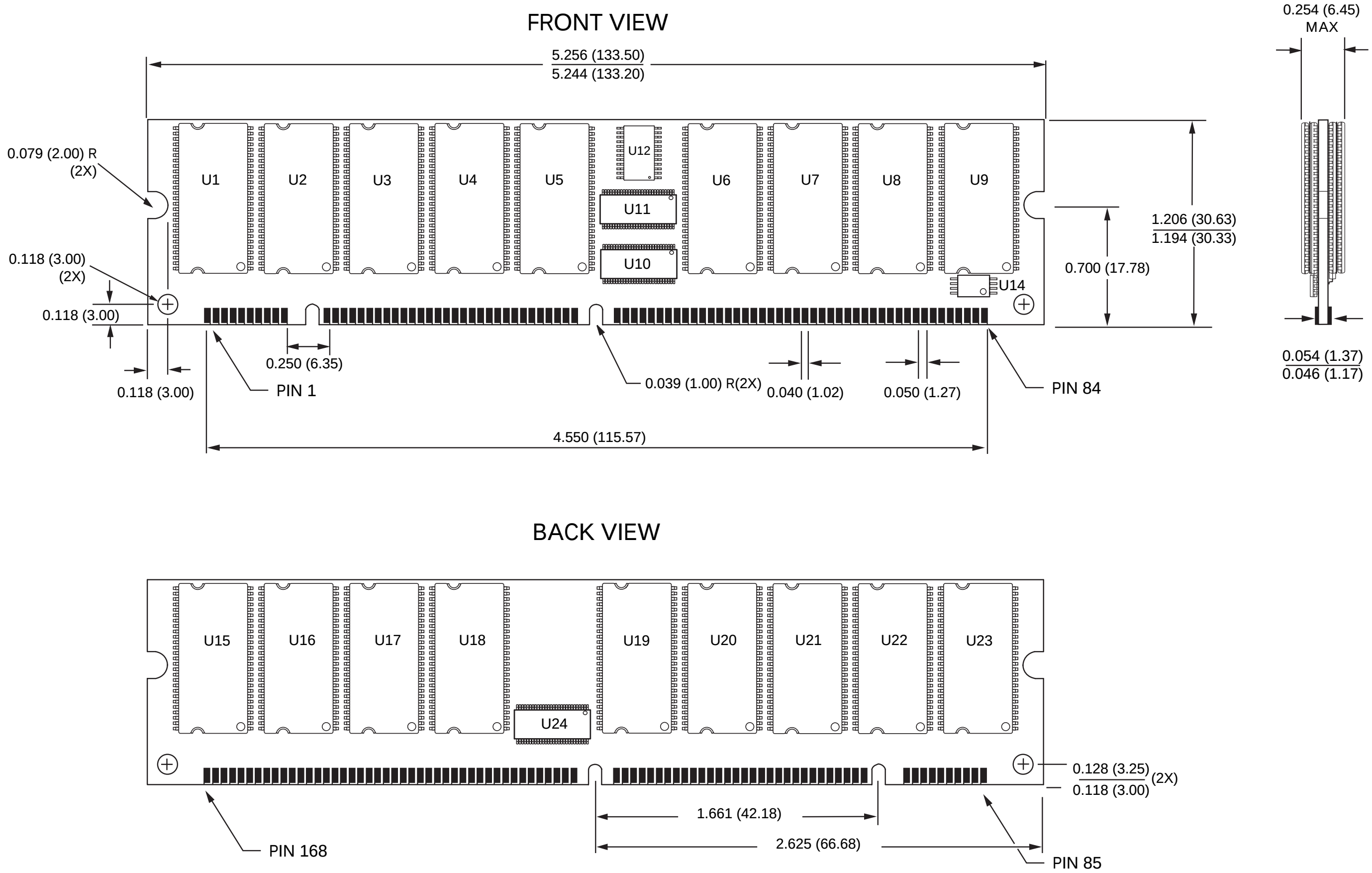
Module Dimensions

Figure 12: 168-Pin DIMM Dimensions – Standard PCB



Note:All dimensions in inches (millimeters); $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

Figure 13: 168-Pin DIMM Dimensions – Low-Profile



Note:All dimensions in inches (millimeters); $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

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This data sheet contains minimum and maximum limits specified over the complete power supply and temperature range for production devices. Although considered final, these specifications are subject to change, as further product development and data characterization sometimes occur.