Dear customer

LAPIS Semiconductor Co., Ltd. ("LAPIS Semiconductor"), on the 1st day of October, 2020, implemented the incorporation-type company split (shinsetsu-bunkatsu) in which LAPIS established a new company, LAPIS Technology Co., Ltd. (“LAPIS Technology”) and LAPIS Technology succeeded LAPIS Semiconductor’s LSI business.

Therefore, all references to "LAPIS Semiconductor Co., Ltd.", "LAPIS Semiconductor" and/or "LAPIS" in this document shall be replaced with "LAPIS Technology Co., Ltd."

Furthermore, there are no changes to the documents relating to our products other than the company name, the company trademark, logo, etc.

Thank you for your understanding.

LAPIS Technology Co., Ltd.
October 1, 2020

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ML610Q304

8-bit Microcontroller with Voice Output Function

■GENERAL DESCRIPTION

Equipped with a 8-bit CPU nX-U8/100, the ML610Q304 is a high-performance 8-bit CMOS microcontroller that integrates a wide variety of peripherals such as timer, synchronous serial port, and voice output function. The nX-U8/100 CPU is capable of executing instructions efficiently on a one-instruction-per-clock-pulse basis through parallel processing by the 3-stage pipelined architecture. The ML610Q304 is also equipped with a flash memory that has achieved low voltage and low power consumption (at read) equivalent to mask ROMs, so it is best suited to battery-driven applications such as alarm and portable devices. In addition, it has an on-chip debugging function, which allows software debugging/rewriting with the LSI mounted on the board.

■FEATURES

•CPU
- 8-bit RISC CPU (CPU name: nX-U8/100)
- Instruction system: 16-bit instructions
- Instruction set: Transfer, arithmetic operations, comparison, logic operations, multiplication/division, bit manipulations, bit logic operations, jump, conditional jump, call return stack manipulations, arithmetic shift, and so on
- On-Chip debug function
- Minimum instruction execution time
  Approx 30.5 µs (@32.768kHz system clock)
  Approx 0.244 µs (@4.096 MHz system clock)@V_{DD}=2.0 to 5.5V
  Approx 0.122 µs (@8.192 MHz system clock)@V_{DD}=2.2 to 5.5V

•Internal memory
- Has 96-Kbyte flash ROM(48K × 16-bits) built in. (1 K byte of test domain that it cannot be used is included)
- Has 2-Kbyte flash ROM built in. (area in which self rewriting is possible (512byte × 4))
- Internal 1Kbyte RAM (1K × 8 bits)

•Interrupt controller
- 2 non-maskable interrupt sources (Internal source: 1, External source: 1)
- 24 maskable interrupt sources (Internal source: 16, External source: 8)

•Time base counter
- Low-speed time base counter × 1 channel
- High-speed time base counter × 1 channel

•Watchdog timer
- Generates a non-maskable interrupt upon the first overflow and a system reset occurs upon the second
- Free running
- Overflow period: 4 types selectable (125ms, 500ms, 2s, and 8s)

•Timers
- 8 bits × 4ch (16-bit configuration available)

•Voice output function
- Voice synthesis method: 4-bit ADPCM2 / non-linear PCM / straight 8-bit PCM / straight 16-bit PCM
- Sampling frequency: 8/16/32 kHz; 10.7/21.3 kHz; 6.4/12.8/25.6 kHz

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•Successive approximation type A/D converter
- 10-bit A/D converter
- Input: 3ch (ch0-2:External input)
- Conversion time: 24.4 μs per channel at 4.096MHz V_{DD}≧2.2V
- Conversion time: 12.2 μs per channel at 8.192MHz V_{DD}≧2.5V

•Synchronous serial port
- 2ch
- Master/slave selectable
- LSB first/MSB first selectable
- 8-bit length/16-bit length selectable

•UART
- Half-duplex × 1ch
- TXD/RXD
- Bit length, parity/no parity, odd parity/even parity, 1 stop bit/2 stop bits
- Positive logic/negative logic selectable
- Built-in baud rate generator

•I^2C bus interface
- Slave function and Master function
- Fast mode (400 kbps), standard mode (100 kbps)

•General-purpose ports
- Input-only port × 1ch
- Output-only port × 3ch (including secondary functions)
- Input/output × 11ch (including secondary functions)(P40 to P42 uses also as an A/D converter input port.)

•Speaker amplifier(D-class) output power
- 1.0W(at 5.0V)/0.45W(at 3.0V)
- Disconnection detection circuit
- Speaker pin short detection circuit
- PLL oscillation stop detection reset

•Reset
- Reset through the RESET_N pin
- Power-on reset generation when powered on
- Reset by the watchdog timer (WDT) overflow
- PLL oscillation stop detection reset

•Clock
- Low-speed clock
  Built-in RC oscillation (32.768 kHz)
- High-speed clock
  Built-in PLL oscillation (4.096MHz,8.192MHz,etc)

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•Power management
- STOP mode: Stop of oscillation (Operations of CPU and peripheral circuits are stopped.)
- HALT mode: Instruction execution by CPU is suspended (peripheral circuits are in operating states).
- Clock gear: The frequency of high-speed system clock can be changed by software (1/1, 1/2, 1/4, or 1/8 of the oscillation clock)
- Block control function: Operation of an intact functional block circuit is powerd down. (register reset and clock stop)

•Shipment
- 28-pin QFN
  ML610Q304-xxxGD (blank product: ML610Q304-NNNGD)
  xxx: ROM code number

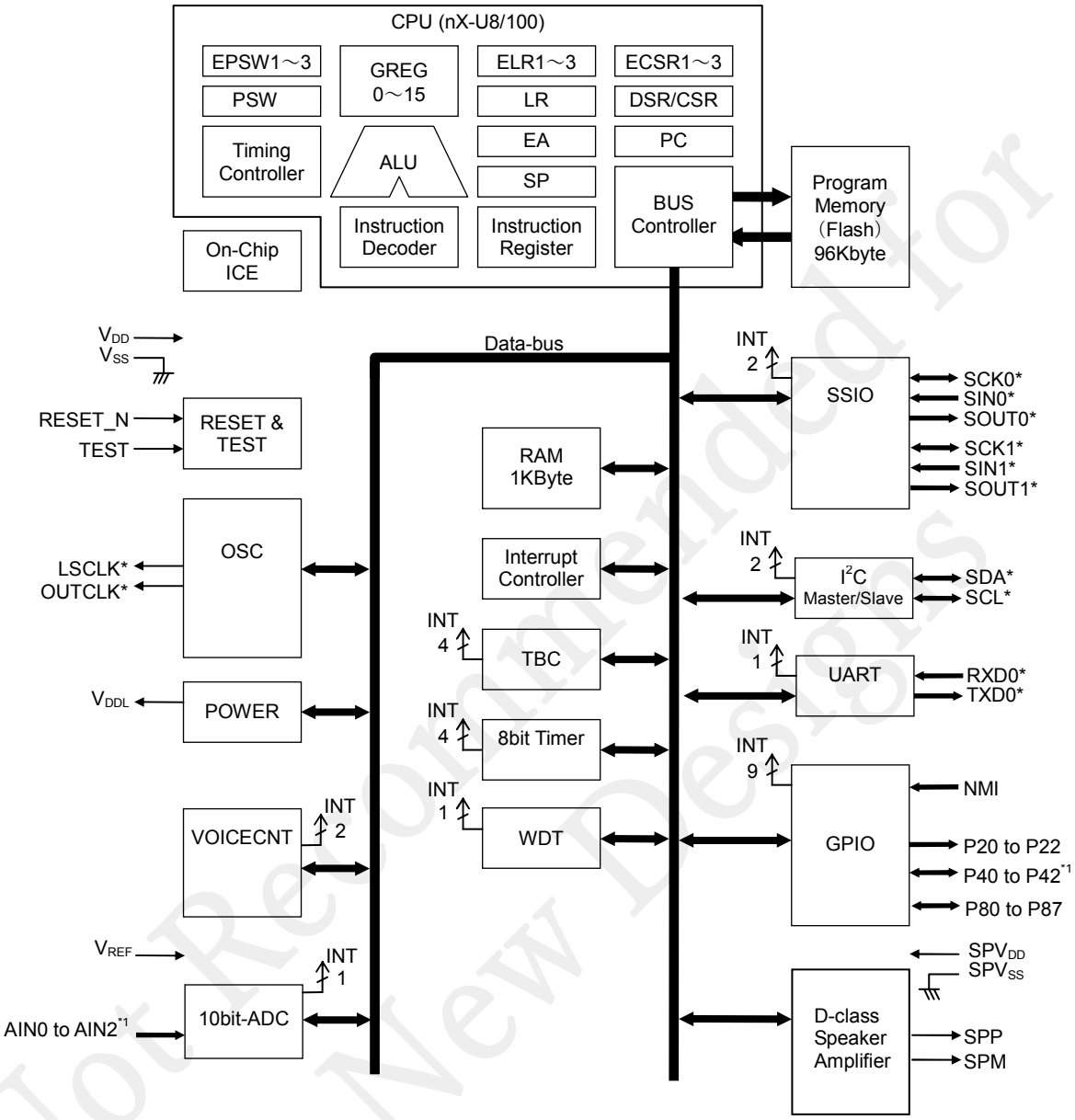
•Guaranteed operating range
- Operating temperature: –40°C to 85°C
- Operating voltage: V_{DD} = 2.0V to 5.5V, SPV_{DD} = 2.0V to 5.5V

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■BLOCK DIAGRAM

Figure 1 is a block diagram of the ML610Q304.



* : Secondary or tertiary function
*1: I/O port or A/D converter input terminal

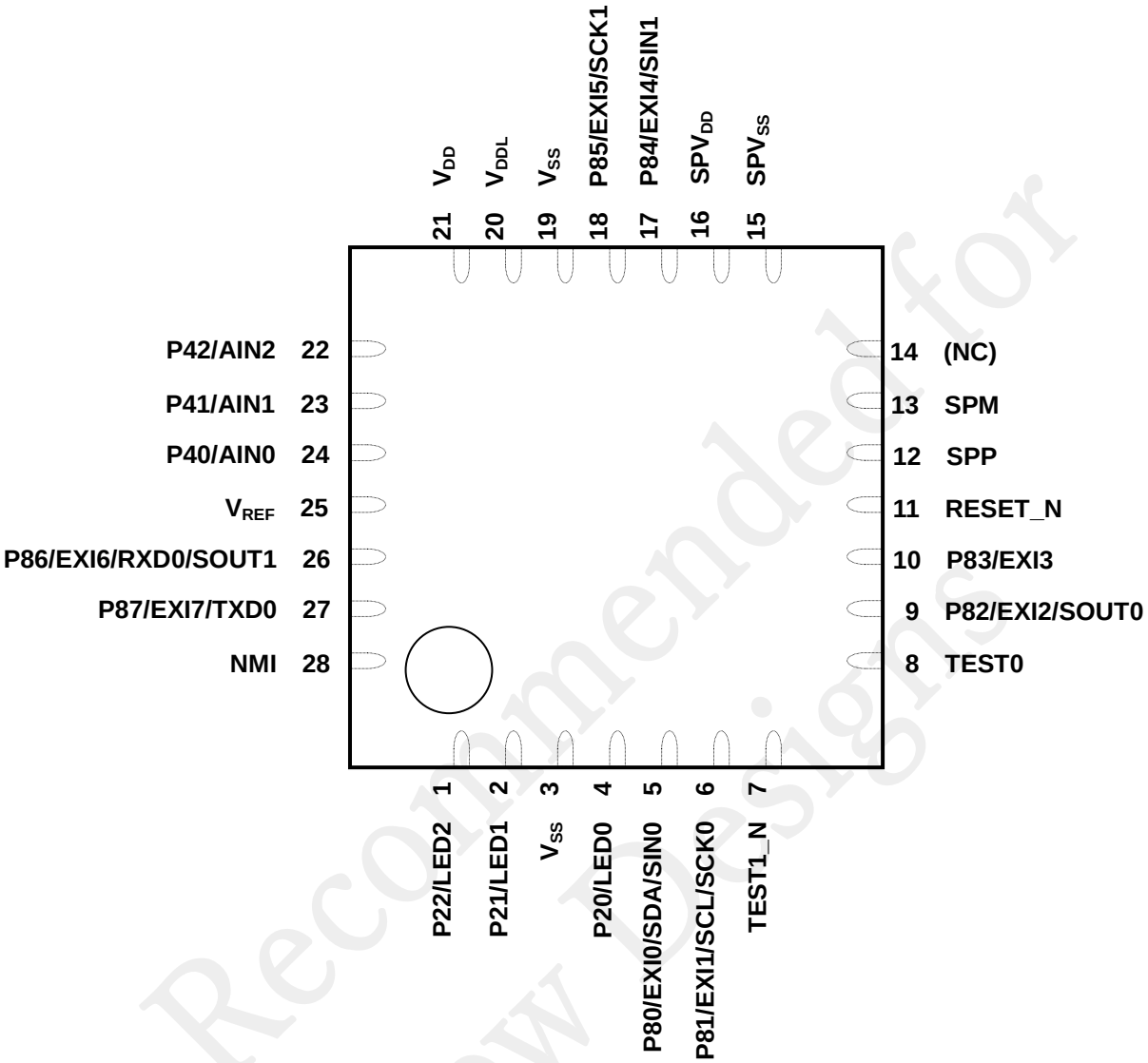
Figure 1-1 Block Diagram of ML610Q304

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■PIN CONFIGURATION

● ML610Q304 QFN package product (Top View)



(NC): No Connection

Figure 1-2 Pin Layout of ML610Q304 Package

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■LIST OF PINS

In the I/O column, "—" denotes an input pin (for primary functions only), "I" an input pin, "O" an output pin, and "I/O" an input/output pin.

PAD No	Primary function			Secondary function			Tertiary function		
	Pin name	I/O	Description	Pin name	I/O	Description	Pin name	I/O	Description
12	SPP	O	Positive output pin of the built-in speaker amplifier	—	—	—	—	—	—
13	SPM	O	Negative output pin of the built-in speaker amplifier	—	—	—	—	—	—
15	SPV_{SS}	—	Negative power supply pin for built-in speaker amplifier	—	—	—	—	—	—
16	SPV_{DD}	—	Positive power supply pin for built-in speaker amplifier	—	—	—	—	—	—
3	V_{SS}	—	Negative power supply pin	—	—	—	—	—	—
19	V_{SS}	—	Negative power supply pin	—	—	—	—	—	—
20	V_{DDL}	—	Power supply for internal logic (internally generated)	—	—	—	—	—	—
21	V_{DD}	—	Positive power supply pin	—	—	—	—	—	—
25	V_{REF}	—	Reference power supply pin for successive-approximation type ADC	—	—	—	—	—	—
11	RESET_N	I	Reset input pin	—	—	—	—	—	—
8	TEST0	I/O	Input/output pin for testing	—	—	—	—	—	—
7	TEST1_N	I	Input pin for testing	—	—	—	—	—	—
28	NMI	I	Input port, non-maskable interrupt	—	—	—	—	—	—
4	P20/LED0	O	Output port / LED port	LSCLK	O	Low-speed clock output	—	—	—
2	P21/LED1	O	Output port / LED port	OUTCLK	O	high-speed clock output	—	—	—
1	P22/LED2	O	Output port / LED port	—	—	—	—	—	—
24	P40/AIN0	I/O	Input port/Output port /Successive-approximation type ADC input	—	—	—	SIN0	I	SSIO0 data input
23	P41/AIN1	I/O	Input port/Output port /Successive-approximation type ADC input	—	—	—	SCK0	I/O	SSIO0 synchronous clock input/output
22	P42/AIN2	I/O	Input port/Output port /Successive-approximation type ADC input	—	—	—	SOUT0	O	SSIO0 data output
5	P80/EXI0	I/O	Input port/Output port / External interrupt	SDA	I/O	I^2C synchronous data input/output	SIN0	I	SSIO0 data input

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PAD No	Primary function			Secondary function			Tertiary function		
	Pin name	I/O	Description	Pin name	I/O	Description	Pin name	I/O	Description
6	P81/EXI1	I/O	Input port/Output port / External interrupt	SCL	I/O	I^2C synchronous clock input/output	SCK0	I/O	SSIO0 synchronous clock input/output
9	P82/EXI2	I/O	Input port/Output port / External interrupt	—	—	—	SOUT0	O	SSIO0 data output
10	P83/EXI3	I/O	Input port/Output port / External interrupt	—	—	—	—	—	—
17	P84/EXI4	I/O	Input port/Output port / External interrupt	—	—	—	SIN1	I	SSIO1 data input
18	P85/EXI5	I/O	Input port/Output port / External interrupt	—	—	—	SCK1	I/O	SSIO1 synchronous clock input/output
26	P86/EXI6	I/O	Input port/Output port / External interrupt	RXD0	I	UART0 data input	SOUT1	O	SSIO1 data output
27	P87/EXI7	I/O	Input port/Output port / External interrupt	TXD0	O	UART0 data output	—	—	—

Note:
The function which is not chosen is lost when either a secondary function or a tertiary function is chosen. However, when using it as an input, read-out of an input data is possible at a PnD

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■PIN DESCRIPTION

In the I/O column, "—" denotes an input pin, "I" an input pin, "O" an output pin, and "I/O" an input/output pin.

Pin name	I/O	Description	Primary/ Secondary/ Tertiary	Logic
Power supply				
V_{SS}	—	Negative power supply pin	—	—
V_{DD}	—	Positive power supply pin	—	—
V_{DDL}	—	Positive power supply pin for internal logic (internally generated)	—	—
SPV_{SS}	—	Negative power supply pin for built-in speaker amplifier	—	—
SPV_{DD}	—	Positive power supply pin for built-in speaker amplifier	—	—
V_{REF}	—	Reference power supply pin for successive-approximation type ADC	—	—
Test				
TEST0	I/O	Input/output pin for testing. Has a pull-down resistor built in.	—	Positive
TEST1_N	I	Input pin for testing. Has a pull-up resistor built in.	—	Negative
System				
RESET_N	I	Reset input pin. When this pin is set to a "L" level, the device is placed in system reset mode and the internal circuit is initialized. If after that this pin is set to a "H" level, program execution starts. This pin has a pull-up resistor built in.	—	Negative
LSCLK	O	Low-speed clock output. This function is allocated to the secondary function of the P20 pin.	Secondary	—
OUTCLK	O	High-speed clock output. This function is allocated to the secondary function of the P21 pin.	Secondary	—
General-purpose Output port				
P20 to P22	O	General-purpose output ports. Provided with a secondary function. Cannot be used as ports if their secondary function is used.	Primary	Positive
General-purpose Input/output port				
P40 to P42	I/O	General-purpose input/output ports. Provided with a tertiary function. Cannot be used as ports if their tertiary function is used.	Primary	Positive
P80 to P87	I/O	General-purpose input/output ports. Provided with a secondary function or a tertiary function. Cannot be used as ports if their secondary function or tertiary function is used.	Primary	Positive

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Pin name	I/O	Description	Primary/ Secondary/ Tertiary	Logic
Synchronous serial (SSIO)				
SIN0	I	Synchronous serial data input pin. Allocated to the tertiary function of the P40 pin and P80 pin.	Tertiary	Positive
SCK0	I/O	Synchronous serial clock input/output pin. Allocated to the tertiary function of the P41 pin and P81 pin.	Tertiary	—
SOUT0	O	Synchronous serial data output pin. Allocated to the tertiary function of the P42 pin and P82 pin.	Tertiary	Positive
SIN1	I	Synchronous serial data input pin. Allocated to the tertiary function of the P84 pin.	Tertiary	Positive
SCK1	I/O	Synchronous serial clock input/output pin. Allocated to the tertiary function of the P85 pin.	Tertiary	—
SOUT1	O	Synchronous serial data output pin. Allocated to the tertiary function of the P86 pin.	Tertiary	Positive
I^2C bus interface				
SDA	I/O	I^2C data input/output pin. This pin is used as the secondary function of the P80 pin. This pin has an NMOS open drain output. When using this pin as a function of the I^2C, externally connect a pull-up resistor.	Secondary	Positive
SCL	I/O	I^2C clock output pin. This pin is used as the secondary function of the P81 pin. This pin has an NMOS open drain output. When using this pin as a function of the I^2C, externally connect a pull-up resistor.	Secondary	Positive
UART				
TXD0	O	UART0 data output pin. Allocated to the secondary function of the P87 pin.	Secondary	Positive
RXD0	I	UART0 data input pin. Allocated to the the secondary function of the P86 pin.	Secondary	Positive
External interrupt				
NMI	I	External non-maskable interrupt input pin. The interrupt occurs on both the rising and falling edges.	Primary	Positive/ Negative
EXI0 to 7	I	External maskable interrupt input pins. It is possible, for each bit, to specify whether the interrupt is enabled and select the interrupt edge by software. Allocated to the primary function of the P80 to P87 pins.	Primary	Positive/ Negative
LED drive				
LED0 to 2	O	Pins for LED driving. Allocated to the primary function of the P20 to P22 pins.	Primary	Positive/ Negative
Voice output function				
SPP	O	Positive output pin of the internal speaker amplifier.	—	—
SPM	O	Negative output pin of the internal speaker amplifier.	—	—
Successive-approximation type A/D converter				
AIN0 to 2	I	Analog inputs to Ch0 to Ch2 of the successive-approximation type A/D converter. Allocated to the primary function of the P40 to P42 pins.	Primary	Positive/ Negative

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■TERMINATION OF UNUSED PINS

●How to Terminate Unused Pins

Pin	Recommended pin termination
RESET_N	Open
TEST0	Open
TEST1_N	Open
V_{REF}	Connect to V_{DD}
P40 to P42 (AIN0 to AIN2)	Open
SPV_{DD}	Connect to V_{DD}
SPV_{SS}	Connect to V_{SS}
SPP	Open
SPM	Open
P20 to P22	Open
P80 to P87	Open
NMI	Open

Note:
For unused input ports or unused input/output ports, if the corresponding pins are configured as high-impedance inputs and left open, the supply current may become excessively large. Therefore, it is recommended to configure those pins as either inputs with a pull-down resistor/pull-up resistor or outputs.

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■ELECTRICAL CHARACTERISTICS

●Absolute Maximum Ratings

(V_{SS}= SPV_{SS}=0V)

Parameter	Symbol	Condition	Rating	Unit
Power supply voltage 1	V_{DD}	Ta=25°C	–0.3 to +7.0	V
Power supply voltage 2	SPV_{DD}	Ta=25°C	–0.3 to +7.0	V
Power supply voltage 3	V_{DDL}	Ta=25°C	–0.3 to +3.6	V
Reference supply voltage	V_{REF}	Ta=25°C	–0.3 to V_{DD}+0.3	V
Input voltage	V_{IN}	Ta=25°C	–0.3 to V_{DD}+0.3	V
Output voltage	V_{OUT}	Ta=25°C	–0.3 to V_{DD}+0.3	V
Output current 1	I_{OUT1}	Port 4,8, Ta=25°C	–12 to +11	mA
Output current 2	I_{OUT2}	Port 2, Ta=25°C	–12 to +20	mA
Power dissipation	PD	Ta=25°C	1.0	W
Storage temperature	T_{STG}	—	–55 to +150	°C

●Recommended Operating Conditions

(V_{SS}= SPV_{SS}=0V)

Parameter	Symbol	Condition	Range	Unit
Operating temperature	T_{OP}	—	–40 to +85	°C
Operating voltage	V_{DD}	—	2.0 to 5.5	V
	SPV_{DD}	—	2.0 to 5.5	
Reference supply voltage	V_{REF}	—	2.2 to V_{DD}	V
Operating frequency (CPU)	f_{OP}	V_{DD} = 2.0 to 5.5V	27k to 4.2M	Hz
		V_{DD} = 2.2 to 5.5V	4.2M to 8.4M	
Capacitor externally connected to V_{DDL} pin	C_L	—	10±30%	μF

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●Operating Conditions of Flash Memory

(V_{SS}= SPV_{SS}=0V)

Parameter	Symbol	Condition	Range	Unit
Operating temperature	T_{OP}	At write/erase (Data flash area)	-40 to +85	°C
		At write/erase (Program code area)	0 to +40	
Operating voltage	V_{DD}	At write/erase	2.2 to 5.5	V
Maximum rewrite count	C_{EPD}	Data flash area(512Byte x 4)	6,000	cycles
	C_{EPP}	Program code area	100	
Write cycles	Y_{DR}	—	10	years

●DC Characteristics (1 of 5)

(V_{DD}= 2.0 to 5.5V, SPV_{DD}=2.0 to 5.5V, V_{SS}= SPV_{SS}=0V, Ta=–40 to +85°C, unless otherwise specified) (1/5)

Parameter	Symbol	Condition	Rating			Unit	Measuring circuit
			Min.	Typ.	Max.		
High-speed oscillation start time	T_{XTH}	—	—	1.0	3.0	ms	1
Built-in RC oscillation frequency	f_{LCR}	Ta = –10 to +50°C	Typ -1.5%	32.768	Typ +1.5%	kHz	
		Ta = –40 to +85°C	Typ -3.0%		Typ +3.0%		
Source oscillation frequency	f_{HPLL}	Ta = –10 to +50°C	Typ -1.5%	4.098 or 8.192	Typ +1.5%	MHz	
		Ta = –40 to +85°C	Typ -3.0%		Typ +3.0%		

●DC Characteristics (2 of 5)

(V_{DD}= 2.0 to 5.5V, SPV_{DD}=2.0 to 5.5V, V_{SS}= SPV_{SS}=0V, Ta=–40 to +85°C, unless otherwise specified) (2/5)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
SPM, SPP output load resistance	R_{LSP}	—	8	—	—	Ω
Speaker amp output power	P_{SPO1}	SPV_{DD}=3.0V, f=1kHz R_{SPO}=8Ω, THD≥10%	—	0.45	—	W
	P_{SPO2}	SPV_{DD}=5.0V, f=1kHz R_{SPO}=8Ω, THD≥10%	—	1.0	—	W

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●DC Characteristics (3 of 5)

(V_{DD}= 2.0 to 5.5V, SPV_{DD}=2.0 to 5.5V, V_{SS}= SPV_{SS}=0V, Ta=–40 to +85°C, unless otherwise specified) (3/5)

Parameter	Symbol	Condition		Rating Min.	Rating Typ.	Rating Max.	Unit	Measuring circuit
Supply current 1	IDD1	CPU: In STOP state. high-speed oscillation: stopped	Ta≦+50°C	—	0.5	3.0	μA	1
			Ta≦+85°C	—	0.5	8.0		
Supply current 2	IDD2	CPU: In HALT state (LTBC,WDT: Operating) High-speed oscillation: Stopped	Ta≦+50°C	—	2.7	5.0		
			Ta≦+85°C	—	2.7	10		
Supply current 3	IDD3	CPU: Running at 32.768 kHz*1 High-speed oscillation: Stopped		—	20	30		
Supply current 4	IDD4	CPU: Running at 4.096MHz CR oscillating mode	V_{DD}=SPV_{DD}= 3.0V	—	3.0	5.0	mA	
			V_{DD}=SPV_{DD}= 5.0V	—	3.0	5.0		
		CPU: Running at 8.192MHz CR oscillating mode	V_{DD}=SPV_{DD}= 3.0V	—	4.0	6.0		
			V_{DD}=SPV_{DD}= 5.0V	—	4.0	6.0		
Supply current 5	IDD5	CPU: Running at 4.096MHz CR oscillating mode During voice playback of 1KHz,0db,SIN-wave (no output load)	V_{DD}=SPV_{DD}= 3.0V	—	4.0	7.0		
			V_{DD}=SPV_{DD}= 5.0V	—	6.0	10		
		CPU: Running at 8.192MHz CR oscillating mode During voice playback of 1KHz,0db,SIN-wave (no output load)	V_{DD}=SPV_{DD}= 3.0V	—	5.0	8.0		
			V_{DD}=SPV_{DD}= 5.0V	—	7.0	11		

*1: Case when the CPU operating rate is 100% (no HALT state).

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●DC Characteristics (4 of 5)

(V_{DD}= 2.0 to 5.5V, SPV_{DD}=2.0 to 5.5V, V_{SS}= SPV_{SS}=0V, Ta=−40 to +85°C, unless otherwise specified) (4/5)

Parameter	Symbol	Condition		Rating Min.	Rating Typ.	Rating Max.	Unit	Measuring circuit
Output voltage 1 (P20 to P22) (P40 to P42) (P80 to P87)	VOH1	IOH1=−0.5mA		V_{DD} −0.5	—	—	V	2
	VOL1	IOL1=+0.5mA		—	—	0.5		
Output voltage 2 (P20 to P22)	VOL2	(when LED drive mode is selected)	IOL2=+5mA V_{DD}≧2.2V	—	—	0.5		
			IOL2=+8mA V_{DD}≧2.3V	—	—	0.5		
Output voltage 3 (P80 to P81)	VOL3	IOL3=+3mA (I^2C bus input/output mode)		—	—	0.4		
Output leakage (P20 to P22) (P40 to P42) (P80 to P87)	IOOH	VOH=V_{DD} (in high-impedance state)		—	—	1.0	μA	3
	IOOL	VOL=V_{SS} (in high-impedance state)		−1.0	—	—		
Input current 1 (RESET_N) (TEST1_N)	IIH1	VIH1=V_{DD}		0	—	1.0	μA	4
	IIL1	VIL1=V_{SS}		−1500	−300	−20		
Input current 2 (NMI) (P40 to P42) (P80 to P87)	IIH2	VIH2=V_{DD} (when pulled-down)		2	30	250		
	IIL2	VIL2=V_{SS} (when pulled-up)		−250	−30	−2		
	IIH2Z	VIH2=V_{DD} (in high-impedance state)		—	—	1.0		
	IIL2Z	VIL2=V_{SS} (in high-impedance state)		−1.0	—	—		
Input current 3 (TEST0)	IIH3	VIH3=V_{DD}		20	300	1500		
	IIL3	VIL3=V_{SS}		−1.0	—	—		

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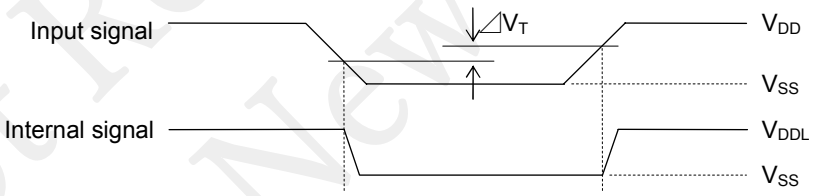
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●DC Characteristics (5 of 5)

(V_{DD}= 2.0 to 5.5V, SPV_{DD}=2.0 to 5.5V, V_{SS}= SPV_{SS}=0V, Ta=–40 to +85°C, unless otherwise specified) (5/5)

Parameter	Symbol	Condition	Rating			Unit	Measuring circuit
			Min.	Typ.	Max.		
Input voltage 1 (RESET_N) (TEST0) (TEST1_N) (NMI) (P40 to P42) (P80 to P87)	VIH1	—	0.7×V_{DD}	—	V_{DD}	V	5
	VIL1	—	0	—	0.3×V_{DD}		
Hysteresis width (RESET_N) (TEST0) (TEST1_N) (NMI) (P40 to P42) (P80 to P87)	⊿VT	—	0.05×V_{DD}	—	0.4×V_{DD}		
Input pin capacitance (NMI) (P40 to P42) (P80 to P87)	CIN	f=10kHz V_{rms}=50mV Ta=25°C	—	—	10	pF	—

●Hysteresis Width

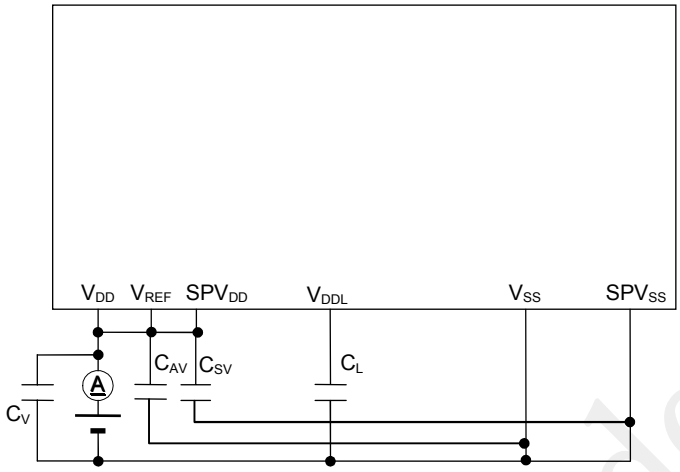


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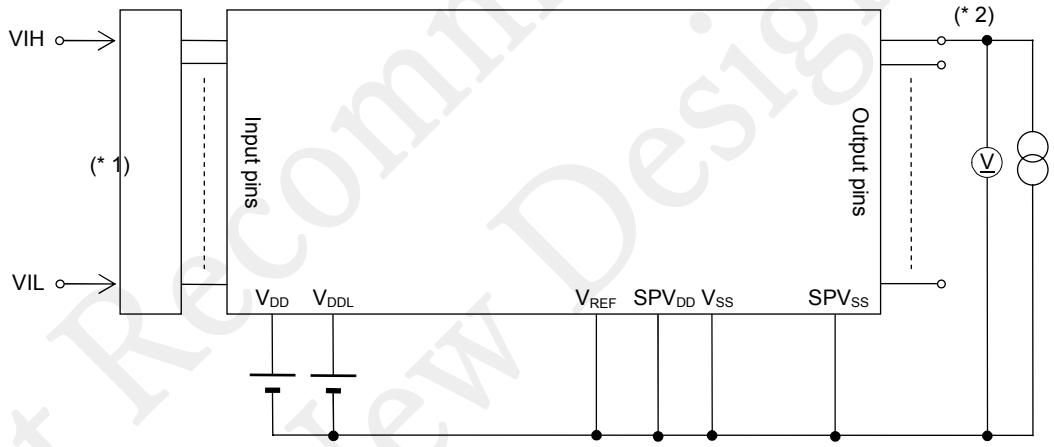
●Measuring Circuits

・Measuring circuit 1



C_V	: 0.1μF
C_{SV}	: 0.1μF
C_{AV}	: 1.0μF
C_L	: 10μF

・Measuring circuit 2

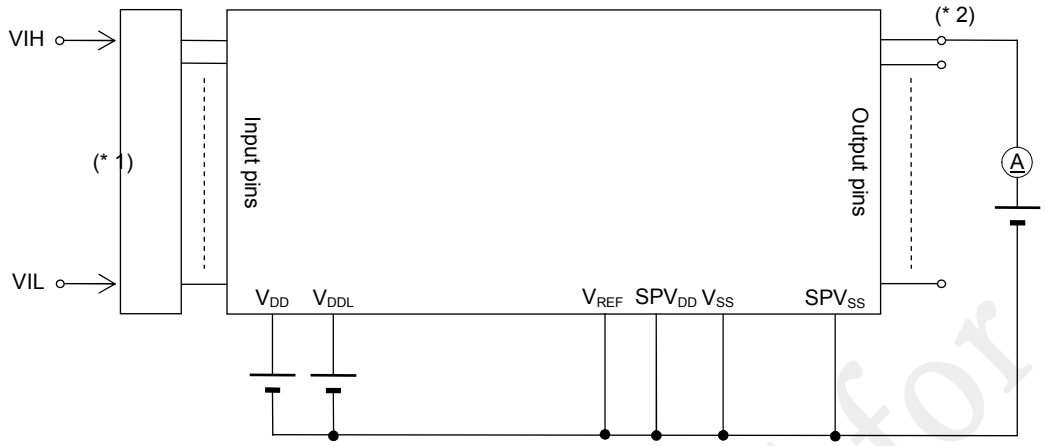


(* 1) Input logic circuit to determine the specified measuring conditions.
(* 2) Measured at the specified output pins.

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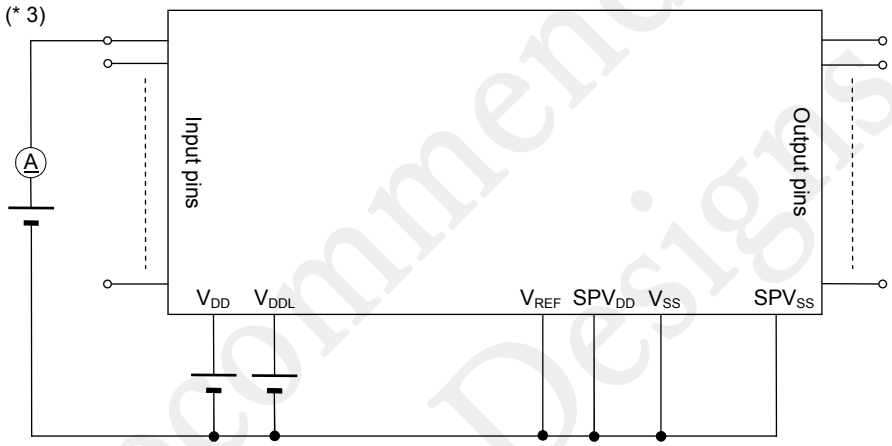
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・Measuring circuit 3



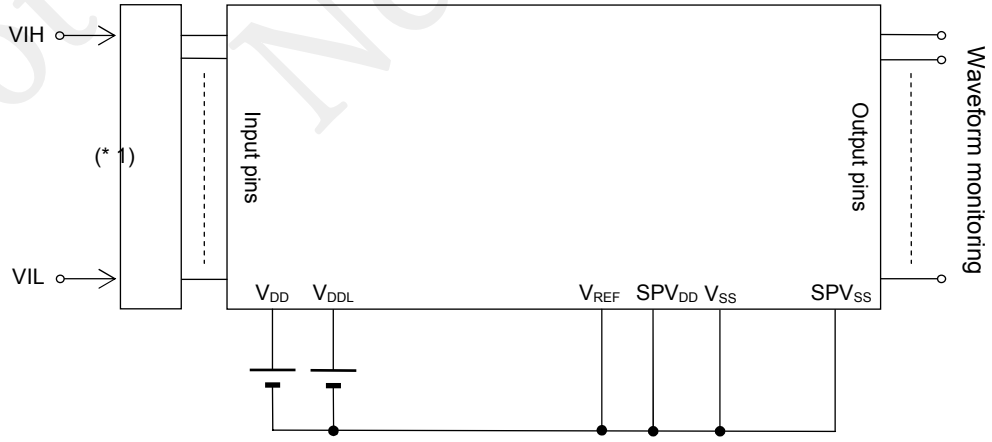
(* 1) Input logic circuit to determine the specified measuring conditions.
(* 2) Measured at the specified output pins.

・Measuring circuit 4



(* 3) Measured at the specified output pins.

・Measuring circuit 5



(* 1) Input logic circuit to determine the specified measuring conditions.

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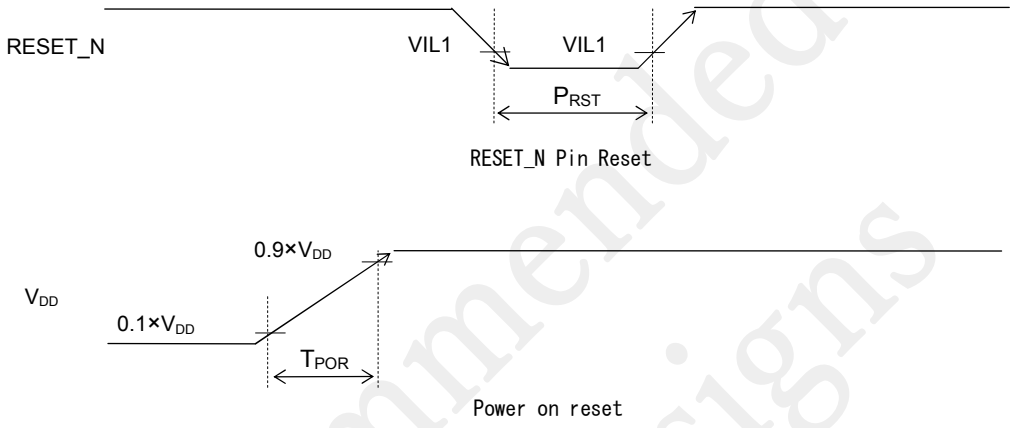
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●AC Characteristics (Reset)

・Reset

(V_{DD}= 2.0 to 5.5V, SPV_{DD}=2.0 to 5.5V, V_{SS}= SPV_{SS}=0V, Ta=−40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit	Measuring circuit
			Min.	Typ.	Max.		
Time until it starts SPVDD after starting VDD	t_{VDD}	—	0	—	—	ns	1
Reset pulse width	P_{RST}	—	100	—	—	µs	
Reset noise elimination pulse width	P_{NRST}	—	—	—	0.4		
Power-on reset activation power rise time	T_{POR}	—	—	—	10	ms	



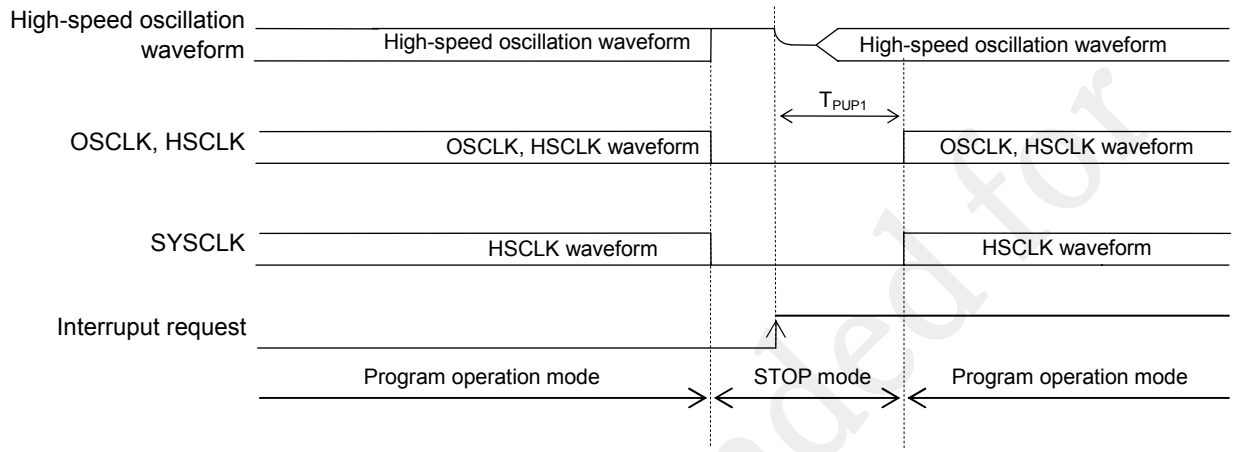
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・AC Characteristics (Oscillation stable time after STOP release)

(V_{DD}= 2.0 to 5.5V, SPV_{DD}=2.0 to 5.5V, V_{SS}= SPV_{SS}=0V, Ta=−40 to +85°C, unless otherwise specified)

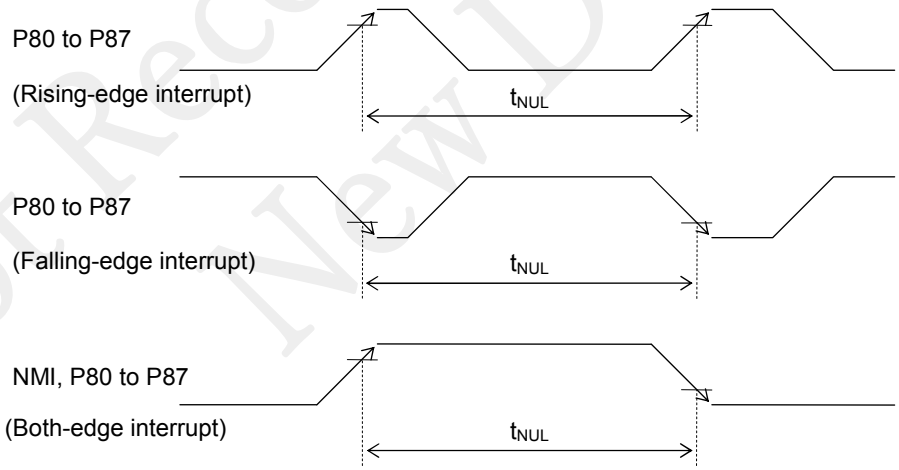
Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
Oscillation stable time after STOP release	T_{PUP1}	—	2	—	—	ms



・AC Characteristics (External Interrupt)

(V_{DD}= 2.0 to 5.5V, SPV_{DD}=2.0 to 5.5V, V_{SS}= SPV_{SS}=0V, Ta=−40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
External interrupt disable period	T_{NUL}	Interrupt: Enabled (MIE=1) CPU: NOP operation	2.5×sysclk	—	3.5×sysclk	μs



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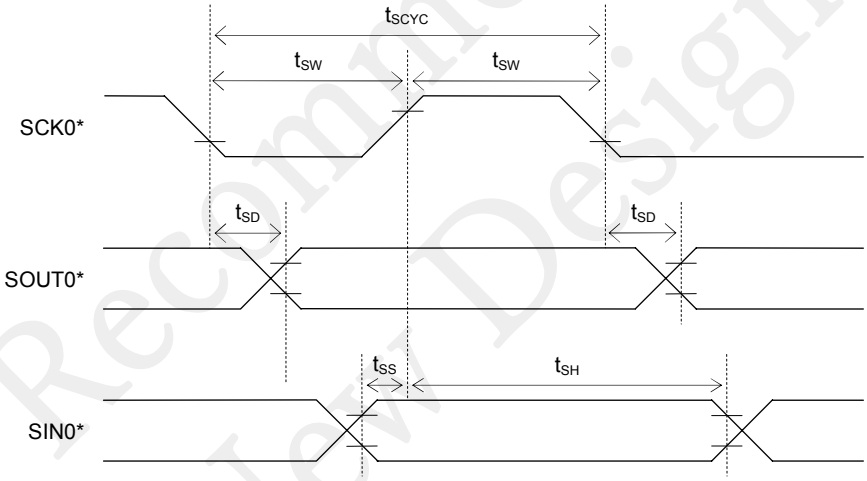
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・AC Characteristics (Synchronous Serial Port)

(V_{DD}= 2.0 to 5.5V, SPV_{DD}=2.0 to 5.5V, V_{SS}= SPV_{SS}=0V, Ta=–40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
SCLK input cycle (slave mode)	t_{SCYC}	When high-speed oscillation is not active	10	—	—	µs
		When high-speed oscillation is active	500	—	—	ns
SCLK output cycle (master mode)	t_{SCYC}	VDD≧2.4V	—	4	—	MHz
		VDD≧2.0V	—	2	—	
SCLK input pulse width (slave mode)	t_{SW}	When high-speed oscillation is not active	4	—	—	µs
		When high-speed oscillation is active	200	—	—	ns
SCLK output pulse width (master mode)	t_{SW}	—	SCLK*1 ×0.4	SCLK*1 ×0.5	SCLK*1 ×0.6	s
SOUT output delay time (slave mode)	t_{SD}	—	—	—	180	ns
SOUT output delay time (master mode)	t_{SD}	—	—	—	80	ns
SIN input setup time (slave mode)	t_{SS}	—	50	—	—	ns
SIN input hold time	t_{SH}	—	50	—	—	ns

*1: Clock period selected with S0CK3–0 of the serial port 0 mode register (SIO0MOD1)



*: Indicates the secondary function of the port.

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・AC Characteristics (I^2C Bus Interface: Standard Mode 100kHz)

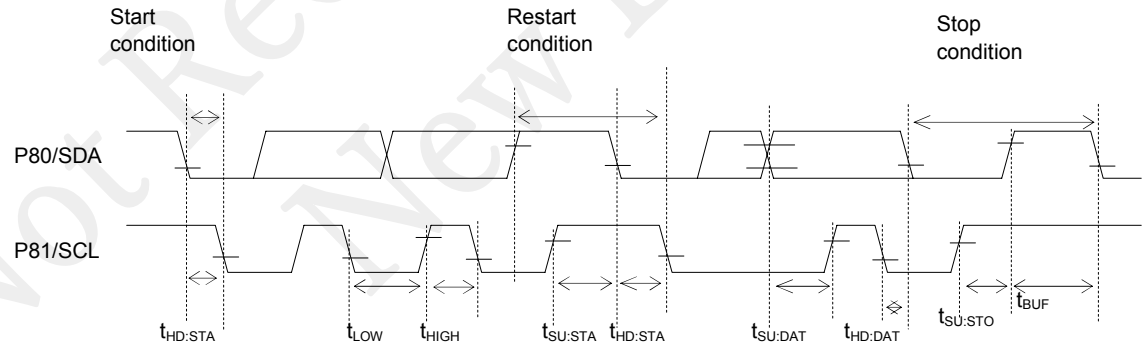
(V_{DD}= 2.0 to 5.5V, SPV_{DD}=2.0 to 5.5V, V_{SS}= SPV_{SS}=0V, Ta=−40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
SCL clock frequency	f_{SCL}	—	0	—	100	kHz
SCL hold time (start/restart condition)	$t_{HD:STA}$	—	4.0	—	—	µs
SCL "L" level time	t_{LOW}	—	4.7	—	—	µs
SCL "H" level time	t_{HIGH}	—	4.0	—	—	µs
SCL setup time (restart condition)	$t_{SU:STA}$	—	4.7	—	—	µs
SDA hold time	$t_{HD:DAT}$	—	0	—	—	µs
SDA setup time	$t_{SU:DAT}$	—	0.25	—	—	µs
SDA setup time (stop condition)	$t_{SU:STO}$	—	4.0	—	—	µs
Bus-free time	t_{BUF}	—	4.7	—	—	µs

・AC Characteristics (I^2C Bus Interface: Fast Mode 400kHz)

(V_{DD}= 2.0 to 5.5V, SPV_{DD}=2.0 to 5.5V, V_{SS}= SPV_{SS}=0V, Ta=−40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
SCL clock frequency	f_{SCL}	—	0	—	400	kHz
SCL hold time (start/restart condition)	$t_{HD:STA}$	—	0.6	—	—	µs
SCL "L" level time	t_{LOW}	—	1.3	—	—	µs
SCL "H" level time	t_{HIGH}	—	0.6	—	—	µs
SCL setup time (restart condition)	$t_{SU:STA}$	—	0.6	—	—	µs
SDA hold time	$t_{HD:DAT}$	—	0	—	—	µs
SDA setup time	$t_{SU:DAT}$	—	0.1	—	—	µs
SDA setup time (stop condition)	$t_{SU:STO}$	—	0.6	—	—	µs
Bus-free time	t_{BUF}	—	1.3	—	—	µs



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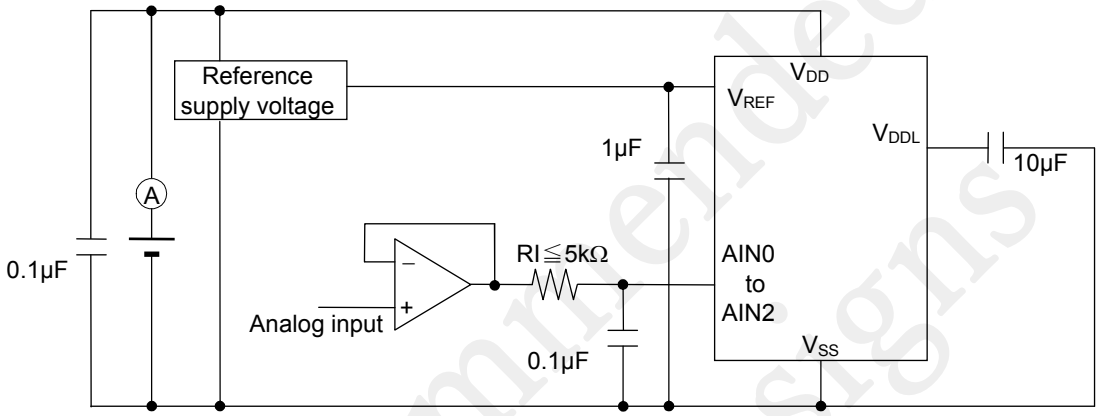
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●Electrical Characteristics of Successive Approximation Type A/D Converter

(DV_{DD}=SPV_{DD}=2.2 to 5.5V, V_{REF}=2.2 to 5.5V, V_{SS}=SPV_{SS}=0V, Ta=–40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
Resolution	n	—	—	—	10	bit
Integral non-linearity error	IDL	2.7V≦V_{REF}≦5.5V	–4	—	+4	LSB
		2.2V≦V_{REF}≦2.7V	–5	—	+5	
Differential non-linearity error	DNL	2.7V≦V_{REF}≦5.5V	–3	—	+3	
		2.2V≦V_{REF}≦2.7V	–4	—	+4	
Zero-scale error	V_{OFF}	R_I≦5kΩ	–4	—	+4	
Full-scale error	FSE	R_I≦5kΩ	–4	—	+4	
Input impedance	R_I	—	—	—	5k	Ω
Reference supply voltage	V_{REF}	—	2.2		V_{DD}	V
Conversion time	t_{CONV}	HSCLK=4M to 8.4MHz	—	102	—	ϕ/CH

ϕ: Period of high-speed clock (HSCLK)

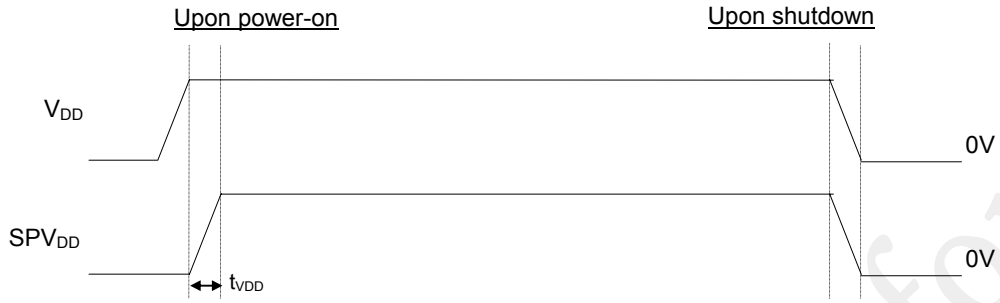


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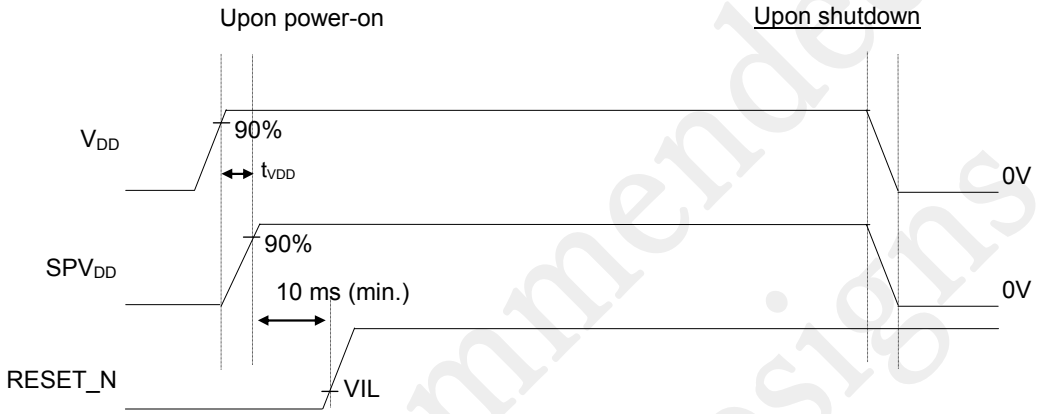
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●Power-on/Shutdown Sequence

・When the power rise time is 10 ms or less



・When the power rise time is more than 10 ms

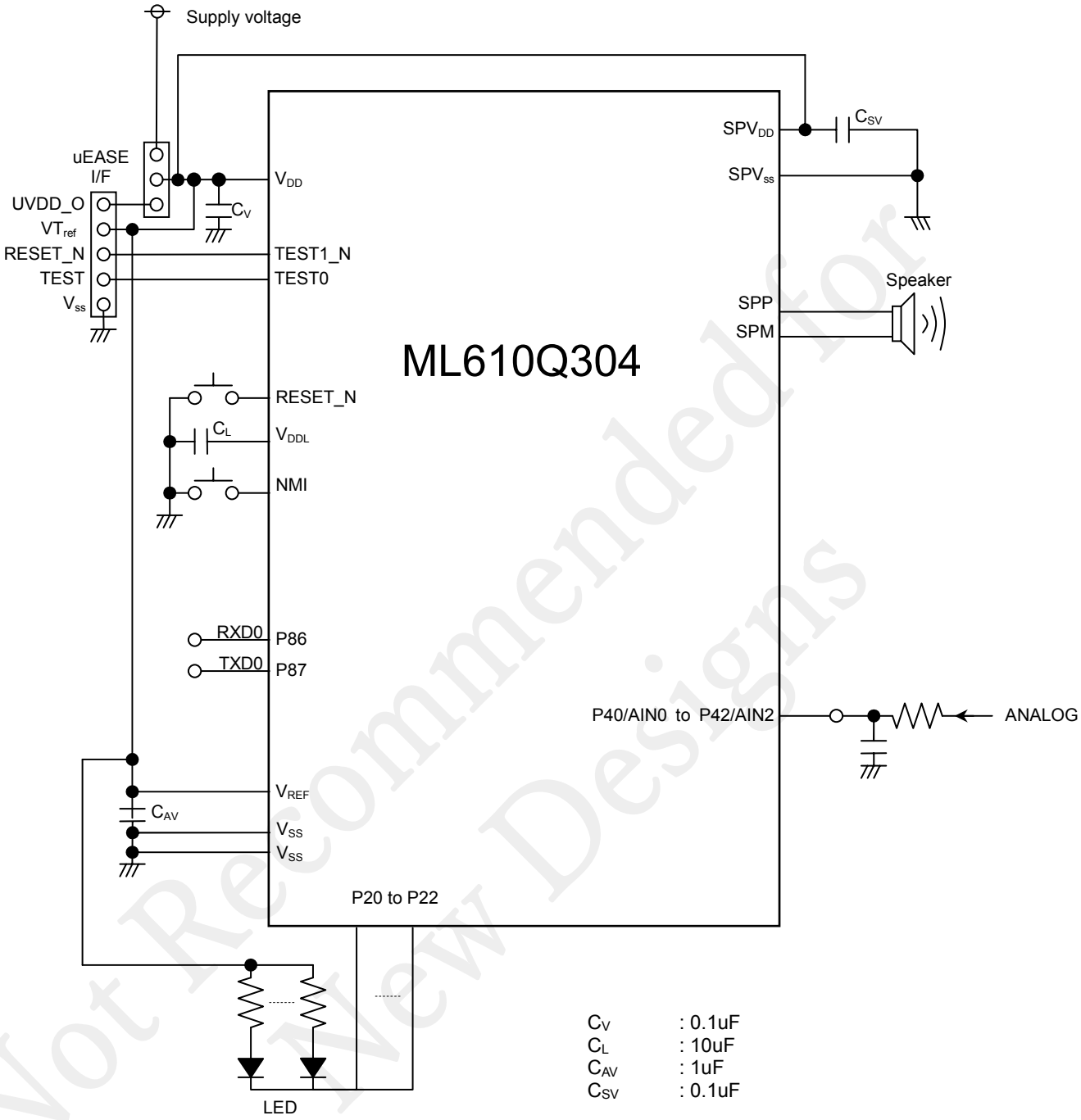


Recommended power-on/shutdown sequence
① Turn on V_{DD} and SPV_{DD} simultaneously, or turn on SPV_{DD} after turning on V_{DD}.
② Turn off V_{DD} and SPV_{DD} simultaneously, or turn off V_{DD} after turning on SPV_{DD}.

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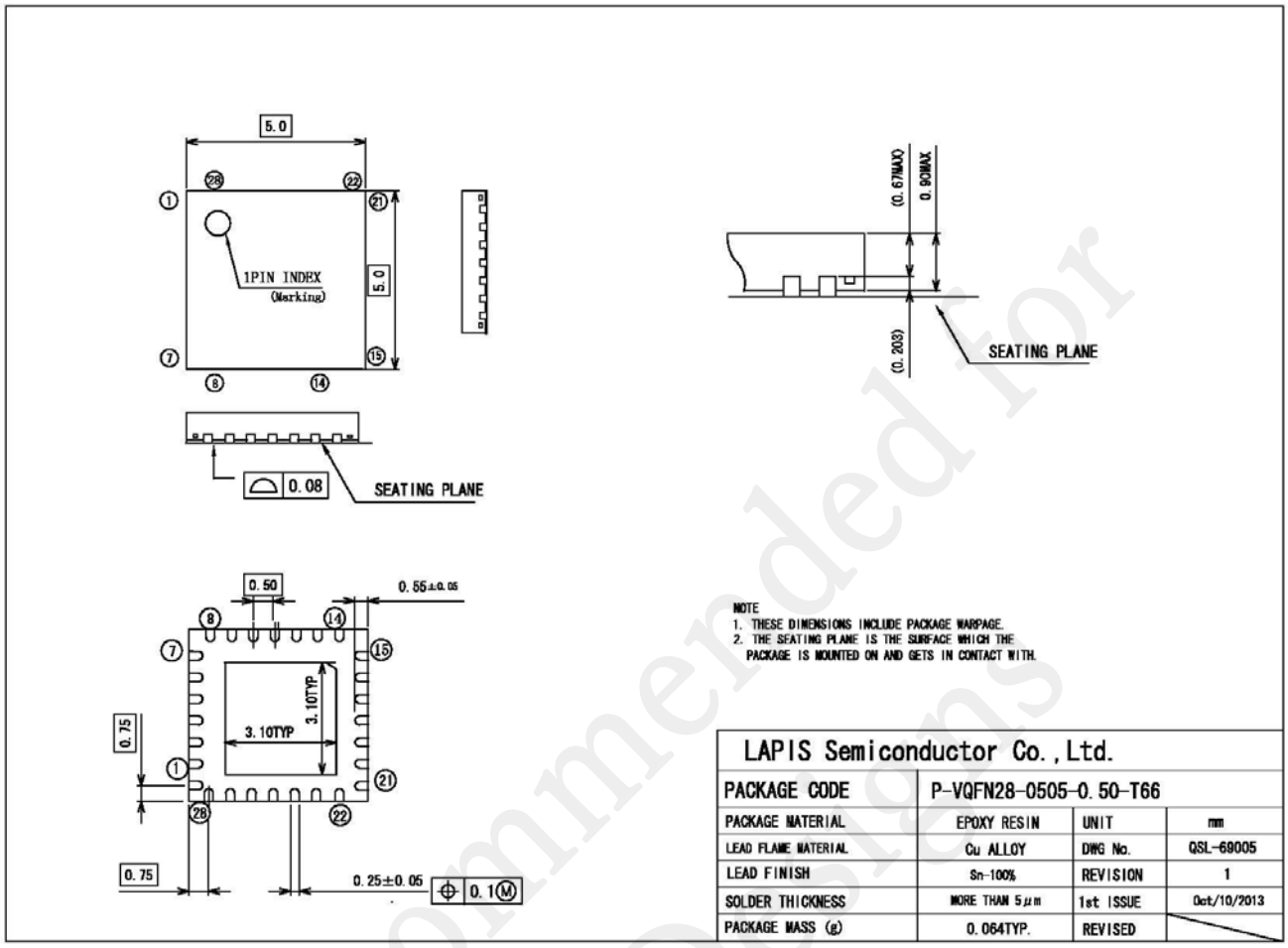
■Example of Application Circuit



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■ PACKAGE DIMENSIONS



[Unit:mm]

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact our responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

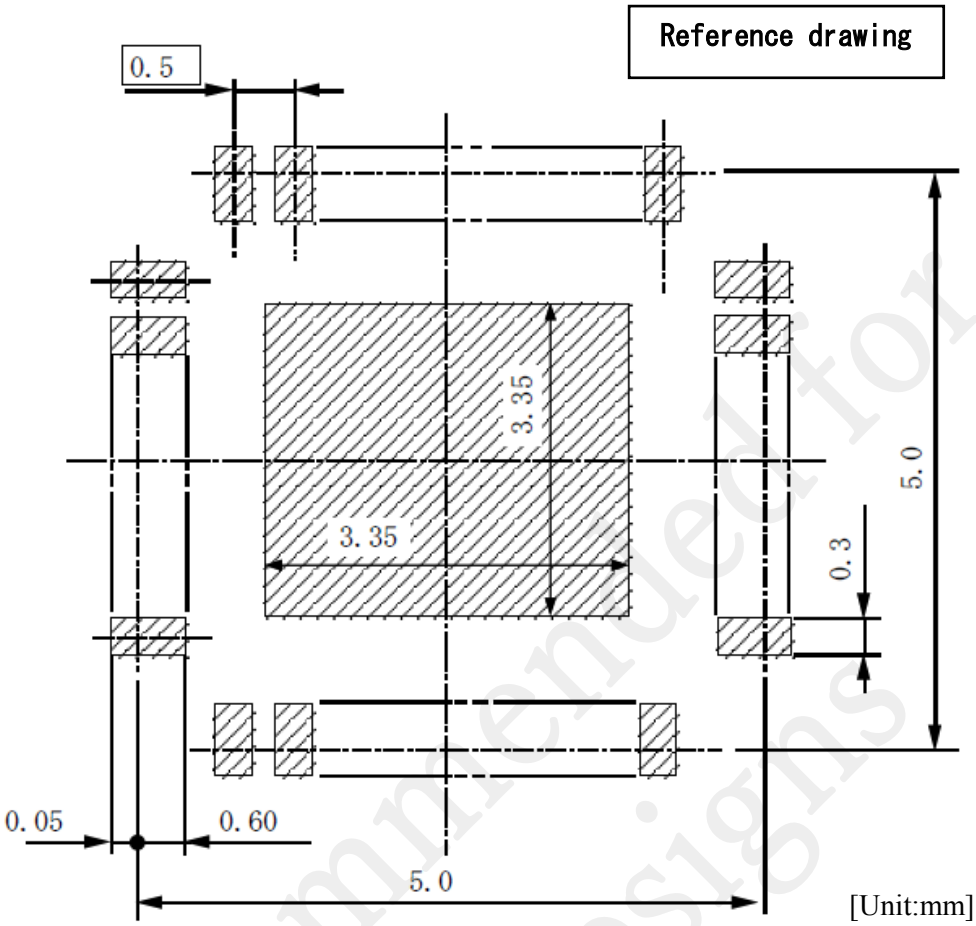
The heat resistance (example) of this LSI is shown below. Heat resistance (θ Ja) changes with the size and the number of layers of a substrate.

PCB	W/L/t=60 / 62 / 1.6(mm)
PCB Layer	1 Layers
Air cooling conditions	Calm(0m/sec)
Heat resistance(θJa)	56.6[℃/W](back diepad contact)
Power consumption of Chip PMax	0.351[W]

TjMax of this LSI is 125℃. TjMax is expressed with the following formulas.
TjMax = TaMax + θJa × PMax

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■Figure pf soldering department terminal existence range



Attention of the layout of a mounting board

Please take into consideration enough that there are not ease of a mounting, the reliability of contact, leading about of a wiring, and a solder bridge generate in the case of layout of the foot pattern of a mounting board.

The optimal layout of a foot pattern changes by the board quality of material, the solder paste category to be used, thickness, the soldering methodology, etc. Therefore, since the span where the terminator of this package may exist is shown as a "soldering part terminator extent drawing", please give as reference data of a foot pattern design.

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■Revision History

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
FEDL610Q304-01	Jul 16,2014	—	—	Final edition 1

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