NL17SV08

Single 2-Input AND Gate, Ultra-Low Voltage

The NL17SV08 is an ultra−high performance 2−Input AND gate manufactured in 0.35 μm technology with excellent performance down to 0.9 volts. This device is ideal for extremely high−speed and high−drive applications. Additionally, limitations of board space are no longer a constraint. The very small SOT−553 makes this device fit most tight designs and spaces.

Features

- Extremely High Speed: t_{PD} = 1.0 ns (Typ) @ V_{CC} = 3.3 V
- Designed for 0.9 to 3.3 V Operation
- Overvoltage Tolerance (OVT)* Input Pins Permit Logic Translation
- Balanced ±24 mA Output Drive @ 3.3 V
- Near Zero Static Supply Current
- Ultra−Tiny SOT−553 5 Pin Package Only 1.6 x 1.6 x 0.6 mm
- These Devices are Pb−Free and are RoHS Compliant

Typical Applications

- Cellular
- Digital Camera
- PDA
- Digital Video

Industry Standard

- Functionally Similar to NC7SV08 and SN74AUC1G08

*Overvoltage Tolerance (OVT) enables input pins to function outside (higher) of their operating voltages, with no damage to the devices or to signal integrity.

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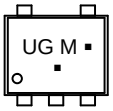
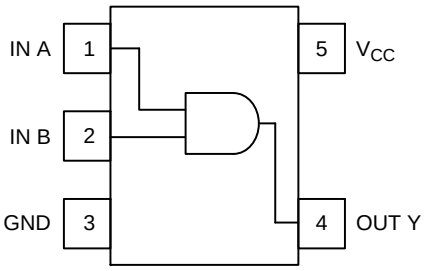
SOT−553
CASE 463B

MARKING DIAGRAM



UG = Specific Device Code
M = Date Code
▪ = Pb−Free Package
(Note: Microdot may be in either location)

PIN DIAGRAM



PIN ASSIGNMENT

PIN #	FUNCTION
1	IN A
2	IN B
3	GND
4	OUT Y
5	V_{CC}

FUNCTION TABLE

Input A	Input B	Output Y
L	L	L
L	H	L
H	L	L
H	H	H

ORDERING INFORMATION

Device	Package	Shipping†
NL17SV08XV5T2G	SOT−553 (Pb−Free)	4000 Tape & Reel (178 mm)

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MAXIMUM RATINGS

Symbol	Rating	Value	Units
V_{CC}	DC Supply Voltage	−0.5 to +4.6	V
V_I	DC Input Voltage	−0.5 to +4.6	V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current V_{IN} < 0 V	 −50	mA
I_{OK}	DC Output Diode Current V_{OUT} < 0 V V_{OUT} > V_{CC}	 −50 +50	mA
I_O	DC Output Sink Current	±50	mA
I_{CC}	DC Supply Current per Supply Pin	±50	mA
I_{GND}	DC Ground Current per Ground Pin	±50	mA
T_{STG}	Storage Temperature Range	−65 to +150	°C
T_L	Lead Temperature, 1.0 mm from Case for 10 seconds	260	°C
T_J	Junction Temperature Under Bias	+150	°C
θ_{JA}	Thermal Resistance (Note 1)	250	°C/W
P_D	Power Dissipation in Still Air at 85°C	250	mW
MSL	Moisture Sensitivity	Level 1	
F_R	Flammability Rating Oxygen Index: 28 to 34	 UL 94 V−0 @ 0.125 in	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Measured with minimum pad spacing on an FR4 board, using 10 mm−by−1 inch, 2 ounce copper trace no air flow.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Units
V_{CC}	Positive DC Supply Voltage	0.9	3.6	V
V_{IN}	Digital Input Voltage	0	3.6	V
V_{out}	Output Voltage	0	V_{CC}	V
I_{OH}/I_{OL}	Output Current V_{CC} = 3.0 V to 3.6 V V_{CC} = 2.3 V to 2.7 V V_{CC} = 1.65 V to 1.95 V V_{CC} = 1.4 V to 1.6 V V_{CC} = 1.1 V to 1.3 V V_{CC} = 0.9 V		 ±24 ±18 ±6 ±4 ±2 ±0.1	mA
t_A	Operating Temperature Range. All Package Types	−40	+85	°C
t_r, t_f	Input Rise or Fall Time V_{CC} = 3.3V ± 0.3 V	 0	 10	nS/V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

DEVICE JUNCTION TEMPERATURE VERSUS TIME TO 0.1% BOND FAILURES

Junction Temperature °C	Time, Hours	Time, Years
80	1,032,200	117.8
90	419,300	47.9
100	178,700	20.4
110	79,600	9.4
120	37,000	4.2
130	17,800	2.0
140	8,900	1.0

DC CHARACTERISTICS – Digital Section (Voltages Referenced to GND)

Symbol	Parameter	Condition	V_{CC}	T_A = 25°C		T_A = −40 to 85°C		Units
				Min	Max	Min	Max	
V_{IH}	High Level Input Voltage		0.90 1.10 ≤ V_{CC} ≤ 1.30 1.40 ≤ V_{CC} ≤ 1.60 1.65 ≤ V_{CC} ≤ 1.95 2.30 ≤ V_{CC} ≤ 2.70 2.70 ≤ V_{CC} ≤ 3.60	0.65 x V_{CC} 0.65 x V_{CC} 0.65 x V_{CC} 0.65 x V_{CC} 1.6 2.0		0.65 x V_{CC} 0.65 x V_{CC} 0.65 x V_{CC} 0.65 x V_{CC} 1.6 2.0		V
V_{IL}	Low Level Input Voltage		0.90 1.10 ≤ V_{CC} ≤ 1.30 1.40 ≤ V_{CC} ≤ 1.60 1.65 ≤ V_{CC} ≤ 1.95 2.30 ≤ V_{CC} ≤ 2.70 2.70 ≤ V_{CC} ≤ 3.60		0.35 x V_{CC} 0.35 x V_{CC} 0.35 x V_{CC} 0.35 x V_{CC} 0.7 0.8		0.35 x V_{CC} 0.35 x V_{CC} 0.35 x V_{CC} 0.35 x V_{CC} 0.7 0.8	V
V_{OH}	High Level Output Voltage	I_{OH} = −100 μA	0.90 1.10 ≤ V_{CC} ≤ 1.30 1.40 ≤ V_{CC} ≤ 1.60 1.65 ≤ V_{CC} ≤ 1.95 2.30 ≤ V_{CC} ≤ 2.70 2.70 ≤ V_{CC} ≤ 3.60	V_{CC} − 0.1 V_{CC} − 0.1 V_{CC} − 0.2 V_{CC} − 0.2 V_{CC} − 0.2 V_{CC} − 0.2		V_{CC} − 0.1 V_{CC} − 0.1 V_{CC} − 0.2 V_{CC} − 0.2 V_{CC} − 0.2 V_{CC} − 0.2		V
		I_{OH} = −2.0 mA	1.10 ≤ V_{CC} ≤ 1.30	0.75 x V_{CC}		0.75 x V_{CC}		
		I_{OH} = −4.0 mA	1.40 ≤ V_{CC} ≤ 1.60	0.75 x V_{CC}		0.75 x V_{CC}		
		I_{OH} = −6.0 mA	1.65 ≤ V_{CC} ≤ 1.95 2.30 ≤ V_{CC} ≤ 2.70	1.25 2.0		1.25 2.0		
		I_{OH} = −12 mA	2.30 ≤ V_{CC} ≤ 2.70 2.70 < V_{CC} ≤ 3.60	1.8 2.2		1.8 2.2		
		I_{OH} = −18 mA	2.30 ≤ V_{CC} ≤ 2.70 2.70 < V_{CC} ≤ 3.60	1.7 2.4		1.7 2.4		
		I_{OH} = −24 mA	2.70 ≤ V_{CC} ≤ 3.60	2.2		2.2		
V_{OL}	Low Level Output Voltage	I_{OL} = 100 μA	0.90 1.10 ≤ V_{CC} ≤ 1.30 1.40 ≤ V_{CC} ≤ 1.60 1.65 ≤ V_{CC} ≤ 1.95 2.30 ≤ V_{CC} ≤ 2.70 2.70 ≤ V_{CC} ≤ 3.60		0.1 0.1 0.2 0.2 0.2 0.2		0.1 0.1 0.2 0.2 0.2 0.2	V
		I_{OL} = 2.0 mA	1.10 ≤ V_{CC} ≤ 1.30		0.25 x V_{CC}		0.25 x V_{CC}	
		I_{OL} = 4.0 mA	1.40 ≤ V_{CC} ≤ 1.60		0.25 x V_{CC}		0.25 x V_{CC}	
		I_{OL} = 6.0 mA	1.65 ≤ V_{CC} ≤ 1.95		0.3		0.3	
		I_{OL} = 12 mA	2.30 ≤ V_{CC} ≤ 2.70 2.70 < V_{CC} ≤ 3.60		0.4 0.4		0.4 0.4	
		I_{OL} = 18 mA	2.30 ≤ V_{CC} ≤ 2.70 2.70 < V_{CC} ≤ 3.60		0.6 0.4		0.6 0.4	
		I_{OL} = 24 mA	2.70 ≤ V_{CC} ≤ 3.60		0.55		0.55	
I_{IN}	Input Leakage Current	0 = V_I = 3.6 V	0.90 to 3.60		±0.1		±0.9	μA
I_{OFF}	Power Off Leakage Current		0		10		10	μA
I_{CC}	Quiescent Supply Current	V_I = V_{CC} or GND	0.90 to 3.60		0.9		5	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

AC CHARACTERISTICS (Input $t_r = t_f = 3.0$ nS)

Symbol	Parameter	Condition	V_{CC}	T_A = 25°C			T_A = −40 to 85°C		Units
				Min	Typ	Max	Min	Max	
T_{PHL}, T_{PLH}	Propagation Delay	C_L = 15 pF, R_L = 1.0 MΩ	0.90		13				nS
		C_L = 15 pF, R_L = 2.0 kΩ	$1.10 \le V_{CC} \le 1.30$ $1.40 \le V_{CC} \le 1.60$	3.0 1.0	6.0 3.2	10.0 6.0	1.0 1.0	14.6 7.2	nS
		C_L = 30 pF, R_L = 500 Ω	$1.65 \le V_{CC} \le 1.95$ $2.30 \le V_{CC} \le 2.70$ $2.70 \le V_{CC} \le 3.60$	1.0 0.8 0.7	2.0 1.2 1.0	4.5 2.6 2.3	1.0 0.7 0.6	5.3 3.7 3.0	nS
C_{IN}	Input Capacitance		0		2.0				pF
C_{OUT}	Output Capacitance		0		4.5				pF
C_{PD}	Power Dissipation Capacitance	V_I = 0 V or V_{CC} F = 10 MHz	0.90 to 3.60		20				pF

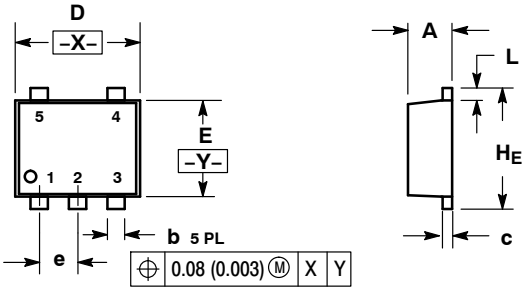
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

SCALE 4:1

SOT−553, 5 LEAD
CASE 463B
ISSUE C

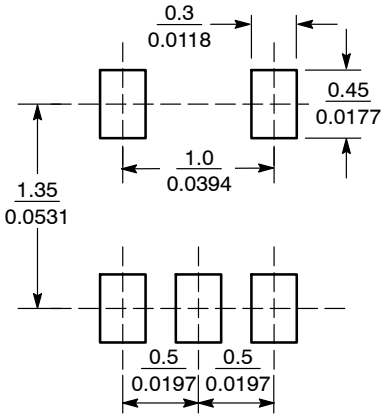
DATE 20 MAR 2013



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	0.50	0.55	0.60	0.020	0.022	0.024
b	0.17	0.22	0.27	0.007	0.009	0.011
c	0.08	0.13	0.18	0.003	0.005	0.007
D	1.55	1.60	1.65	0.061	0.063	0.065
E	1.15	1.20	1.25	0.045	0.047	0.049
e		0.50 BSC			0.020 BSC	
L	0.10	0.20	0.30	0.004	0.008	0.012
H_E	1.55	1.60	1.65	0.061	0.063	0.065

RECOMMENDED SOLDERING FOOTPRINT*



SCALE 20:1 (mm / inches)

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*

XX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

STYLE 1:
PIN 1. BASE
2. EMITTER
3. BASE
4. COLLECTOR
5. COLLECTOR

STYLE 2:
PIN 1. CATHODE
2. COMMON ANODE
3. CATHODE 2
4. CATHODE 3
5. CATHODE 4

STYLE 3:
PIN 1. ANODE 1
2. N/C
3. ANODE 2
4. CATHODE 2
5. CATHODE 1

STYLE 4:
PIN 1. SOURCE 1
2. DRAIN 1/2
3. SOURCE 1
4. GATE 1
5. GATE 2

STYLE 5:
PIN 1. ANODE
2. EMITTER
3. BASE
4. COLLECTOR
5. CATHODE

STYLE 6:
PIN 1. EMITTER 2
2. BASE 2
3. EMITTER 1
4. COLLECTOR 1
5. COLLECTOR 2/BASE 1

STYLE 7:
PIN 1. BASE
2. EMITTER
3. BASE
4. COLLECTOR
5. COLLECTOR

STYLE 8:
PIN 1. CATHODE
2. COLLECTOR
3. N/C
4. BASE
5. EMITTER

STYLE 9:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. ANODE
5. ANODE

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NEW STANDARD:			
DESCRIPTION:	**SOT−553, 5 LEAD**		**PAGE 1 OF 2**

ISSUE	REVISION	DATE
A	ADDED STYLES 3–9. REQ. BY D. BARLOW	11 NOV 2003
B	ADDED NOMINAL VALUES AND UPDATED GENERIC MARKING DIAGRAM. REQ. BY HONG XIAO	27 MAY 2005
C	UPDATED DIMENSIONS D, E, AND HE. REQ. BY J. LETTERMAN.	20 MAR 2013

PUBLICATION ORDERING INFORMATION

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