High Performance Ethernet & Fibre Channel (FC) Clock Generator

Features

- Ethernet and Fibre Channel clock outputs
- Supporting LVDS (PI6LC4872-02) and LVPECL (PI6LC4872-01) outputs
- Pin selectable output frequencies
- Ultra low phase jitter: < 1ps (156.25MHz, 12KHz to 20MHz integration range)
- 25MHz low noise buffered output
- 33MHz PCI clock
- Selectable reference or Xtal input
- 3.3V supply voltage
- TQFN-40 package

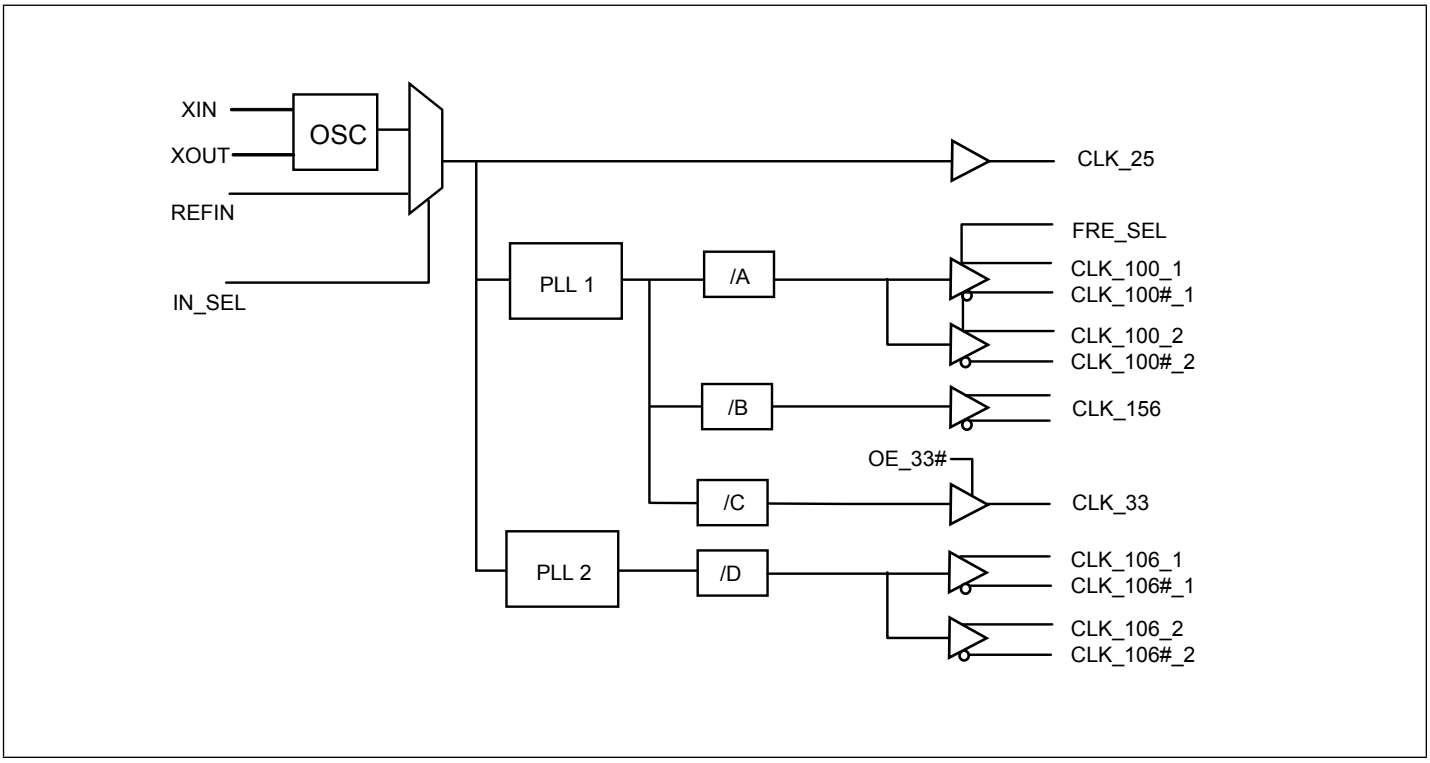
Applications

- Switches and Routers with FC interface
- Storage systems

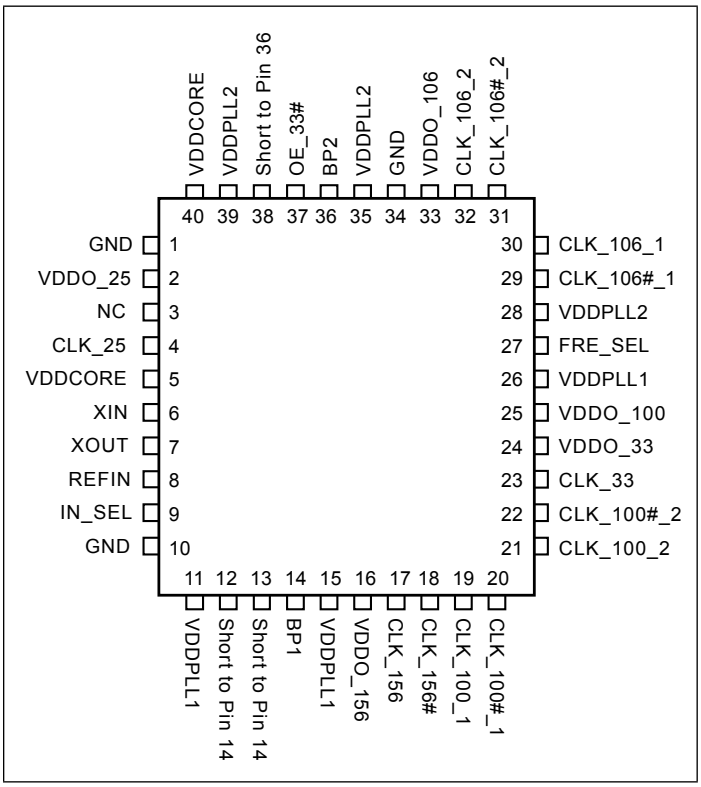
Description

The PI6LC4872 is high performance clock generator which supports both Ethernet frequencies and Fibre Channel (FC) frequencies. Pericom's proprietary PLL technology used in this device generates all these frequencies in the single chip while maintaining ultra low phase jitter. This device is ideal for systems that need both Ethernet and FC clock providing great flexibility.

Block Diagram



Block Diagram



Pinout Table

Pin Number	Pin Name	Description
1, 10, 34	GND	Ground. Includes external paddle (EPAD).
2	V_{DDO_25}	Power Supply Connection for the 25M CMOS Buffer.
3	NC	No Connect. This pin should be left floating.
4	CLK_25	CMOS 25 MHz Output.
5	V_{DDCORE}	Power Supply Connection for the Crystal Oscillator.
6, 7	XIN, XOUT	External 25 MHz Crystal.
8	REFIN	25 MHz Reference Clock Input. Tie low when not in use.
9	IN_SEL	Logic Input. Used to select the reference source.
11	V_{DDPLL1}	Power Supply Connection for the GbE PLL.
14, 36	BP1, BP2	These pins are for bypassing each LDO to ground with a 220 nF capacitor.
15	V_{DDPLL1}	Power Supply Connection for the GbE VCO.
16	V_{DDO_156}	Power Supply Connection for the 156M LVPECL/LVDS Output Buffer and Output Dividers.
17	CLK_156	LVPECL/LVDS Output at 156.25 MHz.
18	CLK_156#	Complementary LVPECL/LVDS Output at 156.25 MHz.
19	CLK_100_1	LVPECL/LVDS Output at 100 MHz or 125 MHz. Selected by FRE_SEL pin strapping.
20	CLK_100#_1	Complementary LVPECL/LVDS Output at 100 MHz or 125 MHz.

Pinout Table (continued from previous page)

Pin No.	Pin Name	Description
21	CLK_100_2	LVPECL/LVDS Output at 100 MHz or 125 MHz. Selected by FRE_SEL pin strapping.
22	CLK_100#_2	Complementary LVPECL/LVDS Output at 100 MHz or 125 MHz.
23	CLK_33	CMOS 33.33 MHz Output.
24	V_{DDO_33}	Power Supply Connection for the 33M CMOS Output Buffer and Output Dividers.
25	V_{DDO_100}	Power Supply Connection for the 100M/125M LVPECL/LVDS Output Buffer and Output Dividers.
26	V_{DDPLL1}	Power Supply Connection for the GbE PLL Feedback Divider.
27	FRE_SEL	Logic Input. Used to configure output drivers.
28	V_{DDPLL2}	Power Supply Connection for the FC PLL Feedback Divider.
29	CLK_106#_1	Complementary LVPECL/LVDS Output at 106.25 MHz.
30	CLK_106_1	LVPECL/LVDS Output at 106.25 MHz.
31	CLK_106#_2	Complementary LVPECL/LVDS Output at 106.25 MHz.
32	CLK_106_2	LVPECL/LVDS Output at 106.25 MHz.
33	V_{DDO_106}	Power Supply Connection for the 106.25 MHz LVPECL/LVDS Output Buffer and Output Dividers.
35	V_{DDPLL2}	Power Supply Connection for the FC VCO.
37	OE_33#	Forces the 33.33 MHz output into a low state.
39	V_{DDPLL2}	Power Supply Connection for the FC PLL.
40	V_{DDCORE}	Power Supply Connection for Miscellaneous Logic.

Function Tables

INSEL Definition

IN_SEL	Input
0	External reference clock
1 or NC	External Xtal

FRE_SEL Definition

FRE_SEL	Pin 19 and pin 20	Pin 21 and pin 22
0	125 MHz	125 MHz
1	100 MHz	100 MHz
NC	125 MHz	100 MHz

OE_33# Definition

OE_33#	CLK_33
0 or NC	33.33MHz
1	Low

Maximum Ratings (Above which the useful life may be impaired. For user guidelines, not tested)

Storage temperature..... -65°C to +155°C
Ambient Operating Temperature.....-40°C to +85°C
3.3V Analog Supply Voltage..... -0.5 to +4.6V

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended Operating Conditions

Symbol	Description	Test Conditions	Min	Type	Max	Unit
V_{DD}	Power supply	-	3.0	-	3.6	V
I_{DD}	Total Power Supply Current	All output frequencies. LVDS outputs	-	-	315	mA
		All output frequencies. LVPECL outputs	-	-	400	mA
T_A	Operating temperature	-	-40		+85	°C

LVCMOS DC Electrical Characteristics (Over Operating Conditions)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{IH}	Input High Voltage	IN_SEL, OE_33#, and REFIN	2	-	V_{DD}+0.3	V
V_{IL}	Input Low Voltage	IN_SEL, OE_33#, and REFIN	-0.3	-	0.8	V
V_{IH}	Input High Voltage	FRE_SEL	2/3V_{DD}+0.2	-		V
V_{IL}	Input Low Voltage	FRE_SEL		-	1/3V_{DD}-0.2	V
V_{OH}	Output High Voltage	I_{OH} = -1mA	V_{DD}-0.1	-	-	V
V_{OL}	Output Low Voltage	I_{OL} = 1mA	-	-	0.1	V
I_{IH}	Input High Current	V_{IN} = V_{DD}, IN_SEL	-	-	1.0	µA
		V_{IN} = V_{DD}, FRE_SEL			45	
		V_{IN} = V_{DD}, OE_33#			240	
I_{IL}	Input Low Current	V_{IN} = 0V, IN_SEL	-155	-		µA
		V_{IN} = 0V, FRE_SEL	-30			
		V_{IN} = 0V, OE_33#	-3.0			

LVCMOS DC Electrical Characteristics (Over Operating Conditions) Continued..

R_{PU}	Internal pull up resistance	IN_SEL	-	30		KΩ
		FRE_SEL		150		
R_{DN}	Internal pull down resistance	OE_33#	-	16	-	KΩ
		FRE_SEL		100		
D_C	Duty Cycle		47		53	%

LVPECL DC Electrical Characteristics (Over Operating Conditions) - For PI6LC4872-01 only

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{OH}	Output High Voltage	-	V_{DD}-1.24	-	V_{DD}-0.83	V
V_{OL}	Output Low Voltage	-	V_{DD}-2.07	-	V_{DD}-1.62	V
V_{OD}	Output differential voltage	-	700	-	950	mV
D_C	Duty Cycle		48		52	%

LVDS DC Electrical Characteristics (Over Operating Conditions) - For PI6LC4872-02 only

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{OD}	Output differential voltage	-	250	-	475	mV
ΔV_{OD}	Difference between V_{OD}	-		-	25	mV
V_{OS}	Output offset voltage	-	1.125	-	1.375	V
ΔV_{OS}	Difference between V_{OS}	-		-	25	mV
D_C	Duty Cycle		48		52	%

AC Switching Characteristics (Over Operating Conditions), Typical is given for VDD=3.3V, TA=25C

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Fin	Input Frequency	-		25		MHz
T_{OE}	Output enable time				100	ns
T_{OEB}	Output disable time				100	ns
LVPECL (For PI6LC4872-01 only)						
T_r /T_f	Output Rise/Fall time	Termination =200Ohm to 0V; C_L=0pf; 20% to 80% measured differentially		600	880	ps
J_{phase}	Phase jitter (12kHz to 20MHz), RMS	Output frequency: 156.25MHz, output combination=1x156.25MHz, 1x100MHz, 1x125MHz, 2x106.25MHz	-	510	-	fs
		Output frequency: 125MHz, output combination=1x156.25MHz, 1x100MHz, 1x125MHz, 2x106.25MHz, 33MHz off	-	560	-	
		Output frequency: 125MHz, output combination=1x156.25MHz, 1x100MHz, 1x125MHz, 2x106.25MHz, 33MHz on	-	600	-	
		Output frequency: 106.25MHz, output combination=1x156.25MHz, 1x100MHz, 1x125MHz, 2x106.25MHz	-	530	-	
		Output frequency: 100MHz, output combination=1x156.25MHz, 1x100MHz, 1x125MHz, 2x106.25MHz	-	600	-	
LVDS (For PI6LC4872-02 only)						
T_r /T_f	Output Rise/Fall time	Termination =100Ohm differential; C_L=0pf; 20% to 80% measured differentially	160	-	540	ps

AC Switching Characteristics (Over Operating Conditions), Typical is given for VDD=3.3V, TA=25C Cont..)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
J_{phase}	Phase jitter (12kHz to 20MHz), RMS	Output frequency: 156.25MHz, output combination=1x156.25MHz, 1x100MHz, 1x125MHz, 2x106.25MHz	-	460	-	fs
		Output frequency: 125MHz, output combination=1x156.25MHz, 1x100MHz, 1x125MHz, 2x106.25MHz, 33MHz off	-	470	-	
		Output frequency: 125MHz, output combination=1x156.25MHz, 1x100MHz, 1x125MHz, 2x106.25MHz, 33MHz on	-	480	-	
		Output frequency: 106.25MHz, output combination=1x156.25MHz, 1x100MHz, 1x125MHz, 2x106.25MHz	-	490	-	
		Output frequency: 100MHz, output combination=1x156.25MHz, 1x100MHz, 1x125MHz, 2x106.25MHz	-	520	-	
CMOS						
T_r /T_f	Output Rise/Fall time	Termination =50Ohm to 0V; CL=5pf; 20% to 80%	250	500	2500	ps
J_{phase}	Phase jitter (12kHz to 5MHz), RMS	Output frequency: 25MHz, output combination=1x156.25MHz, 1x100MHz, 1x125MHz, 2x106.25MHz	-	200	-	fs
		Output frequency: 33MHz, output combination=1x156.25MHz, 1x100MHz, 1x125MHz, 2x106.25MHz	-	505	-	

Crystal Specification

Parameter	Conditions	Min.	Typ.	Max.	Unit
Frequency	Fundamental mode		25		MHz
ESR				50	Ω
Load capacitance			14		pF
Stability		-30		30	ppm
Phase noise	@ 1kHz offset		-135		dBc/Hz

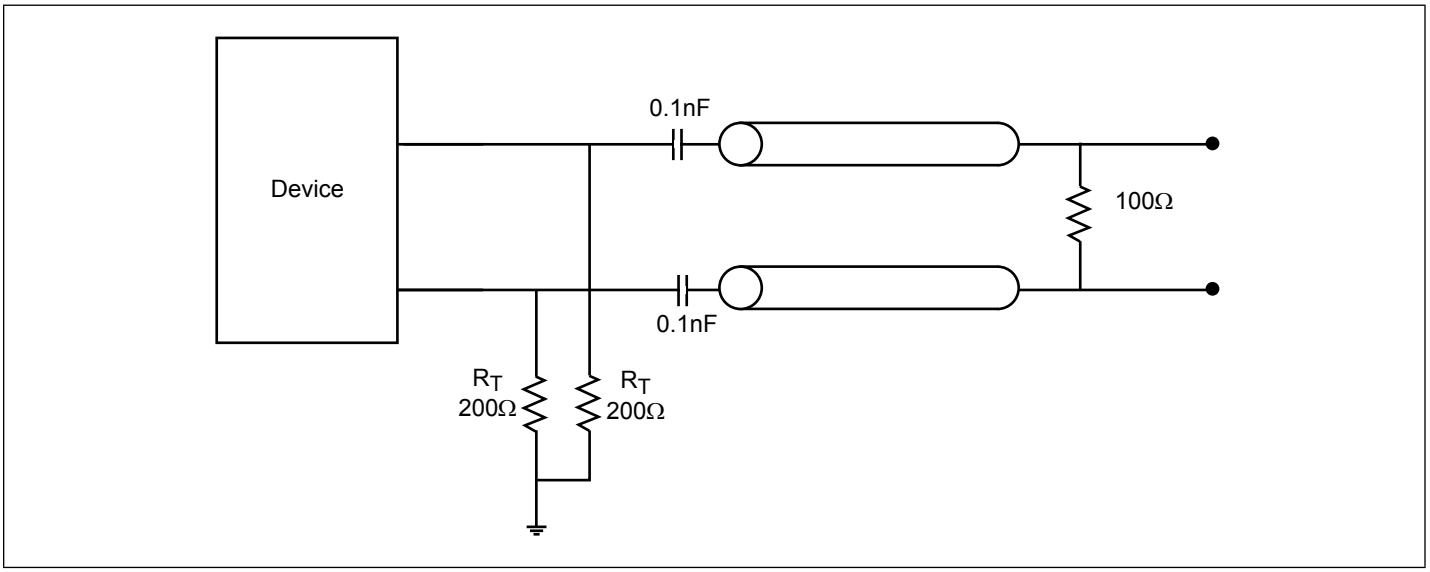


Figure 1. Configuration Test Load Board Termination for LVPECL Output

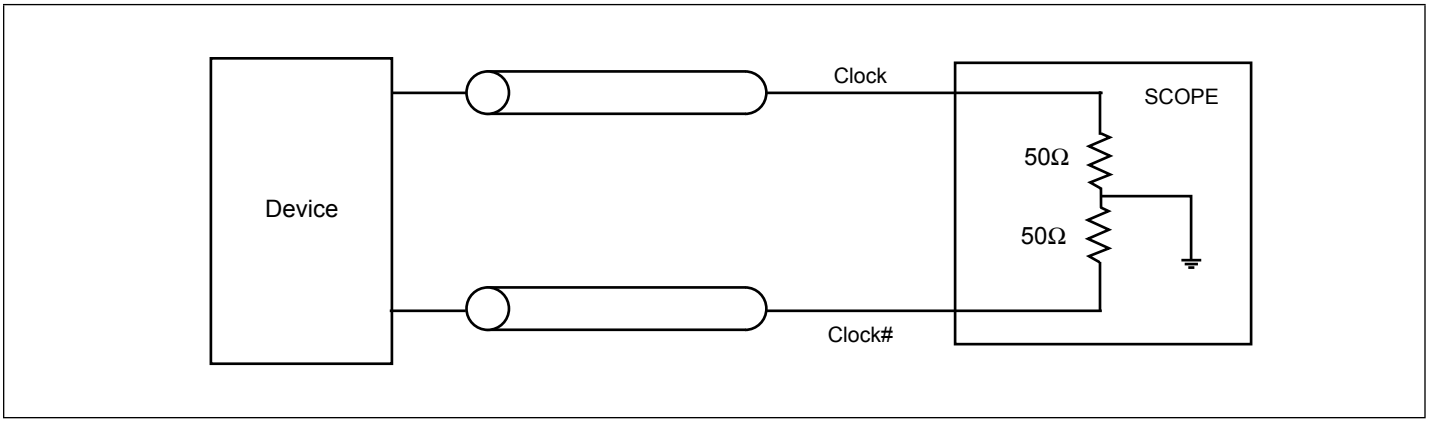


Figure 2. Configuration Test Load Board Termination for LVDS output

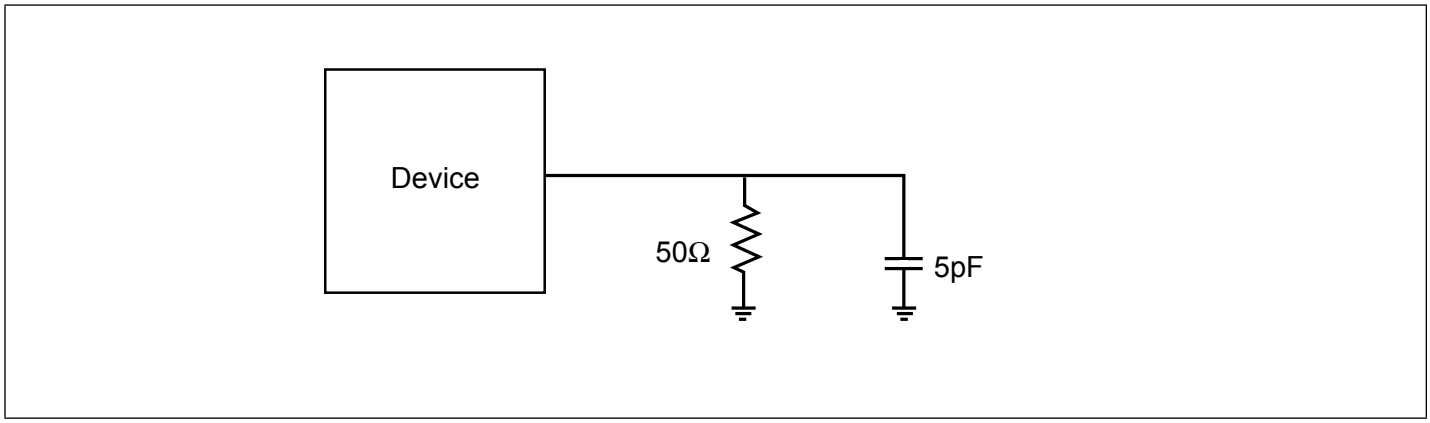


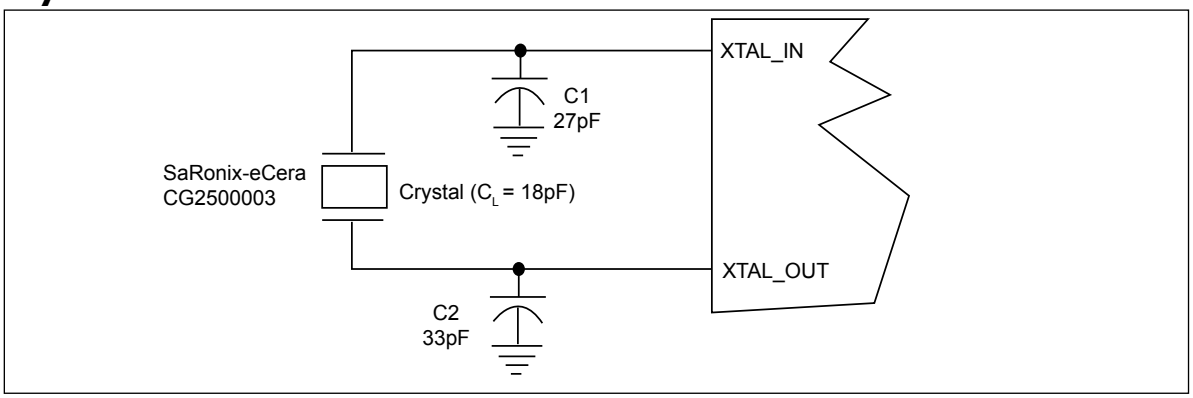
Figure 3. Configuration Test Load Board Termination for LVCMOS output

Application Notes

Crystal circuit connection

The following diagram shows PI6LC4872 crystal circuit connection with a parallel crystal. For the C_L=18pF crystal, it is suggested to use C1=27pF, C2=33pF. C1 and C2 can be adjusted to fine tune to the target ppm of crystal oscillator according to different board layouts.

Crystal Oscillator Circuit



Recommended Crystal Specification

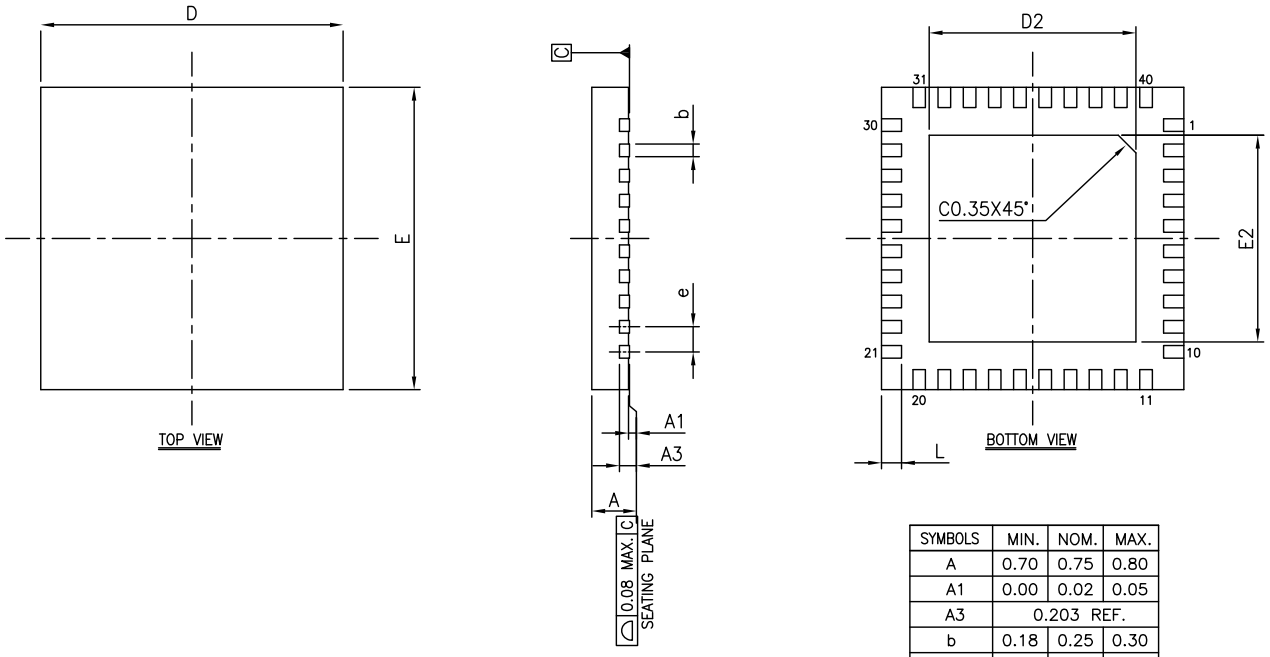
Pericom recommends:

a) GC2500003 XTAL 49S/SMD(4.0 mm), 25M, CL=18pF, +/-30ppm, http://www.pericom.com/pdf/datasheets/se/GC_GF.pdf

b) FY2500081, SMD 5x3.2(4P), 25M, CL=18pF, +/-30ppm, http://www.pericom.com/pdf/datasheets/se/FY_F9.pdf

c) FL2500047, SMD 3.2x2.5(4P), 25M, CL=18pF, +/-20ppm, http://www.pericom.com/pdf/datasheets/se/FL.pdf

Packaging Mechanical: 40-Pin QFN (ZD)



SYMBOLS	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.203 REF.	
b	0.18	0.25	0.30
D	5.90	6.00	6.10
E	5.90	6.00	6.10
e		0.50 BSC	
L	0.35	0.40	0.45
D2	4.40	4.50	4.55
E2	4.40	4.50	4.55

Notes:
1. All dimensions are in mm.
2. Refer JEDEC MO-220.
3. Bilateral coplanarity zone applies to the exposed heat sink slug as well as the terminals.

PERICOM Enabling Serial Connectivity

DATE: 07/12/11

DESCRIPTION: 40-contact, Thin Fine Pitch Quad Flat No-Lead, TQFN

PACKAGE CODE: ZD (ZD40)

DOCUMENT CONTROL #: PD-2021 **REVISION: C**

Ordering Information

Ordering Code	Package Code	Package Type	Output Signaling	Operating Temperature
PI6LC4872-01ZDIE	ZD	Pb-free & Green, 40-pin QFN	LVPECL Outputs	Industrial
PI6LC4872-02ZDIE	ZD	Pb-free & Green, 40-pin QFN	LVDS Outputs	Industrial