

## Buck or Buck/Boost Pre-Regulator with a Synchronous Buck, 5 Internal Linear Regulators, Pulse-Width Watchdog Timer, and SPI

### FEATURES AND BENEFITS

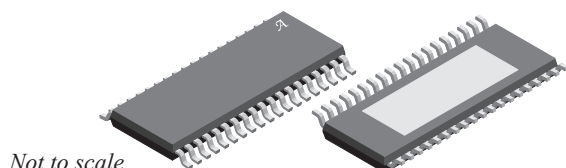
- ASIL-Ready: possesses device features for safety-critical systems
- Automotive AEC-Q100 qualified
- Wide input voltage range, 3.8 to 40 V<sub>IN</sub> operating range, 50 V<sub>IN</sub> maximum
- Buck or buck/boost pre-regulator (VREG)
- Adjustable 1.3 to 3.3 V, 400 mA synchronous buck.
- Four internal linear regulators with foldback short-circuit protection, 3.3 V (3V3) and three 5 V (V5CAN, V5A, and V5B)
- One internal 5 V linear regulator (V5P) with foldback short-circuit and short-to-battery protection
- Power-on reset signal indicating a fault on the synchronous buck, 3V3 or V5A regulator outputs (NPOR)
- Window watchdog timer with fail-safe features
- Dual bandgaps for increased safety coverage and fault detection, BGVREF, BGFAULT
- Control and diagnostic reporting through a serial peripheral interface (SPI)
- Logic enable input (ENB) for microprocessor control
- Ignition enable input (ENBAT) with status indicator output
- Frequency dithering and controlled slew rate helps reduce EMI/EMC
- OV and UV protection for all output rails
- Pin-to-pin and pin-to-ground tolerant at every pin

### APPLICATIONS

- Automotive Control Modules for:
  - EPS modules
  - Automotive power trains
  - CAN power supplies
  - High-temperature applications



### PACKAGE: 38-Pin eTSSOP (suffix LV)



### DESCRIPTION

The A4412 is a power management IC that uses a buck or buck/boost pre-regulator to efficiently convert automotive battery voltages into a tightly regulated intermediate voltage complete with control, diagnostics and protections. The output of the pre-regulator supplies a 5 V / 100 mA protected linear regulator, a 3.3 V / 90 mA linear regulator, a 5 V / 200 mA linear regulator, a 5 V / 55 mA linear regulator, a 5 V / 30 mA linear regulator and an adjustable 400 mA synchronous buck regulator. Designed to supply CAN transceiver, sensor, and microprocessor power supplies in high-temperature environments, the A4412 is ideal for under-hood applications.

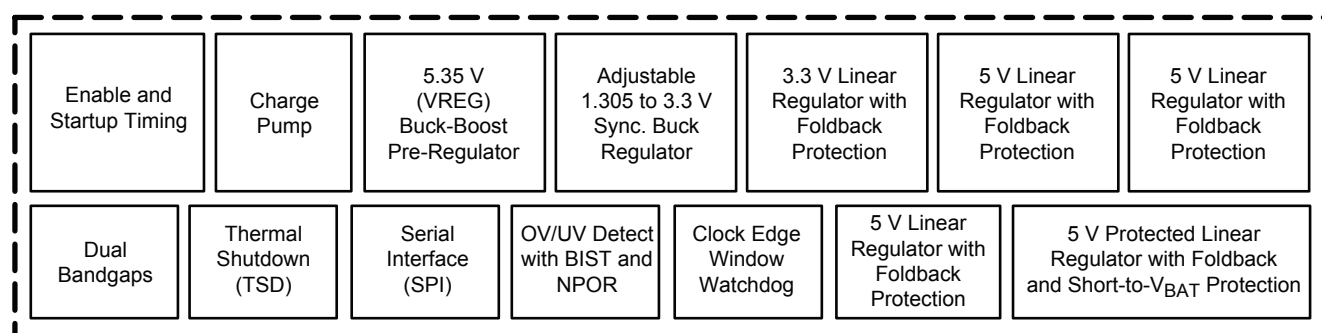
Enable inputs to the A4412 include a logic level (ENB) and a high-voltage (ENBAT). The A4412 also provides flexibility with disable function of the individual 5 V rails through a serial peripheral interface (SPI).

Diagnostic outputs from the A4412 include a power-on-reset output (NPOR), an ENBAT status output, and a fault flag output to alert the microprocessor that a fault has occurred. The microprocessor can read fault status through SPI. Dual bandgaps, one for regulation and one for fault checking, improve safety coverage and fault detection of the A4412.

The A4412 contains a Window Watchdog timer with a detect period of 2 ms. The watchdog timer is activated once it receives valid 2 ms pulses from the processor. The watchdog can be put into flash mode or be reset via secure SPI commands.

Protection features include undervoltage and overvoltage on all output rails. In case of a shorted output, all linear regulators feature foldback overcurrent protection. In addition, the V5P output is protected from a short-to-battery event. Both switching regulators include pulse-by-pulse current limit, hiccup mode short-circuit protection, LX short-circuit protection, missing asynchronous diode protection (VREG only) and thermal shutdown.

The A4412 is supplied in a low-profile (1.2 mm maximum height) 38-lead eTSSOP package (suffix “LV”) with exposed power pad.



A4412 Simplified Block Diagram

# A4412

## Buck or Buck/Boost Pre-Regulator with Synchronous Buck, 5 Internal Linear Regulators, Pulse-Width Watchdog Timer, and SPI

### SELECTION GUIDE

Part Number	Temperature Range	Package	Packing [1]	Lead Frame
A4412KLVTR-T	-40 to 150°C	38-pin eTSSOP w/ thermal pad	4000 pieces per 7-in reel	100% matte tin

[1] Contact Allegro for additional packing options.



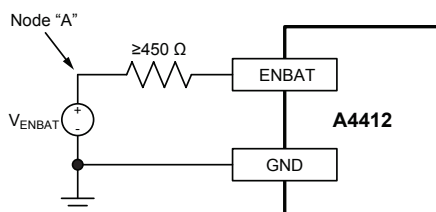
### SPECIFICATIONS

#### ABSOLUTE MAXIMUM RATINGS [2]

Characteristic	Symbol	Notes	Rating	Unit
VIN	V <sub>VIN</sub>		-0.3 to 50	V
ENBAT	V <sub>ENBAT</sub>	With current limiting resistor [3]	-13 to 50	V
			-0.3 to 8	V
	I <sub>ENBAT</sub>		±75	mA
LX1	V <sub>LX1</sub>		-0.3 to V <sub>VIN</sub> + 0.3	V
		t < 250 ns	-1.5	V
		t < 50 ns	V <sub>VIN</sub> + 3 V	V
VCP, CP1, CP2	V <sub>VCP</sub> , V <sub>CP1</sub> , V <sub>CP2</sub>		-0.3 to 60	V
V5P	V <sub>V5P</sub>	Independent of V <sub>VIN</sub>	-1 to 50	V
All other pins			-0.3 to 7	V
Junction Temperature Range	T <sub>J</sub>		-40 to 165	°C
Storage Temperature Range	T <sub>stg</sub>		-40 to 150	°C

[2] Stresses beyond those listed in this table may cause permanent damage to the device. The absolute maximum ratings are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the Electrical Characteristics table is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

[3] The higher ENBAT ratings (-13 V and 50 V) are measured at node "A" in the following circuit configuration:



#### THERMAL CHARACTERISTICS: May require derating at maximum conditions; see application information

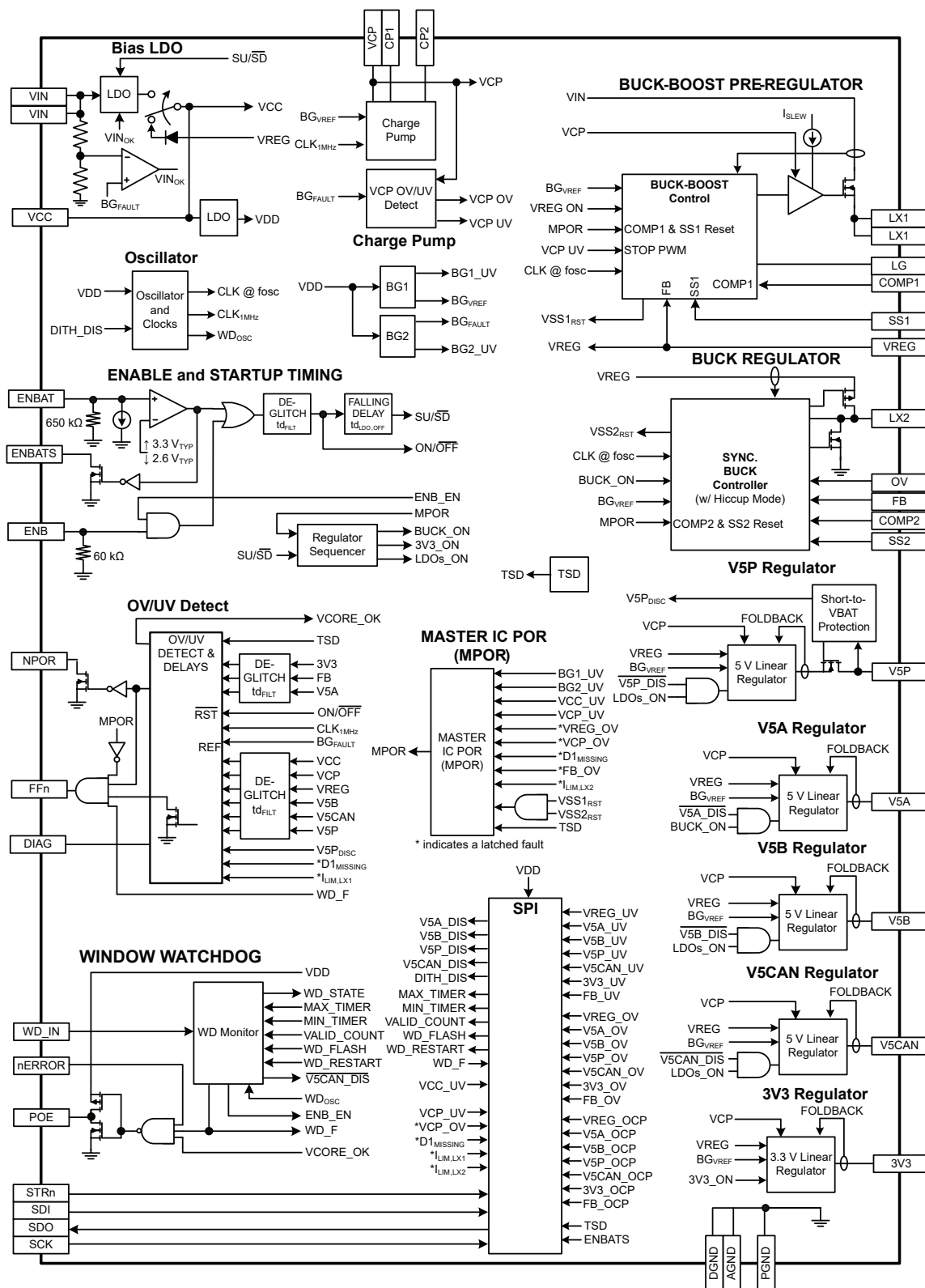
Characteristic	Symbol	Test Conditions [4]	Value	Unit
Junction to Ambient Thermal Resistance	R <sub>θJA</sub>	eTSSOP-38 (LV) package	30	°C/W

[4] Additional thermal information available on the Allegro website.

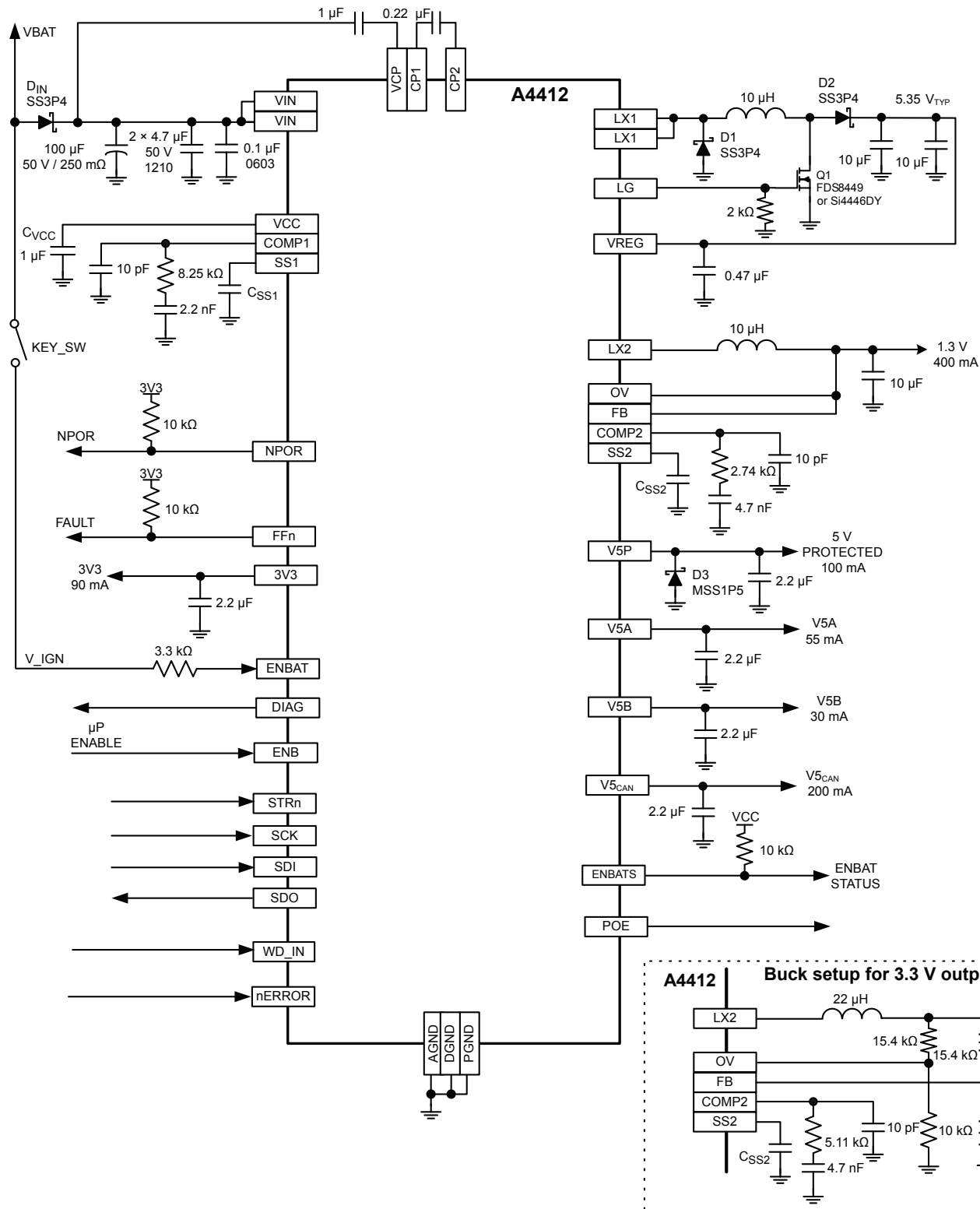
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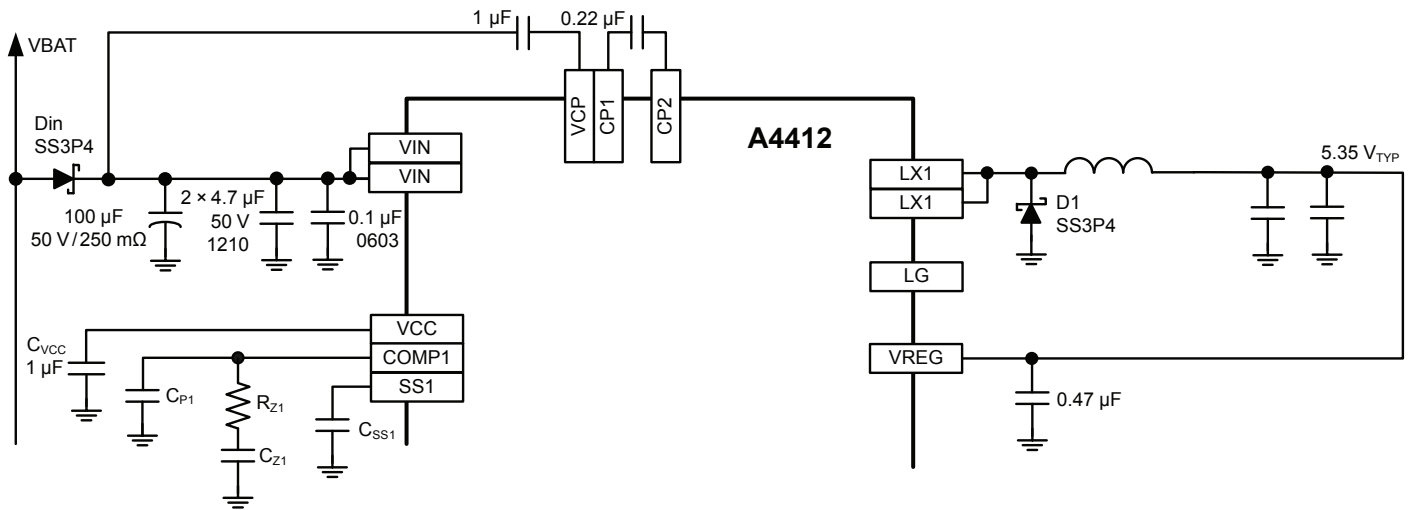
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## FUNCTIONAL BLOCK DIAGRAM

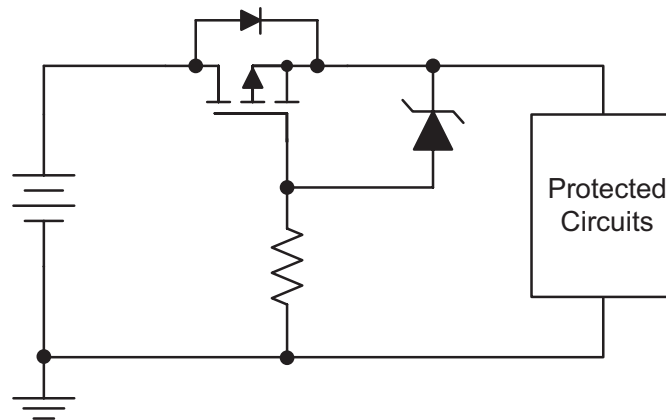


## TYPICAL SCHEMATICS

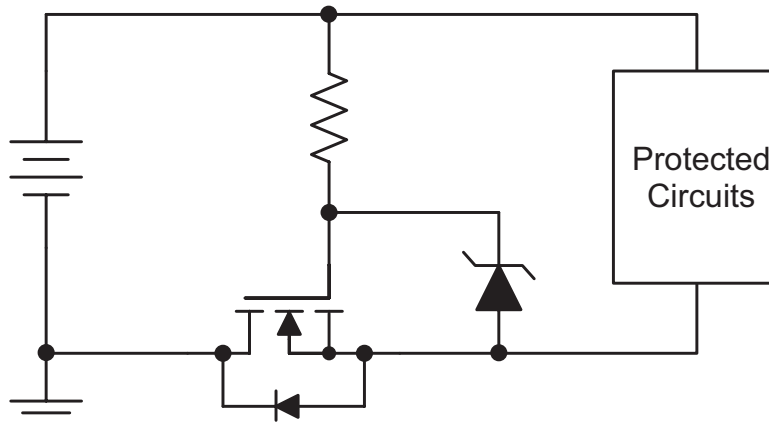
Buck-Boost Mode Using a Series Diode for Reverse-Battery Protection ( $D_{IN}$ )



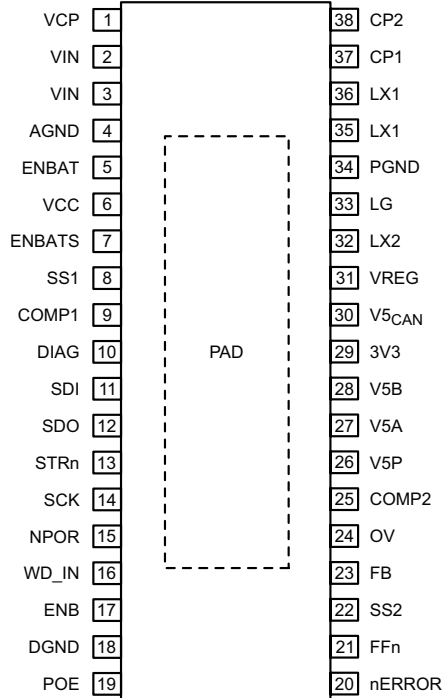
Functional Block Diagram Modifications for Buck Only Mode



Functional Block Diagram Using a PMOS FET for Reverse-Battery Protection Instead of a Series Schottky Diode (D<sub>IN</sub>)



Functional Block Diagram Using an NMOS FET for Reverse-Battery Protection Instead of a Series Schottky Diode (D<sub>IN</sub>)



**Package LV, 38-Pin eTSSOP  
Pinout Diagram**

**Terminal List Table**

Number	Name	Function
1	VCP	Charge pump reservoir capacitor
2,3	VIN	Input voltage pins
4	AGND	Analog ground pin
5	ENBAT	Ignition enable input from the key/switch via a series resistor
6	VCC	Internal voltage regulator bypass capacitor pin
7	ENBATS	Open-drain ignition status output of ENBAT
8	SS1	Soft-start programming pin for the buck/boost pre-regulator
9	COMP1	Error amplifier compensation network pin for the buck/boost pre-regulator
10	DIAG	Diagnostic pin to aid debug. A pulse train whose frequency depends on the fault that occurred is sent to this pin. See fault table.
11	SDI	SPI data input from the microcontroller
12	SDO	SPI data output to the microcontroller
13	STRn	Chip select input from the microcontroller
14	SCK	Clock input from the microcontroller
15	NPOR	Active LOW, open-drain regulator fault detection output
16	WD_IN	Watchdog pulse train input from a microcontroller or DSP
17	ENB	Logic enable input from a microcontroller or DSP
18	DGND	Digital ground pin
19	POE	Gate drive enable signal, goes low if a watchdog fault is detected or nERROR is low
20	nERROR	System fault input. This fault is ANDed with the watchdog fault to create the POE signal
21	FFn	Active-low fault flag, alerts the microprocessor of a fault within the regulator
22	SS2	Soft-start programming pin for the adjustable synchronous buck regulator
23	FB	Feedback pin with 1.305 V reference for synchronous buck regulator
24	OV	Input to synchronous overvoltage sense circuit
25	COMP2	Error amplifier compensation network pin for the adjustable synchronous buck regulator
26	V5P	5 V/100 mA protected regulator output
27	V5A	5 V/55 mA regulator output
28	V5B	5 V/30 mA regulator output
29	3V3	3.3 V/180 mA regulator output
30	5V <sub>CAN</sub>	5 V/200 mA regulator output for communications
31	VREG	Output of the pre-regulator and input to the linear regulators and synchronous buck
32	LX2	Switching node for the adjustable synchronous buck regulator
33	LG	Boost gate drive output for the buck/boost pre-regulator
34	PGND	Power ground for the adjustable synchronous regulator/gate driver
35,36	LX1	Switching node for the buck/boost pre-regulator
37	CP1	Charge pump capacitor connection
38	CP2	Charge pump capacitor connection
–	PAD	Connect to ground

**ELECTRICAL CHARACTERISTICS – GENERAL SPECIFICATIONS** [1]: Valid at 3.8 V [4]  $\leq V_{VIN} \leq 40$  V,  $-40^{\circ}\text{C} \leq T_J \leq 150^{\circ}\text{C}$ , unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
<b>GENERAL SPECIFICATIONS</b>						
Operating Input Voltage	$V_{VIN}$	After $V_{VIN} > V_{IN\_START}$ and $V_{ENB} > 2$ V or $V_{ENBAT} > 3.5$ V, buck-boost mode	3.8	13.5	40	V
		After $V_{VIN} > V_{IN\_START}$ and $V_{ENB} > 2$ V or $V_{ENBAT} > 3.5$ V, buck mode	5.5	13.5	40	V
VIN UVLO START Voltage	$V_{IN\_START}$	$V_{VIN}$ rising	4.55	4.8	5.05	V
VIN UVLO STOP Voltage	$V_{IN\_STOP}$	$V_{VIN}$ falling, $V_{ENBAT} \geq 3.8$ V or $V_{ENB} \geq 2$ V, $V_{VREG} = 5.2$ V	3.25	3.5	3.75	V
VIN UVLO Hysteresis	$V_{IN\_HYS}$	$V_{IN\_START} - V_{IN\_STOP}$	–	1.3	–	V
Supply Quiescent Current [1]	$I_Q$	$V_{VIN} = 13.5$ V, $V_{ENBAT} \geq 3.8$ V or $V_{ENB} \geq 2.0$ V, $V_{VREG} = 5.6$ V (no PWM)	–	13	–	mA
	$I_{Q,SLEEP}$	$V_{VIN} = 13.5$ V, $V_{ENBAT} \leq 2.2$ V and $V_{ENB} \leq 0.8$ V	–	–	10	$\mu\text{A}$
<b>PWM SWITCHING FREQUENCY AND DITHERING</b>						
Switching Frequency	$f_{OSC}$	Dithering disabled 3.8 V [4] $\leq V_{VIN} \leq 18$ V	2	2.2	2.4	MHz
Frequency Dithering	$\Delta f_{OSC}$	As a percent of $f_{OSC}$	–	$\pm 10$	–	%
Dither/Slew START Threshold	$V_{IN\_DS,ON}$	$V_{VIN}$ rising	8.5	9	9.5	V
		$V_{VIN}$ falling	–	17	–	V
Dither/Slew STOP Threshold	$V_{IN\_DS,OFF}$	$V_{VIN}$ falling	7.8	8.3	8.8	V
		$V_{VIN}$ rising	–	18	–	V
VIN Dithering/Slew Hysteresis			–	700	–	mV
<b>CHARGE PUMP (VCP)</b>						
Output Voltage	$V_{VCP}$	$V_{VCP} - V_{VIN}$ , $V_{VIN} \geq 5.5$ V, buck mode	4.1	6.6	–	V
		$V_{VCP} - V_{VIN}$ , $V_{VIN} = 3.8$ V, $V_{VREG} = 5.35$ V, buck-boost mode	3.1	3.8	–	V
Switching Frequency	$f_{SW,CP}$		–	65	–	kHz
<b>VCC PIN VOLTAGE</b>						
Output Voltage	$V_{VCC}$	$V_{VREG} = 5.35$ V	–	4.65	–	V
<b>SYSTEM CLOCK</b>						
Internal Clock Frequency	$f_{SYS}$		–	1	–	MHz
Internal Clock Tolerance	$f_{SYS,TOL}$		–4	–	4	%
<b>THERMAL PROTECTION</b>						
Thermal Shutdown Threshold [2]	$T_{TSD}$	$T_J$ rising	165	–	–	$^{\circ}\text{C}$
Thermal Shutdown Hysteresis [2]	$T_{HYS}$		–	15	–	$^{\circ}\text{C}$

[1] For input and output current specifications, negative current is defined as coming out of the node or pin (sourcing), positive current is defined as going into the node or pin (sinking).

[2] Ensured by design and characterization, not production tested.

[3] Specifications at 25°C or 85°C are guaranteed by design and characterization, not production tested.

[4] The lowest operating voltage is only valid if the conditions  $V_{VIN} > V_{IN\_START}$  and  $V_{VCP} - V_{VIN} > V_{VCP\_UV,H}$  and  $V_{VREG} > V_{VREG\_UV,H}$  are satisfied before  $V_{VIN}$  is reduced.



## ELECTRICAL CHARACTERISTICS – BUCK AND BUCK-BOOST PRE-REGULATOR SPECIFICATIONS <sup>[1]</sup>: Valid at 3.8 V <sup>[4]</sup> ≤ V<sub>VIN</sub> ≤ 40 V, –40°C ≤ T<sub>J</sub> ≤ 150°C, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
OUTPUT VOLTAGE SPECIFICATIONS						
Buck Output Voltage – Regulating	V <sub>VREG</sub>	V <sub>VIN</sub> = 13.5 V, ENB = 1, 0.1 A < I <sub>VREG</sub> < 1.2 A	5.25	5.35	5.45	V
PULSE-WIDTH MODULATION (PWM)						
PWM Ramp Offset	PWM1 <sub>OFFS</sub>	V <sub>COMP1</sub> for 0% duty cycle	–	400	–	mV
LX1 Rising Slew Rate Control [2]	LX1 <sub>RISE</sub>	V <sub>VIN</sub> = 13.5 V, 10% to 90%, I <sub>VREG</sub> = 1 A	–	1.4	–	V/ns
LX1 Falling Slew Rate [2]	LX1 <sub>FALL</sub>	V <sub>VIN</sub> = 13.5 V, 90% to 10%, I <sub>VREG</sub> = 1 A	–	1.5	–	V/ns
Buck Minimum ON-Time	t <sub>ON,MIN,BUCK</sub>		–	85	160	ns
Buck Maximum Duty Cycle	D <sub>MAX,BUCK</sub>	V <sub>VIN</sub> < 7.8 V	–	100	–	%
Boost Maximum Duty Cycle	D <sub>MAX,BST</sub>	After V <sub>VIN</sub> > V <sub>VIN,START</sub> , V <sub>VIN</sub> = 3.8 V	–	65	–	%
COMP1 to LX1 Current Gain	gm <sub>POWER1</sub>		–	4.57	–	A/V
Slope Compensation [2]	S <sub>E1</sub>		1.1	1.62	2.15	A/μs
INTERNAL MOSFET						
MOSFET On-Resistance	R <sub>DSon</sub>	V <sub>VIN</sub> = 13.5 V, T <sub>J</sub> = –40°C [2], I <sub>DS</sub> = 0.1 A	–	60	75	mΩ
		V <sub>VIN</sub> = 13.5 V, T <sub>J</sub> = 25°C [3], I <sub>DS</sub> = 0.1 A	–	95	110	mΩ
		V <sub>VIN</sub> = 13.5 V, T <sub>J</sub> = 150°C, I <sub>DS</sub> = 0.1 A	–	160	190	mΩ
MOSFET Leakage	I <sub>FET,LKG</sub>	V <sub>ENBAT</sub> ≤ 2.2 V, V <sub>ENB</sub> ≤ 0.8 V, V <sub>LX1</sub> = 0 V, V <sub>VIN</sub> = 16 V, –40°C < T <sub>J</sub> < 85°C [3]	–	–	10	μA
		V <sub>ENBAT</sub> ≤ 2.2 V, V <sub>ENB</sub> ≤ 0.8 V, V <sub>LX1</sub> = 0 V, V <sub>VIN</sub> = 16 V, –40°C < T <sub>J</sub> < 150°C	–	50	150	μA
ERROR AMPLIFIER						
Open Loop Voltage Gain	AVOL1		–	60	–	dB
Transconductance	gm <sub>EA1</sub>	V <sub>SS1</sub> = 750 mV	520	720	920	μA/V
		V <sub>SS1</sub> = 500 mV	260	360	460	μA/V
Output Current	I <sub>EA1</sub>		–	±75	–	μA
Maximum Output Voltage	EA1 <sub>VO(max)</sub>	V <sub>VIN</sub> < 8.5 V	1.2	1.52	2.1	V
		V <sub>VIN</sub> > 9.5 V	0.9	1.22	1.7	V
Minimum Output Voltage	EA1 <sub>VO(min)</sub>		–	–	300	mV
COMP1 Pull Down Resistance	R <sub>COMP1</sub>	HICCUP1 = 1 or FAULT1 = 1 or V <sub>ENBAT</sub> ≤ 2.2 V and V <sub>ENB</sub> ≤ 0.8 V, latched until V <sub>SS1</sub> < V <sub>SS1,RST</sub>	–	1	–	kΩ

<sup>[1]</sup> For input and output current specifications, negative current is defined as coming out of the node or pin (sourcing), positive current is defined as going into the node or pin (sinking).

<sup>[2]</sup> Ensured by design and characterization, not production tested.

<sup>[3]</sup> Specifications at 25°C or 85°C are guaranteed by design and characterization, not production tested.

<sup>[4]</sup> The lowest operating voltage is only valid if the conditions V<sub>VIN</sub> > V<sub>VIN,START</sub> and V<sub>VCP</sub> – V<sub>VIN</sub> > V<sub>VCP,UV,H</sub> and V<sub>VREG</sub> > V<sub>VREG,UV,H</sub> are satisfied before V<sub>VIN</sub> is reduced.

**ELECTRICAL CHARACTERISTICS – BUCK AND BUCK-BOOST PRE-REGULATOR SPECIFICATIONS (continued) [1]:**  
Valid at 3.8 V [1] ≤ V<sub>VIN</sub> ≤ 40 V, –40°C ≤ T<sub>J</sub> ≤ 150°C, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
BOOST MOSFET (LG) GATE DRIVER						
LG High Output Voltage	V <sub>LG,ON</sub>	V <sub>VIN</sub> = 6 V, V <sub>VREG</sub> = 5.35 V	4.6	–	5.5	V
LG Low Output Voltage	V <sub>LG,OFF</sub>	V <sub>VIN</sub> = 13.5 V, V <sub>VREG</sub> = 5.35 V	–	0.2	0.4	V
LG Source Current [1]	I <sub>LG,ON</sub>	V <sub>VIN</sub> = 6 V, V <sub>VREG</sub> = 5.35 V, V <sub>LG</sub> = 1 V	–	–300	–	mA
LG Sink Current [1]	I <sub>LG,OFF</sub>	V <sub>VIN</sub> =13.5 V, V <sub>VREG</sub> = 5.35 V, V <sub>LG</sub> = 1 V	–	150	–	mA
SOFT-START						
SS1 Offset Voltage	V <sub>SS1</sub> OFFS	V <sub>SS1</sub> rising due to ISS1 <sub>SU</sub>	–	400	–	mV
SS1 Fault/Hiccup Reset Voltage	V <sub>SS1</sub> RST	V <sub>SS1</sub> falling due to HICCUP1 = 1 or FAULT1 = 1 or V <sub>ENBAT</sub> ≤ 2.2 V and V <sub>ENB</sub> ≤ 0.8 V	140	200	275	mV
SS1 Startup (Source) Current	ISS1 <sub>SU</sub>	V <sub>SS1</sub> = 1 V, HICCUP1 = FAULT1 = 0	–15	–20	–25	μA
SS1 Hiccup (Sink) Current	ISS1 <sub>HIC</sub>	V <sub>SS1</sub> = 0.5 V, HICCUP1 = 1	7.5	10	12.5	μA
SS1 Delay Time	t <sub>SS1,DLY</sub>	C <sub>SS1</sub> = 22 nF	–	440	–	μs
SS1 Ramp Time	t <sub>SS1</sub>	C <sub>SS1</sub> = 22 nF	–	880	–	μs
SS1 Pull-Down Resistance	RPD <sub>SS1</sub>	FAULT1 = 1 or V <sub>ENBAT</sub> ≤ 2.2 V and V <sub>ENB</sub> ≤ 0.8 V, latched until V <sub>SS1</sub> < V <sub>SS1</sub> RST	–	3	–	kΩ
SS1 PWM Frequency Foldback	f <sub>SW1,SS</sub>	0 V ≤ V <sub>VREG</sub> < 1.34 V typical and V <sub>COMP1</sub> = EA1 <sub>VO(max)</sub>	–	f <sub>OSC</sub> /8	–	–
		0 V ≤ V <sub>VREG</sub> < 1.34 V typical and V <sub>COMP1</sub> < EA1 <sub>VO(max)</sub>	–	f <sub>OSC</sub> /4	–	–
		1.34 V ≤ V <sub>VREG</sub> < 2.68 V typical and V <sub>COMP1</sub> < EA1 <sub>VO(max)</sub>	–	f <sub>OSC</sub> /2	–	–
		V <sub>VREG</sub> ≥ 2.68 V typical and V <sub>COMP1</sub> < EA1 <sub>VO(max)</sub>	–	f <sub>OSC</sub>	–	–
HICCUP MODE						
Hiccup1 OCP Enable Threshold	V <sub>HIC1,EN</sub>	V <sub>SS1</sub> rising	–	2.3	–	V
Hiccup1 OCP PWM Counts	t <sub>HIC1,OCP</sub>	V <sub>SS1</sub> > V <sub>HIC1,EN</sub> , V <sub>VREG</sub> < 1.95 V <sub>TYP</sub> , V <sub>COMP</sub> = EA1 <sub>VO(max)</sub>	–	30	–	PWM cycles
		V <sub>SS1</sub> > V <sub>HIC1,EN</sub> , V <sub>VREG</sub> > 1.95 V <sub>TYP</sub> , V <sub>COMP</sub> = EA1 <sub>VO(max)</sub>	–	120	–	PWM cycles
CURRENT PROTECTIONS						
Pulse-by-Pulse Current Limit	I <sub>LIM1,ton(min)</sub>	V <sub>VIN</sub> < 8.5 V	3.83	4.2	4.77	A
		V <sub>VIN</sub> > 9.5 V	2.49	2.8	3.2	A
LX1 Short-Circuit Current Limit	I <sub>LIM,LX1</sub>	Latched fault after 2 <sup>nd</sup> detection	5.3	7.1	–	A

[1] For input and output current specifications, negative current is defined as coming out of the node or pin (sourcing), positive current is defined as going into the node or pin (sinking).

[2] Ensured by design and characterization, not production tested.

[3] Specifications at 25°C or 85°C are guaranteed by design and characterization, not production tested.

[4] The lowest operating voltage is only valid if the conditions V<sub>VIN</sub> > V<sub>VIN,START</sub> and V<sub>VCP</sub> – V<sub>VIN</sub> > V<sub>VCP,UV,H</sub> and V<sub>VREG</sub> > V<sub>VREG,UV,H</sub> are satisfied before V<sub>VIN</sub> is reduced.

**ELECTRICAL CHARACTERISTICS – ADJUSTABLE SYNCHRONOUS BUCK REGULATOR [1]:**Valid at 3.8 V [4] ≤ V<sub>VIN</sub> ≤ 40 V, -40°C ≤ T<sub>J</sub> ≤ 150°C, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
<b>MISSING ASYNCHRONOUS DIODE (D1) PROTECTION</b>						
Detection Level	V <sub>D,OPEN</sub>	-40°C ≤ T <sub>J</sub> ≤ 85°C	-1.72	-1.4	-1.0	V
		-40°C ≤ T <sub>J</sub> ≤ 150°C	-1.72	-1.4	-0.85	V
Time Filtering [2]	t <sub>D,OPEN</sub>		50	–	250	ns
<b>FEEDBACK REFERENCE VOLTAGE</b>						
Reference Voltage	V <sub>FB</sub>		1.27	1.305	1.33	V
<b>PULSE-WIDTH MODULATION (PWM)</b>						
PWM Ramp Offset	PWM2 <sub>OFFS</sub>	V <sub>COMP2</sub> for 0% duty cycle	–	440	–	mV
High-Side MOSFET Minimum ON-Time	t <sub>ON(MIN)</sub>		–	65	105	ns
High-Side MOSFET Minimum OFF-Time	t <sub>OFF(MIN)</sub>	Does not include total gate driver non-overlap time, t <sub>NO</sub>	–	100	200	ns
Gate Driver Non-Overlap Time [2]	t <sub>NO</sub>		–	15	–	ns
COMP2 to LX2 Current Gain	gm <sub>POWER2</sub>		–	1	–	A/V
Slope Compensation [2]	S <sub>E2</sub>		0.19	0.26	0.33	A/μs
<b>INTERNAL MOSFETS</b>						
High-Side MOSFET On-Resistance	RDS <sub>ON (HS)</sub>	T <sub>J</sub> = 25°C [3], I <sub>DS</sub> = 100 mA	–	225	300	mΩ
		I <sub>DS</sub> = 100 mA	–	–	500	mΩ
LX2 Node Rise/Fall Time [2]	t <sub>R/F,LX2</sub>	V <sub>VREG</sub> = 5.5 V	–	12	–	ns
High-Side MOSFET Leakage [1]	I <sub>DSS (HS)</sub>	V <sub>ENB</sub> ≤ 2.2 V, V <sub>ENB</sub> ≤ 0.8 V, V <sub>LX2</sub> = 0 V, V <sub>VREG</sub> = 5.5 V, -40°C < T <sub>J</sub> < 85°C [3]	–	–	2	μA
		V <sub>ENB</sub> ≤ 2.2 V, V <sub>ENB</sub> ≤ 0.8 V, V <sub>LX2</sub> = 0 V, V <sub>VREG</sub> = 5.5 V, -40°C < T <sub>J</sub> < 150°C	–	3	15	μA
Low-Side MOSFET On-Resistance	RDS <sub>ON (LS)</sub>	T <sub>J</sub> = 25°C [3], I <sub>DS</sub> = 100 mA	–	165	195	mΩ
		I <sub>DS</sub> = 100 mA	–	–	280	mΩ
Low-Side MOSFET Leakage [1]	I <sub>DSS (LS)</sub>	V <sub>ENB</sub> ≤ 2.2 V, V <sub>ENB</sub> ≤ 0.8 V, V <sub>LX2</sub> = 5.5 V, -40°C < T <sub>J</sub> < 85°C [3]	–	–	1	μA
		V <sub>ENB</sub> ≤ 2.2 V, V <sub>ENB</sub> ≤ 0.8 V, V <sub>LX2</sub> = 5.5 V, -40°C < T <sub>J</sub> < 150°C	–	4	10	μA
Pulse-by-Pulse Current Limit	I <sub>LIM2,5%</sub>	Duty cycle = 5%	720	840	1020	mA
	I <sub>LIM2,90%</sub>	Duty cycle = 90%	480	640	800	mA
LX2 Short-Circuit Protection	V <sub>LIM,LX2</sub>	V <sub>LX2</sub> stuck low for more than 60 ns, hiccup mode after 2× detection	–	V <sub>VREG</sub> – 1.2 V	–	V

[1] For input and output current specifications, negative current is defined as coming out of the node or pin (sourcing), positive current is defined as going into the node or pin (sinking).

[2] Ensured by design and characterization, not production tested.

[3] Specifications at 25°C or 85°C are guaranteed by design and characterization, not production tested.

[4] The lowest operating voltage is only valid if the conditions V<sub>VIN</sub> > V<sub>VIN,START</sub> and V<sub>VCP</sub> – V<sub>VIN</sub> > V<sub>VCP,UV,H</sub> and V<sub>VREG</sub> > V<sub>VREG,UV,H</sub> are satisfied before V<sub>VIN</sub> is reduced.

**ELECTRICAL CHARACTERISTICS – ADJUSTABLE SYNCHRONOUS BUCK REGULATOR (continued) [1]:**Valid at 3.8 V [4] ≤ V<sub>VIN</sub> ≤ 40 V, −40°C ≤ T<sub>J</sub> ≤ 150°C, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
ERROR AMPLIFIER						
Feedback Input Bias Current [1]	I <sub>FB,ADJ</sub>	V <sub>COMP2</sub> = 0.8 V, V <sub>FB,ADJ</sub> regulated so that I <sub>COMP2</sub> = 0 A	–	–150	–350	nA
Open Loop Voltage Gain [2]	AVOL2		–	60	–	dB
Transconductance	gm <sub>EA2</sub>	I <sub>COMP2</sub> = 0 A, V <sub>SS2</sub> > 500 mV	520	720	920	μA/V
		0 V < V <sub>SS2</sub> < 500 mV	–	250	–	μA/V
Source and Sink Current	I <sub>EA2</sub>	V <sub>COMP2</sub> = 0.8 V	–	±50	–	μA
Maximum Output Voltage	EA2 <sub>VO(max)</sub>		1.04	1.3	1.56	V
Minimum Output Voltage	EA2 <sub>VO(min)</sub>		–	–	150	mV
COMP2 Pull-Down Resistance	R <sub>COMP2</sub>	HICCUP2 = 1 or FAULT2 = 1 or V <sub>ENBAT</sub> ≤ 2.2 V and V <sub>ENB</sub> ≤ 0.8 V, latched until V <sub>SS2</sub> < V <sub>SS2RST</sub>	–	1.3	–	kΩ
SOFT-START						
SS2 Offset Voltage	V <sub>SS2OFFS</sub>	V <sub>SS2</sub> rising due to ISS2 <sub>SU</sub>	120	200	270	mV
SS2 Fault/Hiccup Reset Voltage	V <sub>SS2RST</sub>	V <sub>SS2</sub> falling due to HICCUP2 = 1 or FAULT2 = 1 or V <sub>ENBAT</sub> ≤ 2.2 V and V <sub>ENB</sub> ≤ 0.8 V	–	100	120	mV
SS2 Startup (Source) Current	ISS2 <sub>SU</sub>	V <sub>SS2</sub> = 1 V, HICCUP2 = FAULT2 = 0	–15	–20	–25	μA
SS2 Hiccup (Sink) Current	ISS2 <sub>HIC</sub>	V <sub>SS2</sub> = 0.5 V, HICCUP2 = 1	5	10	15	μA
SS2 to Synchronous Buck Output Delay Time	t <sub>SS2,DLY</sub>	C <sub>SS2</sub> = 10 nF	–	100	–	μs
Synchronous Buck Soft-Start Ramp Time	t <sub>SS2</sub>	C <sub>SS2</sub> = 10 nF	–	400	–	μs
SS2 Pull-Down Resistance	RPD <sub>SS2</sub>	FAULT2 = 1 or V <sub>ENBAT</sub> ≤ 2.2 V and V <sub>ENB</sub> ≤ 0.8 V, latched until V <sub>SS2</sub> < V <sub>SS2RST</sub>	–	2	–	kΩ
SS2 PWM Frequency Foldback	f <sub>SW2,SS</sub>	V <sub>FB</sub> < 450 mV typical	–	f <sub>OSC</sub> /4	–	–
		450 mV < V <sub>FB</sub> < 780 mV typical	–	f <sub>OSC</sub> /2	–	–
		V <sub>FB</sub> > 780 mV typical	–	f <sub>OSC</sub>	–	–
HICCUP MODE						
Hiccup2 OCP Enable Threshold	V <sub>HIC2,EN</sub>	V <sub>SS2</sub> rising	–	1.8	–	V
Hiccup2 OCP Counts	t <sub>HIC2,OCP</sub>	V <sub>SS2</sub> > V <sub>HIC2,EN</sub> , V <sub>FB</sub> < 450 mV <sub>TYP</sub>	–	30	–	PWM cycles
		V <sub>SS2</sub> > V <sub>HIC2,EN</sub> , V <sub>FB</sub> > 450 mV <sub>TYP</sub>	–	120	–	PWM cycles

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[2] Ensured by design and characterization, not production tested.

[3] Specifications at 25°C or 85°C are guaranteed by design and characterization, not production tested.

[4] The lowest operating voltage is only valid if the conditions V<sub>VIN</sub> > V<sub>VIN,START</sub> and V<sub>VCP</sub> – V<sub>VIN</sub> > V<sub>VCP,UV,H</sub> and V<sub>VREG</sub> > V<sub>VREG,UV,H</sub> are satisfied before V<sub>VIN</sub> is reduced.

## ELECTRICAL CHARACTERISTICS – LINEAR REGULATOR SPECIFICATIONS [1]:

Valid at 3.8 V [4]  $\leq V_{VIN} \leq 40$  V,  $-40^{\circ}\text{C} \leq T_J \leq 150^{\circ}\text{C}$ , unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
<b>V5CAN, V5A, V5B AND V5P LINEAR REGULATORS</b>						
V5CAN Accuracy and Load Regulation	$V_{V5CAN}$	10 mA $< I_{V5CAN} < 200$ mA, $V_{VREG} = 5.25$ V	4.9	5	5.1	V
V5CAN Output Capacitance Range [2]	$C_{OUT,V5CAN}$		1	–	15	$\mu\text{F}$
V5A Accuracy and Load Regulation	$V_{V5A}$	5 mA $< I_{V5A} < 55$ mA, $V_{VREG} = 5.25$ V	4.9	5	5.1	V
V5A Output Capacitance Range [2]	$C_{OUT,V5A}$		1	–	15	$\mu\text{F}$
V5B Accuracy and Load Regulation	$V_{V5B}$	5 mA $< I_{V5B} < 30$ mA, $V_{VREG} = 5.25$ V	4.9	5	5.1	V
V5B Output Capacitance Range [2]	$C_{OUT,V5B}$		1	–	15	$\mu\text{F}$
V5P Accuracy and Load Regulation	$V_{V5P}$	5 mA $< I_{V5P} < 100$ mA, $V_{VREG} = 5.25$ V	4.9	5	5.1	V
V5P Output Capacitance Range [2]	$C_{OUT,V5P}$		1	–	15	$\mu\text{F}$
<b>V5CAN OVERCURRENT PROTECTION</b>						
V5CAN Current Limit [1]	$V5CAN_{ILIM}$	$V_{V5CAN} = 5$ V	–220	–310	–	mA
V5CAN Foldback Current [1]	$V5CAN_{IFBK}$	$V_{V5CAN} = 0$ V	–40	–80	–140	mA
<b>V5A OVERCURRENT PROTECTION</b>						
V5A Current Limit [1]	$V5A_{ILIM}$	$V_{V5A} = 5$ V	–60	–100	–	mA
V5A Foldback Current [1]	$V5A_{IFBK}$	$V_{V5A} = 0$ V	–15	–30	–45	mA
<b>V5B OVERCURRENT PROTECTION</b>						
V5B Current Limit [1]	$V5B_{ILIM}$	$V_{V5B} = 5$ V	–40	–90	–	mA
V5B Foldback Current [1]	$V5B_{IFBK}$	$V_{V5B} = 0$ V	–5	–20	–35	mA
<b>V5P OVERCURRENT PROTECTION</b>						
V5P Current Limit [1]	$V5P_{ILIM}$	$V_{V5P} = 5$ V	–110	–155	–	mA
V5P Foldback Current [1]	$V5P_{IFBK}$	$V_{V5P} = 0$ V	–20	–40	–60	mA
<b>V5CAN, V5A, V5B, AND V5P STARTUP TIMING</b>						
V5CAN Startup Time [2]	$t_{V5CAN,START}$	$C_{V5CAN} \leq 2.9$ $\mu\text{F}$ , Load = 200 $\Omega \pm 5\%$ (25 mA)	–	0.4	1	ms
V5A Startup Time [2]	$t_{V5A,START}$	$C_{V5A} \leq 2.9$ $\mu\text{F}$ , Load = 200 $\Omega \pm 5\%$ (25 mA)	–	0.6	1	ms
V5B Startup Time [2]	$t_{V5B,START}$	$C_{V5B} \leq 2.9$ $\mu\text{F}$ , Load = 333 $\Omega \pm 5\%$ (15 mA)	–	0.8	1	ms
V5P Startup Time [2]	$t_{V5C,START}$	$C_{V5P} \leq 2.9$ $\mu\text{F}$ , Load = 100 $\Omega \pm 5\%$ (50 mA)	–	0.5	1	ms
<b>3V3 LINEAR REGULATOR</b>						
3V3 Accuracy and Load Regulation	$V_{3V3}$	5 mA $< I_{3V3} < 90$ mA, $V_{VREG} = 5.25$ V	3.23	3.30	3.37	V
3V3 Output Capacitance Range [2]	$C_{OUT,3V3}$		1.0	–	15	$\mu\text{F}$
<b>3V3 OVERCURRENT PROTECTION</b>						
3V3 Current Limit [1]	$3V3_{ILIM}$	$V_{3V3} = 3.3$ V	–110	–155	–	mA
3V3 Foldback Current [1]	$3V3_{IFBK}$	$V_{3V3} = 0$ V	–20	–50	–80	mA
<b>3V3 STARTUP TIMING</b>						
3V3 Startup Time [2]	$t_{3V3,START}$	$C_{3V3} \leq 2.9$ $\mu\text{F}$ , Load = 66 $\Omega \pm 5\%$ (50 mA)	–	0.5	0.8	ms
3V3 to Synchronous Buck Startup	$t_{3V3,BUCK}$	Time from when 3V3 = $V_{3V3,UV,H}$ to when $V_{FB} = V_{FB,UV,H}$	–	–	1	ms

[1] For input and output current specifications, negative current is defined as coming out of the node or pin (sourcing), positive current is defined as going into the node or pin (sinking).

[2] Ensured by design and characterization, not production tested.

[3] Specifications at 25°C or 85°C are guaranteed by design and characterization, not production tested.

[4] The lowest operating voltage is only valid if the conditions  $V_{VIN} > V_{VIN,START}$  and  $V_{VCP} - V_{VIN} > V_{VCP,UV,H}$  and  $V_{VREG} > V_{VREG,UV,H}$  are satisfied before  $V_{VIN}$  is reduced.

**ELECTRICAL CHARACTERISTICS – CONTROL INPUTS** [1]: Valid at 3.8 V [4]  $\leq V_{VIN} \leq 40$  V,  $-40^{\circ}\text{C} \leq T_J \leq 150^{\circ}\text{C}$ , unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
<b>IGNITION ENABLE (ENBAT) INPUT</b>						
ENBAT Thresholds	$V_{\text{ENBAT,H}}$	$V_{\text{ENBAT}}$ rising	2.9	3.1	3.5	V
	$V_{\text{ENBAT,L}}$	$V_{\text{ENBAT}}$ falling	2.2	2.6	2.9	V
ENBAT Hysteresis	$V_{\text{ENBAT,HYS}}$	$V_{\text{ENBAT,H}} - V_{\text{ENBAT,L}}$	–	500	–	mV
ENBAT Bias Current [1]	$I_{\text{ENBAT,BIAS}}$	$V_{\text{ENBAT}} = 5.5$ V via a 1 k $\Omega$ series resistor	–	50	100	$\mu\text{A}$
		$V_{\text{ENBAT}} = 0.8$ V via a 1 k $\Omega$ series resistor	0.5	–	5	$\mu\text{A}$
ENBAT Pull-Down Resistance	$R_{\text{ENBAT}}$	$V_{\text{ENBAT}} < 1.2$ V	–	600	–	k $\Omega$
<b>LOGIC ENABLE (ENB) INPUT</b>						
ENB Thresholds	$V_{\text{ENB,H}}$	$V_{\text{ENB}}$ rising	–	–	2	V
	$V_{\text{ENB,L}}$	$V_{\text{ENB}}$ falling	0.8	–	–	V
ENB Bias Current [1]	$I_{\text{ENB,IN}}$	$V_{\text{ENB}} = 3.3$ V	–	–	175	$\mu\text{A}$
ENB Resistance	$R_{\text{ENB}}$		–	60	–	k $\Omega$
<b>ENB/ENBAT FILTER/DEGLITCH</b>						
Enable Filter/Deglitch Time	$\text{EN}_{\text{td,FILT}}$		10	15	20	$\mu\text{s}$
<b>nERROR INPUT</b>						
nERROR Thresholds	$V_{\text{nERROR,H}}$	$V_{\text{nERROR}}$ rising	–	–	2	V
	$V_{\text{nERROR,L}}$	$V_{\text{nERROR}}$ falling	0.8	–	–	V

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[2] Ensured by design and characterization, not production tested.

[3] Specifications at 25°C or 85°C are guaranteed by design and characterization, not production tested.

[4] The lowest operating voltage is only valid if the conditions  $V_{VIN} > V_{VIN,START}$  and  $V_{VCP} - V_{VIN} > V_{CP,UV,H}$  and  $V_{VREG} > V_{REG,UV,H}$  are satisfied before  $V_{VIN}$  is reduced.

**ELECTRICAL CHARACTERISTICS – DIAGNOSTIC OUTPUTS** [1]: Valid at 3.8 V [4]  $\leq V_{VIN} \leq 40$  V,  $-40^{\circ}\text{C} \leq T_J \leq 150^{\circ}\text{C}$ , unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
<b>3V3 AND SYNCHRONOUS BUCK OV/UV PROTECTION THRESHOLDS</b>						
3V3 OV Thresholds	$V_{3V3,OV,H}$	$V_{3V3}$ rising	3.41	3.51	3.6	V
	$V_{3V3,OV,L}$	$V_{3V3}$ falling	–	3.49	–	V
3V3 OV Hysteresis	$V_{3V3,OV,HYS}$	$V_{3V3,OV,H} - V_{3V3,OV,L}$	10	20	40	mV
3V3 UV Thresholds	$V_{3V3,UV,H}$	$V_{3V3}$ rising	–	3.12	–	V
	$V_{3V3,UV,L}$	$V_{3V3}$ falling	3	3.1	3.19	V
3V3 UV Hysteresis	$V_{3V3,UV,HYS}$	$V_{3V3,UV,H} - V_{3V3,UV,L}$	10	20	40	mV
Synchronous Buck FB OV Thresholds	$V_{FB,OV,H}$	$V_{FB}$ rising	1.35	1.385	1.42	V
Synchronous Buck FB UV Thresholds	$V_{FB,UV,H}$	$V_{FB}$ rising	1.210	1.245	1.27	V
	$V_{FB,UV,L}$	$V_{FB}$ falling	1.205	1.235	1.26	V
Synchronous Buck FB UV Hysteresis	$V_{FB,UV,HYS}$	$V_{FB,UV,H} - V_{FB,UV,L}$	5	15	25	mV
<b>V5CAN, V5A, V5B AND V5P OV/UV PROTECTION THRESHOLDS</b>						
V5CAN, V5A, V5B and V5P OV Thresholds	$V_{V5,OV,H}$	$V_{V5}$ rising	5.15	5.33	5.5	V
	$V_{V5,OV,L}$	$V_{V5}$ falling	–	5.30	–	V
V5CAN, V5A, V5B and V5P OV Hysteresis	$V_{V5,OV,HYS}$	$V_{V5,OV,H} - V_{V5,OV,L}$	15	30	50	mV
V5CAN, V5A, V5B and V5P UV Thresholds	$V_{V5,UV,H}$	$V_{V5}$ rising	–	4.71	–	V
	$V_{V5,UV,L}$	$V_{V5}$ falling	4.5	4.68	4.85	V
V5CAN, V5A, V5B and V5P UV Hysteresis	$V_{V5,UV,HYS}$	$V_{V5,UV,H} - V_{V5,UV,L}$	15	30	50	mV
V5P Output Disconnect Threshold	$V_{V5P,DISC}$	$V_{V5P}$ rising	–	7.2	–	V
<b>VREG, VCP, AND BG THRESHOLDS</b>						
VREG Non-Latching OV Threshold	$V_{VREG,OV1,H}$	$V_{VREG}$ rising, LX1 PWM disabled	5.5	5.62	5.75	V
	$V_{VREG,OV1,L}$	$V_{VREG}$ falling, LX1 PWM enabled	–	5.53	–	V
VREG Non-Latching OV Hysteresis	$V_{VREG,OV1,HYS}$	$V_{VREG,OV1,H} - V_{VREG,OV1,L}$	–	100	–	mV
VREG Latching OV Threshold	$V_{VREG,OV2,H}$	$V_{VREG}$ rising, all regulators latched off	–	6.55	–	V
VREG UV Thresholds	$V_{VREG,UV,H}$	$V_{VREG}$ rising, triggers rise of 3V3 linear regulator	4.14	4.38	4.62	V
	$V_{VREG,UV,L}$	$V_{VREG}$ falling	–	4.28	–	V
VREG UV Hysteresis	$V_{VREG,UV,HYS}$	$V_{VREG,UV,H} - V_{VREG,UV,L}$	–	100	–	mV
VCP OV Thresholds	$V_{VCP,OV,H}$	$V_{VCP}$ rising, latches all regulators off	11	12.5	14	V
VCP UV Thresholds	$V_{VCP,UV,H}$	$V_{VCP}$ rising, PWM enabled	3	3.2	3.4	V
	$V_{VCP,UV,L}$	$V_{VCP}$ falling, PWM disabled	–	2.8	–	V
VCP UV Hysteresis	$V_{VCP,UV,HYS}$	$V_{VCP,UV,H} - V_{VCP,UV,L}$	–	400	–	mV
BG <sub>REF</sub> and BG <sub>FAULT</sub> UV Thresholds [2]	BG <sub>XUV</sub>	BG <sub>VREF</sub> or BG <sub>FAULT</sub> rising	1	1.05	1.1	V

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[2] Ensured by design and characterization, not production tested.

[3] Specifications at 25°C or 85°C are guaranteed by design and characterization, not production tested.

[4] The lowest operating voltage is only valid if the conditions  $V_{VIN} > V_{VIN,START}$  and  $V_{VCP} - V_{VIN} > V_{VCP,UV,H}$  and  $V_{VREG} > V_{VREG,UV,H}$  are satisfied before  $V_{VIN}$  is reduced.

**ELECTRICAL CHARACTERISTICS – DIAGNOSTIC OUTPUTS (continued) [1]:**Valid at 3.8 V [4] ≤ V<sub>VIN</sub> ≤ 40 V, –40°C ≤ T<sub>J</sub> ≤ 150°C, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
<b>NPOR TURN-ON AND TURN-OFF DELAYS</b>						
NPOR Turn-On Delay	td <sub>NPOR,ON</sub>	Time from when 3V3, synchronous buck output, and V5A are all in regulation to NPOR being asserted high	15	20	25	ms
<b>NPOR OUTPUT VOLTAGES</b>						
NPOR Output Low Voltage	V <sub>NPOR,L</sub>	ENB or ENBAT high, V <sub>VIN</sub> ≥ 2.5 V, I <sub>NPOR</sub> = 2 mA	–	150	400	mV
NPOR Leakage Current [1]	I <sub>NPOR,LKG</sub>	V <sub>NPOR</sub> = 3.3 V	–	–	2	μA
<b>FAULT FLAG OUTPUT VOLTAGES (FFn)</b>						
FFn Output Voltage	V <sub>FF,L</sub>	ENB = 1 or ENBAT = 1 and FFn is tripped, V <sub>VIN</sub> ≥ 2.5 V, I <sub>FF</sub> = 2 mA	–	150	400	mV
FFn Leakage Current	I <sub>FF,LKG</sub>	V <sub>FF</sub> = 3.3 V	–	–	2	μA
<b>IGNITION STATUS (ENBATS)</b>						
ENBATS Output Voltage	VO <sub>ENBATS,LO</sub>	I <sub>ENBATS</sub> = 2 mA, V <sub>ENBAT</sub> < V <sub>ENBAT,L</sub>	–	–	400	mV
ENBATS Leakage Current [1]	I <sub>ENBATS</sub>	V <sub>ENBATS</sub> = 3.3 V	–	–	2	μA
<b>OV FILTERING/DEGLITCH TIME</b>						
Overvoltage Detection Delay	OV <sub>td,FILT</sub>	Overvoltage detection delay time	10	15	20	μs
<b>UV FILTERING/DEGLITCH TIME</b>						
UV Filter/Deglitch Times	UV <sub>td,FILT</sub>	Undervoltage detection delay time	10	15	20	μs

[1] For input and output current specifications, negative current is defined as coming out of the node or pin (sourcing), positive current is defined as going into the node or pin (sinking).

[2] Ensured by design and characterization, not production tested.

[3] Specifications at 25°C or 85°C are guaranteed by design and characterization, not production tested.

[4] The lowest operating voltage is only valid if the conditions V<sub>VIN</sub> > V<sub>VIN,START</sub> and V<sub>VCP</sub> – V<sub>VIN</sub> > V<sub>VCP,UV,H</sub> and V<sub>VREG</sub> > V<sub>VREG,UV,H</sub> are satisfied before V<sub>VIN</sub> is reduced.



**ELECTRICAL CHARACTERISTICS – WINDOW WATCHDOG TIMER (WWDT) [1]:**Valid at 3.8 V [4]  $\leq V_{VIN} \leq 40$  V,  $-40^{\circ}\text{C} \leq T_J \leq 150^{\circ}\text{C}$ , unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
<b>WD_IN VOLTAGE THRESHOLDS AND CURRENT</b>						
WD <sub>IN</sub> Input Voltage Thresholds	WD <sub>IN,LO</sub>	V <sub>WD_IN</sub> falling	0.8	–	–	V
	WD <sub>IN,HI</sub>	V <sub>WD_IN</sub> rising	–	–	2	V
WD <sub>IN</sub> Pull-Down Resistance [2]	R <sub>WD_IN</sub>		–	50	–	kΩ
<b>WD_IN TIMING SPECIFICATIONS</b>						
WD <sub>IN</sub> Frequency	f <sub>WDIN</sub>		–	500	–	Hz
WD <sub>IN</sub> Pulse High Time	t <sub>WDIN,HI</sub>		50	–	–	μs
WD <sub>IN</sub> Pulse Low Time	t <sub>WDIN,LO</sub>		50	–	–	μs
<b>GATE DRIVE ENABLE (POE)</b>						
POE Output Voltage	V <sub>POE,L</sub>	I <sub>POE</sub> = 4 mA	–	150	400	mV
POE Output Voltage	V <sub>POE,H</sub>	I <sub>POE</sub> = –3.5 mA	2.85	–	–	V
Power Supply Disable Delay	t <sub>PS_DISABLE</sub>	Time from POE going low due to watchdog fault to V5CAN starts to decay	–	250	–	ms
Anti-Latchup Timeout	t <sub>ANTI_LATCHUP</sub>	Time from POE going low due to watchdog fault to when enable control is removed from the ENB pin	–	10	–	s

[1] For input and output current specifications, negative current is defined as coming out of the node or pin (sourcing), positive current is defined as going into the node or pin (sinking).

[2] Ensured by design and characterization, not production tested.

[3] Specifications at 25°C or 85°C are guaranteed by design and characterization, not production tested.

[4] The lowest operating voltage is only valid if the conditions  $V_{VIN} > V_{VIN,START}$  and  $V_{VCP} - V_{VIN} > V_{CP_{UV,H}}$  and  $V_{VREG} > V_{REG_{UV,H}}$  are satisfied before VIN is reduced.

**ELECTRICAL CHARACTERISTICS – COMMUNICATIONS INTERFACE [1]:**Valid at 3.8 V [4]  $\leq V_{VIN} \leq 40$  V,  $-40^{\circ}\text{C} \leq T_J \leq 150^{\circ}\text{C}$ , unless otherwise specified

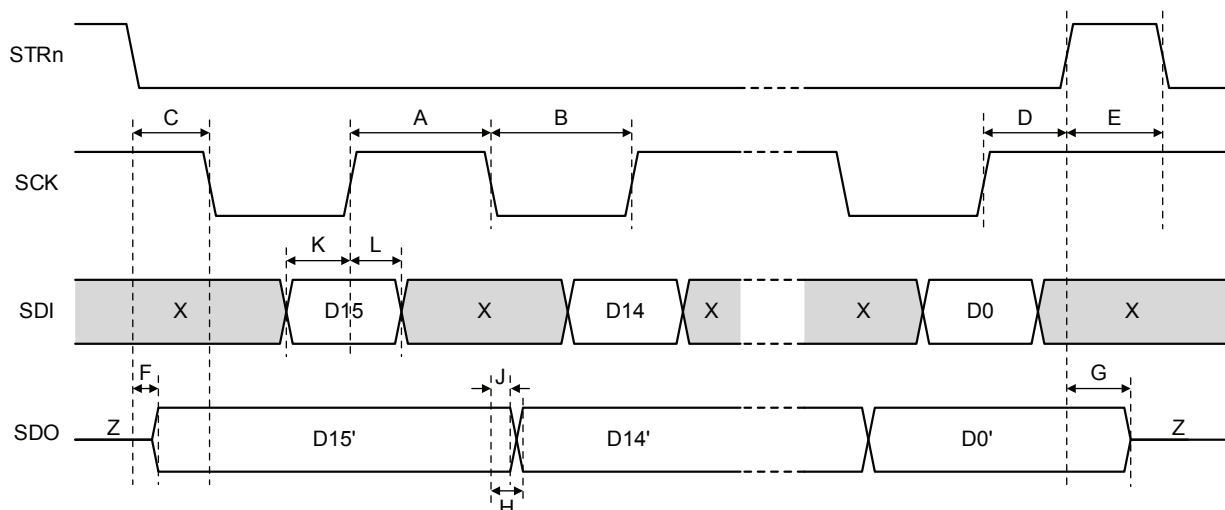
Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
<b>SERIAL INTERFACE (STRn, SDI, SDO, SCK)</b>						
Input Low Voltage	$V_{IL}$		–	–	0.8	V
Input High Voltage	$V_{IH}$	All logic inputs	2	–	–	V
Input Hysteresis	$V_{Ihys}$	All logic inputs	250	550	–	mV
Input Pull-Down SDI, SCK	$R_{PDS}$	$0\text{ V} < V_{IN} < 5\text{ V}$	–	50	–	k $\Omega$
Input Pull-Up To VCC	$I_{PU}$	STRn	–	50	–	k $\Omega$
Output Low Voltage	$V_{OL}$	$I_{OL} = 1\text{ mA}$ [1]	–	0.2	0.4	V
Output High Voltage	$V_{OH}$	$I_{OL} = -1\text{ mA}$ [1]	2.8	$V_{DD} - 0.2$	–	V
Output Leakage [1]	$I_{LK,SDO}$	$0\text{ V} < V_{SDO} < 5.5\text{ V}$ , STRn = 1	–1	–	1	$\mu\text{A}$
Clock High Time	$t_{SCKH}$	A in figure 4	50	–	–	ns
Clock Low Time	$t_{SCKL}$	B in figure 4	50	–	–	ns
Strobe Lead Time	$t_{STLD}$	C in figure 4	30	–	–	ns
Strobe Lag Time	$t_{STLG}$	D in figure 4	30	–	–	ns
Strobe High Time	$t_{STRH}$	E in figure 4	300	–	–	ns
Data Out Enable Time	$t_{SDOE}$	F in figure 4	–	–	40	ns
Data Out Disable Time	$t_{SDOD}$	G in figure 4	–	–	30	ns
Data Out Valid Time From Clock Falling	$t_{SDOV}$	H in figure 4	–	–	40	ns
Data Out Hold Time From Clock Falling	$t_{SDOH}$	J in figure 4	5	–	–	ns
Data In Setup Time To Clock Rising	$t_{SDIS}$	K in figure 4	15	–	–	ns
Data In Hold Time From Clock Rising	$t_{SDIH}$	L in figure 4	10	–	–	ns
Wake Up From Sleep	$t_{EN}$		–	–	2	ms

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[2] Ensured by design and characterization, not production tested.

[3] Specifications at  $25^{\circ}\text{C}$  or  $85^{\circ}\text{C}$  are guaranteed by design and characterization, not production tested.

[4] The lowest operating voltage is only valid if the conditions  $V_{VIN} > V_{VIN,START}$  and  $V_{VCP} - V_{VIN} > V_{VCP,UV,H}$  and  $V_{VREG} > V_{VREG,UV,H}$  are satisfied before  $V_{VIN}$  is reduced.



**Figure 1: Serial Interface Timing**  
X = don't care; Z = high-impedance (tri-state)

Table 1: Startup and Shutdown Logic (signal names consistent with Functional Block Diagram)

A4412 MODE	Regulator Control Bits (0=OFF, 1=ON)				A4412 Status Signals						
	VREG ON	3V3 ON	SYNC BUCK and V5A ON	V5B, V5P, and V5CAN ON	EN	MPOR	VREG UV	3V3 UV	SYNC BUCK and V5A UV	V5B, V5P, and V5CAN UV	NPOR
RESET	0	0	0	0	0	1	0	0	0	0	0
OFF	0	0	0	0	0	0	1	1	1	1	0
STARTUP	1	0	0	0	1	0	1	1	1	1	0
↓	1	1	0	0	1	0	0	1	1	1	0
↓					1	0	0	0	1	1	0
↓	1	1	1	0	1	0	0	0	0	1	1
RUN	1	1	1	1	1	0	0	0	0	0	1
15 μs DEGLITCH	1	1	1	1	0	0	0	0	0	0	0
SHUTTING DOWN	1	1	1	1	0	0	0	0	0	0	0
↓	1	1	0	0	0	0	0	0	1	1	0
↓	1	0	0	0	0	0	0	1	1	1	0
OFF	0	0	0	0	0	0	1	1	1	1	0

TIME

X = DON'T CARE

EN = ENBAT + ENB

MPOR = VCC\_UV + VCP\_UV + BG1\_UV + BG2\_UV + TSD + VCP\_OV (latched) + D1<sub>MISSING</sub> (latched) + I<sub>LIM,LX1</sub> (latched)

## STARTUP TIMING DIAGRAM

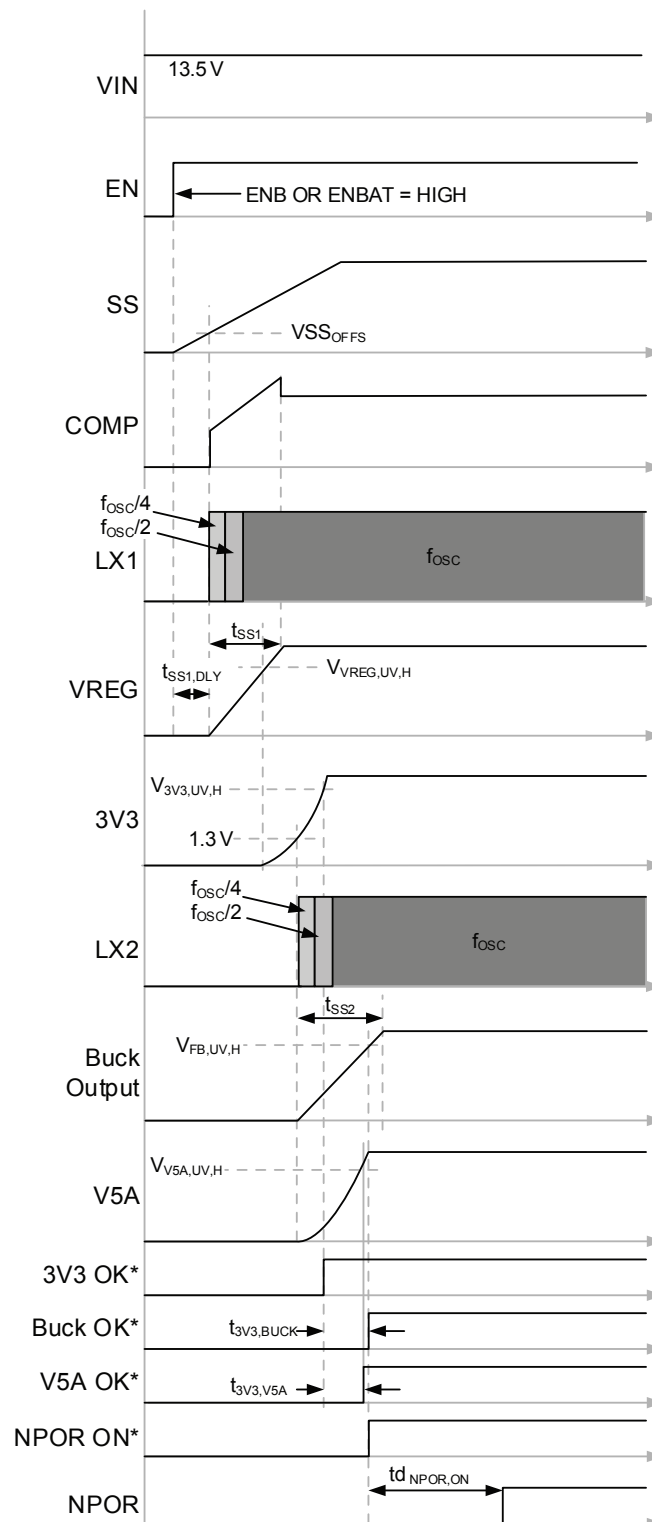
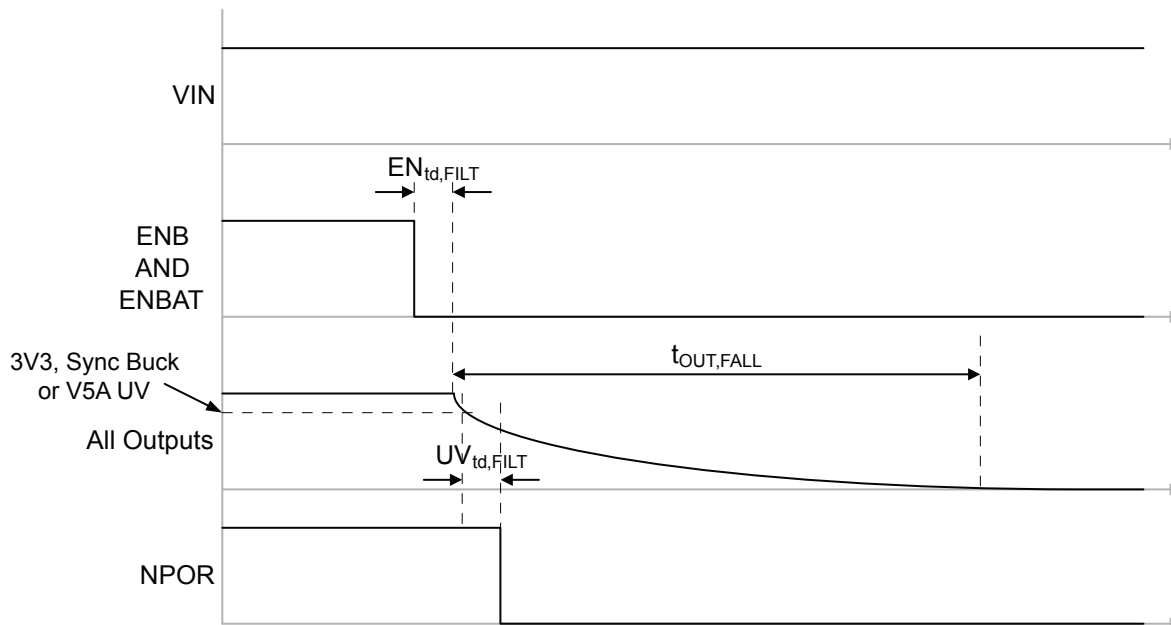


Figure 2: Startup Timing Diagram

## SHUTDOWN TIMING DIAGRAM



All outputs start to decay  $EN_{td,FILT}$  seconds after ENB and ENBAT are low.

Time for outputs to drop to zero,  $t_{OUT,FALL}$ , various for each output and depends on load current and capacitance.

NPOR falls when 3V3, Sync Buck or V5A reaches its UV point.

Figure 3: Shutdown Timing Diagram

Table 2: Summary of Fault Mode Operation

FAULT TYPE and CONDITION	A4412 RESPONSE TO FAULT	LATCHED FAULT?	VCC	VCP	VREG	SYNC BUCK O/P	3V3	V5CAN	V5A	V5B	V5P	NPOR	FFn	POE	DIAG	SPI	WD	RESET METHOD
<b>Latching Faults</b>																		
CPUMP OV	Results in an MPOR after 1 detection, so all regulators are shut off	Yes	No effect	?	off	off	off	off	off	off	off	Low	Low	Low	102 kHz	On	On	None
VREG overvoltage $V_{REGOV2,H} < V_{VREG}$	Results in an MPOR after 1 detection, so all regulators are shut off	Yes	No effect	No effect	off	off	off	off	off	off	off	Low	Low	Low	204 kHz	On	On	Check the short/ Cycle EN or Vin / replace 4412
VREG asynchronous diode (D1) missing	Results in an MPOR after 1 detection, so all regulators are shut off	Yes	No effect	No effect	off	off	off	off	off	off	off	Low	Low	Low	315 kHz	xx	xx	Place D1 then cycle EN or VIN
Asynchronous diode (D1) short circuited or LX1 shorted to ground	Results in an MPOR after the high side MOSFET current exceeds ILIM.LX1 so all regulators are shut off	Yes	No effect	No effect	off	off	off	off	off	off	off	Low	Low	Low	409 kHz	xx	xx	Remove the short then cycle EN or VIN
1V25 overvoltage	If OV condition persists for more than tDOV then set NPOR Low and shut off all regulators	Yes	No effect	No effect	off	off	off	off	off	off	off	Low	Low	Low	512 kHz	xx	xx	Check for short circuits then cycle EN or VIN
FB pin is open	FB pin will be pulled high, LX2 will stop switching	Yes	No effect	No effect	No effect	Low	off	off	off	off	off	Low	Low	Low	512 kHz	xx	xx	Connect the FB pin
<b>Non-Latching Faults</b>																		
Vin UVLO	4412 is in reset state	No	Ramping	Vin	off	off	off	off	off	off	off	Low	Low	Low	Low	xx	xx	None
BG1 UVLO	4412 is in reset state	No	Ramping	Vin	off	off	off	off	off	off	off	Low	Low	Low	Low	xx	xx	None
BG2 UVLO	4412 is in reset state	No	Ramping	Vin	off	off	off	off	off	off	off	Low	Low	Low	Low	xx	xx	None
VCC UVLO	4412 is in reset state	No	ON	Vin	off	off	off	off	off	off	off	Low	Low	Low	Low	xx	xx	None
VCC short limit	4412 is in reset state	No	UVLO	Vin	off	off	off	off	off	off	off	Low	Low	Low	Low	xx	xx	None
CPUMP UVLO	4412 is in reset state	No	ON	Ramping	off	off	off	off	off	off	off	Low	Low	Low	Low	xx	xx	None
VREG over voltage $V_{REGOV1,H} < V_{VREG}$	Stop PWM switching of LX1	No	No effect	No effect	No effect	No effect	No effect	No effect	No effect	No effect	No effect	Low if 3V3, 1V25 or V5A are too Low	Low if V5 or V5P are too Low	Low	Low	No effect	No effect	None
VREG pin open circuit	VREG will decay to 0 V, LX1 will switch at maximum duty cycle so the voltage on the output capacitors will be very close to VBAT	No	No effect	No effect	off	off	off	off	off	off	off	Low	Low	Low	Low	No effect	No effect	Connect the VREG pin
VREG shorted to ground $V_{SS1} < V_{HIC1,EN}$ , $V_{VREG} < 1.95 V$ , $V_{COMP1} \neq EA1_{VO(MAX)}$	Continue to PWM but turn off LX1 when the high side MOSFET current exceeds ILIM1	No	No effect	No effect	Shorted	off if Vreg < UVLO	off if Vreg < UVLO	off if Vreg < UVLO	off if Vreg < UVLO	off if Vreg < UVLO	off if Vreg < UVLO	Low if 3V3, 1V25 or V5A are too Low	Low	Low	Low	No effect	No effect	Remove the short circuit
VREG overcurrent $V_{SS1} > V_{HIC1,EN}$ , $V_{VREG} < 1.95 V$ , $V_{COMP1} = EA1_{VO(MAX)}$	Enters hiccup mode after 30 OCP faults	No	No effect	No effect	Shorted	off if Vreg < UVLO	off if Vreg < UVLO	off if Vreg < UVLO	off if Vreg < UVLO	off if Vreg < UVLO	off if Vreg < UVLO	Low if 3V3, 1V25 or V5A are too Low	Low	Low	Low	No effect	No effect	Decrease the load
VREG overcurrent $V_{SS1} > V_{HIC1,EN}$ , $V_{VREG} < 1.95 V$ , $V_{COMP1} = EA1_{VO(MAX)}$	Enters hiccup mode after 120 OCP faults	No	No effect	No effect	Shorted	off if Vreg < UVLO	off if Vreg < UVLO	off if Vreg < UVLO	off if Vreg < UVLO	off if Vreg < UVLO	off if Vreg < UVLO	Low if 3V3, 1V25 or V5A are too Low	Low	Low	Low	No effect	No effect	Decrease the load

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Table 2: Summary of Fault Mode Operation (continued)

FAULT TYPE and CONDITION	A4412 RESPONSE TO FAULT	LATCHED FAULT?	VCC	VCP	VREG	SYNC BUCK O/P	3V3	V5CAN	V5A	V5B	V5P	NPOR	FFn	POE	DIAG	SPI	WD	RESET METHOD
FB/OV undervoltage	Closed loop control will try to raise the voltage but may be constrained by the foldback or pulse-by-pulse current limit	No	No effect	No effect	No effect	Low	No effect	No effect	No effect	No effect	No effect	Low	Low	Low	Low	No effect	No effect	Decrease the load
SYNC Buck overcurrent $V_{SS2} > V_{HIC2,EN}$ , $V1V25 > 470$ mV	Enters hiccup mode after 120 OCP faults	No	No effect	No effect	No effect	Low	No effect	No effect	No effect	No effect	No effect	Low	Low	Low	Low	No effect	No effect	Decrease the load
FB shorted to ground $V_{SS2} < V_{HIC2,EN}$ , $V1V25 < 470$ mV	Continue to PWM but turn off LX2 when the high-side MOSFET current exceeds ILIM2	No	No effect	No effect	No effect	Low	No effect	No effect	No effect	No effect	No effect	Low	Low	Low	Low	No effect	No effect	Remove the short circuit
3V3 undervoltage	Closed loop control will try to raise the voltage but may be constrained by the foldback or pulse-by-pulse current limit	No	No effect	No effect	No effect	No effect	Low	No effect	No effect	No effect	No effect	Low	Low	Low	Low	No effect	No effect	Decrease the load
3V3 overvoltage	If OV condition persists for more than $t_{dOV}$ then set NPOR Low	No	No effect	No effect	No effect	No effect	$> V_{3V3,OV,H}$	No effect	No effect	No effect	No effect	Low	Low	Low	Low	No effect	No effect	Check for short circuits
3V3 overcurrent	Foldback current limit will reduce the output voltage	No	No effect	No effect	No effect	No effect	Falling	No effect	No effect	No effect	No effect	Low if $3V3 < V_{3V3,UVL}$	Low if $3V3 < V_{3V3,UVL}$	Low if $3V3 < V_{3V3,UVL}$	Low	No effect	No effect	Decrease the load
V5P undervoltage	Closed loop control will try to raise the voltage but may be constrained by the foldback current limit	No	No effect	No effect	No effect	No effect	No effect	No effect	No effect	No effect	UVLO	No effect	Low	No effect	Low	No effect	No effect	Decrease the load
V5P over voltage or shorted to Vbat	If OV condition persists for more than $t_{dOV}$ then set FF Low	No	No effect	No effect	No effect	No effect	No effect	No effect	No effect	No effect	$> V_{V5P,OV,H}$	No effect	Low	No effect	Low	No effect	No effect	Check for short circuits on V5P
V5P overcurrent	Foldback current limit will reduce the output voltage	No	No effect	No effect	No effect	No effect	No effect	No effect	No effect	No effect	Falling	No effect	Low if V5P are too Low	No effect	Low	No effect	No effect	Decrease the load
V5A undervoltage	Closed loop control will try to raise the voltage but may be constrained by the foldback current limit	No	No effect	No effect	No effect	No effect	No effect	No effect	Low	No effect	No effect	Low	Low	Low	Low	No effect	No effect	Decrease the load
V5A overvoltage	If OV condition persists for more than $t_{dOV}$ then set POK5V Low	No	No effect	No effect	No effect	No effect	No effect	No effect	$> V_{V5A,OV,H}$	No effect	No effect	Low	Low	Low	Low	No effect	No effect	Check for short circuits on V5A
V5A overcurrent	Foldback current limit will reduce the output voltage	No	No effect	No effect	No effect	No effect	No effect	No effect	Falling	No effect	No effect	Low if $V5A < V_{V5A,UVL}$	Low if $V5A < V_{V5A,UVL}$	Low if $V5A < V_{V5A,UVL}$	Low	No effect	No effect	Decrease the load
V5CAN overvoltage	If OV condition persists for more than $t_{dOV}$ then set POK5V Low	No	No effect	No effect	No effect	No effect	No effect	$> V_{V5CAN,OV,H}$	No effect	No effect	No effect	No effect	Low	No effect	Low	No effect	No effect	Check for short circuits on V5CAN

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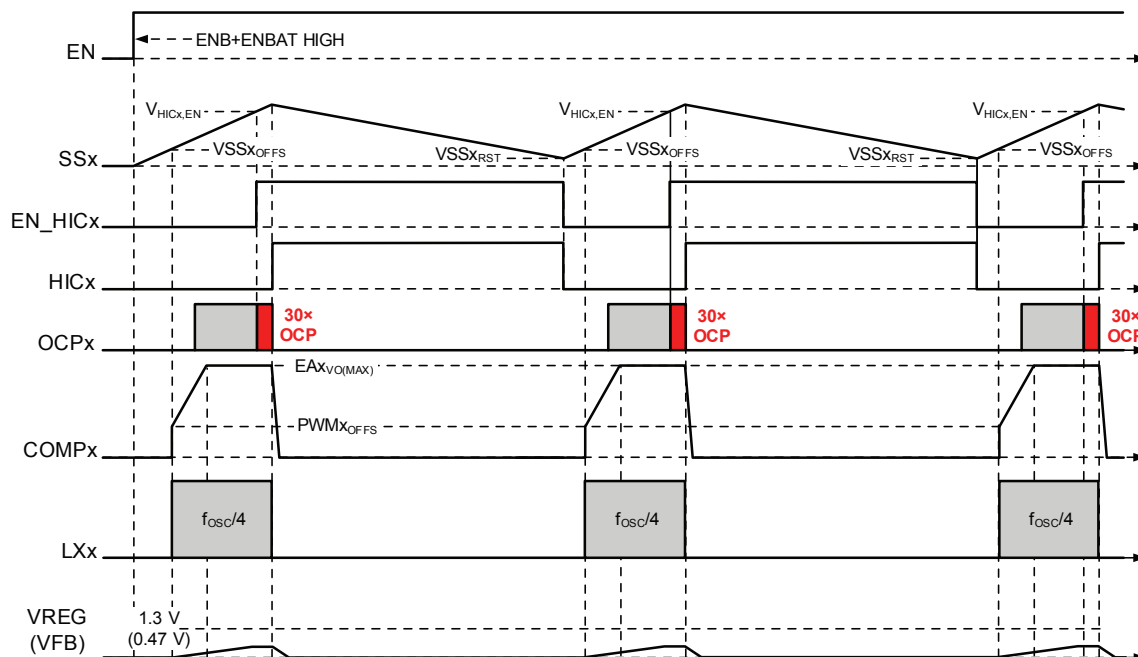
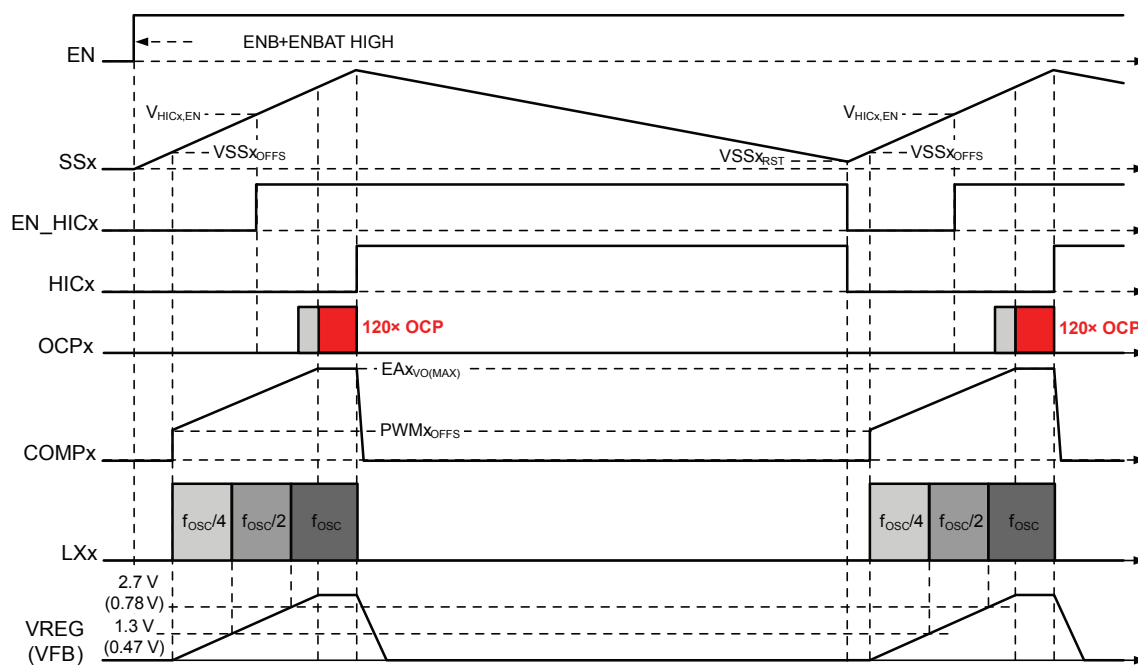
Table 2: Summary of Fault Mode Operation (continued)

FAULT TYPE and CONDITION	A4412 RESPONSE TO FAULT	LATCHED FAULT?	VCC	VCP	VREG	SYNC BUCK O/P	3V3	V5CAN	V5A	V5B	V5P	NPOR	FFn	POE	DIAG	SPI	WD	RESET METHOD
V5CAN undervoltage	Closed loop control will try to raise the voltage but may be constrained by the foldback current limit	No	No effect	No effect	No effect	No effect	No effect	Low	No effect	No effect	No effect	No effect	Low	No effect	Low	No effect	No effect	Decrease the load
V5CAN overcurrent	Foldback current limit will reduce the output voltage	No	No effect	No effect	No effect	No effect	No effect	Falling	No effect	No effect	No effect	No effect	Low if V5CAN is too Low	No effect	Low	No effect	No effect	Decrease the load
V5B overvoltage	If OV condition persists for more than $t_{DOY}$ then set POK5V Low	No	No effect	No effect	No effect	No effect	No effect	No effect	No effect	$> V_{V5B, OV,H}$	No effect	No effect	Low	No effect	Low	No effect	No effect	Check for short circuits on V5B
V5B undervoltage	Closed loop control will try to raise the voltage but may be constrained by the foldback current limit	No	No effect	No effect	No effect	No effect	No effect	No effect	No effect	No effect	No effect	No effect	Low	No effect	Low	No effect	No effect	Decrease the load
V5B overcurrent	Foldback current limit will reduce the output voltage	No	No effect	No effect	No effect	No effect	No effect	No effect	No effect	No effect	No effect	No effect	Low if V5B is too Low	No effect	Low	No effect	No effect	Decrease the load
Thermal shutdown	Results in an MPOR, so all regulators are shut off	No	No effect	No effect	No effect	off	off	off	off	off	off	off	Low	Low	Low	No effect	No effect	Let the A4412 cool



## TIMING DIAGRAMS (not to scale)

\* is for "and", + is for "or"

Figure 4: Hiccup Mode Operation with VREG or Synchronous Buck Shorted to GND ( $R_{LOAD} < 50 \text{ m}\Omega$ )Figure 5: Hiccup Mode Operation with VREG or Synchronous Buck Overloaded ( $R_{LOAD} \approx 0.5 \Omega$ )

## FUNCTIONAL DESCRIPTION

### Overview

The A4412 is a power management IC designed for safety critical applications. It contains seven DC/DC regulators to create the voltages necessary for typical automotive applications such as electrical power steering.

The A4412 pre-regulator can be configured as a buck converter or buck-boost. Buck-boost is suitable for when applications need to work with extremely low battery voltages. This pre-regulator generates a fixed 5.35 V and can deliver up to 1.2 A to power the internal or external post-regulators. These post-regulators generate the various voltage levels for the end system.

The A4412 includes six internal post-regulators: five linear regulators and one adjustable output synchronous buck regulator.

### Pre-Regulator

The pre-regulator incorporates an internal high side buck switch and a boost switch gate driver. An external freewheeling diode and LC filter are required to complete the buck converter. By adding a MOSFET and boost diode the pre-regulator can now maintain all outputs with input voltages down to 3.8 V.

The pre-regulator provides many protection and diagnostic functions:

1. Pulse-by-pulse and hiccup mode current limit
2. Undervoltage and overvoltage detection and reporting
3. Shorted switch node to ground
4. Open freewheeling diode protection
5. High voltage rating for load dump

### Bias Supply

The bias supply (VCC) is generated by an internal linear regulator. This supply is the first rail to start up. Most of the internal control circuitry is powered by this supply. The bias supply includes some unique features to ensure safe operation of the A4412. These features include:

1. Input voltage undervoltage lockout
2. Output undervoltage detection and reporting
3. Overcurrent and short-circuit limit
4. Dual input, VIN and VREG, for low battery voltage operation
5. Short protection of the series pass device. If the internal linear regulator shorts to VIN this protection will ensure that the A4412 enters a safe mode.

### Charge Pump

A charge pump doubler provides the voltage necessary to drive high-side n-channel MOSFETs in the pre-regulator and linear regulators. Two external capacitors are required for charge pump operation. During the first cycle of the charge pump action the flying capacitor, between pins CP1 and CP2, is charged either from VIN or VREG, whichever is highest. During the second cycle the voltage on the flying capacitor charges the VCP capacitor. The VCP minus VIN voltage is regulated to around 6.6 V

The charge pump incorporates some safety features:

1. Undervoltage and overvoltage detection and reporting
2. Overcurrent safe mode protection

### Bandgap

Dual bandgaps are implemented within the A4412. One bandgap is dedicated to the voltage regulation loops within each of the regulators, VCC, VCP, VREG and the six post-regulators. The second is dedicated to the monitoring function of all the regulators undervoltage and overvoltage. This improves safety coverage and fault reporting from the A4412.

Should the regulation bandgap fail, then the outputs will be out of specification and the monitoring bandgap will report the fault.

If the monitoring bandgap fails, the outputs will remain in regulation, but the monitoring circuits will report the outputs as out of specification and trip the fault flag.

The bandgap circuits include two other bandgaps that are used to monitor the undervoltage state of the main bandgaps.

### Enable

Two Enable pins are available on the A4412. A high signal on either of these pins enables the regulated outputs of the A4412. One Enable (ENB) is logic-level compatible. The second enable (ENBAT), is battery-level rated and can be connected to the ignition switch through a resistor.

A logic-level battery enable status (ENBATS) pin provides the user with a low-level signal of what the ENBAT input is doing.

### Synchronous Buck

The A4412 integrates both the high-side and low-side switches necessary for implementing a synchronous buck converter. It is powered by the pre-regulator output. A 1.305 V feedback pin is

provided to allow adjustment of the output from 1.305 to 3.3 V. A simple voltage divider sets the output voltage. If 1.305 V is required, then no divider is necessary and the converter output can be connected directly to the feedback pin. If the synchronous buck converter is configured as 1.305 V, then a minimum load of 100  $\mu$ A is required. This can either be the system load or an additional 10 k $\Omega$  from 1.305 V output to ground.

The synchronous buck requires an LC filter on its switch node to compete the regulation function.

Protection and safety functions provided by the synchronous buck are:

1. Pulse-by-pulse and hiccup mode current limit
2. Undervoltage and overvoltage detection and reporting
3. Shorted switch node to ground
4. Open feedback pin protection
5. Shorted high-side switch protection, OVP shuts down pre-regulator

## Linear Regulators

The A4412 has five linear regulators, one 3.3V, three 5V and one protected 5V.

All linear regulators provide the following protection features:

1. Current limit with foldback
2. Undervoltage and overvoltage detection and reporting

The protected 5 V regulator includes protection against connection to the battery voltage. This makes this output most suitable for powering remote sensors or circuitry where short-to-battery is possible.

The pre-regulator powers these linear regulators which reduces power dissipation and temperature.

## Fault Detection and Reporting

There is extensive fault detection within the A4412, as discussed previously. There are two fault reporting mechanisms used by the A4412: through hardwired pins and through a serial communications interface (SPI).

Two hardwired pins on the A4412 are used for fault reporting. The first pin, NPOR, reports on the status of the 3V3, the V5A, and synchronous buck outputs. This signal goes low if either of these outputs is out of regulation. The second pin, FFn (Active Low fault flag), reports on all other faults. FFn goes low if a fault within the A4412 exists. The FFn pin can be used by the processor as an alert to check the status of the A4412 via SPI and see where the fault occurred.

The A4412 also includes a diagnostic pin, DIAG, to aid system debugging in the event of a failure. A series of pulses with 50% duty cycle will be sent to this pin. Their frequency will indicate what fault occurred within the A4412.

Fault	DIAG
LX1 or D1 short-to-ground	Low
Charge pump overvoltage	102 kHz
VREG overvoltage $V_{REG_{OV2,H}} < V_{VREG}$	204 kHz
VREG asynchronous diode (D1) missing	409 kHz
Synchronous buck overvoltage	512 kHz

## Startup Self-Test

The A4412 includes self-test which is performed during the startup sequence. This self-test verifies the operation of the undervoltage and overvoltage detect circuits for the main outputs.

In the event the self-test fails, the A4412 will report the failure through SPI.

## Undervoltage Detect Self-Test

The undervoltage (UV) detectors are verified during startup of the A4412. A voltage that is higher than the undervoltage threshold is applied to each UV comparator; this should cause the relative undervoltage fault bit in the diagnostic registers to change state. If the diagnostic UV register bits change state, the corresponding verify register bits will latch high. When the test of all UV detectors is complete, the verify register bits will remain high if the test passed. If any UV bits in the verify registers after test are not set high, then the verification has failed. The following UV detectors are tested: VREG, 3V3, V5A, V5B, V5P, V5CAN, and the synchronous buck.

## Overvoltage Detect Self-Test

The overvoltage (OV) detectors are verified during startup of the A4412. A voltage is applied to each OV comparator that is higher than the overvoltage threshold; this should cause the relative overvoltage fault bit in the diagnostic registers to change state. If the diagnostic OV register bits change state, the corresponding verify register bits will latch high. When the test of all OV detectors is complete, the verify register bits will remain high if the test passed. If any OV bits in the verify registers after test are not set high, then the verification has failed. The following OV detectors are tested: VREG, 3V3, V5A, V5B, V5P, V5CAN, and the synchronous buck.

## Overtemperature Shutdown Self-Test

The overtemperature shutdown (TSD) detector is verified on startup of the A4412. A voltage is applied to the comparator that

is lower than the overtemperature threshold and should cause the general fault flag to be active and an overtemperature fault bit, TSD, to be latched in the Verify Result register 0. When the test is complete, the general fault flag will be cleared, and the overtemperature fault will remain in the Verify Result register 0 until reset. If the TSD bit is not set, then the verification has failed.

### Power-On Enable Self-Test

The A4412 also incorporates continuous self-testing of the power-on enable (POE) output. It compares the status of the POE pin with the internal demanded status. If they differ for any reason, an FFn is set and the POE\_OK in SPI diagnostic register goes low.

### Watchdog

The watchdog circuit within the A4412 will monitor a temporal signal from a processor for its period between pulses. If the signal does not meet the requirements, the A4412 watchdog will put the system into a safe state. It does this by setting the power-on enable (POE) pin Low, removing enabling function of ENB pin for the A4412 and disabling the V5CAN output. See Figure 6 for a simplified block diagram of the watchdog circuit.

The watchdog function (see Figure 7) uses two timers and two counters to validate the incoming temporal signal. The user has some ability to program the counters and timer windows through SPI.

The first counter counts the rising edges of the temporal signal. If the correct count is completed after the minimum timer expires and before the maximum timer expires, then the second (valid) counter is incremented. Once the valid counter has incremented the programmed number of counts, the watchdog issues a watchdog OK (WD\_IN\_OK) signal. This signal, along with NPOR, 3V3 enable, synchronous buck enable, and nERROR, enables the POE.

If the edge count reaches its final value before the minimum timer or after the maximum timer expires, the valid counter decrements. Once the valid counter reaches zero, the watchdog fault signal issues a fault has occurred. The POE is driven low; after a timeout period, the V5CAN output is disabled, and after a further timeout, enabling of the A4412 via the ENB pin is no longer possible.

If insufficient edges are received before the maximum timer expires, the valid counter decrements and the minimum and maximum counters are reset and start to count again. If an edge is subsequently received the timers reset once again to synchronize on the incoming pulses. The valid counter is not decremented in this instance (see Figure 7).

The number of edge counts, valid counts, and timer windows can

be programmed through SPI. The min and max timer nominal values in milliseconds are calculated by the following equations:

$$t_{WD,MIN} = k_{EDGE} \times (2 + WD\_MIN)$$

$$t_{WD,MAX} = k_{EDGE} \times (2 + WD\_MAX)$$

where  $k_{EDGE}$  is the edge count number programmed through SPI (default is 2),

WD\_MIN is the min timer adjust value in milliseconds programmed in SPI (default is -0.12 ms), and

WD\_MAX is the min timer adjust value in milliseconds programmed in SPI (default is 0.12 ms).

Tolerance on  $t_{WD,MIN}$  and  $t_{WD,MAX}$  is related to the system clock tolerance,  $f_{SYS,TOL}$  in %, by the following equations:

$$\frac{100}{100 - f_{SYS,TOL}} - 1$$

$$\frac{100}{100 + f_{SYS,TOL}} - 1$$

The watchdog also has provision to be placed in “flash mode”. While in flash mode the watchdog keeps the POE signal low but does not disable the V5CAN or the ENB function. This is required should the processor need to be re-flashed. Flash mode is accessed through secure SPI commands. To exit “flash mode”, the watchdog must be restarted via separate secure SPI commands. If the A4412 has not lost power during flash mode, then the watchdog will restart with the previous configuration. If power was lost during flash mode, then the watchdog configuration will be reset to default.

On startup, the watchdog (WD\_IN) must receive a series of valid and qualified pulse trains, per the programmed EDGE\_COUNT and VALID\_COUNT registers, followed by a series of invalid qualified pulses. Once a second series of valid and qualified pulses are received before the power supply disable time ( $t_{PS\_DISABLE}$ ) expires, then the watchdog enters the active state and the WD\_F signal on SPI becomes active (see Figure 6). During the test state, WD\_F is not active and FFn does not alert a watchdog fault. When the watchdog is waiting for the second series of pulse on WD\_IN, it sets the valid counter to one half its programmed value. This aids in speeding up startup of a system using the A4412. Once the WD\_IN pulses have met all criteria and POE is released, then the valid counter reverts to its correct programmed value. If the second series of pulses is not received before the  $t_{PS\_DISABLE}$  time, then the watchdog will enter watchdog fault mode. It will set the POE signal low, disable the V5CAN, and after  $t_{ANTI\_LATCHUP}$  remove enable control via ENB.

If the watchdog has indicated invalid WD\_IN pulses, it latches the POE signal low. Once the power supply disable time ( $t_{PS\_DISABLE}$ ) expires, then the watchdog will disable the V5CAN. After the anti-latchup timeout,  $t_{ANTI\_LATCHUP}$ , then the watchdog will remove Enable control via the ENB pin. The only way to prevent this would be to restart the watchdog either through SPI or shutting down and restarting the A4412.

The processor can restart the watchdog by using a secure SPI command.

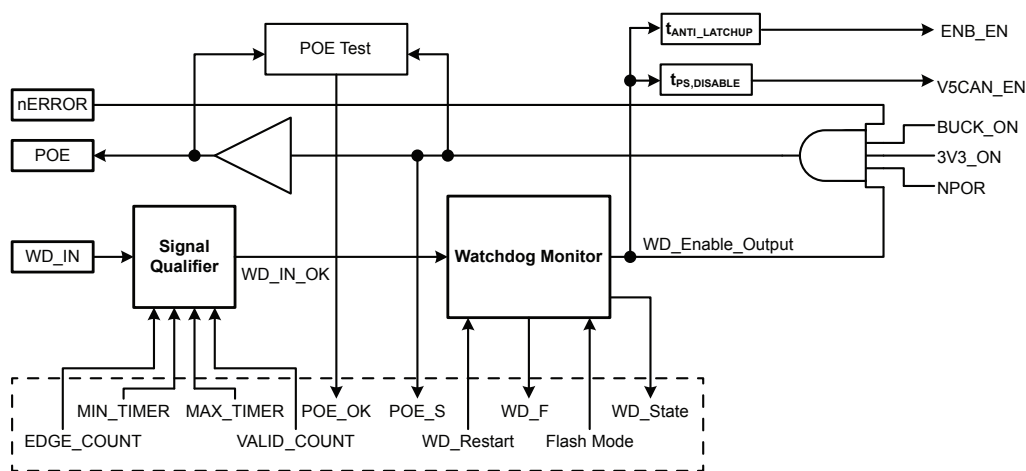


Figure 6: Watchdog Block Diagram

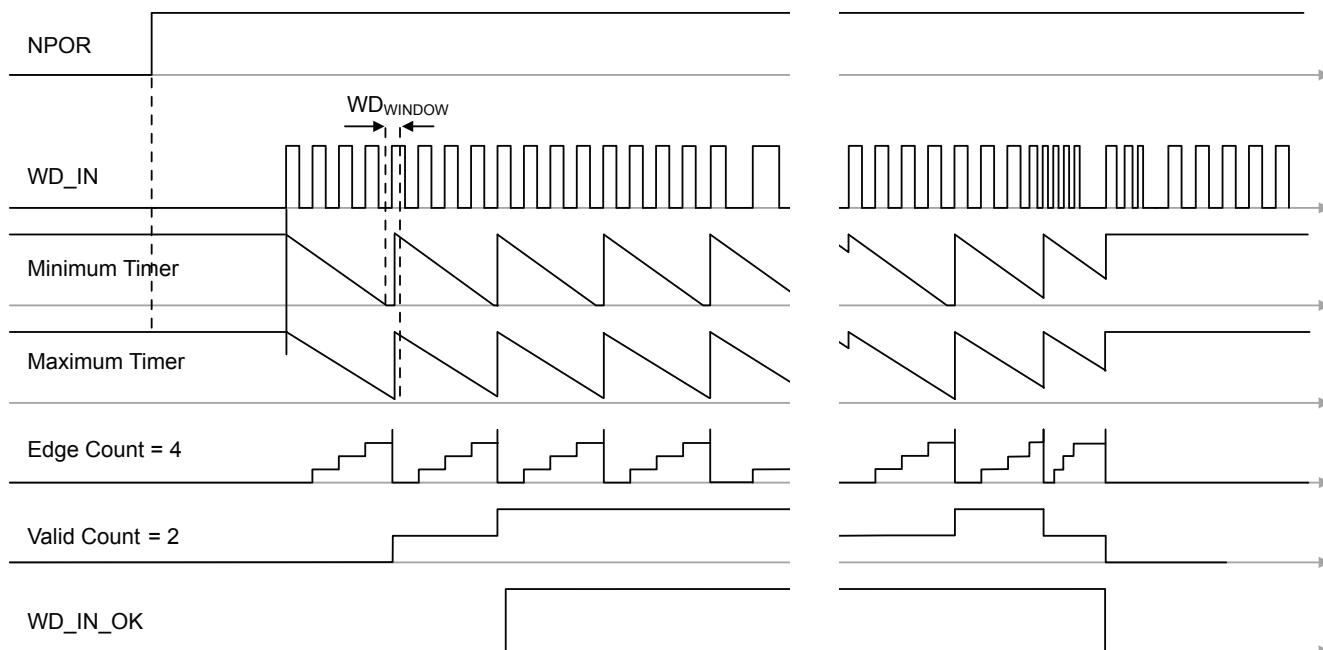


Figure 7: Watchdog Valid Signal Timing Diagram

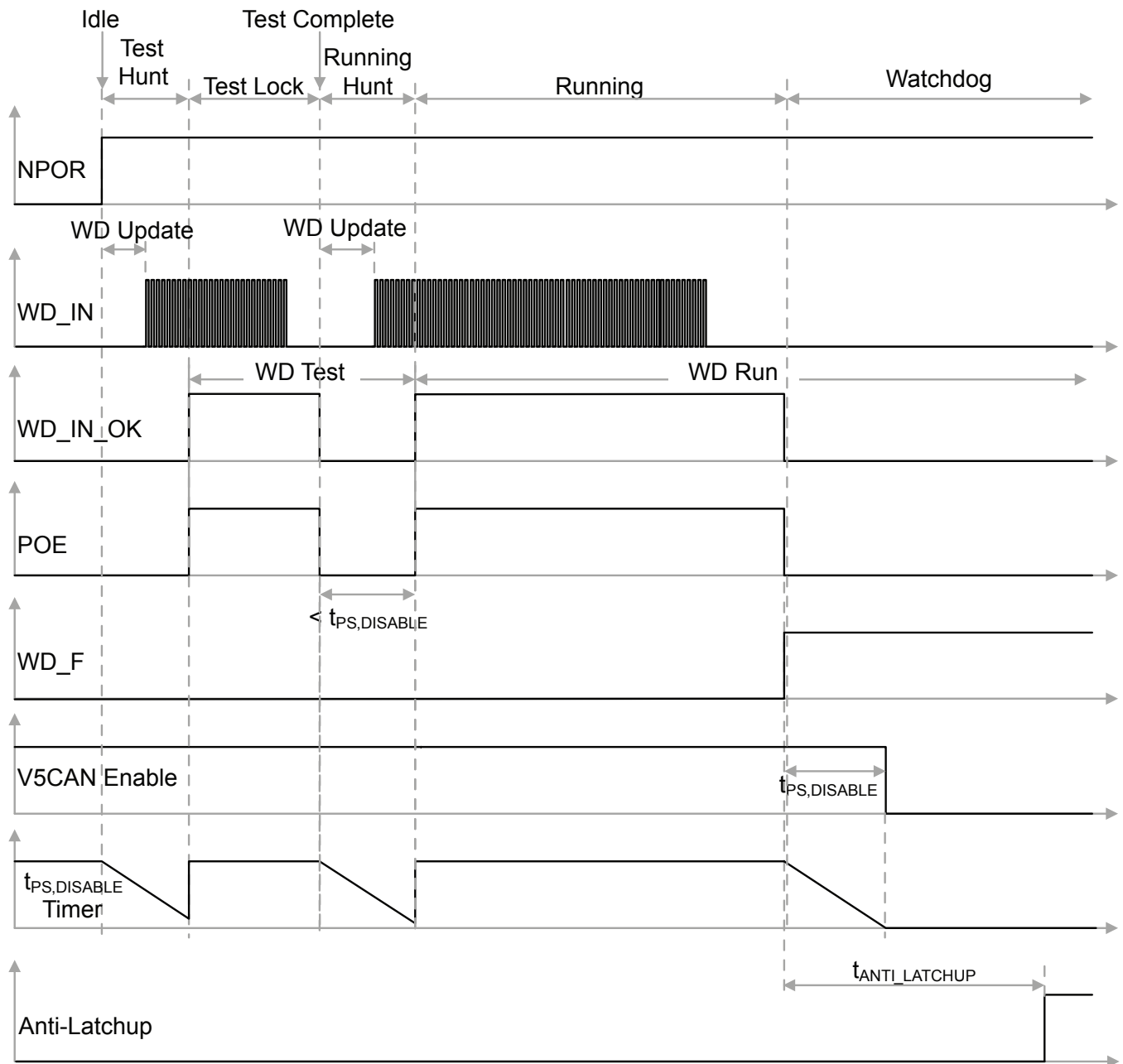


Figure 8: Watchdog Timing at Startup



## SERIAL COMMUNICATION INTERFACE

The A4412 provides the user with a three-wire synchronous serial interface that is compatible with SPI (Serial Peripheral Interface). A fourth wire can be used to provide diagnostic feedback and readback of the register content.

The serial interface timing requirements are specified in the electrical characteristics table and illustrated in the Serial Interface Timing diagram (Figure 1). Data is received on the SDI terminal and clocked through a shift register on the rising edge of the clock signal input on the SCK terminal. STRn is normally held high and is only brought low to initiate a serial transfer. No data is clocked through the shift register when STRn is high, allowing multiple SDI slave units to use common SDI, SCK and SDO connections. Each slave then requires an independent STRn connection.

When 16 data bits have been clocked into the shift register, STRn must be taken high to latch the data into the selected register. When this occurs, the internal control circuits act on the new data and the Diagnostic register is reset.

If there are more than 16 rising edges on SCK or if STRn goes high and there are fewer than 16 rising edges on SCK, the write will be cancelled without writing data to the registers. In addition, the Diagnostic register will not be reset and the SE (serial error) bit will be set to indicate a data transfer error.

Diagnostic information or the contents of the configuration and control registers are output on the SDO terminal MSB first, while STRn is low, and changes to the next bit on each falling edge of SCK. The first bit, which is always the FF (fault flag) bit from the Diagnostic register, is output as soon as STRn goes low.

Each of the programmable (configuration and control) registers has a write bit, WR (bit 10), as the first bit after the register address. This bit must be set to 1 to write the subsequent bits into the selected register. If WR is set to 0, then the remaining data bits (bits 9 to 0) are ignored. The state of the WR bit also determines the data output on SDO. If WR is set to 1 then the Diagnostic register is output. If WR is set to 0, then the contents of the register selected by the first five bits is output. In all cases, the first bit output on SDO will always be the FF bit from the Diagnostic Register.

The A4412 has 12 register banks. Bit <15:11> represents the register address for read and write. Bit <10> detects the read and write operation: for write operation, Bit <10> = 1, and for read operation, bit value is logic low. Bit <9> is an unused bit. Maximum data size is eight bits so Bit <8:1> represents the data word. The last bit in a serial transfer, Bit <0>, is a parity bit that is set to ensure odd parity in the complete 16-bit word. Odd parity means that the total number of 1s in any transmission should always be an odd number. This ensures that there is always at least one bit

## Pattern at SDI Pin

MSB															LSB
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
A4	A3	A2	A1	A0	W/R	NU	D7	D6	D5	D4	D3	D2	D1	D0	P
5-Bit Address							8-Bit Data								

## Pattern at SDO Pin after SDI Write

MSB															LSB
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FF	SE	ENBATS	WD_F	TSD_OK	VREG_OK	BUCK_OK	VCC_OK	VCP_OK	V5P_OK	V5B_OK	V5A_OK	V5CAN_OK	3V3_OK	0	P
Diagnostics															

## Pattern at SDO Pin after SDI Read

MSB															LSB
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FF	SE	ENBATS	WD_F	TSD_OK	VREG_OK	BUCK_OK	D7	D6	D5	D4	D3	D2	D1	D0	P
Diagnostics							8-Bit Data								

set to 1 and one bit set to 0 and allows detection of stuck-at faults on the serial input and output data connections. The parity bit is not stored but generated on each transfer.

Register data is output on the SDO terminal MSB first, while STRn is low, and changes to the next bit on each falling edge of the SCK. The first bit which is always the FF bit from the status register, is output as soon as STRn goes low.

If there are more than 16 rising edges on SCL, or if STRn goes high and there are fewer than 16 rising edges on SCK, then the write will be cancelled without writing data to the registers. In addition, the diagnostic register will not be reset; the SE bit will be set to indicate a data transfer error

**SDI:** Serial data logic input with pull-down. 16-bit serial word, input MSB first.

**SCK:** Serial clock logic input with pull-down. Data is latched in from SDI on the rising edge of SCL. There must be 16 rising edges per write and SCK must be held high when STRn changes.

**STRn:** Serial data strobe and serial access enable logic input with pull-up. When STRn is high, any activity on SCK or SDI is ignored and SDO is high impedance, allowing multiple SDI slaves to have common SDI, SCK, and SDO connections.

**SDO:** Serial data output. High impedance when STRn is high. Output bit 15 of the status register, the fault flag (FF), as soon as STRn goes low.

## Register Mapping

### STATUS REGISTERS

The A4412 provides 3 status registers. These registers are read-only. They provide real-time status of various functions within the A4412.

These registers report on the status of all six system rails. They also report on internal rail status, including the charge pump, VREG, VCC, and VDD rails. The general fault flag and watchdog fault state are found in these status registers.

The logic that creates the power-on enable and power reset status are reported through these registers.

### CONFIGURATION REGISTERS

The A4412 allows configuration of the window watchdog timing and pulse validation parameters.

An edge counter increments on every rising edge received at WD\_IN. The EDGE\_COUNT register stores the number of edges that must occur after the minimum timer has expired and before the maximum timer has expired. The valid counter increments

upwards on a successful edge count or decrements on an unsuccessful edge count. Once the valid counter reaches the VALID\_COUNT upward counts, the pulses on WD\_IN are considered valid and the watchdog fault, WD\_F, goes low.

The number of watchdog edges counted before incrementing the valid counter can be selected. This also sets the timer value. The minimum and maximum timers can be adjusted from nominal in 0.01 ms steps. The number of positive counts before the valid signal state changes can also be set.

EDGE\_COUNT [0:1], 2-bit integer to set the number of edges before the valid counter is incremented.

MIN\_TIMER [0:2], 3-bit integer to adjust the minimum timer nominal value in 0.01 ms steps.

MAX\_TIMER [0:2], 3-bit integer to adjust the maximum timer nominal value in 0.01 ms steps.

VALID\_COUNT [0:1] 2-bit integer to set the number of up counts on the valid counter before declaring a valid pulse train on WD\_IN.

The watchdog configuration registers can be written to at any time. The watchdog will update during either hunt states when it receives the first pulse on WD\_IN, as shown in Figure 8 WD update. If the user wants to change the watchdog configuration after the hunt states, then a WD\_RESTART is required.

The A4412 uses frequency dithering for the two switching regulators to help reduce EMC noise. The user can disable this feature through the SPI. Default is enabled.

### DIAGNOSTIC REGISTERS

There are multiple diagnostic registers in the A4412. These registers can be read to evaluate the status of the A4412. The high-level registers will tell which area a fault has occurred. Logic high on a data bit in this register implies that no fault has occurred. The following are monitored by these registers.

- All six outputs
- A4412 bias voltage
- Charge pump voltage
- Pre-regulator voltage
- Overtemperature
- Watchdog output
- Shorts on LX pins or open diode on pre-regulator

Note some of these faults will cause the A4412 to shut down, which might shutdown the microprocessor monitoring the SPI. In this event, the only way to read the fault would be to have alternative power to the microprocessor so it can read the registers. If



VCC of the A4412 shuts down, all stored register information is lost and the registers revert back to default values.

Other diagnostic registers store more detail on each fault; these include:

- Overvoltage on a particular output or internal rail
- Undervoltage on a particular output or internal rail
- Overcurrent on a rail

The diagnostic registers are latch registers and will hold data if a fault has occurred but recovered. So during startup, these registers will record a UV event on all outputs. On first read, these UV events will be reported. It is recommended to reset these registers after startup to ensure full fault reporting. These registers are reset by writing a 1 to them.

## DISABLE REGISTER

The disable register provides the user control of the 5 V outputs. Two bits must be set high to disable an output. If only one bit is high, then the outputs remain on. Note V5CAN requires a watchdog reset to re-enable its output. Set register 0x06 bit 0 and bit 4 to 0; issue watchdog reset through register 0x07.

## WATCHDOG MODE KEY REGISTER

At times it may be necessary to re-flash or restart the processor. To do this, the user must put the watchdog into “Flash Mode” or “restart. This is done writing a sequence of key words to the “watchdog\_mode\_key” register. If the correct word sequence is not received, then the sequence must restart.

Once flash is complete, the processor must send the restart sequence of key words for the watchdog to exit “Flash Mode”. If VCC has not been removed from the A4412, the watchdog will restart with the current configuration.

## VERIFY RESULT REGISTERS

On every startup, the A4412 performs a self-test of the UV and OV detect circuits. This test should cause the diagnostic registers to toggle state. If the diagnostic register successfully changes state, the verify result register will latch high. Upon completion of startup, the system’s microprocessor can check the verify result registers to see if the self-test passed.

## Register Map

HEX Address	Register Name	DEC Address	Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x00	status_0	0	RO	FF	POE_OK	VCC_OK	VDD_OK	V5P_OK	V5B_OK	V5A_OK	V5CAN_OK
0x01	status_1	1	RO		NPOR_OK	WD_F	TSD_OK	VCP_OK	VREG_OK	3V3_OK	BUCK_OK
0x02	status_2	2	RO	CLK_Hi	CLK_Lo	NPOR_S	POE_S	ENBATS	WD_STATE		
0x03	diag_0	3	RW1C	V5A_OV	V5A_UV	V5CAN_OV	V5CAN_UV	V5P_OV	V5P_UV	V5B_OV	V5B_UV
0x04	diag_1	4	RW1C	VDD_OV	VDD_UV	VREG_OV	VREG_UV	3V3_OV	3V3_UV	BUCK_OV	BUCK_UV
0x05	diag_2	5	RW1C		LX2_OK	LX1_OK	D1_OK		VCC_UV	VCP_OV	VCP_UV
0x06	output_disable	6	RW	V5P_DIS1	V5A_DIS1	V5B_DIS1	V5CAN_DIS1	V5P_DIS0	V5A_DIS0	V5B_DIS0	V5CAN_DIS0
0x07	watchdog_mode_key	7	WO	Keycode Entry (Write Only)							
			RO	0	0	0	0	0	0	0	Unlocked
0x08	config_0	8	RW			MAX_TIMER			MIN_TIMER		
0x09	config_1	9	RW				DITH_DIS	VALID_COUNT		EDGE_COUNT	
0x0A	verify_result_0	10	RW1C	V5A_OV_OK	V5A_UV_OK	V5CAN_OV_OK	V5CAN_UV_OK	V5P_OV_OK	V5P_UV_OK	V5B_OV_OK	V5B_UV_OK
0x0B	verify_result_1	11	RW1C	BIST_PASS	TSD_OK	VREG_OV_OK	VREG_UV_OK	3V3_OV_OK	3V3_UV_OK	BUCK_OV_OK	BUCK_UV_OK

### Register Types:

RO = Read-Only  
RW = Read or Write  
RW1C = Read or Write 1 to clear  
WO = Write-Only

**0X00. STATUS REGISTER 0:**

D7	D6	D5	D4	D3	D2	D1	D0
FF	POE_OK	VCC_OK	VDD_OK	V5P_OK	V5B_OK	V5A_OK	V5CAN_OK
0	0	0	0	0	0	0	0

Address 00000

Read-only register

Data

FF [D7]: Fault flag, 0 = no fault, 1 = fault

POE\_OK [D6]: Power-on enable signal matches what A4412 is demanding, 0 = fault, 1 = no fault

VCC\_OK [D5]: Internal VCC rail is OK, 0 = fault, 1 = no fault

VDD\_OK [D4]: Internal VDD rail is OK, 0 = fault, 1 = no fault

V5P\_OK [D3]: Protected 5V rail is OK, 0 = fault, 1 = no fault

V5B\_OK [D2]: 5V rail B is OK, 0 = fault, 1 = no fault

V5A\_OK [D1]: 5V rail A is OK, 0 = fault, 1 = no fault

V5CAN\_OK [D0]: CAN bus 5V rail is OK, 0 = fault, 1 = no fault

**0X01. STATUS REGISTER 1:**

D7	D6	D5	D4	D3	D2	D1	D0
	NPOR_OK	WD_F	TSD_OK	VCP_OK	VREG_OK	3V3_OK	BUCK_OK
0	0	0	0	0	0	0	0

Address 00001

Read-only register

Data

NPOR\_OK [D6]: NPOR signal matches what A4412 is demanding, 0 = fault, 1 = no fault

WD\_F [D5]: Watchdog is active, 0 = watchdog off or no fault, 1 = watchdog fault

TSD\_OK [D4]: Thermal shutdown status, 0 = overtemperature event, 1 = temperature OK

VCP\_OK [D3]: Charge pump rail is OK, 0 = fault, 1 = no fault

VREG\_OK [D2]: Pre-regulator voltage is OK, 0 = fault, 1 = no fault

3V3\_OK [D1]: 3.3 V rail is OK, 0 = fault, 1 = no fault

BUCK\_OK [D0]: Synchronous buck adjustable rail is OK, 0 = fault, 1 = no fault

**0X02. STATUS REGISTER 2:**

D7	D6	D5	D4	D3	D2	D1	D0
CLK_Hi	CLK_Lo	NPOR_S	POE_S	ENBATS	WD_state_2	WD_state_1	WD_state_0
0	0	0	0	0	0	0	0

Address 00010

Read-only register

Data

CLK\_Hi [D7]: Indicates if watchdog clock input is stuck high, 0 = CLK is not stuck high, 1 = clock is stuck high

CLK\_Lo [D6]: Indicates if watchdog clock input is stuck low, 0 = CLK is not stuck low, 1 = clock is stuck low

NPOR\_S [D5]: Power-on reset internal logic status, 0 = NPOR is low, 1 = NPOR is high

POE\_S [D4]: Power-on enable internal logic status, 0 = POE is low, 1 = POE is high

ENBATS [D3]: Battery-enable status, reports the status of the high-voltage enable pin ENBAT on the A4412, 0 = ENBAT is low, 1 = ENBAT is high

WD\_state\_x [D2:D0]: Shows the state that the watchdog is currently in, see table for the different states.

WD_state_2	WD_state_1	WD_state_0	Watchdog State
0	0	0	Idle
0	0	1	Flash
0	1	0	Test Hunt
0	1	1	Test Lock
1	0	0	Test Complete
1	0	1	Running Hunt
1	1	0	Running
1	1	1	Watchdog

**0X03. DIAGNOSTIC REGISTER 0:**

D7	D6	D5	D4	D3	D2	D1	D0
V5A_OV	V5A_UV	V5CAN_OV	V5CAN_UV	V5P_OV	V5P_UV	V5B_OV	V5B_UV
0	0	0	0	0	0	0	0

Address 00011

Read register, write 1 to clear

Data

V5A\_OV [D7]: 5 V rail A overvoltage occurred, 0 = rail OK, 1 = overvoltage occurred

V5A\_UV [D6]: 5 V rail A undervoltage occurred, 0 = rail OK, 1 = undervoltage occurred

V5CAN\_OV [D5]: 5 V CAN bus rail overvoltage occurred, 0 = rail OK, 1 = overvoltage occurred

V5CAN\_UV [D4]: 5 V CAN bus rail undervoltage occurred, 0 = rail OK, 1 = undervoltage occurred

V5P\_OV [D3]: Protected 5 V rail overvoltage occurred, 0 = rail OK, 1 = overvoltage occurred

V5P\_UV [D2]: Protected 5 V rail undervoltage occurred, 0 = rail OK, 1 = undervoltage occurred

V5B\_OV [D1]: 5 V rail B overvoltage occurred, 0 = rail OK, 1 = overvoltage occurred

V5B\_UV [D0]: 5 V rail B undervoltage occurred, 0 = rail OK, 1 = undervoltage occurred

**0X04. DIAGNOSTIC REGISTER 1:**

D7	D6	D5	D4	D3	D2	D1	D0
VDD_OV	VDD_UV	VREG_OV	VREG_UV	3V3_OV	3V3_UV	BUCK_OV	BUCK_UV
0	0	0	0	0	0	0	0

Address 00100

Read register, write 1 to clear

Data

VDD\_OV [D7]: Internal VDD rail overvoltage occurred, 0 = rail OK, 1 = overvoltage occurred

VDD\_UV [D6]: Internal VDD rail undervoltage occurred, 0 = rail OK, 1 = undervoltage occurred

VREG\_OV [D5]: Pre-regulator voltage rail overvoltage occurred, 0 = rail OK, 1 = overvoltage occurred

VREG\_UV [D4]: Pre-regulator voltage rail undervoltage occurred, 0 = rail OK, 1 = undervoltage occurred

3V3\_OV [D3]: 3.3 V rail overvoltage occurred, 0 = rail OK, 1 = overvoltage occurred

3V3\_UV [D2]: 3.3 V rail undervoltage occurred, 0 = rail OK, 1 = undervoltage occurred

BUCK\_OV [D1]: Synchronous buck adjustable voltage rail overvoltage occurred, 0 = rail OK, 1 = overvoltage occurred

BUCK\_UV [D0]: Synchronous buck adjustable voltage rail undervoltage occurred, 0 = rail OK, 1 = undervoltage occurred

**0X05. DIAGNOSTIC REGISTER 2:**

D7	D6	D5	D4	D3	D2	D1	D0
	LX2_OK	LX1_OK	D1_OK		VCC_UV	VCP_OV	VCP_UV
0	0	0	0	0	0	0	0

Address 00101

Read register, write 1 to clear

Data

LX2\_OK [D6]: Adjustable synchronous buck switch node is OK, 0 = fault on LX2, 1 = LX2 is working correctly

LX1\_OK [D5]: Pre-regulator switch node is OK, 0 = fault on LX1, 1 = LX1 is working correctly

D1\_OK [D4]: Pre-regulator freewheeling diode is OK, 0 = diode is open circuit, 1 = diode is working correctly

VCC\_UV [D2]: Internal VCC rail undervoltage occurred, 0 = rail OK, 1 = undervoltage occurred

VCP\_OV [D1]: Charge pump voltage rail overvoltage occurred, 0 = rail OK, 1 = overvoltage occurred

VCP\_UV [D0]: Charge pump voltage rail undervoltage occurred, 0 = rail OK, 1 = undervoltage occurred

**0X06. OUTPUT DISABLE REGISTER:**

D7	D6	D5	D4	D3	D2	D1	D0
V5P_DIS1	V5A_DIS1	V5B_DIS1	V5CAN_DIS1	V5P_DIS0	V5A_DIS0	V5B_DIS0	V5CAN_DIS0
0	0	0	0	0	0	0	0

Address 00110

Read or write register

Data

V5P\_DIS [D7:D3]: Disable protected 5 V output, 11 = disabled, x0 = enabled, 0x = enabled

V5A\_DIS [D6:D2]: Disable 5 V rail A output, 11 = disabled, x0 = enabled, 0x = enabled

V5B\_DIS [D5:D1]: Disable 5 V rail B output, 11 = disabled, x0 = enabled, 0x = enabled

V5CAN\_DIS [D4:D0]: Disable 5 V CAN bus rail, 11 = disabled, x0 = enabled, 0x = enabled;

A watchdog reset is required to re-enable V5CAN if it was disabled.

**0X07. WATCHDOG MODE KEY REGISTER:**

D7	D6	D5	D4	D3	D2	D1	D0
KEY_7	KEY_6	KEY_5	KEY_4	KEY_3	KEY_2	KEY_1	KEY_0
0	0	0	0	0	0	0	0

Address 00111

Write register

Data

KEY [D7:D0]: Three 8-bit words must be sent in the correct order to enable flash mode or restart the watchdog. If an incorrect word is received, then the register resets and the first word have to be resent.

	Flash Mode	Restart
WORD1	0xD3	0xD3
WORD2	0x33	0x33
WORD3	0xCC	0xCD

## 0X08. CONFIGURATION REGISTER 0:

D7	D6	D5	D4	D3	D2	D1	D0
		WD_MAX_2	WD_MAX_1	WD_MAX_0	WD_MIN_2	WD_MIN_1	WD_MIN_0
0	0	1	0	0	1	0	0

Address 01000

Read or write register

Data

WD\_MAX [D5:D3]: 3-bit word to adjust the watchdog maximum timer set point

WD_MAX_2	WD_MAX_1	WD_MAX_0	Maximum Timer	WD Typical Maximum Pulse
0	0	0	+0.08 ms	2.08 ms
0	0	1	+0.09 ms	2.09 ms
0	1	0	+0.10 ms	2.10 ms
0	1	1	+0.11 ms	2.11 ms
1	0	0	+0.12 ms	2.12 ms
1	0	1	+0.13 ms	2.13 ms
1	1	0	+0.14 ms	2.14 ms
1	1	1	+0.15 ms	2.15 ms

WD\_MIN [D2:D0]: 3-bit word to adjust the watchdog minimum timer set point

WD_MIN_2	WD_MIN_1	WD_MIN_0	Minimum Timer	WD Typical Minimum Pulse
0	0	0	-0.08 ms	1.92 ms
0	0	1	-0.09 ms	1.90 ms
0	1	0	-0.10 ms	1.89 ms
0	1	1	-0.11 ms	1.88 ms
1	0	0	-0.12 ms	1.86 ms
1	0	1	-0.13 ms	1.87 ms
1	1	0	-0.14 ms	1.86 ms
1	1	1	-0.15 ms	1.85 ms

**0X09. CONFIGURATION REGISTER 1:**

D7	D6	D5	D4	D3	D2	D1	D0
			DITH_DIS	VALID_1	VALID_0	EDGE_1	EDGE_0
0	0	0	0	0	0	0	0

Address 01001

Read or write register

Data

DITH\_DIS [D4]: This bit allows the user to disable the dither function for the switching converters, 0 = dither enabled, 1 = dither disabled.

VALID [D3:D2]: 2-bit counter to set the number of counts before a valid watchdog signal is set or reset.

VALID_1	VALID_0	Valid Counts
0	0	2
0	1	4
1	0	6
1	1	8

EDGE [D1:D0]: 2-bit counter to set the number of edges to count before incrementing the VALID counter. The EDGE value also sets the minimum and maximum nominal timers. The minimum and maximum timers will be based on the number of edge counts times 2 ms plus the delta stored in WD\_MIN and WD\_MAX.

EDGE_1	EDGE_0	Edge Counts	Nominal Timer
0	0	4	8 ms
0	1	6	12 ms
1	0	8	16 ms
1	1	10	20 ms

**0X0A. VERIFY RESULT REGISTER 0:**

D7	D6	D5	D4	D3	D2	D1	D0
V5A_OV_OK	V5A_UV_OK	V5CAN_OV_OK	V5CAN_UV_OK	V5P_OV_OK	V5P_UV_OK	V5B_OV_OK	V5B_UV_OK
0	0	0	0	0	0	0	0

Address 01010

Read register, write 1 to clear

Data

V5A\_OV\_OK [D7]: 5 V rail A overvoltage self-test passed, 0 = test failed, 1 = test passed

V5A\_UV\_OK [D6]: 5 V rail A undervoltage self-test passed, 0 = test failed, 1 = test passed

V5CAN\_OV\_OK [D5]: 5 V CAN bus rail overvoltage self-test passed, 0 = test failed, 1 = test passed

V5CAN\_UV\_OK [D4]: 5 V CAN bus rail undervoltage self-test passed, 0 = test failed, 1 = test passed

V5P\_OV\_OK [D3]: Protected 5V rail overvoltage self-test passed, 0 = test failed, 1 = test passed

V5P\_UV\_OK [D2]: Protected 5V rail undervoltage self-test passed, 0 = test failed, 1 = test passed

V5B\_OV\_OK [D1]: 5V rail B overvoltage self-test passed, 0 = test failed, 1 = test passed

V5B\_UV\_OK [D0]: 5V rail B undervoltage self-test passed, 0 = test failed, 1 = test passed

**0X0B. VERIFY RESULT REGISTER 1:**

D7	D6	D5	D4	D3	D2	D1	D0
BIST_PASS	TSD_OK	VREG_OV_OK	VREG_UV_OK	3V3_OV_OK	3V3_UV_OK	BUCK_OV_OK	BUCK_UV_OK
0	0	0	0	0	0	0	0

Address 01011

Read register, write 1 to clear

Data

BIST\_PASS [D7]: Self-test status, 0 = self-test failed, 1 = self-test passed

TSD\_OK [D6]: Thermal shutdown circuit passed self-test, 0 = test failed, 1 = test passed

VREG\_OV\_OK [D5]: Pre-regulator voltage rail overvoltage self-test passed, 0 = test failed, 1 = test passed

VREG\_UV\_OK [D4]: Pre-regulator voltage rail undervoltage self-test passed, 0 = test failed, 1 = test passed

3V3\_OV\_OK [D3]: 3.3 V rail overvoltage self-test passed, 0 = test failed, 1 = test passed

3V3\_UV\_OK [D2]: 3.3 V rail undervoltage self-test passed, 0 = test failed, 1 = test passed

BUCK\_OV\_OK [D1]: Synchronous buck adjustable voltage rail overvoltage self-test passed, 0 = test failed, 1 = test passed

BUCK\_UV\_OK [D0]: Synchronous buck adjustable voltage rail undervoltage self-test passed, 0 = test failed, 1 = test passed



## DESIGN AND COMPONENT SELECTION

The following section briefly describes the component selection procedure for the A4412.

## Setting up the Pre-Regulator

This section discusses the component selection for the A4412 pre-regulator. It covers the charge pump circuit, inductor, diodes, boost MOSFET, and input and output capacitors. It will also cover soft-start and loop compensation.

## Charge Pump Capacitors

The charge pump requires two capacitors: a 1  $\mu\text{F}$  connected from pin VCP to VIN and 0.22  $\mu\text{F}$  connected between pins CP1 and CP2. These capacitors should be a high-quality ceramic capacitors, such as an X5R or X7R, with a voltage rating of at least 16 V.

## PWM Switching Frequency

The switching frequency of the A4412 is fixed at 2.2 MHz nominal. The A4412 includes a frequency foldback scheme that starts when  $V_{\text{IN}}$  is greater than 18 V. Between 18 V and 36 V, the switching frequency will foldback from 2.2 MHz typical to 1 MHz typical. The switching frequency for a given input voltage above 18 V and below 36 V is:

$$f_{\text{sw}} = 3.4 - \frac{1.2}{18} \times V_{\text{IN}} (\text{MHz}) \quad (1)$$

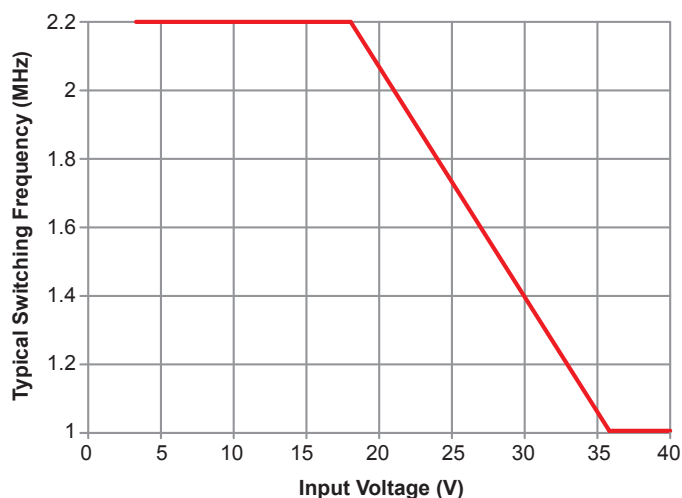


Figure 9: Typical Switching Frequency versus Input Voltage

## Pre-Regulator Output Inductor (L1)

For peak current mode control, it is well known that the system will become unstable when the duty cycle is above 50% without adequate Slope Compensation ( $S_E$ ). However, the slope compensation in the A4412 is a fixed value. Therefore, it is important to calculate an inductor value so the falling slope of the inductor current ( $S_F$ ) will work well with the A4412's slope compensation.

Equation 2 can be used to calculate a range of values for the output inductor for the buck-boost. In equation 2, slope compensation can be found in the Electrical Characteristic table,  $V_F$  is the asynchronous diodes forward voltage,  $S_E$  is in A/ $\mu\text{s}$ , and L will be in  $\mu\text{H}$ :

$$\frac{(V_{\text{REG}} + V_F)}{S_{EI}} \leq L1 \leq \frac{2 \times (V_{\text{REG}} + V_F)}{S_{EI}} \quad (2)$$

If equation 2 yields an inductor value that is not a standard value, then the next closest available value should be used. The final inductor value should allow for 10%-20% of initial tolerance and 20%-30% for inductor saturation.

Due to topology and frequency switching of the A4412 pre-regulator, the inductor ripple current varies with input voltage per Figure 10 below:

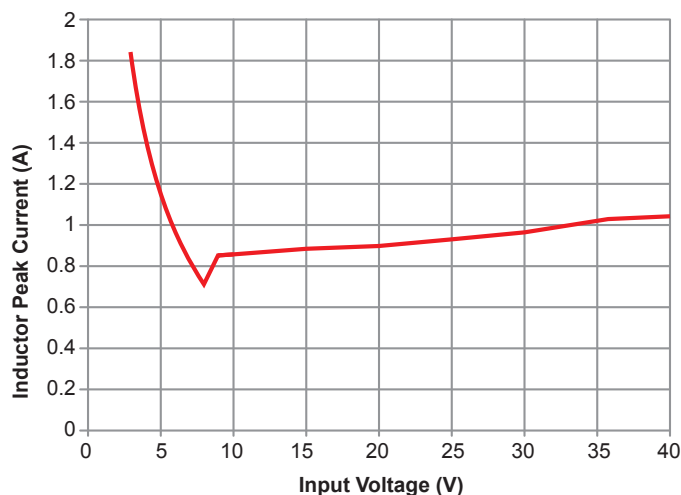


Figure 10: Typical Peak Inductor Current versus Input Voltage for 0.8 A Output Current and 10  $\mu\text{H}$  Inductor

The inductor should not saturate given the peak operating current during overload. Equation 3 calculates this current. In equation 3,

$V_{IN,MAX}$  is the maximum continuous input voltage, such as 16 V, and  $V_F$  is the asynchronous diode forward voltage.

$$I_{PEAK1} = 4.6 A - \frac{S_{E1} \times (V_{REG} + V_F)}{0.9 \times f_{SW} \times (V_{IN,MAX} + V_F)} \quad (3)$$

After an inductor is chosen, it should be tested during output overload and short-circuit conditions. The inductor current should be monitored using a current probe. A good design should ensure the inductor or the regulator are not damaged when the output is shorted to ground at maximum input voltage and the highest expected ambient temperature.

Inductor ripple current can be calculated using equation 4 for buck mode, and equation 5 for buck-boost mode.

$$\Delta I_{LI} = \frac{(V_{IN} - V_{REG}) \times V_{REG}}{f_{SW} \times LI \times V_{IN}} \quad (4)$$

$$\Delta I_{B/B} = \frac{V_{IN} \times D_{BOOST}}{f_{SW} \times LI} \quad (5)$$

## Pre-Regulator Output Capacitors

The output capacitors filter the output voltage to provide an acceptable level of ripple voltage. They also store energy to help maintain voltage regulation during a load transient. The voltage rating of the output capacitors must support the output voltage with sufficient design margin.

The output voltage ripple ( $\Delta V_{OUT}$ ) is a function of the output capacitors parameters:  $C_O$ ,  $ESR_{CO}$ ,  $ESL_{CO}$ .

$$\Delta V_{OUT} = \Delta I_L \times ESR_{CO} + \frac{V_{IN} - V_{OUT}}{LI} \times ESL_{CO} + \frac{\Delta I_{LI}}{8 \times f_{SW} \times C_O} \quad (6)$$

The type of output capacitors will determine which terms of equation 6 are dominant. For ceramic output capacitors, the  $ESR_{CO}$  and  $ESL_{CO}$  are virtually zero, so the output voltage ripple will be dominated by the third term of equation 6.

$$\Delta V_{REG} = \frac{\Delta I_{LI}}{8 \times f_{SW} \times C_O} \quad (7)$$

To reduce the voltage ripple of a design using ceramic output

capacitors, simply increase the total capacitance, reduce the inductor current ripple (i.e. increase the inductor value), or increase the switching frequency.

The transient response of the regulator depends on the number and type of output capacitors. In general, minimizing the ESR of the output capacitance will result in a better transient response. The ESR can be minimized by simply adding more capacitors in parallel or by using higher quality capacitors. At the instant of a fast load transient ( $di/dt$ ), the output voltage will change by the amount:

$$\Delta V_{REG} = \Delta I_{LOAD} \times ESR_{CO} + \frac{di}{dt} \times ESL_{CO} \quad (8)$$

After the load transient occurs, the output voltage will deviate from its nominal value for a short time. This time will depend on the system bandwidth, the output inductor value, and output capacitance. Eventually, the error amplifier will bring the output voltage back to its nominal value.

The speed at which the error amplifier will bring the output voltage back to its setpoint will depend mainly on the closed-loop bandwidth of the system. A higher bandwidth usually results in a shorter time to return to the nominal voltage. However, a higher bandwidth system may be more difficult to obtain acceptable gain and phase margins. Selection of the compensation components ( $R_Z$ ,  $C_Z$ ,  $C_P$ ) are discussed in more detail in the Compensation Components section of this datasheet.

## Ceramic Input Capacitors

The ceramic input capacitor(s) must limit the voltage ripple at the VIN pin to a relatively low voltage during maximum load. Equation 8 can be used to calculate the minimum input capacitance,

$$C_{IN} \geq \frac{I_{VREG,MAX} \times 0.25}{0.90 \times f_{SW} \times 50 mV} \quad (9)$$

where  $I_{VREG,MAX}$  is the maximum current from the pre-regulator,

$$I_{VREG,MAX} = I_{LINEAR} + I_{AUX} + \frac{V_{SYNC\_BUCK} \times I_{SYNC\_BUCK}}{0.85 \times V_{REG}} + 20 mA \quad (10)$$

where  $I_{LINEAR}$  is the sum of all the internal linear regulators output currents,  $I_{AUX}$  is any extra current drawn from the VREG output to power other devices external to the A4412,  $I_{SYNC\_BUCK}$  and  $V_{SYNC\_BUCK}$  are the output current and voltage of the synchronous buck converter

A good design should consider the dc-bias effect on a ceramic capacitor—as the applied voltage approaches the rated value, the

capacitance value decreases. The X5R and X7R type capacitors should be the primary choices due to their stability versus both DC bias and temperature. For all ceramic capacitors, the DC bias effect is even more pronounced on smaller case sizes so a good design will use the largest affordable case size.

Also for improved noise performance, it is recommended to add smaller sized capacitors close to the input pin and the D1 anode. Use a 0.1  $\mu\text{F}$  0603 capacitor.

### Buck-Boost Asynchronous Diode (D1)

The highest peak current in the asynchronous diode (D1) occurs during overload and is limited by the A4412. Equation 3 can be used to calculate this current.

The highest average current in the asynchronous diode occurs when  $V_{\text{IN}}$  is at its maximum,  $D_{\text{BOOST}} = 0\%$ , and  $D_{\text{BUCK}} = \text{minimum}$  (10%),

$$I_{\text{AVG}} = 0.9 \times I_{\text{VREG,MAX}} \quad (11)$$

where  $I_{\text{VREG,MAX}}$  is calculated using equation 10.

### Boost MOSFET (Q1)

The RMS current in the boost MOSFET (Q1) occurs when  $V_{\text{IN}}$  is at its minimum and both the buck and boost operate at their maximum duty cycles (approximately 64% and 58%, respectively),

$$I_{Q1,\text{RMS}} = \sqrt{D_{\text{BOOST}} \times \left[ \left( I_{\text{PEAK1}} - \frac{\Delta I_{\text{B/B}}}{2} \right)^2 + \frac{\Delta I_{\text{B/B}}^2}{12} \right]} \quad (12)$$

where  $\Delta I_{\text{B/B}}$  and  $I_{\text{PEAK1}}$  are derived using equations 3 and 5, respectively.

### Boost Diode (D2)

In buck mode, this diode will simply conduct the output current. However, in buck-boost mode, the peak currents in this diode may increase a lot. The A4412 limits the peak current to the value calculated using equation 3. The average current is simply the output current.

### Pre-Regulator Soft Start and Hiccup Mode Timing ( $C_{\text{SS1}}$ )

The soft-start time of the buck-boost converter is determined by the value of the capacitance at the soft-start pin,  $C_{\text{SS1}}$ .

If the A4412 is starting into a very heavy load, a very fast soft-start time may cause the regulator to exceed the pulse-by-pulse overcurrent threshold. This occurs because the total of the full

load current, the inductor ripple current, and the additional current required to charge the output capacitors ( $I_{\text{CO}} = C_{\text{O}} \times V_{\text{OUT}} / t_{\text{SS}}$ ) is higher than the pulse-by-pulse current threshold, as shown in Figure 11.

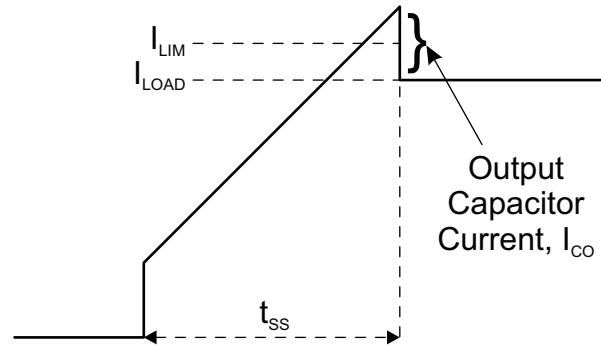


Figure 11: Output Current ( $I_{\text{CO}}$ ) during Startup

To avoid prematurely triggering hiccup mode the soft start time,  $t_{\text{SS1}}$ , should be calculated according to equation 13,

$$t_{\text{SS1}} = V_{\text{REG}} \times \frac{C_{\text{O}}}{I_{\text{CO}}} \quad (13)$$

where  $V_{\text{OUT}}$  is the output voltage,  $C_{\text{O}}$  is the output capacitance,  $I_{\text{CO}}$  is the amount of current allowed to charge the output capacitance during soft-start (recommend  $0.1 \text{ A} < I_{\text{CO}} < 0.3 \text{ A}$ ). Higher values of  $I_{\text{CO}}$  ensure that hiccup mode is not falsely triggered. Allegro recommends starting the design with an  $I_{\text{CO}}$  of 0.1 A and increasing it only if the soft-start time is too slow.

Then  $C_{\text{SS1}}$  can be selected based on equation 14,

$$C_{\text{SS1}} > \frac{I_{\text{SS1SU}} \times t_{\text{SS1}}}{0.8} \quad (14)$$

If a non-standard capacitor value for  $C_{\text{SS1}}$  is calculated, the next larger value should be used.

The voltage at the soft-start pin will start from 0 V and will be charged by the soft-start current,  $I_{\text{SS1SU}}$ . However, PWM switching will not begin instantly because the voltage at the soft-start pin must rise above the soft-start offset voltage ( $V_{\text{SS1OFFS}}$ ). The soft-start delay ( $t_{\text{SS1,DELAY}}$ ) can be calculated using equation 15,

$$t_{\text{SS1,DELAY}} = C_{\text{SS1}} \times \frac{V_{\text{SS1OFFS}}}{I_{\text{SS1SU}}} \quad (15)$$

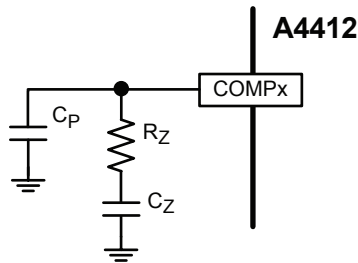
When the A4412 is in hiccup mode, the soft-start capacitor sets

the hiccup period. During a startup attempt, the soft-start pin charges the soft-start capacitor with  $ISS1_{SU}$  and discharges the same capacitor with  $ISS1_{HIC}$  between startup attempts.

In applications where the A4412 will be enabled with  $V_{REG} > V_{REGUV,H}$ , the outputs will not start up in the typical sequenced manner but will turn on immediately. This can lead to rapid discharge of the VREG rail, potentially resulting in overshoot of the LDOs and synchronous buck output as VREG recovers. To avoid this,  $C_{SS1}$  must be small enough to allow VREG to charge up before excessive droop can occur on the VREG rail. However, if  $C_{SS1}$  is too small, VREG can overshoot during a typical startup sequence. Additionally, the soft-start capacitor for the synchronous buck ( $C_{SS2}$ ) must be large enough to prevent the synchronous buck output from overshooting when the A4412 is started with  $V_{REG} > V_{REGUV,H}$ . Due to complexity, these calculations are outside the scope of this datasheet. If the application requires the A4412 to be enabled with  $V_{REG} > V_{REGUV,H}$ , using Allegro's *A4412 Soft-Start Optimization Design Tool* is recommended to assist in calculating optimal  $C_{SS1}$  and  $C_{SS2}$  values for the application.

### Pre-Regulator Compensation Components ( $R_Z$ , $C_Z$ , $C_P$ )

Although the A4412 can operate in buck-boost mode at low input voltages, it still can be considered a buck converter when looking at the control loop. The following equations can be used to calculate the compensation components.



**Figure 12: A4412 Compensation Components**

First, we need to select the target crossover frequency for our final system. While we are switching at over 2 MHz, the crossover is governed by the required phase margin. Since we are using a type II compensation scheme, we are limited to the amount of phase we can add. Hence, we select a crossover frequency,  $f_c$ , in the region of 55 kHz. The total system phase will drop off at higher crossover frequencies. The  $R_Z$  selection is based on the gain required at the crossover frequency and can be calculated by the following simplified equation:

$$R_Z = \frac{13.36 \times \pi \times f_c \times C_O}{g_{mPOWER1} \times g_{mEAI}} \quad (16)$$

The series capacitor,  $C_Z$ , along with the resistor,  $R_Z$ , set the location of the compensation zero. This zero should be placed no lower than  $\frac{1}{4}$  the crossover frequency and should be kept to a minimum value. Equation 17 can be used to estimate this capacitor value.

$$C_Z > \frac{4}{2\pi \times R_Z \times f_c} \quad (17)$$

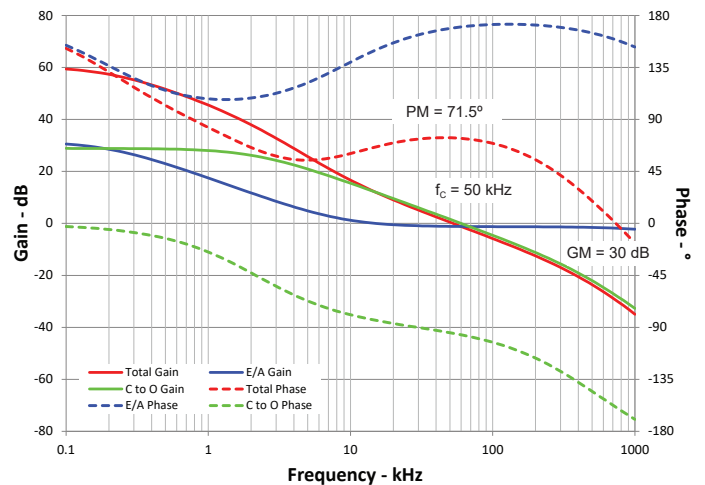
Determine if the second compensation capacitor ( $C_P$ ) is required. It is required if the ESR zero of the output capacitor is located at less than half of the switching frequency or the following relationship is valid:

$$\frac{1}{2\pi \times C_O \times ESR_{CO}} < \frac{f_{sw}}{2} \quad (18)$$

If this is the case, then add the second compensation capacitor ( $C_P$ ) to set the pole at the location of the ESR zero. Determine the  $C_P$  value by the equation:

$$C_P = \frac{C_{OUT} \times ESR}{R_Z} \quad (19)$$

Finally, we take a look at the combined bode plot of both the control-to-output and the compensated error amp—see the red curves shown in Figure 13. Careful examination of this plot shows that the magnitude and phase of the entire system are simply the sum of the error amp response (blue) and the control to output response (green). As shown in Figure 13, the bandwidth of this system ( $f_c$ ) is 50 kHz, the phase margin is 71.5 degrees, and the gain margin is 30 dB.



**Figure 13: Bode Plot of the Complete System (red curve)**  
 $R_Z = 8.25 \text{ k}\Omega$ ,  $C_Z = 2.2 \text{ nF}$ ,  $C_P = 10 \text{ pF}$   
 $L_O = 10 \text{ }\mu\text{H}$ ,  $C_O = 2 \times 10 \text{ }\mu\text{F}$  Ceramic

## Synchronous Buck Component Selection

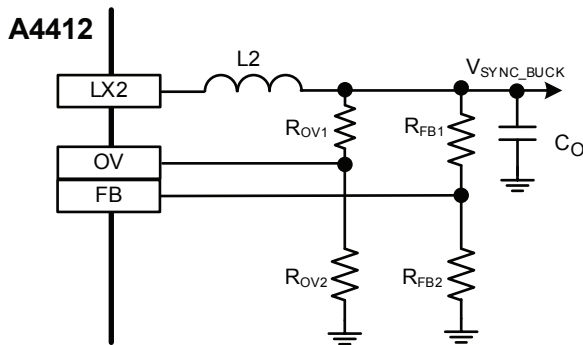
Similar design methods can be used for the synchronous buck, however, the complexity of variable input voltage and boost operation are removed.

## Setting the Output Voltage, RFB1 and RFB2

If the output of the synchronous buck is connected directly to the FB pin, then the output will be regulated to  $V_{FB}$  or 1.305 V nominal. The OV pin should also be connected to the output to provide open feedback protection.

The A4412 also allows the user to program the output voltage. This is achieved by adding a resistor divider from its output to ground and connecting the center point to FB, see Figure 14 below.

A second divider, ROV1 and ROV2, using the same values as RFB1 and RFB2 respectively, should be connected to the OV pin of the A4412 as shown in Figure 14.



**Figure 14: Programing the A4412 Synchronous Buck Output**

The resistors can be selected based on the following equation, set  $R_{FB2} = R_{OV2} = 10 \text{ k}\Omega$ .  $V_{SYNC\_BUCK}$  is the required output voltage.

$$R_{FB1} = R_{OV1} = \frac{V_{SYNC\_BUCK}}{V_{FB}} \times R_{FB2} - R_{FB2} \quad (20)$$

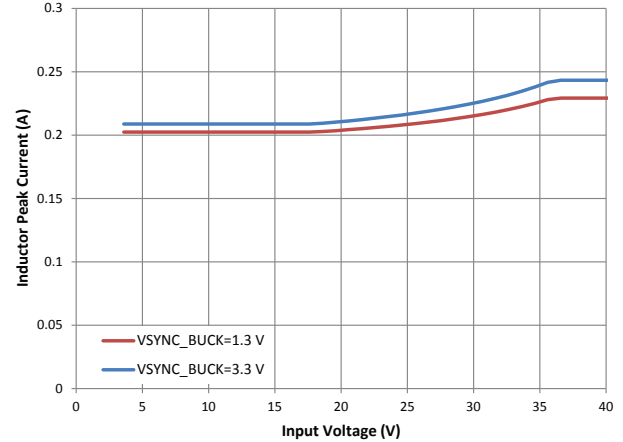
## Synchronous Buck Output Inductor (L2)

Equation 21 can be used to calculate a range of values for the output inductor for the synchronous buck regulator. In equation 21, slope compensation  $S_{E2}$  be found in the electrical characteristic table.

$$\frac{V_{SYNC\_BUCK}}{S_{E2}} \leq L2 \leq \frac{2 \times V_{SYNC\_BUCK}}{S_{E2}} \quad (21)$$

If equation 21 yields an inductor value that is not a standard value, then the next closest available value should be used. The

final inductor value should allow for 10%-20% of initial tolerance and 20%-30% for inductor saturation.



**Figure 15: Typical Peak Inductor Current versus Input Voltage for 0.18 A Output Current and 10 µH Inductor**

The inductor should not saturate given the peak current at overload according to equation 22. The synchronous buck uses the same switching frequency,  $f_{SW}$ , as the pre-regulator.

$$I_{PEAK2} = 840 \text{ mA} - \frac{S_{E2} \times V_{SYNC\_BUCK}}{0.9 \times f_{SW} \times V_{REG}} \quad (22)$$

After an inductor is chosen, it should be tested during output short-circuit conditions. The inductor current should be monitored using a current probe. A good design should ensure the inductor or the regulator are not damaged when the output is shorted to ground at maximum input voltage and the highest expected ambient temperature.

Once inductor value is known the ripple current can be calculated:

$$\Delta I_{L2} = \frac{(V_{REG} - V_{SYNC\_BUCK}) \times V_{SYNC\_BUCK}}{f_{SW} \times L2 \times V_{REG}} \quad (23)$$

## Synchronous Buck Output Capacitors

Similar criteria as the pre-regulator can be used in selecting the output capacitors. Ceramic output capacitors should be used so for a given output voltage ripple the minimum output capacitor value can be calculated using equation 24.

$$C_O \geq \frac{\Delta I_{L2}}{8 \times f_{SW} \times \Delta V_{SYNC\_BUCK}} \quad (24)$$



## Synchronous Buck Compensation Components

Again, similar techniques as used with the pre-regulator can be used to compensate the synchronous buck.

For the synchronous buck, we select a crossover frequency,  $f_c$ , in the region of 50 kHz. The  $R_Z$  selection is based on the gain required at the crossover frequency, and can be calculated by the following simplified equation:

$$R_Z = \frac{V_{\text{SYNC\_BUCK}} \times 2\pi \times f_c \times C_O}{V_{\text{FB}} \times g_{m\text{POWER2}} \times g_{m\text{EA2}}} \quad (25)$$

The series capacitor,  $C_Z$ , along with the resistor,  $R_Z$ , set the location of the compensation zero. This zero should be placed no lower than  $\frac{1}{4}$  the crossover frequency and should be kept to a minimum value. Equation 26 can be used to estimate this capacitor value

$$C_Z > \frac{4}{2\pi \times R_Z \times f_c} \quad (26)$$

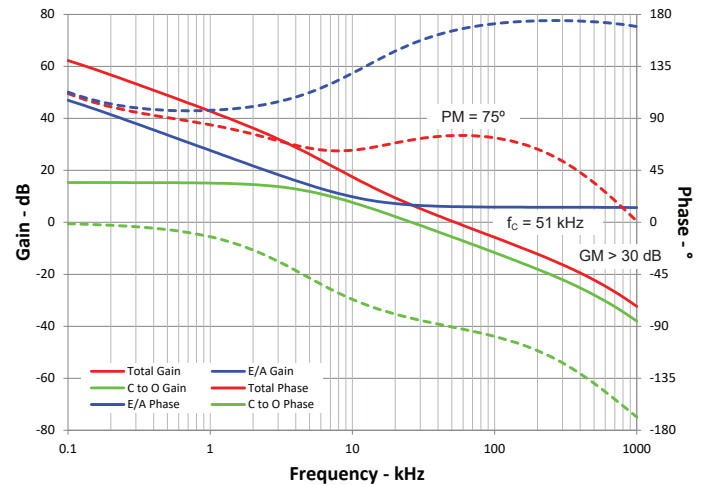
Determine if the second compensation capacitor ( $C_P$ ) is required. It is required if the ESR zero of the output capacitor is located at less than half of the switching frequency or the following relationship is valid:

$$\frac{1}{2\pi \times C_O \times \text{ESR}_{CO}} < \frac{f_{\text{SW}}}{2} \quad (27)$$

If this is the case, then add the second compensation capacitor ( $C_P$ ) to set the pole at the location of the ESR zero. Determine the  $C_P$  value by the equation:

$$C_P = \frac{C_{\text{OUT}} \times \text{ESR}}{R_Z} \quad (28)$$

Finally, we take a look at the combined bode plot of both the control-to-output and the compensated error amp—see the red curves shown in Figure 16. The bandwidth of this system ( $f_c$ ) is 51 kHz, the phase margin is  $75^\circ$ , and the gain margin is  $> 30$  dB.



**Figure 16: Bode Plot of the Complete System (red curve)**  
 $R_Z = 2.74 \text{ k}\Omega$ ,  $C_Z = 4.7 \text{ nF}$ ,  $C_P = 10 \text{ pF}$   
 $L_O = 10 \text{ }\mu\text{H}$ ,  $C_O = 10 \text{ }\mu\text{F}$  Ceramic

## Synchronous Buck Soft-Start and Hiccup Mode Timing

The soft-start time of the synchronous buck is determined by the value of the capacitance at the soft-start pin,  $C_{\text{SS2}}$ .

If the A4412 is starting into a very heavy load, a very fast soft-start time may cause the regulator to exceed the pulse-by-pulse overcurrent threshold. To avoid prematurely triggering hiccup mode, the soft-start time,  $t_{\text{SS2}}$ , should be calculated according to equation 29,

$$t_{\text{SS2}} = V_{\text{SYNC\_BUCK}} \times \frac{C_O}{I_{\text{CO}}} \quad (29)$$

Where  $V_{\text{SYNC\_BUCK}}$  is the output voltage,  $C_O$  is the output capacitance,  $I_{\text{CO}}$  is the amount of current allowed to charge the output capacitance during soft-start (recommend  $20 \text{ mA} < I_{\text{CO}} < 30 \text{ mA}$ ). Higher values of  $I_{\text{CO}}$  result in faster soft-start time and lower values of  $I_{\text{CO}}$  ensure that hiccup mode is not falsely triggered. We recommend starting the design with an  $I_{\text{CO}}$  of 20 mA and increasing it only if the soft-start time is too slow.

Then  $C_{\text{SS2}}$  can be selected based on equation 30,

$$C_{\text{SS2}} > \frac{\text{ISS2}_{\text{SU}} \times t_{\text{SS1}}}{0.8} \quad (30)$$

If a non-standard capacitor value for  $C_{\text{SS2}}$  is calculated, the next larger value should be used.

The voltage at the soft-start pin will start from 0 V and will be

charged by the soft-start current,  $ISS2_{SU}$ . However, PWM switching will not begin instantly because the voltage at the soft-start pin must rise above the soft-start offset voltage ( $VSS2_{OFFS}$ ). The soft start delay ( $t_{SS2,DELAY}$ ) can be calculated using equation 31,

$$t_{SS2,DELAY} = C_{SS2} \times \frac{VSS2_{OFFS}}{ISS2_{SU}} \quad (31)$$

When the A4412 is in hiccup mode, the soft-start capacitor sets the hiccup period. During a startup attempt, the soft-start pin charges the soft-start capacitor with  $ISS2_{SU}$  and discharges the same capacitor with  $ISS2_{HIC}$  between startup attempts.

In applications where the A4412 will be enabled with  $V_{REG} > V_{REGUV,H}$ , the above guidance for  $C_{SS2}$  will not be optimal and could result in output overshoot on  $V_{SYNC\_BUCK}$ . For further information on properly sizing both  $C_{SS1}$  and  $C_{SS2}$  in this event, see the *Pre-Regulator Soft Start and Hiccup Mode Timing ( $C_{SS1}$ )* section of this datasheet.

## Linear Regulators

The five linear regulators only require an ceramic capacitor to ensure stable operation. The capacitor can be any value between 1 and 15  $\mu F$ . A 2.2  $\mu F$  capacitor per regulator is recommended.

Also, since the V5P is used to power remote circuitry, its load can include long cables. The inductance of these cables may cause negative spikes on the V5P pin if a short occurs. It is recommended to use a small diode to clamp this negative spike. A MSS1P5 is recommended.

## Internal Bias (VCC)

The internal bias voltage should be decoupled at the VCC pin using a 1  $\mu F$  ceramic capacitor. It is not recommended to use this pin as a source.

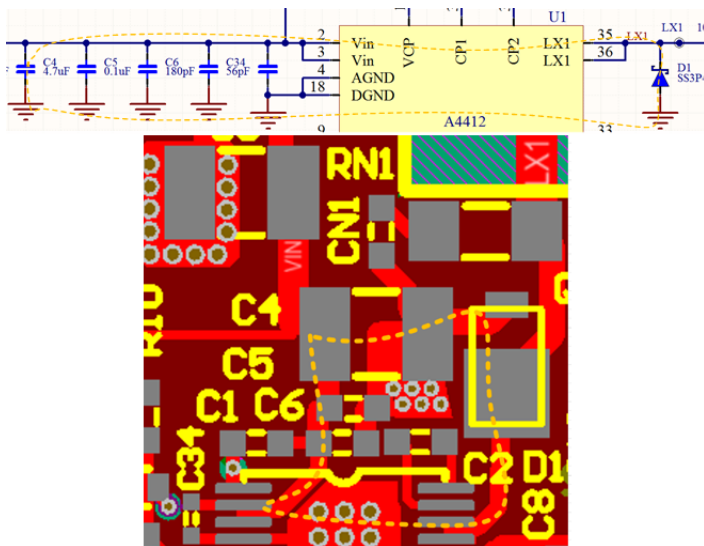
## Signal Pins (NPOR, ENBATs, FFn, POE, DIAG)

The A4412 has many signal level pins. The NPOR, FFn, and ENBATs are open-drain outputs and require external pull-up resistors. The DIAG and POE signals are push-pull outputs and do not require external pull-up resistors.

### PCB LAYOUT RECOMMENDATIONS

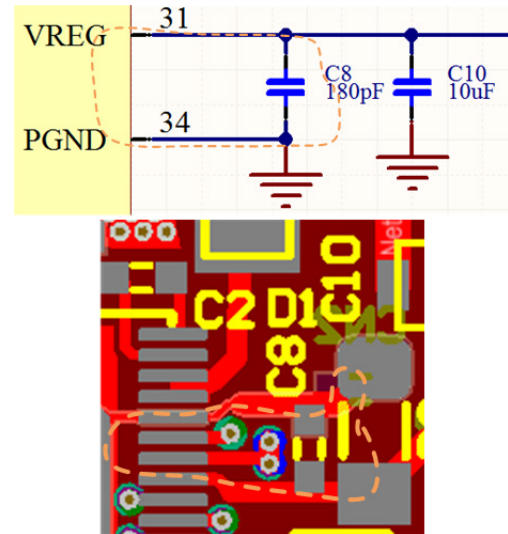
The input ceramic capacitors must be located as close as possible to the VIN pins. In general, the smaller capacitors (0402, 0603) must be placed very close to the VIN pin. The larger capacitors should be placed within 0.5 inches of the VIN pin. There must not be any vias between the input capacitors and the VIN pins.

The pre-regulator input ceramic capacitors, A4412 VIN and LX1, and asynchronous diode (D1), must be routed on one layer. This loop should be as small as possible, see below. The snubber (RN1 and CN1) should be placed close to D1. A single star point ground connected to the ground plane using multiple vias is recommended.



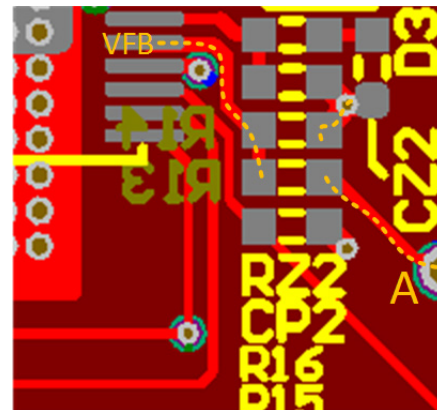
The pre-regulator output inductor (L1) should be located close to the LX1 pins. The LX1 trace widths (to L1, D1) should be relatively wide and preferably on the same layer as the IC.

The pre-regulators output ceramic capacitors should be located near the VREG pin. There must be 1 or 2 smaller ceramic capacitors as close as possible to the VREG pin.



The synchronous buck output inductor should be located near the LX2 pins. The trace from the LX2 pins to the output inductor (L2) should be relatively wide and preferably on the same layer as the IC.

The two synchronous buck feedback resistors (RFB1, RFB2) must be located near the FB pin. The output capacitors should be located near the load. The output voltage sense trace (to RFB1) must connect at the load for the best regulation, trace A in figure below goes to load.

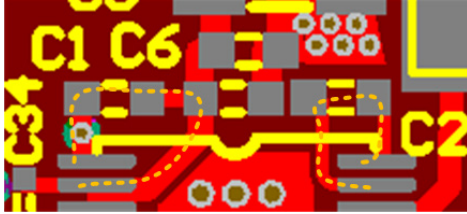




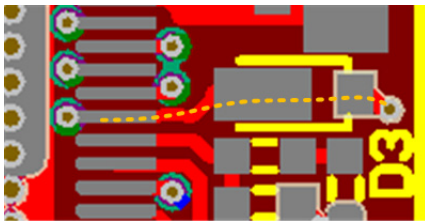
# A4412

## Buck or Buck/Boost Pre-Regulator with Synchronous Buck, 5 Internal Linear Regulators, Pulse-Width Watchdog Timer, and SPI

The two charge pump capacitors must be placed as close as possible to VCP and CP1/CP2.

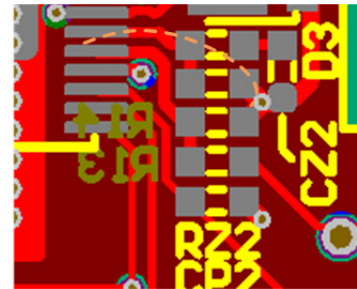
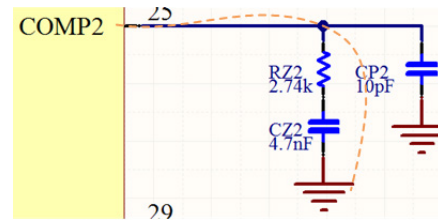
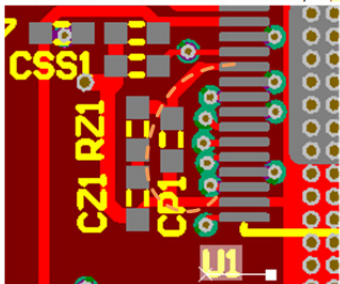
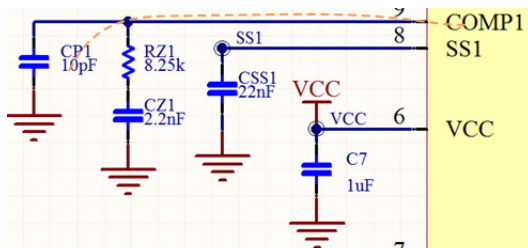


The ceramic capacitors for the LDOs (3V3, V5A, V5B, V5P, and V5CAN) must be placed near their output pins. The V5P output must have a 1 A / 40 V Schottky diode (D3) located very close to its pin to limit negative voltages.

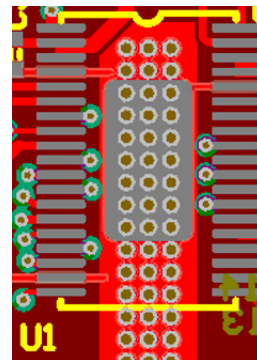


The VCC bypass capacitor must be placed very close to the VCC pin.

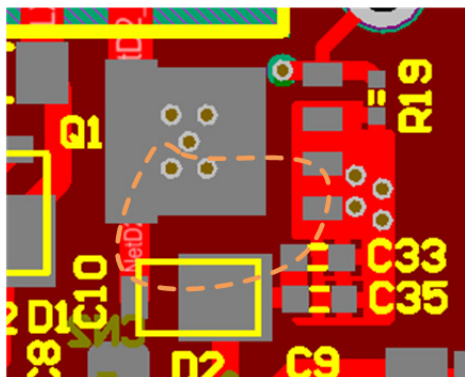
The COMP network for both buck regulators (CZx, RZx, CPx) must be located very close to the COMPx pin.



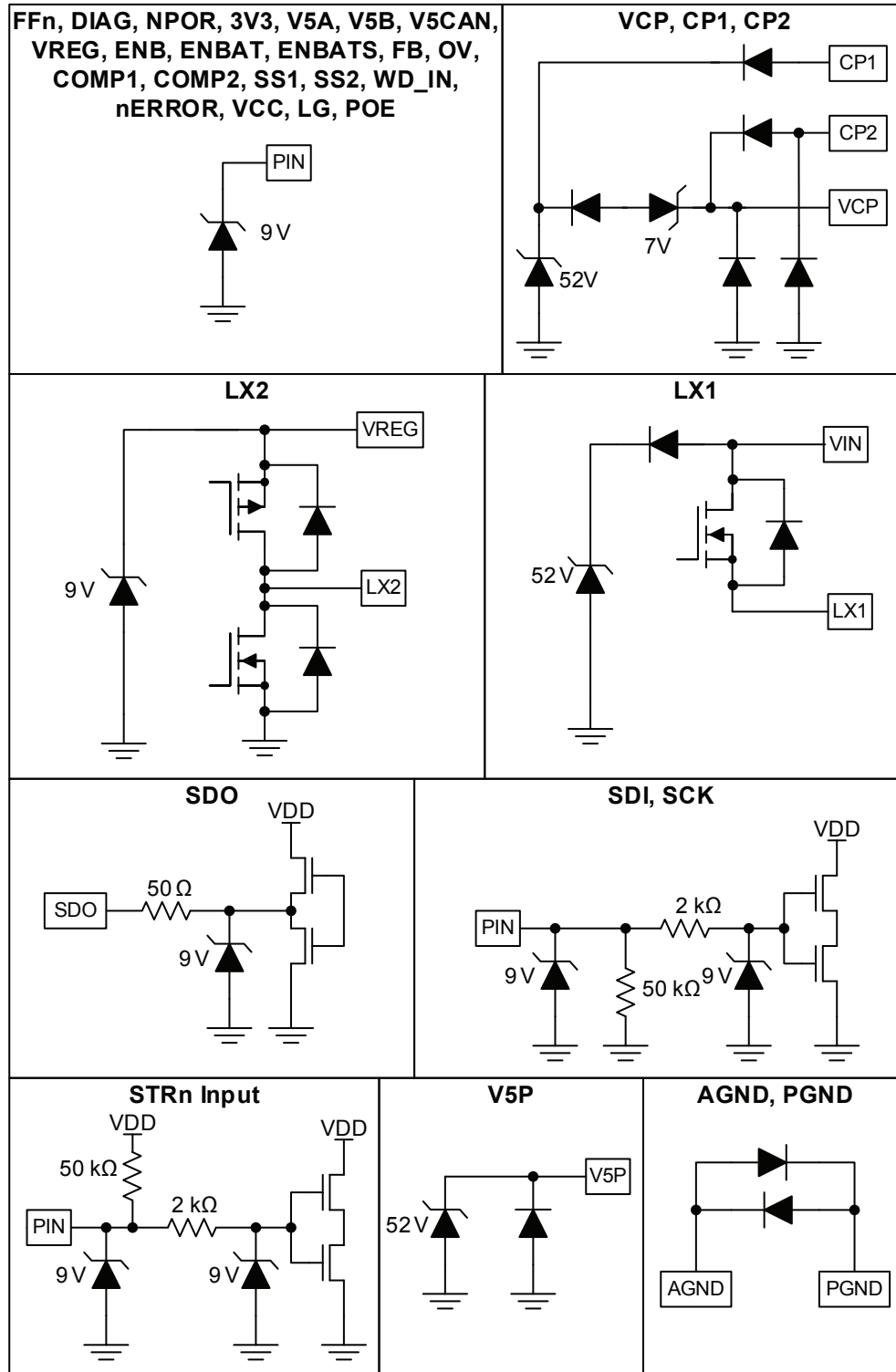
The thermal pad under the A4412 must connect to the ground plane(s) with multiple vias.



## Buck or Buck/Boost Pre-Regulator with Synchronous Buck, 5 Internal Linear Regulators, Pulse-Width Watchdog Timer, and SPI



## INPUT/OUTPUT STRUCTURES



## PACKAGE OUTLINE DRAWING

### For Reference Only – Not for Tooling Use

(Reference Allegro DWG-0000379, Rev. 3 and JEDEC MO-153 BDT-1)

Dimensions in millimeters

NOT TO SCALE

Dimensions exclusive of mold flash, gate burrs, and dambar protrusions

Exact case and lead configuration at supplier discretion within limits shown

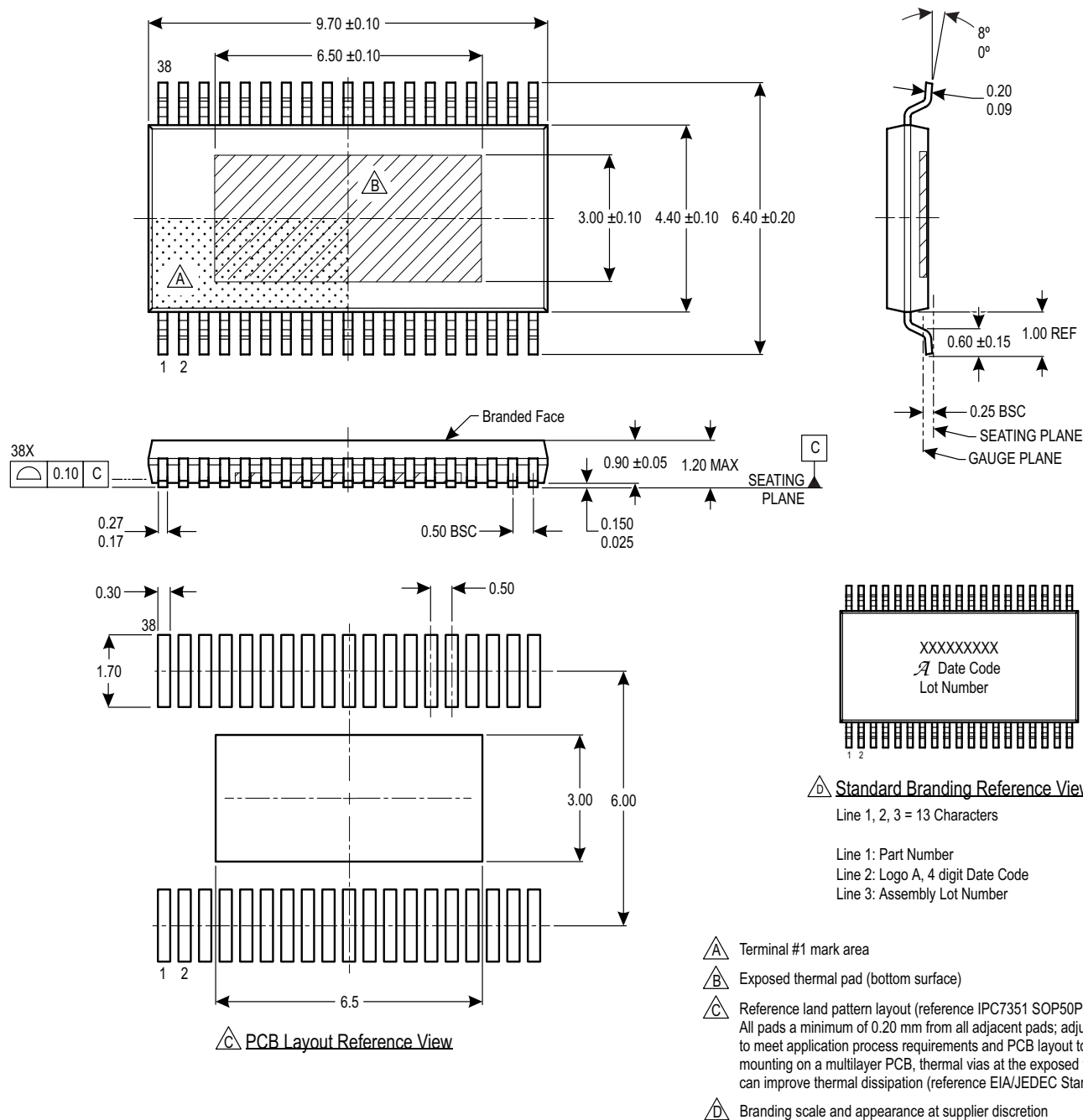


Figure 30: Package LV, 38-Pin eTSSOP

## Revision History

Number	Date	Description
–	March 22, 2017	Initial release
1	June 28, 2017	Added Table of Contents (page 3); updated Synchronous Buck FB UV Thresholds (page 14) and Input/Output Structures (page 51)
2	July 5, 2018	Minor editorial updates
3	April 23, 2019	Updated Functional Block Diagrams (page 6), Figure 13 (page 44), and Figure 16 (page 46).
4	August 13, 2019	Updated Synchronous Buck FB UV Thresholds minimum values (page 15), Equation 2 (page 41), Equation 6 and 10 (page 42).
5	May 20, 2020	Corrected V5B Overvoltage fault type (page 24).
6	August 27, 2020	Updated Functional Block Diagram (page 4) and Equation 22 (page 45).
7	February 9, 2021	Added guidance on soft-start capacitor selection (pages 44, 47).
8	February 8, 2022	Updated package drawing (page 52)
9	April 15, 2022	Updated Pulse-by-Pulse Current Limit maximum value (pages 10-11), Reference Voltage minimum value, and High-Side MOSFET Minimum Off-Time maximum value (page 11)
10	May 16, 2025	Editorial update of ASIL language and logo (page 1)

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