2-BITS BIDIRECTIONAL LEVEL TRANSLATOR OPEN-DRAIN AND PUSH-PULL APPLICATIONS

Description

The LSF0102 is a 2-channel bidirectional multi-voltage level translator for open-drain and push-pull applications. This device is a universal level translator that A port operates from 0.65V to 4.5V (Vref_A) and B port 1.8V to 5.5V (Vref_B). This range allows for bidirectional voltage translations between 0.65V and 5.0V. Be aware that Vref_B is recommended to be at 1.0V higher than Vref_A for best signal integrity.

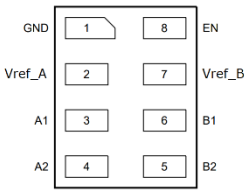
The EN pin is used to activate the device. When EN is HIGH, the translator switch is on. Otherwise, EN is LOW, the translator switch is off, and a high-impedance state exists between ports. The EN input circuit is designed to be supplied by Vref_B via an external Rpu (pull-up resistor, typ. 200kΩ) and The EN must be LOW during power-up or power-down to avoid miss operation.

Be aware that external Rpu (pull-up resistor) is required on each signal in both A and B ports for push-pull application because a pull-high state can avoid miss operation during power-up or power-down. As same as open-drain application, the smaller Rpu results in the larger driving current. For bidirectional signal flows, there is no need for a direction pin to minimize system effort. This device supports 5V tolerant I/O pins in a variety of applications which require different voltage translation levels.

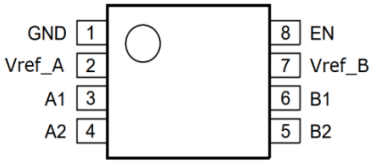
Features

- External Rpu (pull-up resistor) sets driving current in both push-pull and open-drain applications
- Maximum data rate is dominated by the system capacitance and pull-up resistors
  - ≤ 100MHz; C_L = 15pF, 30pF, R_{PU} <= 300Ω
  - ≤ 50MHz; C_L = 50pF, R_{PU} <= 300Ω
- Bidirectional voltage level translation between:
  - 0.65V and 1.5V, 1.8V, 2.5V, 3.3V and 5.0V
  - 1.2V and 1.8V, 2.5V, 3.3V and 5.0V
  - 1.8V and 2.5V, 3.3V and 5.0V
  - 2.5V and 3.3V and 5.0V
  - 3.3V and 5.0V
- ESD Protection Exceeds JESD 22
  - 4000V HBM (A114)
  - 1500V CDM (C101)
- Latch-up Exceeds 100mA per JESD 17
- Specified from -40°C to +125°C
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
  For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/104/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please contact us or your local Diodes representative.
  https://www.diodes.com/quality/product-definitions/

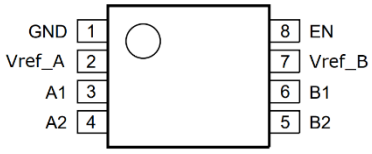
Pin Assignments



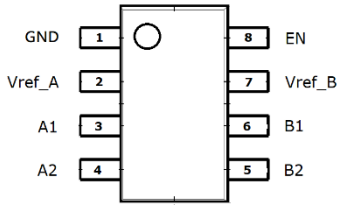
X2-DFN1410-8



SSOP-8



VSSOP-8



SOT28

Applications

- GPIO, MDIO, SDIO, SVID, UART
- PMBus, SMBus, I2C, and other interfaces
- Telecom infrastructure
- Industrial
- High performance computing
- Wide array of products such as:
  - PCs, networking, notebooks
  - Smart phones
  - Tablet

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

Pin Descriptions

Pin Name	X2-DFN1418-8	SSOP-8	VSSOP-8	SOT28	Function
GND	1	1	1	1	Ground
V_{ref_A}	2	2	2	2	Reference supply voltage; A port
A1	3	3	3	3	Input/output
A2	4	4	4	4	Input/output
B2	5	5	5	5	Input/output
B1	6	6	6	6	Input/output
V_{ref_B}	7	7	7	7	Reference supply voltage; B port
EN	8	8	8	8	Enable input (active HIGH)

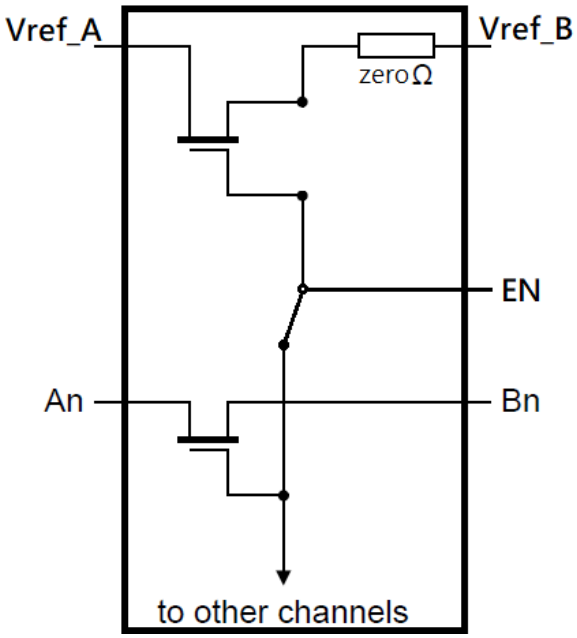
Absolute Maximum Ratings (Note 4)

Symbol	Parameter	Rating	Unit
ESD HBM	Human Body Model ESD Protection	±4	kV
ESD CDM	Charged Device Model ESD Protection	±1.5	kV
V_{REF}	Supply Reference Voltage Range	-0.5 to +6.0	V
V_I	Input Voltage Range	-0.5 to +6.0	V
V_O	Voltage Range Applied to Any Output in the High-Z or Power-Off State	-0.5 to +6.0	V
I_{CH}	Continuous channel current	128	mA
I_{IK}	Input Clamp Current, $V_I < 0$	-50	mA
T_J	Operating Junction Temperature	-40 to +150	°C
T_{STG}	Storage Temperature	-65 to +150	°C

Note: 4. Stresses greater than those listed under *Absolute Maximum Ratings* can cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to *Absolute Maximum Ratings* for extended periods can affect device reliability.

Functional Diagram

NOTE: See load circuit.
EN pin is shorted to Vref_B with an external pull up resistor for gate bias voltage.
Recommend: 200 kΩ



Recommended Operating Conditions

Symbol	Parameter	Min	Max	Units
Vref_A	Reference Voltage, A port	0.65	4.5	V
Vref_B	Reference Voltage, B port, when Vref_A >= 1V	Vref_A + 0.6	5.5	V
	Reference Voltage, B port, when Vref_A < 1V	Vref_A + 0.8	5.5	V
$V_{I/O}$	Input/output Voltage	0	5.5	V
V_{EN}	Enable Voltage when Vref_A >= 1V	Vref_A + 0.6	5.5	V
	Enable Voltage when Vref_A < 1V	Vref_A + 0.8	5.5	V
I_{PASS}	Pass transistor current		64	mA
T_A	Operating Free-Air Temperature	-40	+125	°C

Electrical Characteristics (All typical values are measured at T_A = 25 °C, unless otherwise specified.)

Symbol	Parameter	Test Conditions		Min	Typ	Max	Unit
Vref_A	A port supply voltage	What if config to be low voltage side		0.65		4.5	V
Vref_B	B port supply voltage	What if config to be high voltage side		1.8		5.5	V
V_{IK}	Input clamping voltage	I_I = -18 mA, V_{EN} = 0		–1.2			V
I_L	Leakage current	pins An, Bn, Vref_A, Vref_B and EN; VI = GND to 5.0 V			1.0	5.0	µA
I_{CC}	Supply current	Vref_B = EN = 5.5 V, Vref_A = 4.5 V, I_O = 0, VI = 0V or Vcc			6		µA
$C_{IO(off)}$		V_O = 3 V or 0, EN = 0 V			5	6	
$C_{IO(on)}$		V_O = 3 V or 0, EN = 3 V			10	13	pF
$C_{I(Vref\_A/B/EN)}$		V_O = 3 V or 0			10		pF
V_{IL} (EN)	Device turn-off threshold of EN pin					Vref_A	V
V_{IH} (EN)	Device turn-on threshold of EN pin	When Vref_A >= 1V. See load circuit.		Vref_A+0.6		5.5	V
		When Vref_A < 1V. See load circuit.		Vref_A+0.8		5.5	V
Ron (Note 5)		V_I = 0, I_O = 64 mA	Vref_A = 3.3V; Vref_B = EN = 5V		5		Ω
			Vref_A = 1.8V; Vref_B = EN = 5V		6		
		V_I = 0, I_O = 32 mA	Vref_A = 1.0V; Vref_B = EN = 5V		9		Ω
			Vref_A = 1.8V; Vref_B = EN = 5V		8		
			Vref_A = 2.5V; Vref_B = EN = 5V		6		
		V_I = 1.8V, I_O = 15mA, Vref_A = 3.3V; Vref_B = EN = 5V			8		Ω
		V_I = 1.0V, I_O = 10mA, Vref_A = 1.8V; Vref_B = EN = 3.3V			14		Ω
		V_I = 0V, I_O = 10mA, Vref_A = 1.0V; Vref_B = EN = 3.3V			10		Ω
		V_I = 0V, I_O = 10mA, Vref_A = 1.0V; Vref_B = EN = 1.8V			12		Ω
		V_I = 0V, I_O = 10mA, Vref_A = 0.65V; Vref_B = EN = 1.5V			15		Ω

Note: 5. Measured by the voltage drop between the A and B pins at the indicated current through the switch. On-state resistance is determined by the lowest voltage of the two (A or B) pins.

Translating Down Switching Characteristics (Note 6, T_A = 25°C, unless otherwise specified.)

Translating Down, 5.0V to 1.8V

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C_L = 50pF	C_L = 30pF	C_L = 15pF	UNIT
			TYP	TYP	TYP	
t_{PLH}	B	A	0.4	0.3	0.2	ns
t_{PHL}			1.0	0.7	0.5	ns
Test Conditions : V_{ref_A}= 1.8 V, V_{PU} = V_{IH} = 5.0V, V_M = 2.15V, PRR = 10MHz (unless otherwise noted, see load circuit)						

Translating Down, 3.3V to 1.8V

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C_L = 50pF	C_L = 30pF	C_L = 15pF	UNIT
			TYP	TYP	TYP	
t_{PLH}	B	A	0.4	0.3	0.2	ns
t_{PHL}			1.0	0.7	0.5	ns
Test Conditions : V_{ref_A}= 1.8 V, V_{PU} = V_{IH} = 3.3V, V_M = 1.15V, PRR = 10MHz (unless otherwise noted, see load circuit)						

Translating Down, 3.3V to 1.2V

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C_L = 50pF	C_L = 30pF	C_L = 15pF	UNIT
			TYP	TYP	TYP	
t_{PLH}	B	A	0.6	0.4	0.2	ns
t_{PHL}			1.1	0.8	0.6	ns
Test Conditions: V_{ref_A}= 1.2 V, V_{PU} = V_{IH} = 3.3V, V_M = 0.85V, PRR = 10MHz (unless otherwise noted, see load circuit)						

Translating Down, 1.8V to 1.2V

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C_L = 50pF	C_L = 30pF	C_L = 15pF	UNIT
			TYP	TYP	TYP	
t_{PLH}	B	A	0.8	0.5	0.3	ns
t_{PHL}			1.6	1.4	1.1	ns
Test Conditions: V_{ref_A}= 1.2 V, V_{PU} = V_{IH} = 1.8V, V_M = 0.65V, PRR = 10MHz (unless otherwise noted, see load circuit)						

Translating Down, 1.8V to 0.8V

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C_L = 50pF	C_L = 30pF	C_L = 15pF	UNIT
			TYP	TYP	TYP	
t_{PLH}	B	A	0.8	0.5	0.3	ns
t_{PHL}			1.6	1.2	1.0	ns
Test Conditions: V_{ref_A}= 0.8 V, V_{PU} = V_{IH} = 1.8V, V_M = 0.55V, PRR = 10MHz (unless otherwise noted, see load circuit)						

Translating Down, 1.5V to 0.65V

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C_L = 50pF	C_L = 30pF	C_L = 15pF	UNIT
			TYP	TYP	TYP	
t_{PLH}	B	A	1.0	0.6	0.4	ns
t_{PHL}			1.9	1.5	1.1	ns
Test Conditions: V_{ref_A}= 0.65 V, V_{PU} = V_{IH} = 1.5V, V_M = 0.4V, PRR = 10MHz (unless otherwise noted, see load circuit)						

Translating Up Switching Characteristics (Note 6, T_A = 25°C, unless otherwise specified.)

Translating Up, 1.8 V to 5.0 V

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C_L = 50 pF	C_L = 30 pF	C_L = 15 pF	UNIT
			TYP	TYP	TYP	
t_{PLH}	A	B	0.4	0.3	0.3	ns
t_{PHL}			1.9	1.4	1.0	ns
Test Conditions : V_{IH} = V_{ref_A} = 1.8V, V_{EXT} = V_{PU} = 5.0V, R_L = 300Ω, V_M = 2.05V, PRR = 10MHz (unless otherwise noted, see load circuit)						

Translating Up, 1.8 V to 3.3 V

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C_L = 50 pF	C_L = 30 pF	C_L = 15 pF	UNIT
			TYP	TYP	TYP	
t_{PLH}	A	B	0.4	0.3	0.3	ns
t_{PHL}			1.9	1.4	1.0	ns
Test Conditions : V_{IH} = V_{ref_A} = 1.8V, V_{EXT} = V_{PU} = 3.3V, R_L = 300Ω, V_M = 0.9V, PRR = 10MHz (unless otherwise noted, see load circuit)						

Translating Up, 1.2 V to 3.3 V

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C_L = 50 pF	C_L = 30 pF	C_L = 15 pF	UNIT
			TYP	TYP	TYP	
t_{PLH}	A	B	0.4	0.3	0.2	ns
t_{PHL}			3.2	2.4	1.6	ns
Test Conditions : V_{IH} = V_{ref_A} = 1.2V, V_{EXT} = V_{PU} = 3.3V, R_L = 300Ω, V_M = 0.75V, PRR = 10MHz (unless otherwise noted, see load circuit)						

Translating Up, 1.2 V to 1.8 V

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C_L = 50 pF	C_L = 30 pF	C_L = 15 pF	UNIT
			TYP	TYP	TYP	
t_{PLH}	A	B	0.6	0.3	0.2	ns
t_{PHL}			2.8	2.2	1.6	ns
Test Conditions : V_{IH} = V_{ref_A} = 1.2V, V_{EXT} = V_{PU} = 1.8V, R_L = 300Ω, V_M = 0.6V, PRR = 10MHz (unless otherwise noted, see load circuit)						

Translating Up, 0.8 V to 1.8 V

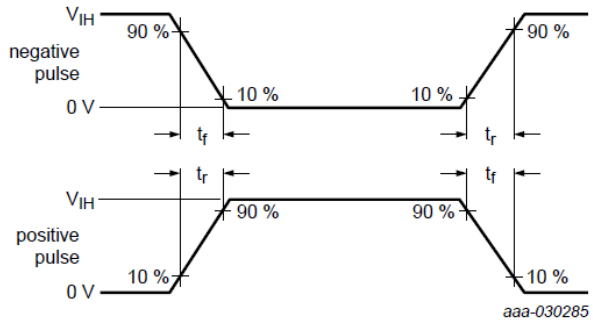
PARAMETER	FROM (INPUT)	TO (OUTPUT)	C_L = 50 pF	C_L = 30 pF	C_L = 15 pF	UNIT
			TYP	TYP	TYP	
t_{PLH}	A	B	0.6	0.3	0.2	ns
t_{PHL}			3.7	2.9	2.1	ns
Test Conditions : V_{IH} = V_{ref_A} = 0.8V, V_{EXT} = V_{PU} = 1.8V, R_L = 300Ω, V_M = 0.55V, PRR = 10MHz (unless otherwise noted, see load circuit)						

Translating Up, 0.65 V to 1.5 V

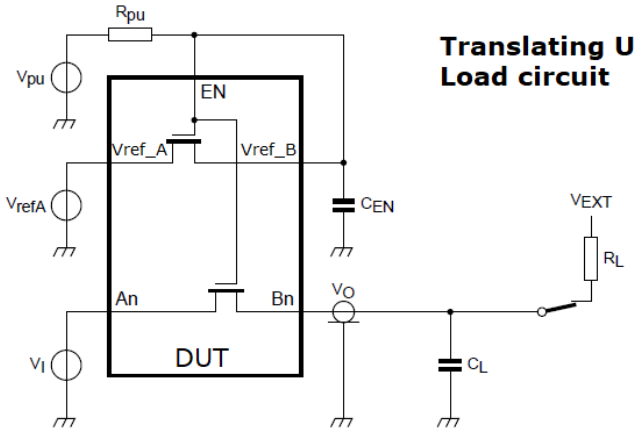
PARAMETER	FROM (INPUT)	TO (OUTPUT)	C_L = 50 pF	C_L = 30 pF	C_L = 15 pF	UNIT
			TYP	TYP	TYP	
t_{PLH}	A	B	0.7	0.3	0.2	ns
t_{PHL}			5.0	3.8	2.7	ns
Test Conditions : V_{IH} = V_{ref_A} = 0.65V, V_{EXT} = V_{PU} = 1.8V, R_L = 300Ω, V_M = 0.4V, PRR = 10MHz (unless otherwise noted, see load circuit)						

Note: 6. All typical values are measured at T_A = 25°C. Logic levels: VOL and VOH are typical output voltage levels that occur with the output load. All input pulses are supplied by generators having the following characteristics: PRR ⩽ 10MHz; ZO = 50Ω. Definitions test circuit: CL = Load capacitance including jig and probe capacitance; RL = Load resistance = 300Ω; Rpu = ext. pull up resistance = 200kΩ

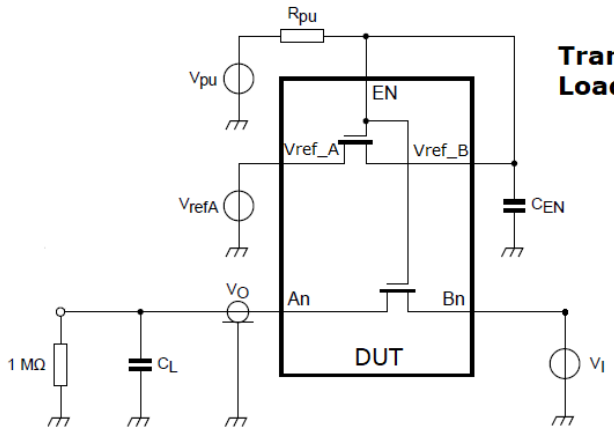
Parameter Measurement Information



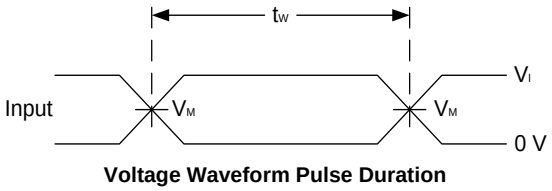
V_I source waveform



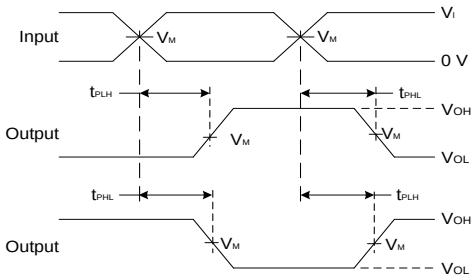
Translating Up Load circuit



Translating Down Load circuit



Voltage Waveform Pulse Duration



Voltage Waveform Propagation Delay Times
Inverting and Non Inverting Outputs

Figure 1. Load Circuit and Voltage Waveforms, Rpu=200kΩ, CEN = 0.1µF, RL=300Ω, CL= 15pF, 30pF, 50pF

Application Circuit Information

I2C or I3C protocol typically occurs in a modern application as shown in Figure 2. For the I2C or I3C voltage translation up or down, consideration should be taken for I3C because it is using higher speeds, which require careful design and attention to signal integrity to ensure reliable communication.

Since I3C uses open-drain mode when necessary for compatibility of I2C, but switches to push-pull outputs whenever possible. The existing I2C devices can be connected to an I3C bus but still have the bus able to switch to a higher data rate for communication at higher speeds between compliant I3C devices. Always refer to the I3C specifications and device datasheets for detailed information and recommendations to ensure reliable communication. Especially at higher speeds, which involve proper PCB layout, termination resistors, and cable selection based on your specific application requirements.

- Standard Data Rate (SDR): This is the default mode of I3C and operates at 11Mbps or 12.5Mbps.
- High Data Rate (HDR): This mode of I3C supports speeds up to 25Mbps where it is further enhanced to reach up to 33Mbps.
- Voltage levels: I3C supports a variety of voltage levels including 1.8V, 2.5V, 3.3V, and 5V.
- Output type: I3C utilizes both open-drain and push-pull outputs for SCL, offering flexibility for different voltage level combinations.
- Rise time and fall time: I3C defines minimum rise and fall times for the SCL signal to ensure proper signal integrity at different speeds.
- SCL is a conventional digital clock signal: driven with a push-pull output by the current bus controller during data transfers. When communication with known I3C targets occurs, the bus controller may switch to a higher frequency and/or alter the duty cycle.
- SDA carries the serial data stream: which may be driven by either a controller or target, but is driven at a rate determined by the controller's SCL signal. For compatibility with the I2C protocol, each transaction begins with SDA operating as an open-drain output, which limits the transmission speed. For messages addressed to an I3C target, the SDA driver mode switches to push-pull after the first few bits in the transaction, allowing the clock to be further increased.

Therefore, this presents a challenge with LSF0102 for I3C because the LSF0102 relies on a pull-up resistor to translate the voltage up from the low-voltage side. The pull-up resistor selected shall be not only strong enough to meet the timing requirements, but also not so strong that it violates the VIL requirements of the I3C devices. So, the pull-up resistors are needed on both sides for the normal translation setup. This means that the pull-up resistors are required to pull the bus voltage on the high-voltage side from VPU_1 to VPU_2.

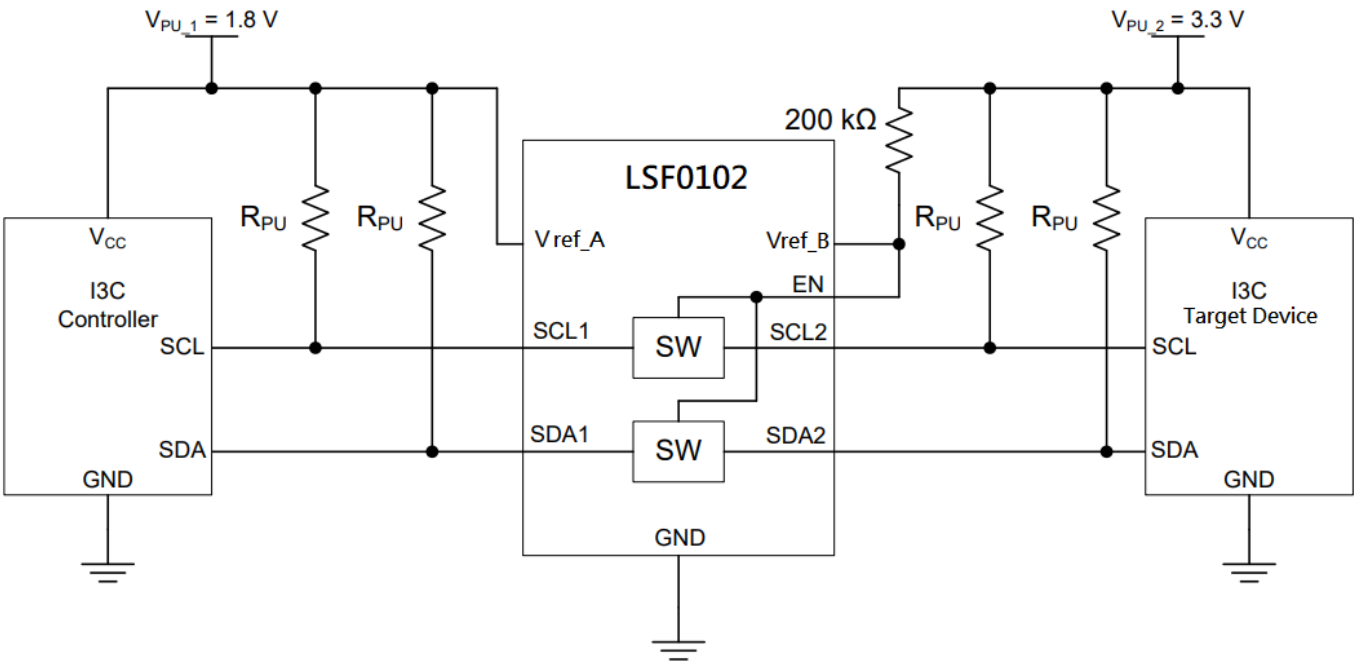


Figure 2. Typical application circuit for I2C or I3C bus voltage translation

Package Characteristics

Symbol	Parameter	Package	Test Conditions	Min	Typ	Max	Unit
θ_{JA}	Thermal Resistance Junction-to-Ambient	X2-DFN1410-8	(Note 7)	—	235	—	°C/W
		SSOP-8		—	202	—	
		VSSOP-8		—	185	—	
		SOT28		—	225	—	
θ_{JC}	Thermal Resistance Junction-to-Case	X2-DFN1410-8	(Note 7)	—	158	—	
		SSOP-8		—	52	—	
		VSSOP-8		—	54	—	
		SOT28		—	121	—	

Note: 7. Test condition for each of the 3 package types: Device mounted on JEDEC standard PCB per JESD51, with minimum recommended pad layout.

Ordering Information

LSF 0102 xx - 7

Family	Numbers	Package	Packing
LSF	2 : 2-bits	HK3 : X2-DFN1410-8 SS8 : SSOP-8 V8 : VSSOP-8 TA8 : SOT28	7 : 7” Tape & Reel 13: 13” Tape & Reel

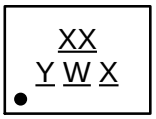
Part Number	Part Number Suffix	Package Code	Package	Packing (Note 8)	
				Qty.	Carrier
LSF0102HK3-7	-7	HK3	X2-DFN1410-8	5,000	7” Tape and Reel
LSF0102SS8-7	-7	SS8	SSOP-8	3,000	7” Tape and Reel
LSF0102V8-7	-7	V8	VSSOP-8	3,000	7” Tape and Reel
LSF0102TA8-7	-7	TA8	SOT28	3,000	7” Tape and Reel

Notes: 8. The taping orientation is located on our website at https://www.diodes.com/assets/Packaging-Support-Docs/ap02007.pdf.
9. For packaging details, go to our website at https://www.diodes.com/design/support/packaging/diodes-packaging/.
10. Pad layout as shown in Diodes Incorporated’s package outline PDFs, which can be found on our website at https://www.diodes.com/design/support/packaging/diodes-packaging/diodes-package-outlines-and-pad-layouts/.

Marking Information

(1) X2-DFN1410-8

(Top View)



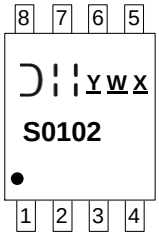
XX : Identification Code
Y : Year : 0~9
W : Week : A~Z : 1~26 week;
a~z : 27~52 week; z represents 52 and 53 week
X : Internal Code

Part Number	Package	Identification Code
LSF0102HK3-7	X2-DFN1410-8	J8

Marking Information (continued)

(2) SSOP-8

(Top View)

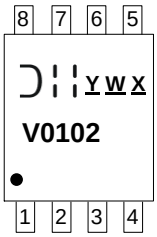


Y : Year : 0 to 9
W : Week : A to Z : 1 to 26 week;
a to z : 27 to 52 week; z represents 52 and 53 week
X : Internal Code

Part Number	Packaging	Identification code
LSF0102SS8-7	SSOP-8	S0102

(3) VSSOP-8

(Top View)

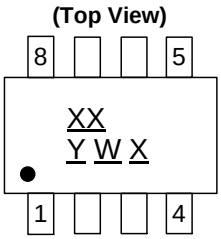


Y : Year : 0 to 9
W : Week : A to Z : 1 to 26 week;
a to z : 27 to 52 week; z represents 52 and 53 week
X : Internal Code

Part Number	Package	Identification Code
LSF0102V8-7	VSSOP-8	V0102

(4) SOT28

(Top View)



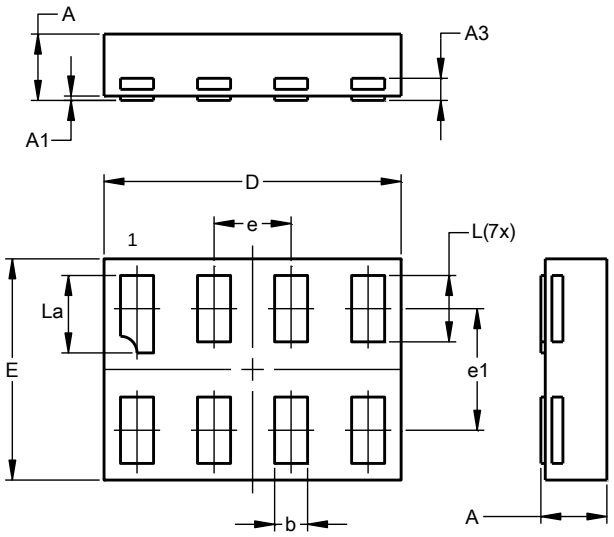
XX : Identification Code
Y : Year 0 to 9
W : Week : A to Z : 1 to 26 week;
a to z : 27 to 52 week; z represents 52 and 53 week
X : Internal Code

Part Number	Package	Identification Code
LSF0102TA8-7	SOT28	J8

Package Outline Dimensions

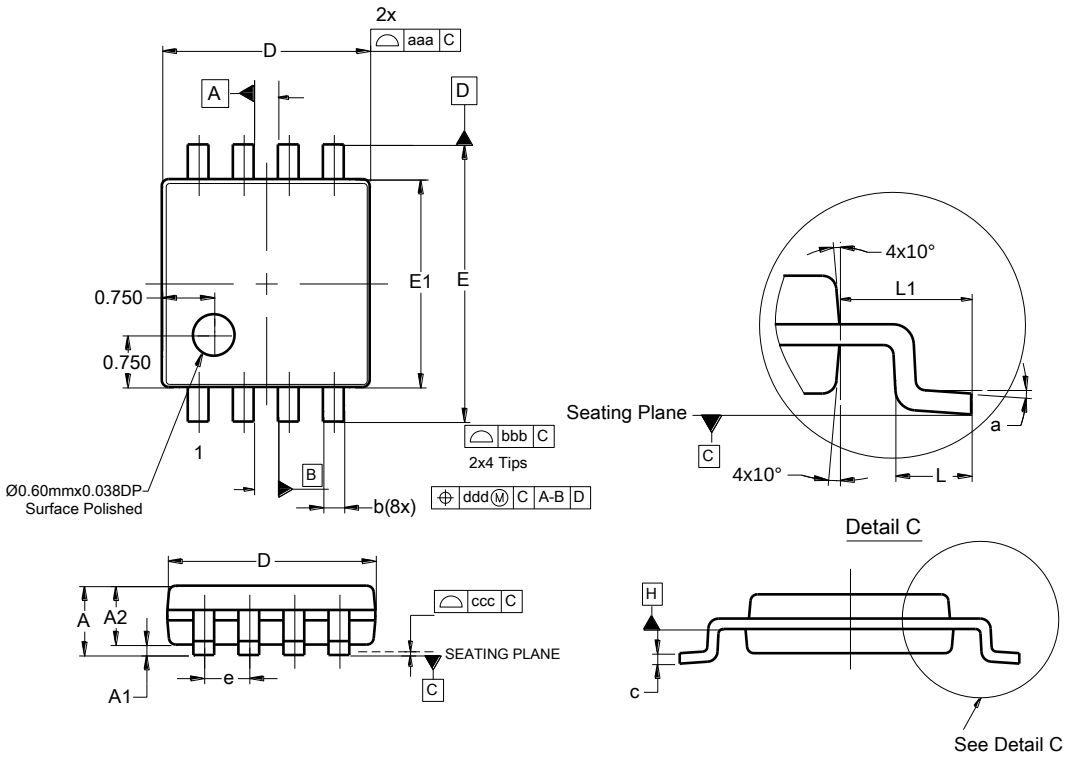
Please see http://www.diodes.com/package-outlines.html for the latest version.

X2-DFN1410-8



X2-DFN1410-8			
Dim	**Min**	**Max**	**Typ**
A	0.30	0.35	0.33
A1	0.00	0.03	0.02
A3	--	--	0.10
b	0.12	0.20	0.15
D	1.30	1.40	1.35
E	0.95	1.05	1.00
e	--	--	0.35
e1	--	--	0.55
L	0.27	0.35	0.30
L1	0.32	0.40	0.35
All Dimensions in mm			

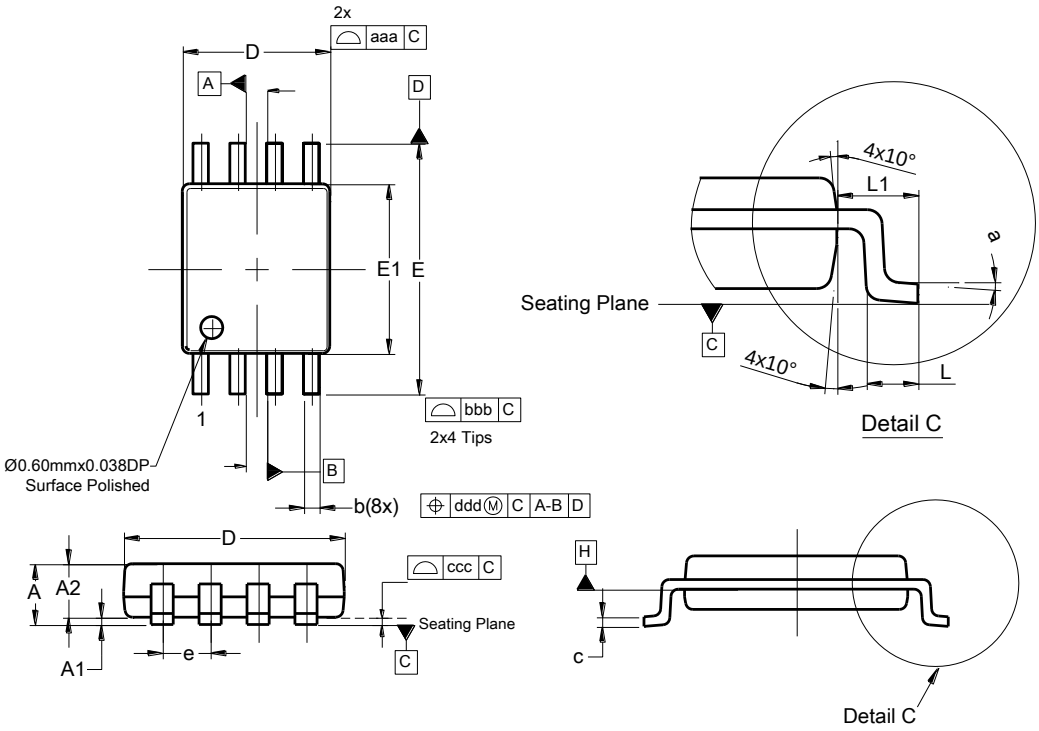
SSOP-8



SSOP-8			
Dim	**Min**	**Max**	**Typ**
A	--	1.30	--
A1	0.05	0.15	--
A2	0.95	1.20	1.05
b	0.15	0.30	0.225
c	0.08	0.23	--
D	2.75	3.15	2.95
E	3.75	4.25	4.00
E1	2.70	2.90	2.80
e	--	--	0.65
L	0.20	0.60	0.40
L1	0.525	0.675	0.60
a	0°	8°	4°
aaa	0.20		
bbb	0.25		
ccc	0.10		
ddd	0.13		
All Dimensions in mm			

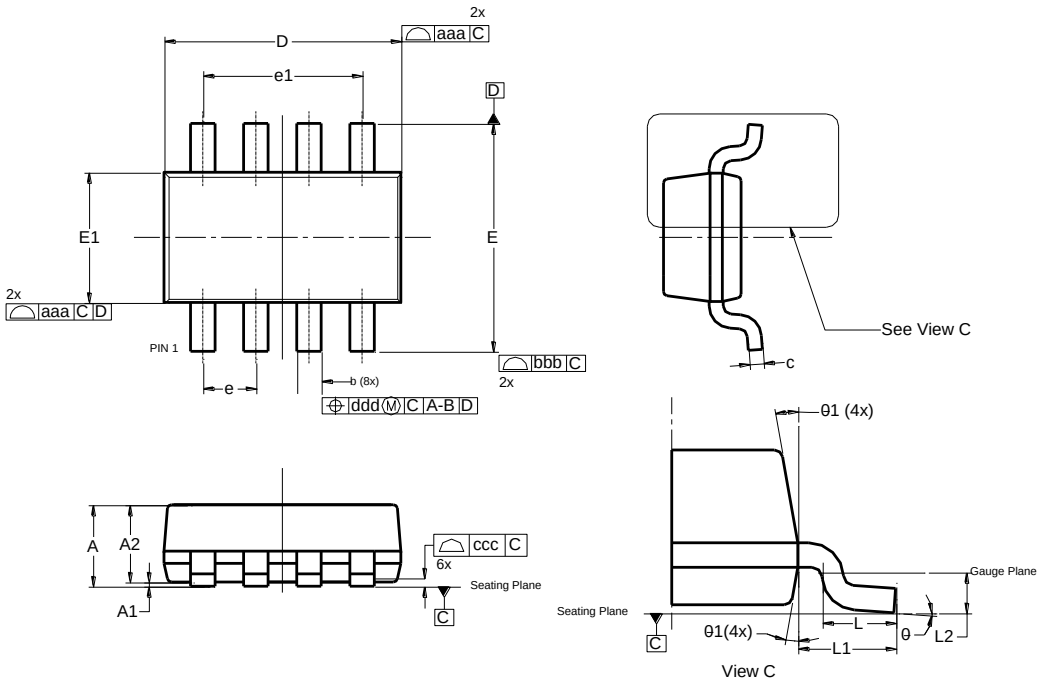
Package Outline Dimensions (continued)

VSSOP-8



VSSOP-8			
Dim	**Min**	**Max**	**Typ**
A	0.60	0.90	--
A1	--	0.10	--
A2	0.60	0.80	--
b	0.17	0.25	0.21
c	0.08	0.13	--
D	1.90	2.10	2.00
E	3.20	3.60	3.40
E1	2.20	2.40	2.30
e	--	--	0.50
L	0.30	0.40	0.35
L1	0.50	0.60	0.55
a	0°	6°	3°
aaa	0.20		
bbb	0.25		
ccc	0.10		
ddd	0.13		
All Dimensions in mm			

SOT28

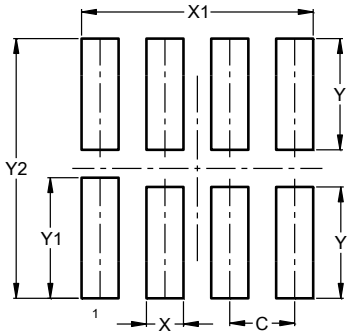


SOT28			
Dim	**Min**	**Max**	**Typ**
A	0.90	1.10	1.00
A1	0.00	0.10	--
A2	--	--	0.95
b	0.20	0.40	0.30
c	0.08	0.20	--
D	2.85	2.95	2.90
E	2.65	2.95	2.80
E1	1.55	1.65	1.60
e	0.65 BSC		
e1	1.95 BSC		
L	0.30	0.60	0.45
L1	0.60 REF		
L2	0.25 BSC		
θ	0°	8°	--
θ1	9°	11°	10°
aaa	0.15		
bbb	0.25		
ccc	0.10		
ddd	0.20		
All Dimensions in mm			

Suggested Pad Layout

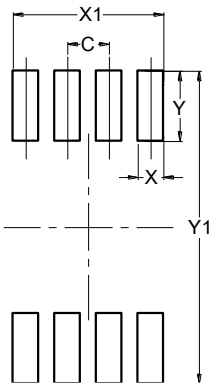
Please see http://www.diodes.com/package-outlines.html for the latest version.

X2-DFN1410-8



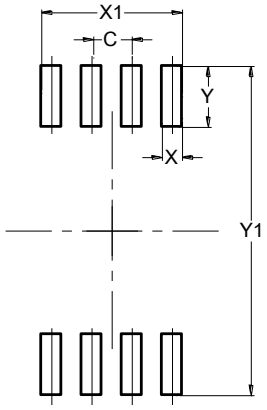
Dimensions	Value (in mm)
C	0.350
X	0.200
X1	1.250
Y	0.600
Y1	0.650
Y2	1.400

SSOP-8



Dimensions	Value (in mm)
C	0.650
X	0.400
X1	2.350
Y	1.100
Y1	4.900

VSSOP-8

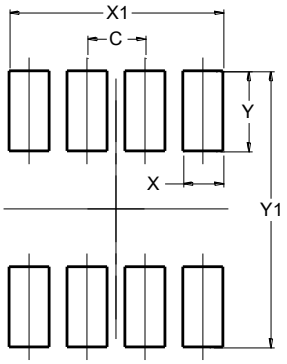


Dimensions	Value (in mm)
C	0.500
X	0.250
X1	1.750
Y	0.750
Y1	4.050

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

SOT28



Dimensions	Value (in mm)
C	0.950
G	1.600
X	0.700
Y	0.900
Y1	3.400

Mechanical Data

X2-DFN1410-8

- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish – Matte Tin Plated Leads, Solderable per MIL-STD-202, Method 208 e3
- Weight: TBD grams (Approximate)
- Max Soldering Temperature +260°C for 30 secs as per JEDEC J-STD-020

SSOP-8

- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish – Matte Tin Plated Leads, Solderable per MIL-STD-202, Method 208 e3
- Weight: TBD grams (Approximate)
- Max Soldering Temperature +260°C for 30 secs as per JEDEC J-STD-020

VSSOP-8

- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish – Matte Tin Plated Leads, Solderable per MIL-STD-202, Method 208 e3
- Weight: TBD grams (Approximate)
- Max Soldering Temperature +260°C for 30 secs as per JEDEC J-STD-020

SOT28

- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish – Matte Tin Plated Leads, Solderable per MIL-STD-202, Method 208 e3
- Weight: TBD grams (Approximate)
- Max Soldering Temperature +260°C for 30 secs as per JEDEC J-STD-020

IMPORTANT NOTICE

1. DIODES INCORPORATED (Diodes) AND ITS SUBSIDIARIES MAKE NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARDS TO ANY INFORMATION CONTAINED IN THIS DOCUMENT, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION).

2. The Information contained herein is for informational purpose only and is provided only to illustrate the operation of Diodes' products described herein and application examples. Diodes does not assume any liability arising out of the application or use of this document or any product described herein. This document is intended for skilled and technically trained engineering customers and users who design with Diodes' products. Diodes' products may be used to facilitate safety-related applications; however, in all instances customers and users are responsible for (a) selecting the appropriate Diodes products for their applications, (b) evaluating the suitability of Diodes' products for their intended applications, (c) ensuring their applications, which incorporate Diodes' products, comply the applicable legal and regulatory requirements as well as safety and functional-safety related standards, and (d) ensuring they design with appropriate safeguards (including testing, validation, quality control techniques, redundancy, malfunction prevention, and appropriate treatment for aging degradation) to minimize the risks associated with their applications.

3. Diodes assumes no liability for any application-related information, support, assistance or feedback that may be provided by Diodes from time to time. Any customer or user of this document or products described herein will assume all risks and liabilities associated with such use, and will hold Diodes and all companies whose products are represented herein or on Diodes' websites, harmless against all damages and liabilities.

4. Products described herein may be covered by one or more United States, international or foreign patents and pending patent applications. Product names and markings noted herein may also be covered by one or more United States, international or foreign trademarks and trademark applications. Diodes does not convey any license under any of its intellectual property rights or the rights of any third parties (including third parties whose products and services may be described in this document or on Diodes' website) under this document.

5. Diodes' products are provided subject to Diodes' Standard Terms and Conditions of Sale (https://www.diodes.com/about/company/terms-and-conditions/terms-and-conditions-of-sales/) or other applicable terms. This document does not alter or expand the applicable warranties provided by Diodes. Diodes does not warrant or accept any liability whatsoever in respect of any products purchased through unauthorized sales channel.

6. Diodes' products and technology may not be used for or incorporated into any products or systems whose manufacture, use or sale is prohibited under any applicable laws and regulations. Should customers or users use Diodes' products in contravention of any applicable laws or regulations, or for any unintended or unauthorized application, customers and users will (a) be solely responsible for any damages, losses or penalties arising in connection therewith or as a result thereof, and (b) indemnify and hold Diodes and its representatives and agents harmless against any and all claims, damages, expenses, and attorney fees arising out of, directly or indirectly, any claim relating to any noncompliance with the applicable laws and regulations, as well as any unintended or unauthorized application.

7. While efforts have been made to ensure the information contained in this document is accurate, complete and current, it may contain technical inaccuracies, omissions and typographical errors. Diodes does not warrant that information contained in this document is error-free and Diodes is under no obligation to update or otherwise correct this information. Notwithstanding the foregoing, Diodes reserves the right to make modifications, enhancements, improvements, corrections or other changes without further notice to this document and any product described herein. This document is written in English but may be translated into multiple languages for reference. Only the English version of this document is the final and determinative format released by Diodes.

8. Any unauthorized copying, modification, distribution, transmission, display or other use of this document (or any portion hereof) is prohibited. Diodes assumes no responsibility for any losses incurred by the customers or users or any third parties arising from any such unauthorized use.

9. This Notice may be periodically updated with the most recent version available at https://www.diodes.com/about/company/terms-and-conditions/important-notice

www.diodes.com