



# PMEG10050ELP

100 V, 5 A low leakage current Schottky barrier rectifier

10 March 2025

Product data sheet

## 1. General description

Planar Schottky barrier rectifier with an integrated guard ring for stress protection, encapsulated in a SOD128 small and flat lead Surface-Mounted Device (SMD) plastic package.

## 2. Features and benefits

- Extremely low leakage current
- High power capability due to clip-bonding technology
- High temperature  $T_j \leq 175$  °C
- Small and flat lead SMD plastic package

## 3. Applications

- Low voltage rectification
- High efficiency DC-to-DC conversion
- Switch mode power supply
- Reverse polarity protection
- Low power consumption applications

## 4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$I_{F(AV)}$	average forward current	$\delta = 0.5$ ; $f = 20$ kHz; square wave; $T_{sp} \leq 148$ °C		-	-	5	A
$V_R$	reverse voltage	$T_j = 25$ °C		-	-	100	V
$V_F$	forward voltage	$I_F = 5$ A; pulsed; $T_j = 25$ °C	[1]	-	780	880	mV
$I_R$	reverse current	$V_R = 100$ V; pulsed; $T_j = 25$ °C	[1]	-	110	450	nA

[1] Very short pulse, in order to maintain a stable junction temperature.

## 5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	K	cathode[1]		
2	A	anode	 CFP5 (SOD128)	

[1] The marking bar indicates the cathode.

**nexperia**

## 6. Ordering information

**Table 3. Ordering information**

Type number	Package		
	Name	Description	Version
PMEG10050ELP	CFP5	plastic, surface mounted package; 2 terminals; 4 mm pitch; 3.8 mm x 2.6 mm x 1 mm body	<a href="#">SOD128</a>

## 7. Marking

**Table 4. Marking codes**

Type number	Marking code
PMEG10050ELP	GM

## 8. Limiting values

**Table 5. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
$V_R$	reverse voltage	$T_j = 25 \text{ }^\circ\text{C}$		-	100	V
$I_{F(AV)}$	average forward current	$\delta = 0.5$ ; $f = 20 \text{ kHz}$ ; square wave; $T_{sp} \leq 148 \text{ }^\circ\text{C}$		-	5	A
$I_{FSM}$	non-repetitive peak forward current	$t_p = 8.3 \text{ ms}$ ; half-sine wave; $T_{j(init)} = 25 \text{ }^\circ\text{C}$		-	70	A
$P_{tot}$	total power dissipation	$T_{amb} \leq 25 \text{ }^\circ\text{C}$	[1]	-	750	mW
			[2]	-	1250	mW
$T_j$	junction temperature			-	175	$^\circ\text{C}$
$T_{amb}$	ambient temperature			-55	175	$^\circ\text{C}$
$T_{stg}$	storage temperature			-65	175	$^\circ\text{C}$

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for cathode  $1 \text{ cm}^2$ .

## 9. Thermal characteristics

**Table 6. Thermal characteristics**

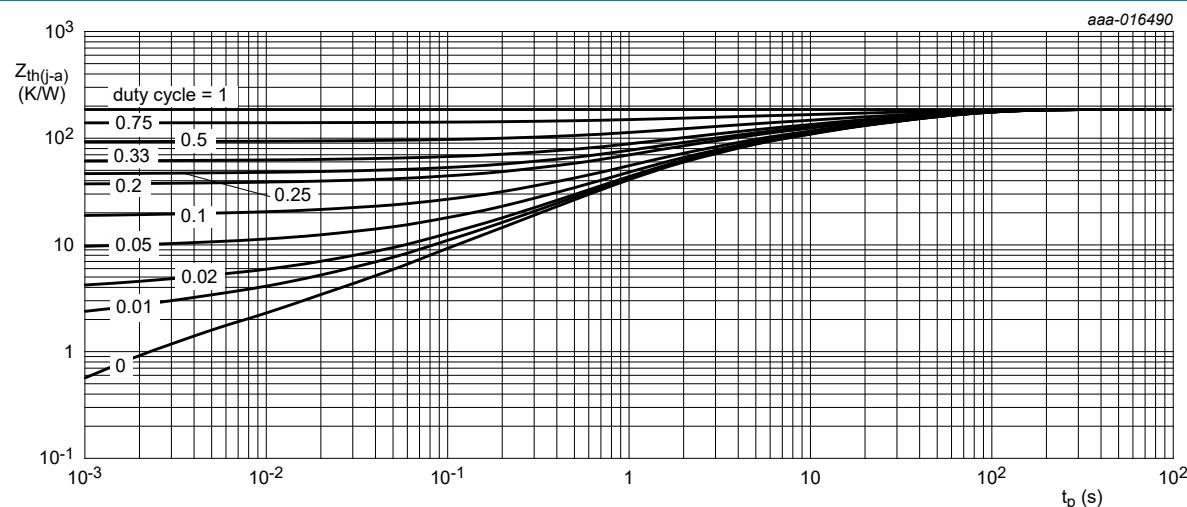
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1] [2]	-	-	200	K/W
			[1] [3]	-	-	120	K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point		[4]	-	-	12	K/W

[1] For Schottky barrier diodes thermal runaway has to be considered, as in some applications the reverse power losses  $P_R$  are a significant part of the total power losses.

[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

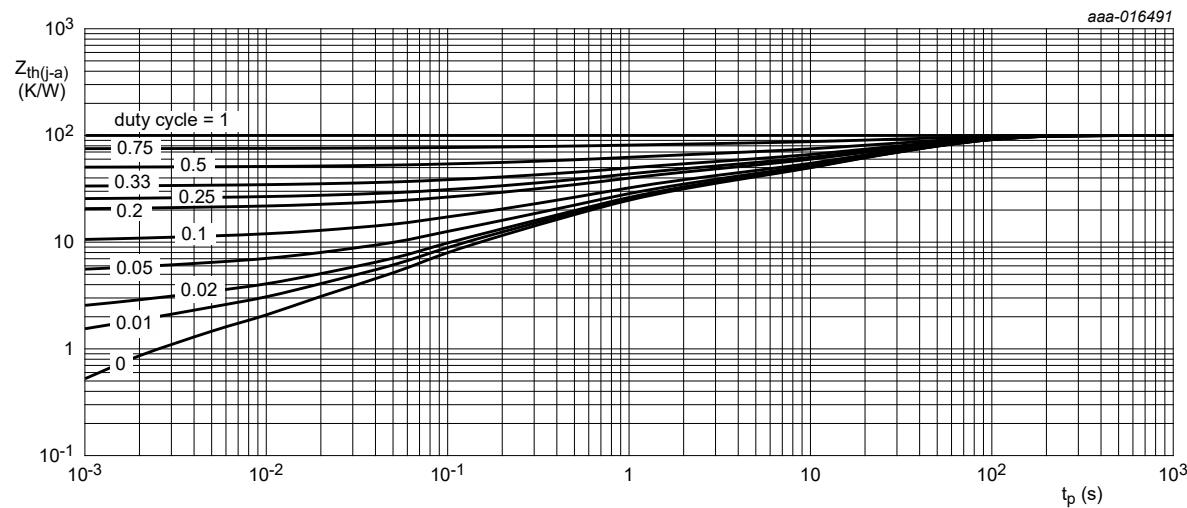
[3] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for cathode 1 cm<sup>2</sup>.

[4] Soldering point of cathode tab.



FR4 PCB, standard footprint

**Fig. 1. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values**



FR4 PCB, mounting pad for cathode 1 cm<sup>2</sup>

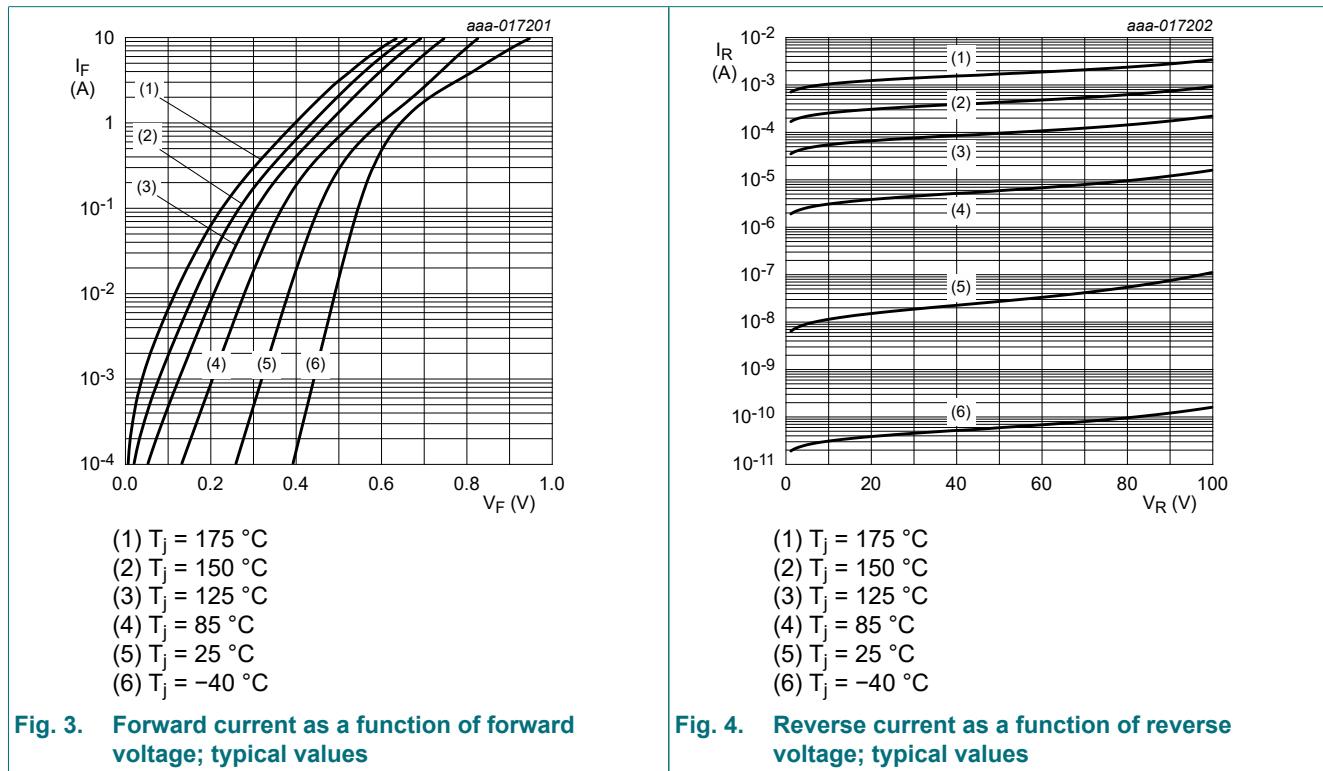
**Fig. 2. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values**

## 10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$V_{(BR)R}$	reverse breakdown voltage	$I_R = 1 \text{ mA}$ ; pulsed; $T_j = 25^\circ\text{C}$	[1]	100	-	-	V
$V_F$	forward voltage	$I_F = 1 \text{ A}$ ; pulsed; $T_j = 25^\circ\text{C}$	[1]	-	600	670	mV
		$I_F = 5 \text{ A}$ ; pulsed; $T_j = 25^\circ\text{C}$	[1]	-	780	880	mV
		$I_F = 5 \text{ A}$ ; pulsed; $T_j = -40^\circ\text{C}$	[1]	-	860	-	mV
		$I_F = 5 \text{ A}$ ; pulsed; $T_j = 125^\circ\text{C}$	[1]	-	650	-	mV
$I_R$	reverse current	$V_R = 60 \text{ V}$ ; pulsed; $T_j = 25^\circ\text{C}$	[1]	-	35	-	nA
		$V_R = 100 \text{ V}$ ; pulsed; $T_j = 25^\circ\text{C}$	[1]	-	110	450	nA
		$V_R = 100 \text{ V}$ ; pulsed; $T_j = 125^\circ\text{C}$	[1]	-	220	1500	$\mu\text{A}$
$C_d$	diode capacitance	$V_R = 1 \text{ V}$ ; $f = 1 \text{ MHz}$ ; $T_j = 25^\circ\text{C}$		-	200	-	pF
		$V_R = 4 \text{ V}$ ; $f = 1 \text{ MHz}$ ; $T_j = 25^\circ\text{C}$		-	120	-	pF
		$V_R = 10 \text{ V}$ ; $f = 1 \text{ MHz}$ ; $T_j = 25^\circ\text{C}$		-	78	-	pF
$t_{rr}$	reverse recovery time ramp recovery	$dI_F/dt = 200 \text{ A}/\mu\text{s}$ ; $I_F = 6 \text{ A}$ ; $V_R = 26 \text{ V}$ ; $T_j = 25^\circ\text{C}$		-	13.4	-	ns
$I_{RM}$	peak reverse recovery current			-	1.35	-	A
$Q_{rr}$	reverse recovery charge			-	10.2	-	nC

[1] Very short pulse, in order to maintain a stable junction temperature.



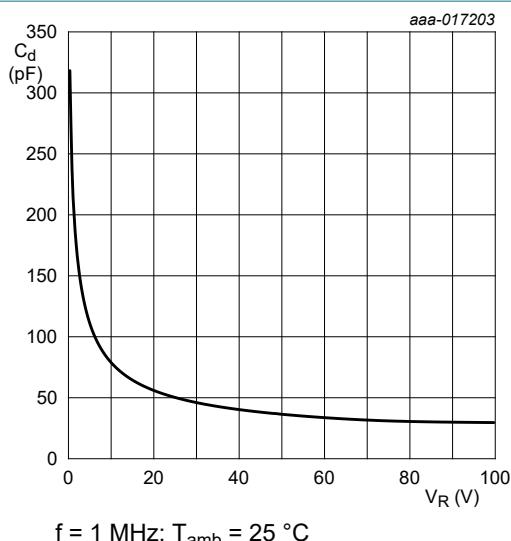


Fig. 5. Diode capacitance as a function of reverse voltage; typical values

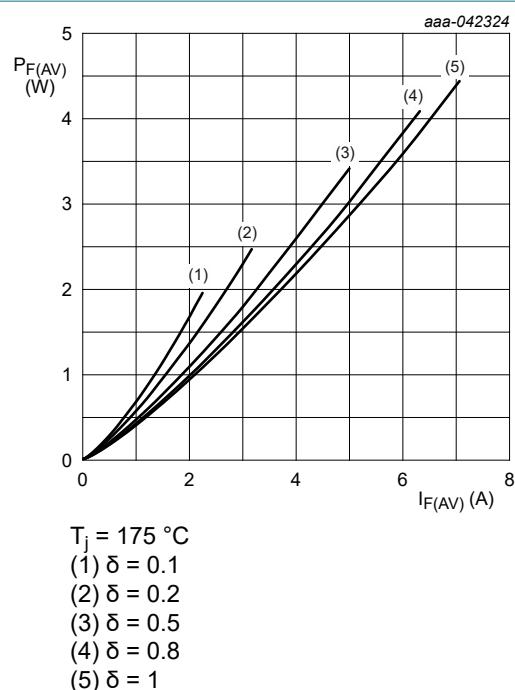


Fig. 6. Average forward power dissipation as a function of average forward current; typical values

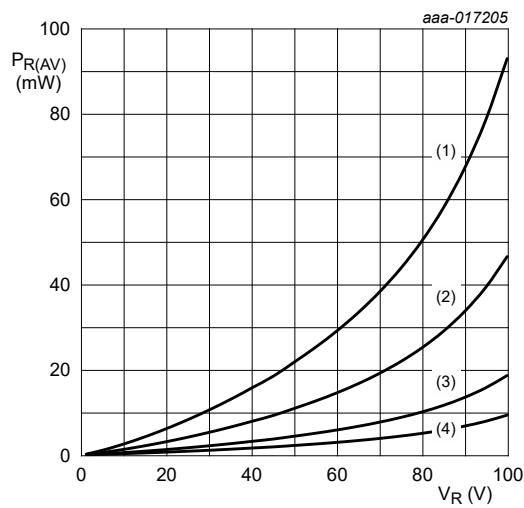


Fig. 7. Average reverse power dissipation as a function of reverse voltage; typical values

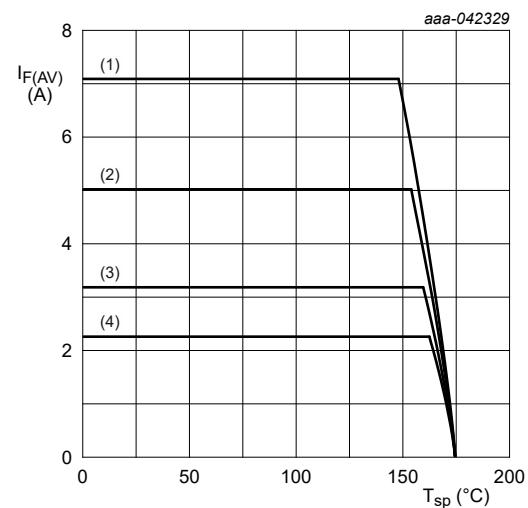


Fig. 8. Average forward current as a function of solder point temperature; typical values

## 11. Test information

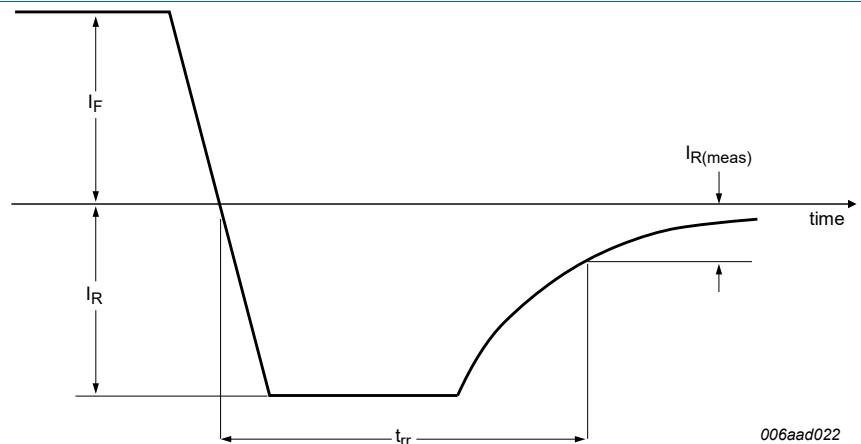


Fig. 9. Reverse recovery definition

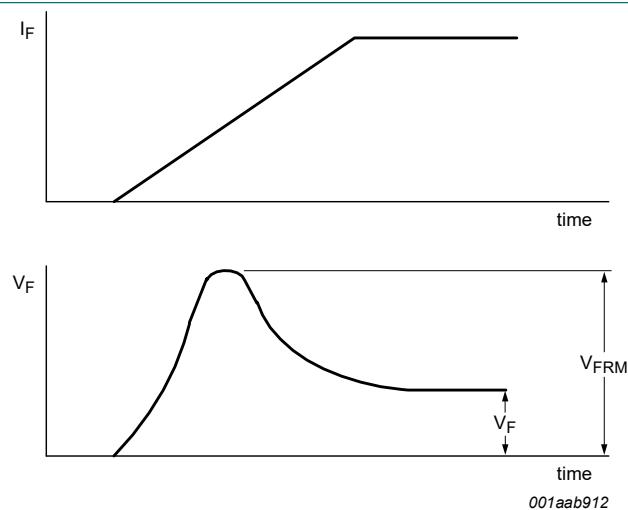


Fig. 10. Forward recovery definition

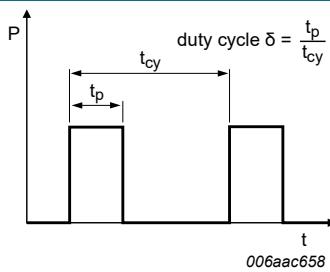


Fig. 11. Duty cycle definition

The current ratings for the typical waveforms are calculated according to the equations:

$$I_{F(AV)} = I_M \times \delta \text{ with } I_M \text{ defined as peak current,}$$

$$I_{RMS} = I_{F(AV)} \text{ at DC,}$$

$$I_{RMS} = I_M \times \sqrt{\delta} \text{ with } I_{RMS} \text{ defined as RMS current.}$$

## 12. Package outline

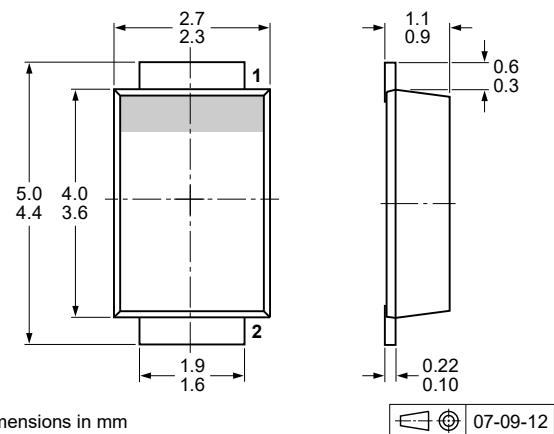


Fig. 12. Package outline CFP5 (SOD128)

## 13. Soldering

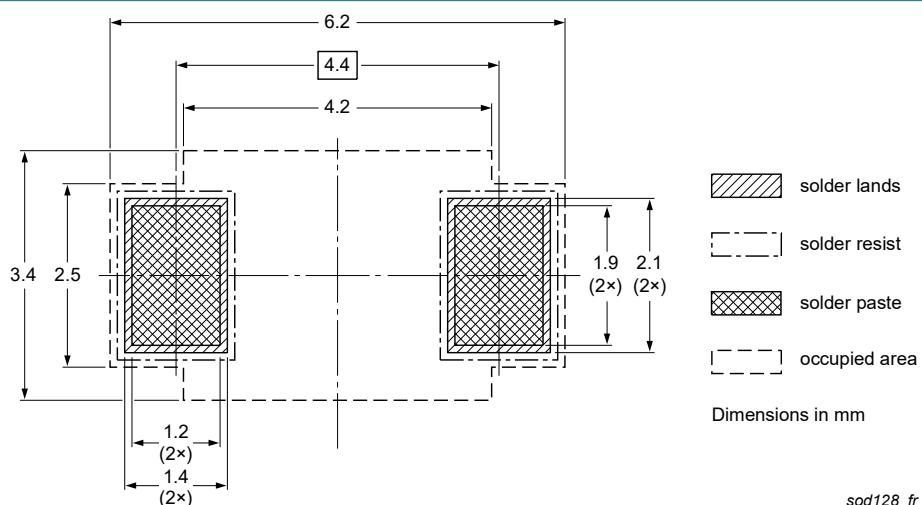
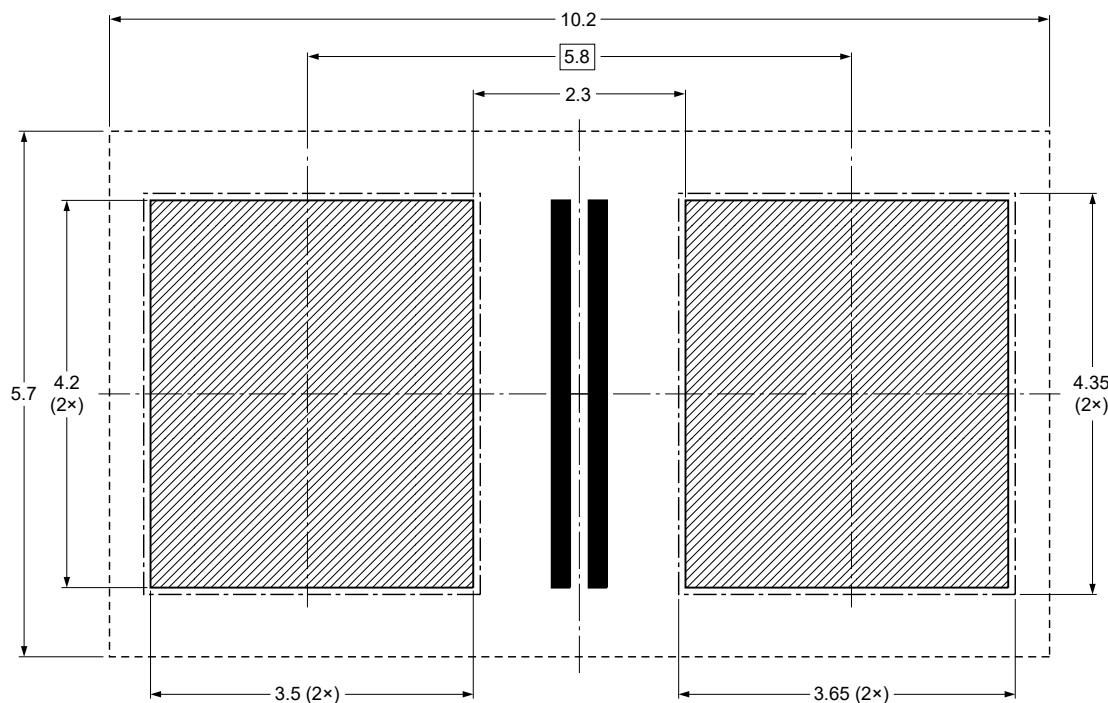


Fig. 13. Reflow soldering footprint for CFP5 (SOD128)

## Wave soldering footprint information

SOD128



occupied area

solder resist

solder lands

dummy track (solder resist and Cu free)

Dimensions in mm

Issue date 17-06-06  
17-06-07

sod128\_fw

Fig. 14. Wave soldering footprint for CFP5 (SOD128)

## 14. Revision history

**Table 8. Revision history**

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PMEG10050ELP v.1	20250310	Product data sheet	-	-

## 15. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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