

E3M0900170D

1700V 900mΩ Silicon Carbide Power MOSFET
N-Channel Enhancement Mode

Features

- High blocking voltage with low on-resistance
- High-speed switching with low capacitances
- 12V...15V/ 0V V_{GS} compatible with most flyback controllers
- Ultra-low drain-gate capacitance
- Qualified to operate under high humidity and high temperature environmental conditions
- Halogen free, RoHS compliant
- Automotive qualified (AEC-Q101) and PPAP capable

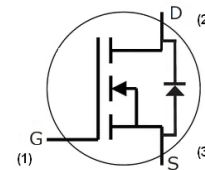
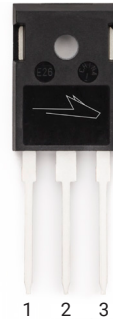
Benefits

- Smooth switching waveforms
- Reduce switching losses and minimize gate ringing
- Higher system efficiency
- Increases system switching frequency
- Increases system reliability

Typical Applications

- Auxillary power supplies
- Switch Mode Power Supplies
- High-Voltage capacitive loads

Package



Orderable Part Number	Package	Marking
E3M0900170D	TO-247-3L	E3M0900170D

Key Parameters

Parameter	Symbol	Min.	Typ.	Max	Unit	Conditions	Note
Drain - Source Voltage	V_{DS}			1700	V	$T_c = 25^\circ\text{C}$	
Maximum Gate - Source Voltage (Transient)	$V_{GS(max)}$	-8		+19		Transient	
Operational Turn-On Gate-Source Voltage	$V_{GS op}$		+12...+15			Static	
Operational Turn-Off Gate-Source Voltage	$V_{GS op}$		-4...0				
DC Continuous Drain Current	I_D			4.4	A	$V_{GS} = 15\text{ V}, T_c = 25^\circ\text{C}, T_J \leq 175^\circ\text{C}$	Note 2
				3.3		$V_{GS} = 15\text{ V}, T_c = 100^\circ\text{C}, T_J \leq 175^\circ\text{C}$	
Pulsed Drain Current	I_{DM}			15		t_{pmax} limited by T_{Jmax} $V_{GS} = 15\text{ V}, T_c = 25^\circ\text{C}$	Fig. 22
Power Dissipation	P_D			41	W	$T_c = 25^\circ\text{C}, T_J = 175^\circ\text{C}$	Fig. 20
Operating Junction and Storage Temperature	T_J, T_{stg}			-55 to +175	$^\circ\text{C}$		
Mounting Torque	M_D			1 8.8	Nm lbf-in	M3 or 6-32 screw	

Note (1): Review application Note PRD-04814 for additional details

Note (2): Verified by design

Electrical Characteristics ($T_c = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions	Note
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	1700			V	$V_{GS} = 0\text{ V}, I_D = 100\text{ }\mu\text{A}$	
$V_{GS(th)}$	Gate Threshold Voltage	1.8	3.1	4.2	V	$V_{DS} = V_{GS}, I_D = 0.55\text{ mA}$	Fig. 11
			2.6		V	$V_{DS} = V_{GS}, I_D = 0.55\text{ mA}, T_J = 175^\circ\text{C}$	
I_{DSS}	Zero Gate Voltage Drain Current		1	50	μA	$V_{DS} = 1700\text{ V}, V_{GS} = 0\text{ V}$	
I_{GSS}	Gate-Source Leakage Current		10	250	nA	$V_{GS} = 15\text{ V}, V_{DS} = 0\text{ V}$	
$R_{DS(on)}$	Drain-Source On-State Resistance		900	1250	m Ω	$V_{GS} = 15\text{ V}, I_D = 1.99\text{ A}$	Fig. 4, 5, 6
			1938			$V_{GS} = 15\text{ V}, I_D = 1.99\text{ A}, T_J = 175^\circ\text{C}$	
g_{fs}	Transconductance		1		S	$V_{DS} = 20\text{ V}, I_{DS} = 1.99\text{ A}$	Fig. 7
			1			$V_{DS} = 20\text{ V}, I_{DS} = 1.99\text{ A}, T_J = 175^\circ\text{C}$	
C_{iss}	Input Capacitance		202		pF	$V_{GS} = 0\text{ V}, V_{DS} = 0\text{ V to }1200\text{ V}$ $F = 100\text{ kHz}$ $V_{AC} = 25\text{ mV}$	Fig. 17, 18
C_{oss}	Output Capacitance		8				
C_{rss}	Reverse Transfer Capacitance		1.4				
E_{oss}	C_{oss} Stored Energy		8		μJ		Fig. 16
$C_{o(er)}$	Effective Output Capacitance (Energy Related)		10		pF	$V_{GS} = 0\text{ V}, V_{DS} = 0\text{ V to }1200\text{ V}$	Note: 3
$C_{o(tr)}$	Effective Output Capacitance (Time Related)		14		pF		
E_{ON}	Turn-On Switching Energy (External Diode)		154		μJ	$V_{DS} = 1200\text{ V}, V_{GS} = -4\text{ V}/15\text{ V}, I_D = 1.99\text{ A},$ $R_{G(ext)} = 2.5\text{ }\Omega, L = 1707\text{ }\mu\text{H}, T_J = 175^\circ\text{C}$ FWD = External SiC DIODE	Fig. 26, 28
E_{OFF}	Turn Off Switching Energy (External Diode)		15				
$t_{d(on)}$	Turn-On Delay Time		23		ns	$V_{DD} = 1200\text{ V}, V_{GS} = -4\text{ V}/15\text{ V}$ $I_D = 1.99\text{ A}, R_{G(ext)} = 2.5\text{ }\Omega, T_J = 175^\circ\text{C},$ $L = 1707\text{ }\mu\text{H}$ Timing relative to V_{DS} Inductive load	Fig. 27, 28
t_r	Rise Time		18				
$t_{d(off)}$	Turn-Off Delay Time		19				
t_f	Fall Time		43				
$R_{G(int)}$	Internal Gate Resistance		31		Ω	$f = 1\text{ MHz}$	
Q_{gs}	Gate to Source Charge		4		nC	$V_{DS} = 1200\text{ V}, V_{GS} = -4\text{ V}/15\text{ V}$ $I_D = 1.99\text{ A}$ Per IEC60747-8-4 pg 21	Fig. 12
Q_{gd}	Gate to Drain Charge		4				
Q_g	Total Gate Charge		10				

Note (3): $C_{o(er)}$, a lumped capacitance that gives same stored energy as C_{oss} while V_{ds} is rising from 0 to 1200V

$C_{o(tr)}$, a lumped capacitance that gives same charging time as C_{oss} while V_{ds} is rising from 0 to 1200V

Reverse Diode Characteristics ($T_c = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Typ.	Max.	Unit	Test Conditions	Note
V_{SD}	Diode Forward Voltage	4.7		V	$V_{GS} = -4\text{ V}, I_{SD} = 1\text{ A}, T_J = 25^\circ\text{C}$	Fig. 8, 9, 10
		4.2		V	$V_{GS} = -4\text{ V}, I_{SD} = 1\text{ A}, T_J = 175^\circ\text{C}$	
I_S	Continuous Diode Forward Current	5.8		A	$V_{GS} = -4\text{ V}, T_c = 25^\circ\text{C}$	
I_{SM}	Diode pulse Current		15	A	$V_{GS} = -4\text{ V}$, pulse width t_p limited by T_{Jmax}	
t_{rr}	Reverse Recover time	40		ns	$V_{GS} = -4\text{ V}, I_{SD} = 1.99\text{ A}, V_R = 1200\text{ V}$ $dif/dt = 3710\text{ A}/\mu\text{s}, T_J = 25^\circ\text{C}$	
Q_{rr}	Reverse Recovery Charge	72		nC		
I_{rrm}	Peak Reverse Recovery Current	3		A		
t_{rr}	Reverse Recover time	40		ns	$V_{GS} = -4\text{ V}, I_{SD} = 1.99\text{ A}, V_R = 1200\text{ V}$ $dif/dt = 1030\text{ A}/\mu\text{s}, T_J = 25^\circ\text{C}$	
Q_{rr}	Reverse Recovery Charge	57		nC		
I_{rrm}	Peak Reverse Recovery Current	2		A		

Thermal Characteristics

Symbol	Parameter	Typ.	Max.	Unit	Test Conditions	Note
$R_{\theta JC}$	Thermal Resistance from Junction to Case	2.8	3.7	$^\circ\text{C}/\text{W}$		Fig. 21

Typical Performance

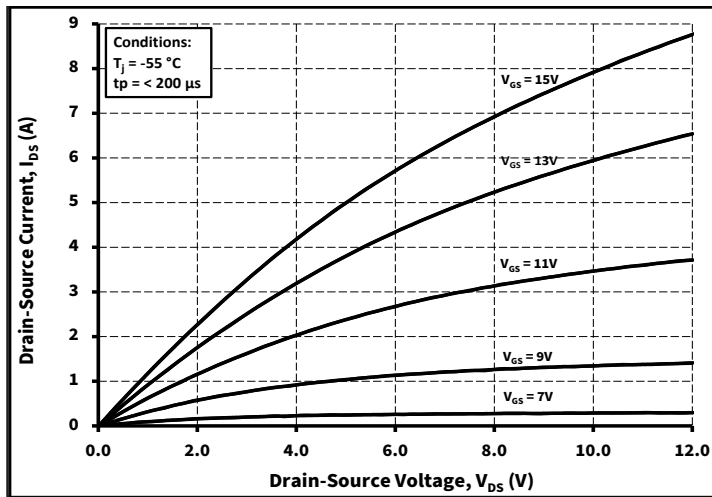
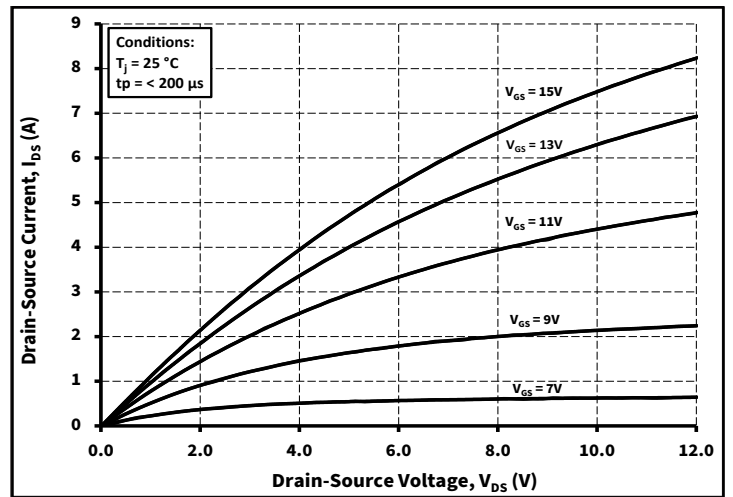
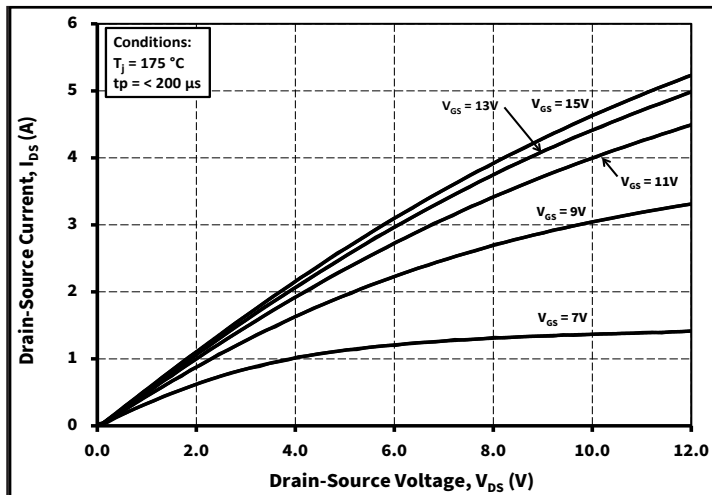
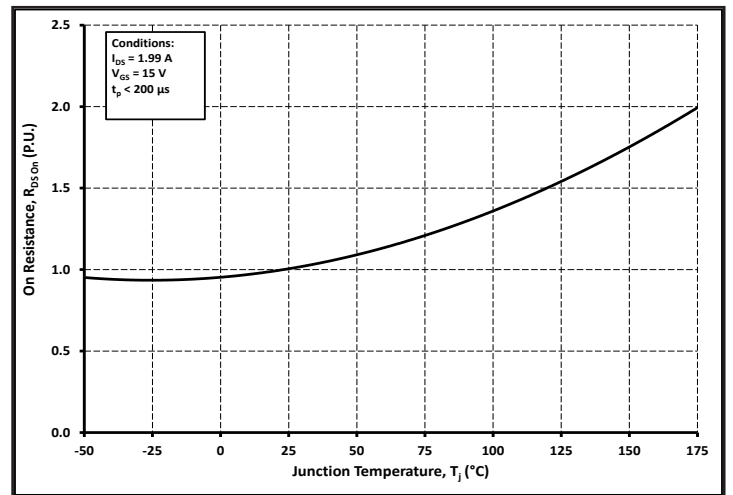
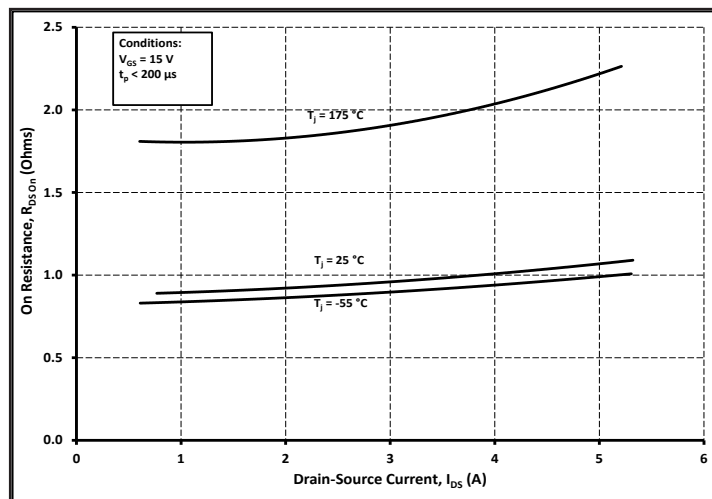
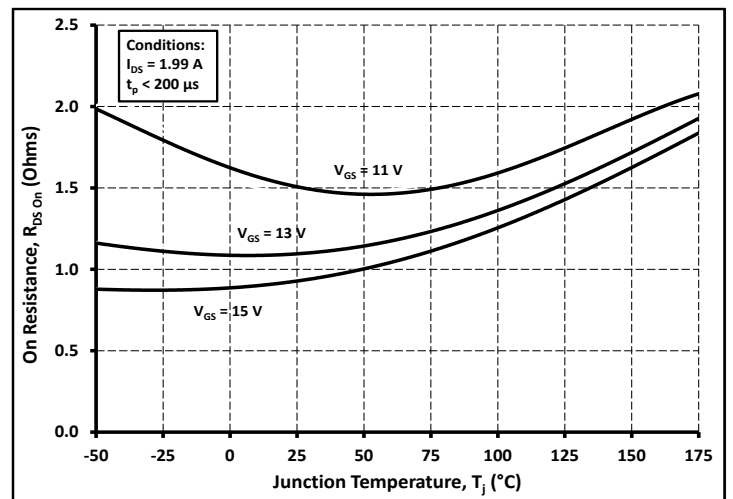
Figure 1. Output Characteristics $T_J = -55\text{ }^{\circ}\text{C}$ Figure 2. Output Characteristics $T_J = 25\text{ }^{\circ}\text{C}$ Figure 3. Output Characteristics $T_J = 175\text{ }^{\circ}\text{C}$ 

Figure 4. Normalized On-Resistance vs. Temperature

Figure 5. On-Resistance vs. Drain Current
For Various TemperaturesFigure 6. On-Resistance vs. Temperature
For Various Gate Voltage

Typical Performance

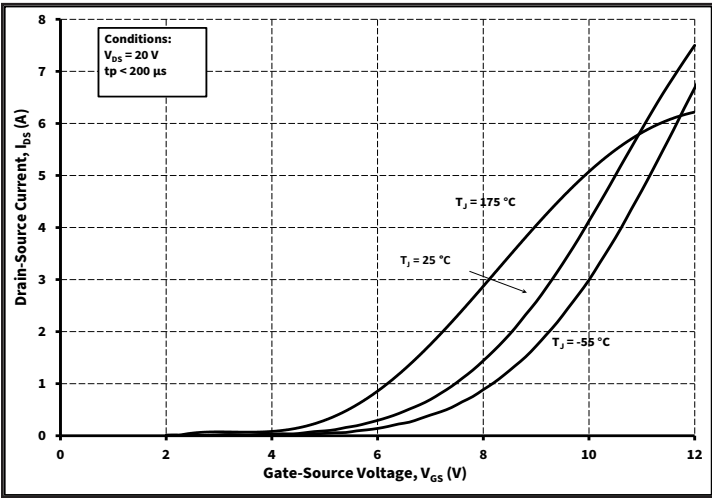


Figure 7. Transfer Characteristic for Various Junction Temperatures

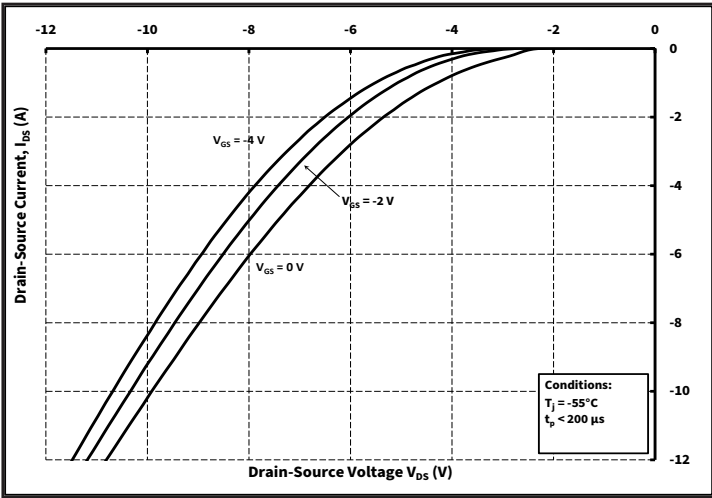


Figure 8. Body Diode Characteristic at $-55\text{ }^{\circ}\text{C}$

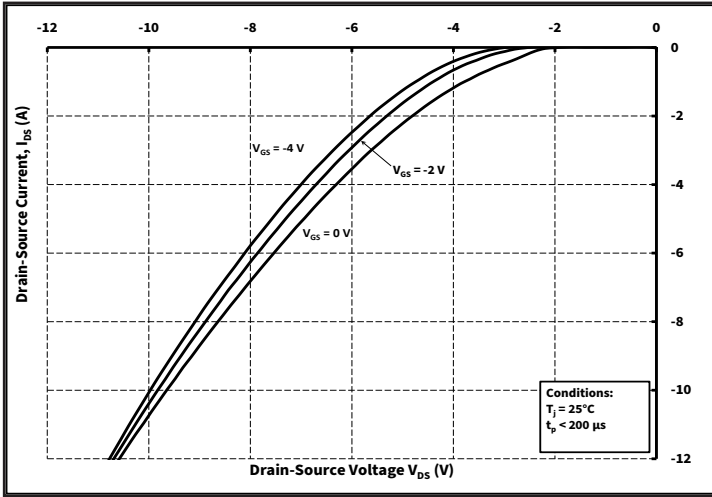


Figure 9. Body Diode Characteristic at $25\text{ }^{\circ}\text{C}$

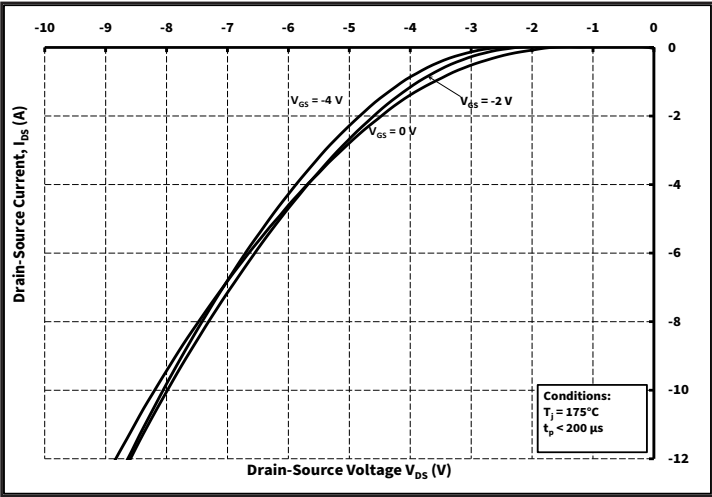


Figure 10. Body Diode Characteristic at $175\text{ }^{\circ}\text{C}$

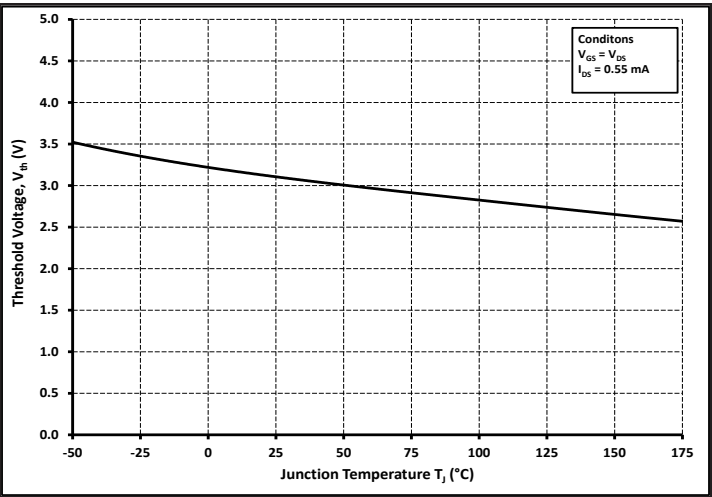


Figure 11. Threshold Voltage vs. Temperature

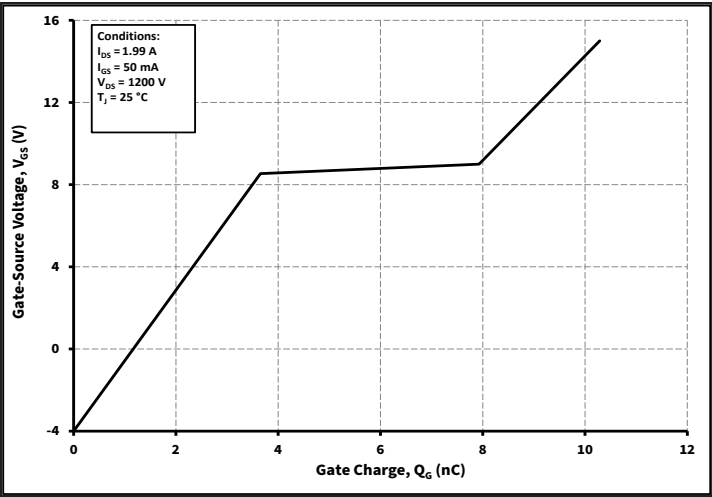


Figure 12. Gate Charge Characteristics

Typical Performance

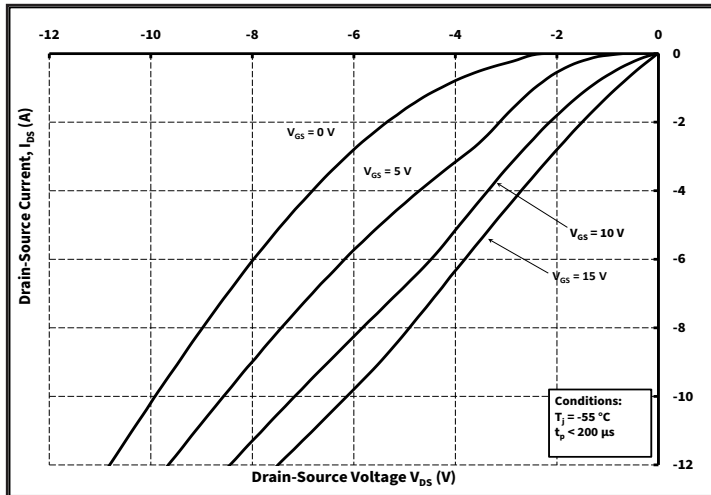


Figure 13. 3rd Quadrant Characteristic at -55 °C

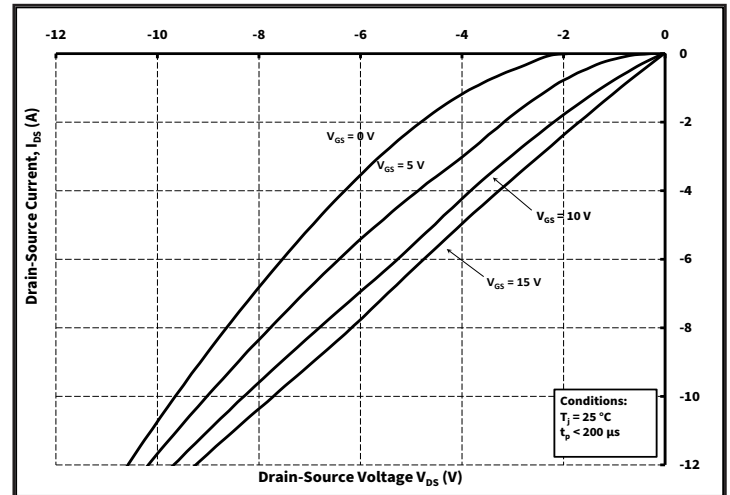


Figure 14. 3rd Quadrant Characteristic at 25 °C

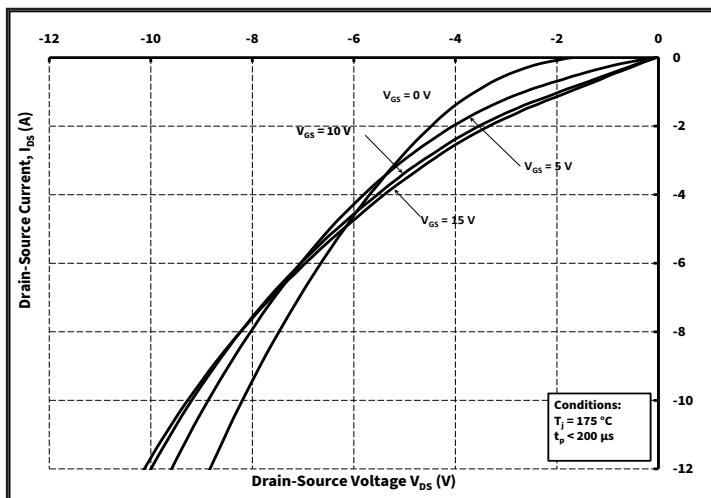


Figure 15. 3rd Quadrant Characteristic at 175 °C

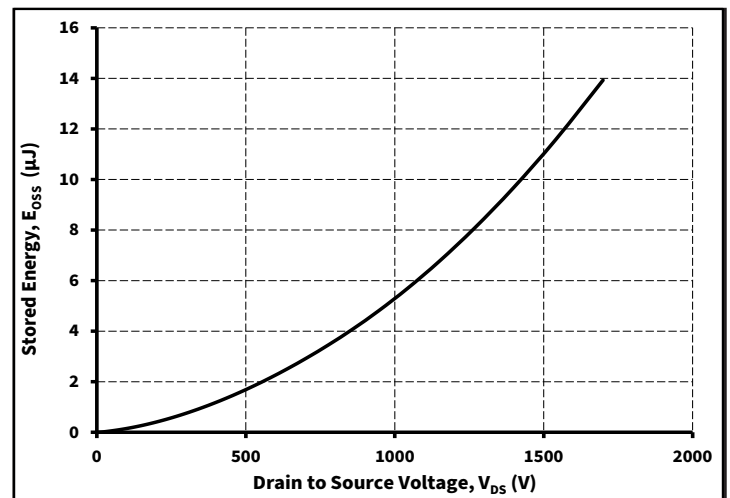


Figure 16. Output Capacitor Stored Energy

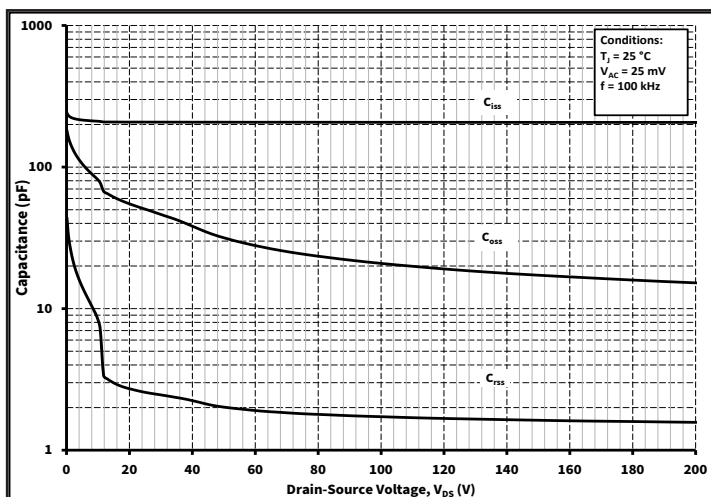


Figure 17. Capacitances vs. Drain-Source Voltage (0 - 200V)

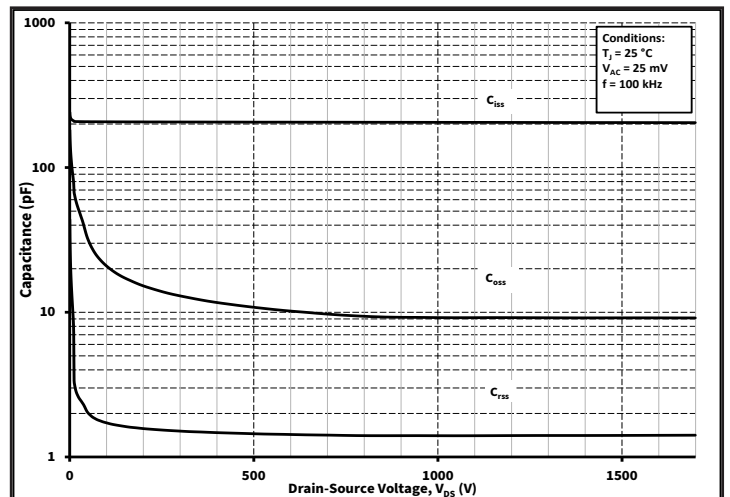


Figure 18. Capacitances vs. Drain-Source Voltage (0 - 1700V)

Typical Performance

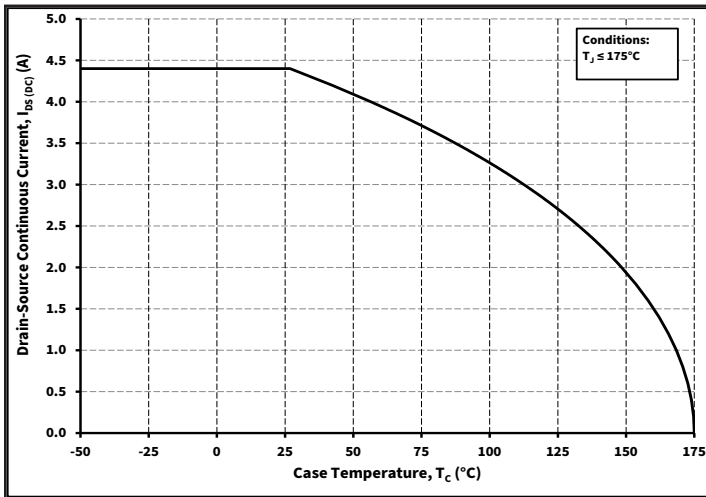


Figure 19. Continuous Drain Current Derating vs. Case Temperature

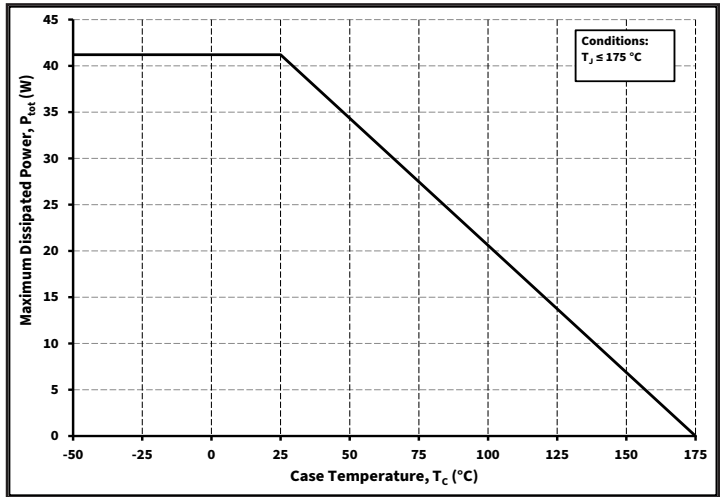


Figure 20. Maximum Power Dissipation Derating vs. Case Temperature

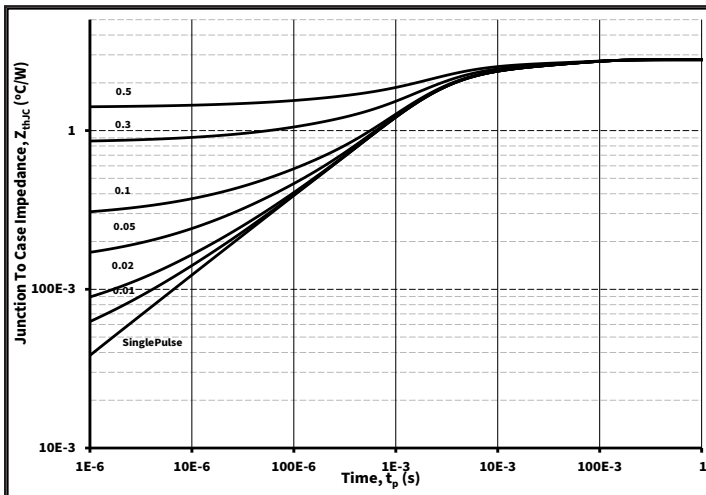


Figure 21. Transient Thermal Impedance (Junction - Case)

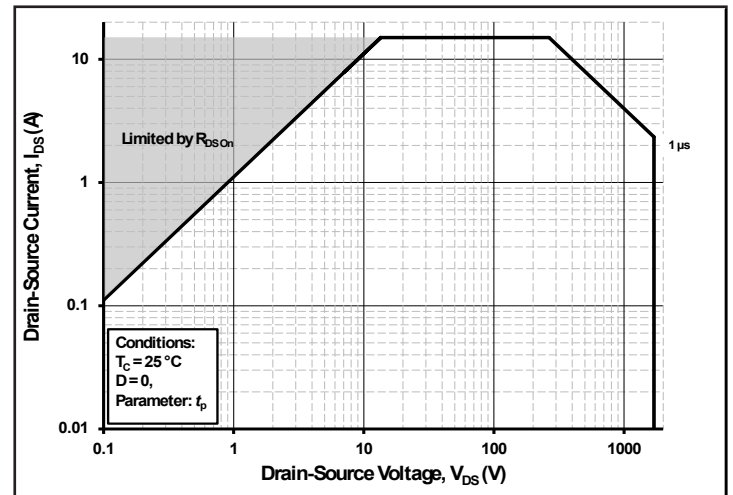
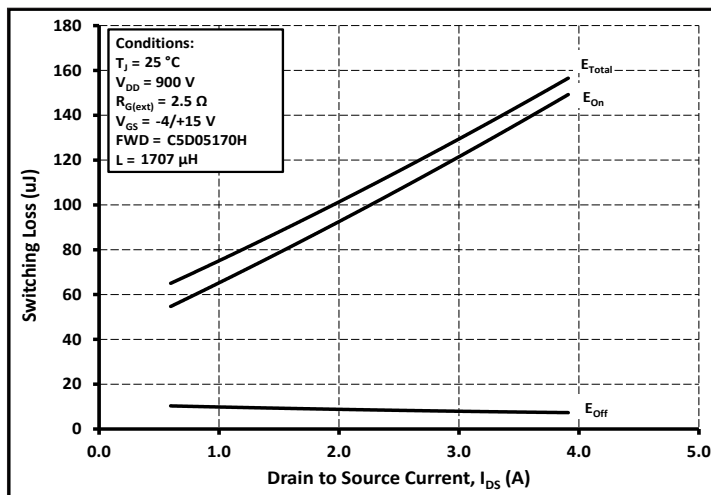
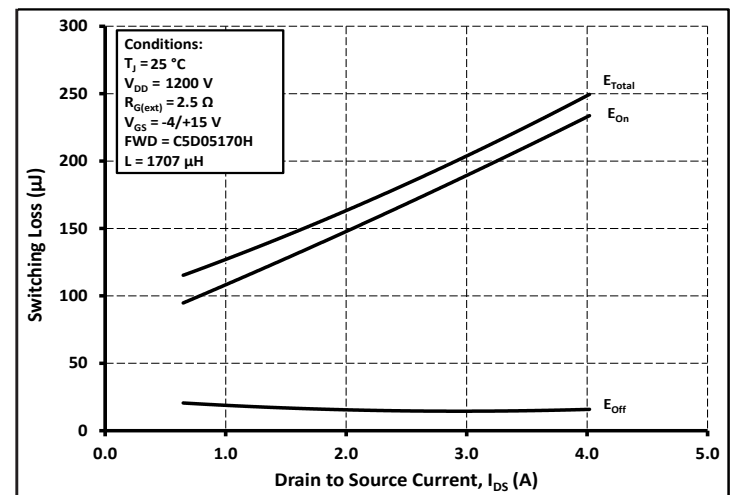


Figure 22. Safe Operating Area

Figure 23. Clamped Inductive Switching Energy vs. Drain Current ($V_{DD} = 900V$)Figure 24. Clamped Inductive Switching Energy vs. Drain Current ($V_{DD} = 1200V$)

Typical Performance

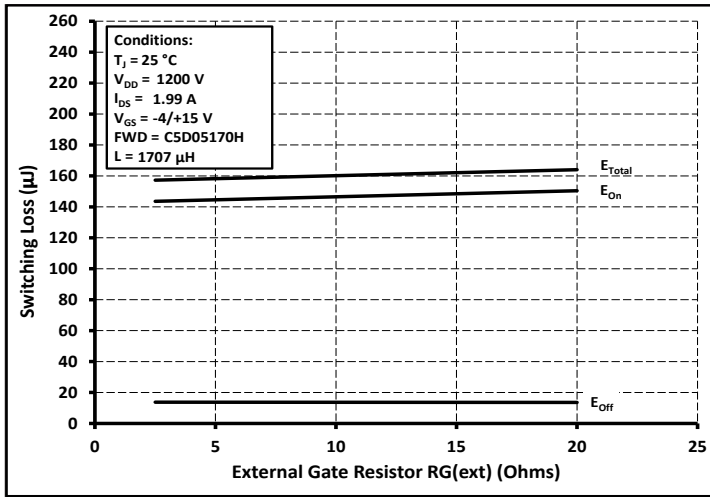


Figure 25. Clamped Inductive Switching Energy vs. $R_{G(\text{ext})}$

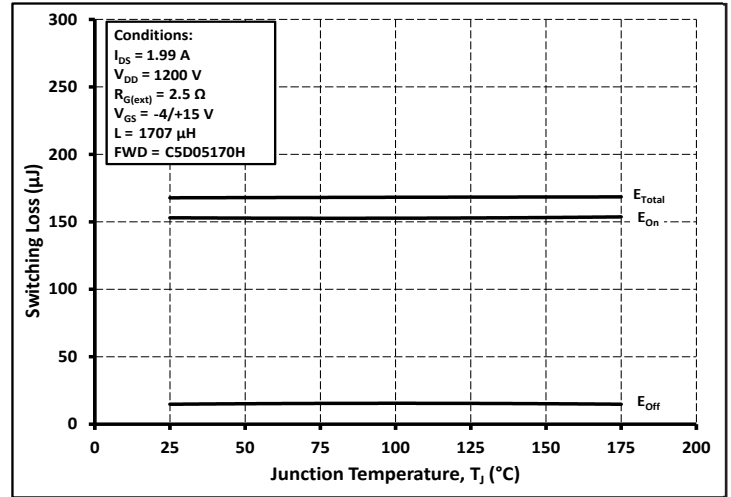


Figure 26. Clamped Inductive Switching Energy vs. Temperature

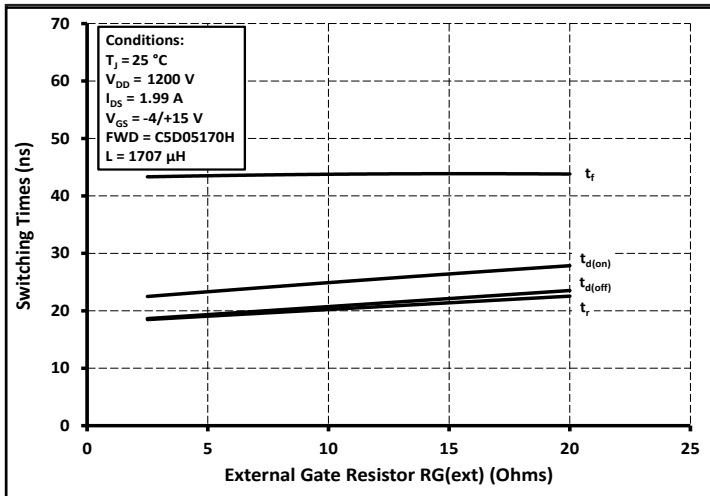


Figure 27. Switching Times vs. $R_{G(\text{ext})}$

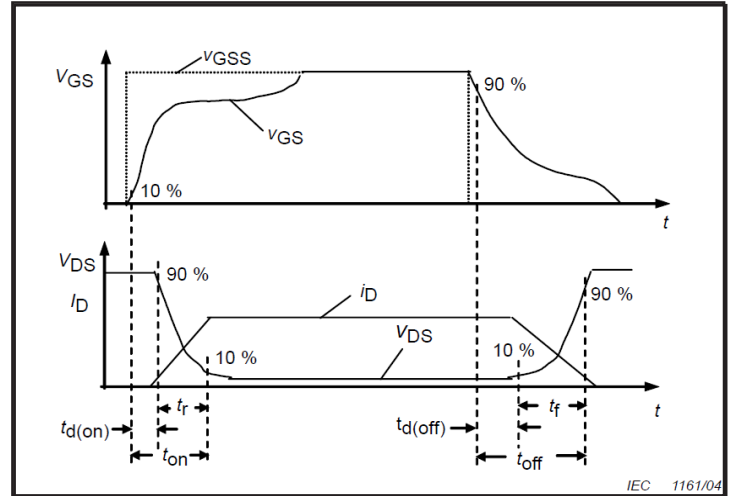


Figure 28. Switching Times Definition

Test Circuit Schematic

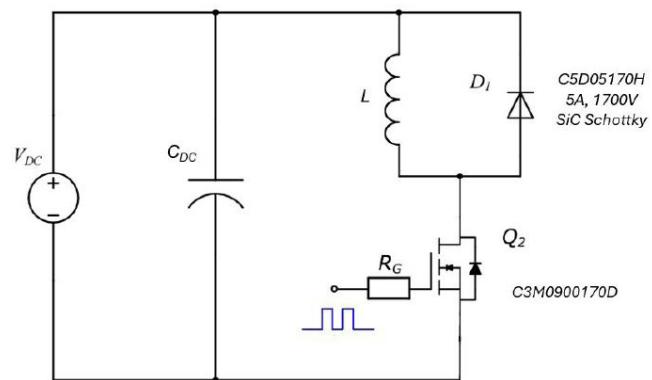
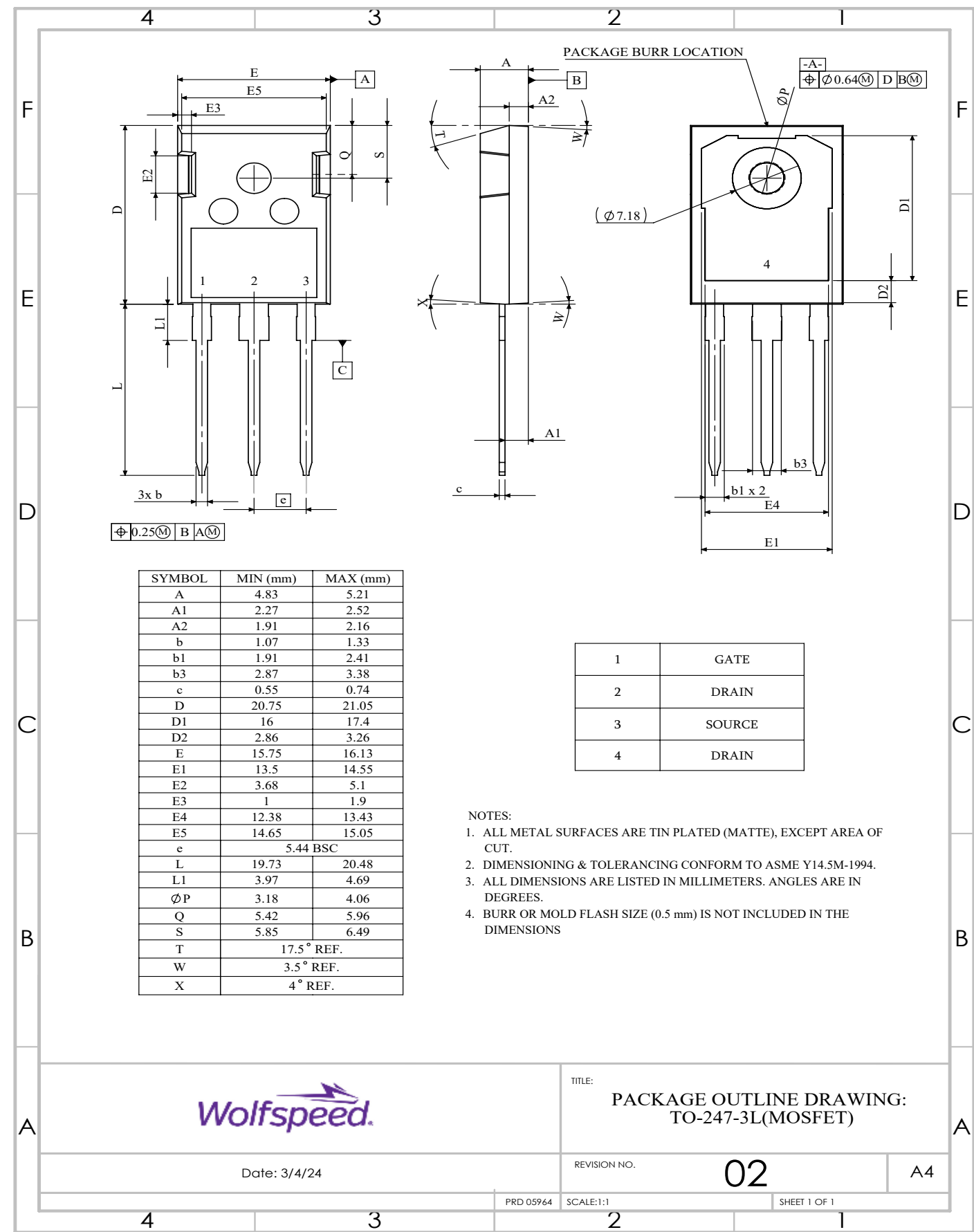


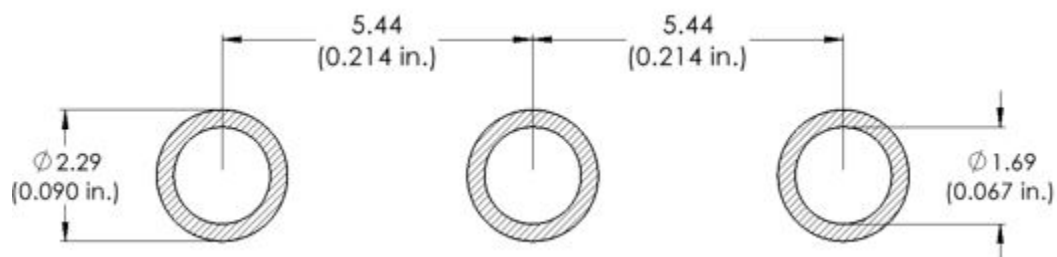
Figure 29. Clamped Inductive Switching
Waveform Test Circuit

Package Dimensions



Recommended Solder Pad Layout

All dimensions in mm





Revision history

Document Version	Date of release	Description of changes
1	February - 2025	Initial Release
2	March - 2025	$V_{GS\,OP}$ corrected

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