4.75V to 18V, 2A/3A/4A 1ch Buck Converter with Integrated FET

BD9325FJ-LB BD9326EFJ-LB BD9327EFJ-LB

General Description

This is the product guarantees long time support in Industrial market.

The BD9325FJ-LB, BD9326EFJ-LB and BD9329EFJ –LB are step-down regulators with built-in low resistance high side N-Channel MOSFET. These ICs can supply continuous output current of 2A / 3A / 4A respectively over a wide input range, and provides not only fast transient response, but also easy phase compensation because of current mode control.

Features

- Long Time Support Product for Industrial Applications.
- Low ESR Output Ceramic Capacitors are Available
- Low Standby Current during Shutdown Mode
- Feedback Voltage
  - 0.9V ± 1.5%(Ta=25°C)
  - 0.9V ± 3.0%(Ta=-25°C to +85°C)
- Protection Circuit:
  - Under Voltage Protection
  - Thermal Shutdown
  - Over-Current Protection

Applications

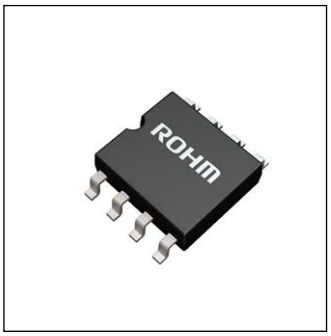
Industrial Equipment
Distributed Power System
Pre-Regulator for Linear Regulator

Key Specifications

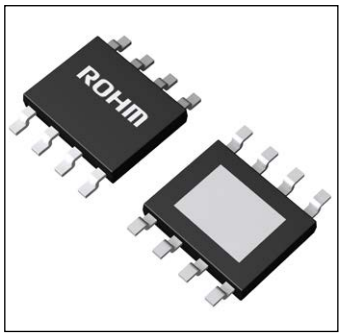
- Input Voltage Range: 4.75V to 18V
- Output Current
  - BD9327EFJ-LB : 4.0A (Max)
  - BD9326EFJ-LB: 3.0A (Max)
  - BD9325FJ-LB: 2.0A (Max)
- Switching Frequency: 380kHz (Typ)
- High Side FET ON-Resistance
  - BD9327EFJ-LB: 0.11Ω(Typ)
  - BD9326EFJ-LB: 0.12Ω(Typ)
  - BD9325FJ-LB: 0.16Ω(Typ)
- Low Side FET ON-Resistance: 10Ω(Typ)
- Standby Current: 80μA (Typ)
- Operating Temperature Range: -40°C to +85°C

Packages

	(Typ.)	(Typ.)	(Max.)
HTSOP-J8	**4.90mm**	**x 6.00mm**	**x 1.00mm**
SOP-J8	**4.90mm**	**x 6.00mm**	**x 1.65mm**



SOP-J8



HTSOP-J8

Typical Application Circuit

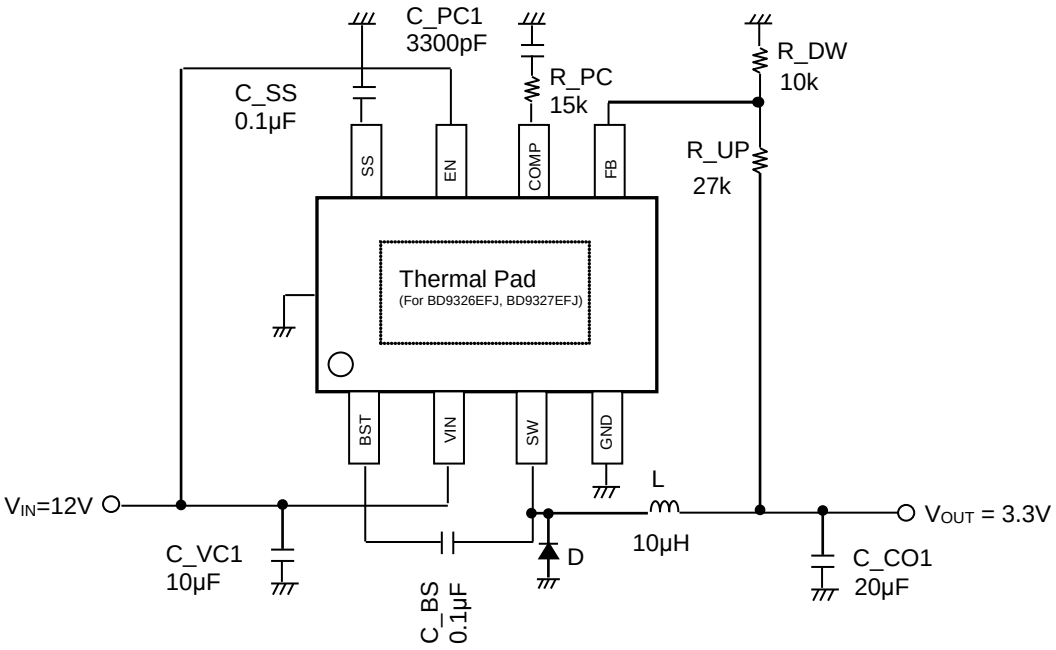


Figure 1. Typical Application Circuit

○Product structure : Silicon monolithic integrated circuit ○This product has no designed protection against radioactive rays

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Pin Configuration

(TOP VIEW)



Figure 2. Pin Configuration

Block Diagram

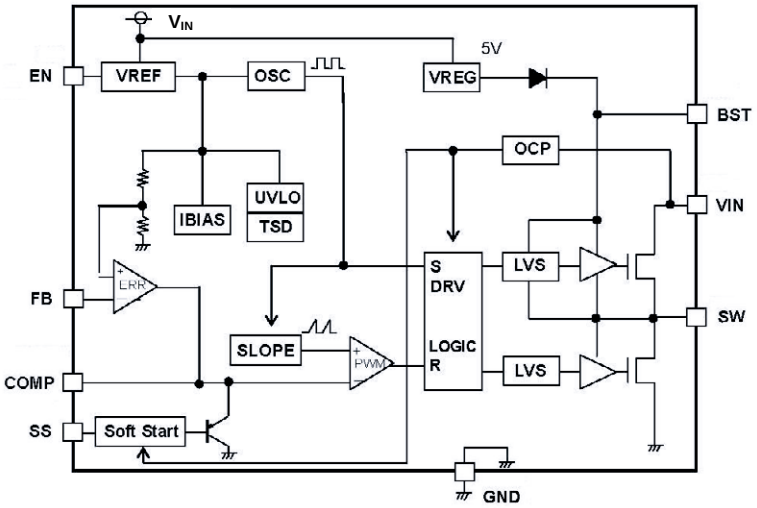


Figure 3. Block Diagram

Pin Description

Pin No.	Pin Name	Function
1	BST	High-side gate drive boost input
2	VIN	Power supply input terminal
3	SW	Power switching output
4	GND	Ground terminal
5	FB	Feedback input
6	COMP	Compensation node
7	EN	Enable input
8	SS	Soft start control input

Ordering Information

B D 9 3 2 x x x x - L B E 2

Part Number
BD932xxxx

Package
FJ : SOP-J8
EFJ : HTSOP-J8

Product class
LB for Industrial applications
Packaging and forming specification
E2: Embossed tape and reel

Lineup

High Side FET ON resistance (Typ.)	OUTPUT CURRENT (Max.)	Package		Orderable Part Number
0.16 Ω	2.0 A	SOP-J8	Reel of 2500	BD9325FJ-LBE2
0.12 Ω	3.0 A	HTSOP-J8	Reel of 2500	BD9326EFJ-LBE2
0.11 Ω	4.0 A	HTSOP-J8	Reel of 2500	BD9327EFJ-LBE2

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Absolute Maximum Ratings (Ta = 25°C)

Parameter	Symbol	Rating	Unit
Supply Voltage [VIN]	V_{IN}	20	V
Switch Voltage [SW]	V_{SW}	20	V
Power Dissipation for HTSOP-J8	Pd1	3.76 (Note 1)	W
Power Dissipation for SOP-J8	Pd2	0.67 (Note 2)	W
Operating Temperature Range	Topr	-40 to +85	°C
Storage Temperature Range	Tstg	-55 to +150	°C
Maximum Junction Temperature	Tjmax	150	°C
BST Voltage	V_{BST}	V_{SW}+7	V
EN Voltage	V_{EN}	20	V
All Other Pins	V_{OTH}	7	V

(Note 1) Mounted on 4- layer 70mmx70mmx1.6mm board. Reduce by 30.08mW/°C for Ta above 25°C.
(Note 2) Mounted on 1- layer 70mmx70mmx1.6mm board. Reduce by 5.4mW/°C for Ta above 25°C.
Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Recommended Operating Conditions (Ta= -40°C to +85°C)

Parameter	Symbol	Rating			Unit
		Min	Typ	Max	
Supply Voltage	V_{IN}	4.75	12	18	V
SW Voltage	V_{SW}	-0.5	-	+18	V
Output Current for BD9325FJ	I_{SW2}	-	-	2 (Note 3)	A
Output Current for BD9326EFJ	I_{SW3}	-	-	3 (Note 3)	A
Output Current for BD9327EFJ	I_{SW4}	-	-	4 (Note 3)	A

(Note 3) Pd, ASO should not be exceeded

Electrical Characteristics (Unless otherwise specified V_{IN}=12V Ta=25°C)

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
Error Amplifier Block						
FB Input Bias Current	I_{FB}	-	0.1	2	µA	
Feedback Voltage1	V_{FB1}	0.886	0.900	0.914	V	Voltage Follower
Feedback Voltage2	V_{FB2}	0.873	0.900	0.927	V	Ta=-40°C to +85°C
SW Block – SW						
Hi-Side FET ON-Resistance for BD9325FJ	R_{ON2}	-	0.16	-	Ω	I_{SW}= -0.8A (Note 4)
Hi-Side FET ON-Resistance for BD9326EFJ	R_{ON3}	-	0.12	-	Ω	I_{SW}= -0.8A (Note 4)
Hi-Side FET ON-Resistance for BD9327EFJ	R_{ON4}	-	0.11	-	Ω	I_{SW}= -0.8A (Note 4)
Low-Side FET ON-Resistance	R_{ONL}	-	10	-	Ω	I_{SW}= 0.1A
Leak Current N-Channel	I_{LEAKN}	-	0	10	µA	V_{IN}= 18V, V_{SW}= 0V
Switch Current Limit for BD9325FJ	I_{LIMIT2}	2.5	-	-	A	(Note 4)
Switch Current Limit for BD9326EFJ	I_{LIMIT3}	3.5	-	-	A	(Note 4)
Switch Current Limit for BD9327EFJ	I_{LIMIT4}	4.5	-	-	A	(Note 4)
Maximum Duty Cycle	M_{DUTY}	-	90	-	%	V_{FB}= 0V
General						
Enable Sink Current	I_{EN}	86	181	275	µA	V_{EN}= 12V
Enable Threshold Voltage	V_{EN}	1.1	1.18	1.4	V	
Under Voltage Lockout Threshold	V_{UVLO}	4.05	4.40	4.75	V	V_{IN} Rising
Under Voltage Lockout Hysteresis	V_{HYS}	-	0.1	-	V	
Soft Start Current	I_{SS}	23	41	62	µA	V_{SS}= 0 V
Soft Start Time	t_{SS}	-	1.6	-	ms	C_{SS}= 0.1 µF
Operating Frequency	f_{OSC}	300	380	460	kHz	
Circuit Current	I_{CC}	-	2.1	4.3	mA	V_{FB}= 1.5V, V_{EN}= 12V
Standby Current	I_{QUI}	-	80	170	µA	V_{EN}= 0V

(Note 4) See the lineup table .

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Typical Performance Curves

(Unless otherwise specified, V_{IN}= 12V Ta = 25°C)

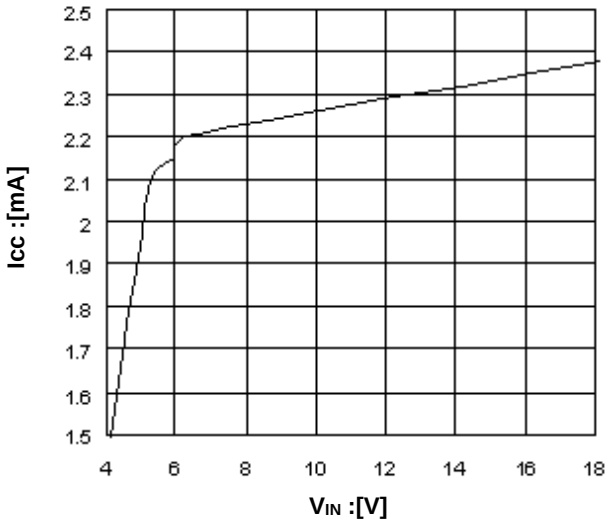


Figure 4. Circuit Current vs Input Voltage (No Switching)

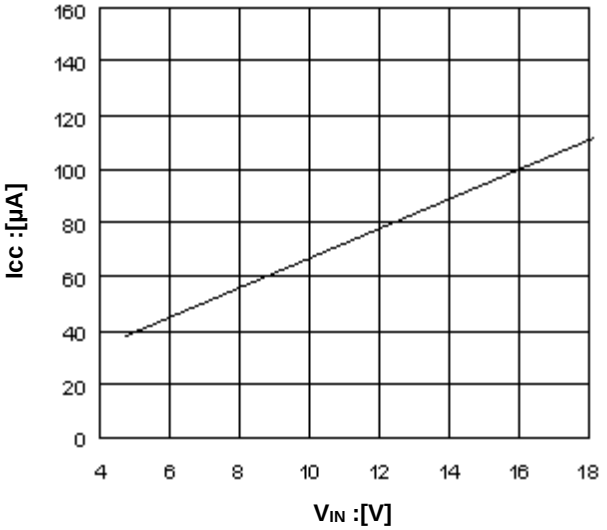


Figure 5. Standby Current vs Input Voltage (IC Not Active)

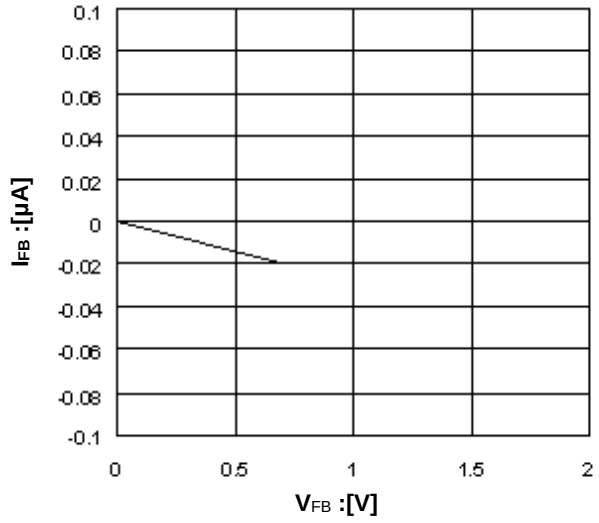


Figure 6. Input Bias Current vs Feedback Voltage

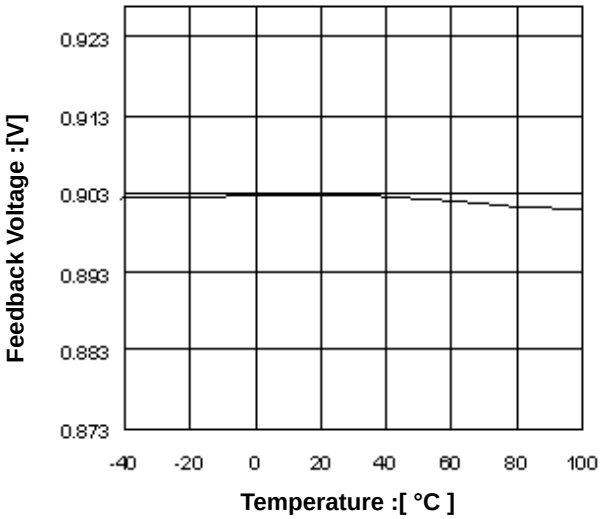


Figure 7. Feedback Voltage vs Temperature

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Typical Performance Curves - continued

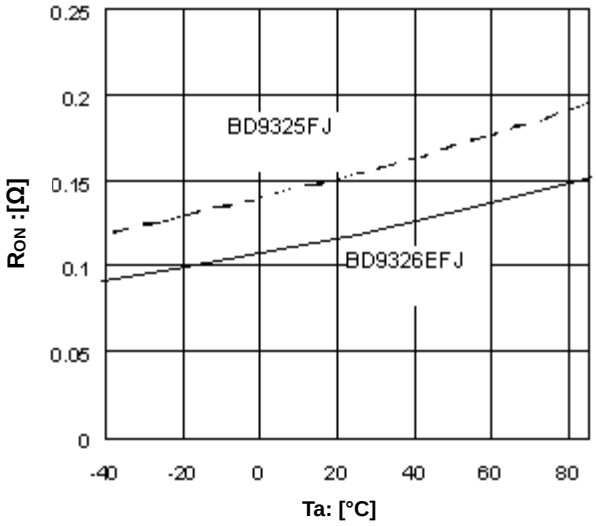


Figure 8. Hi-Side ON-Resistance vs Temperature

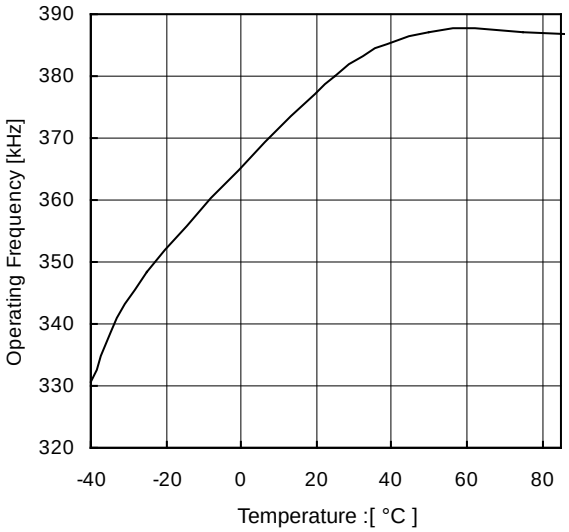


Figure 9. Operating Frequency vs Temperature

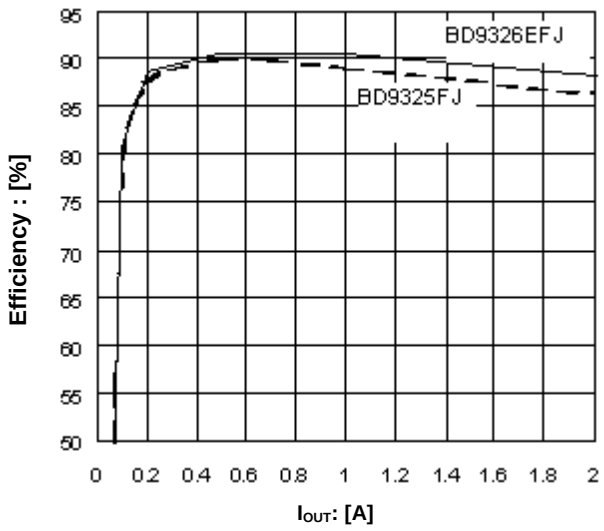


Figure 10. Efficiency vs Output Current (V_{IN}= 12V V_{OUT}= 3.3V L=10µH)

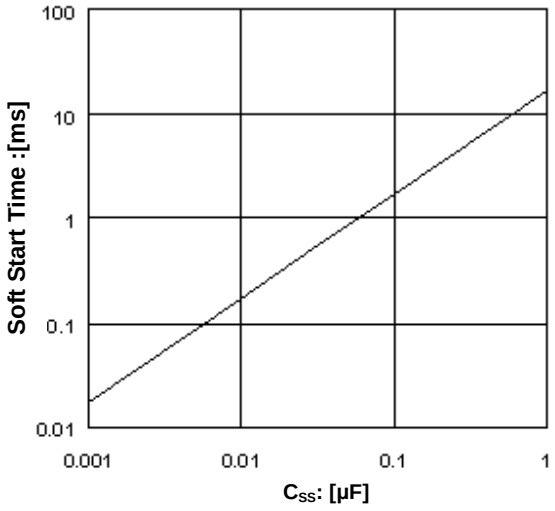


Figure 11. Soft Start Time vs Soft Start Capacitor

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Typical Waveforms

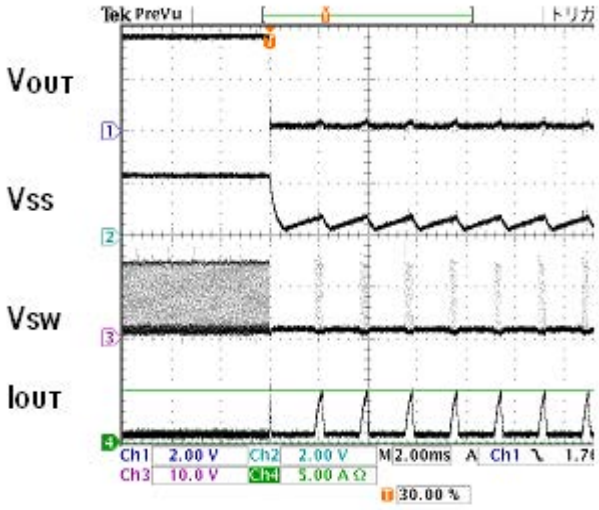


Figure 12. Over-Current Protection
(V_{OUT} is shorted to GND)

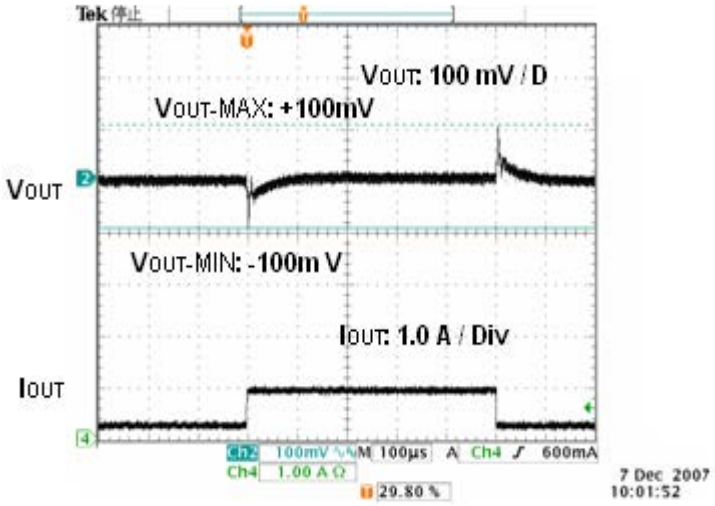


Figure 13. Transient Response
(V_{IN}= 12V V_{OUT}= 3.3V L= 10µH C_{OUT} =22µF I_{OUT}= 0.2-1.0A)

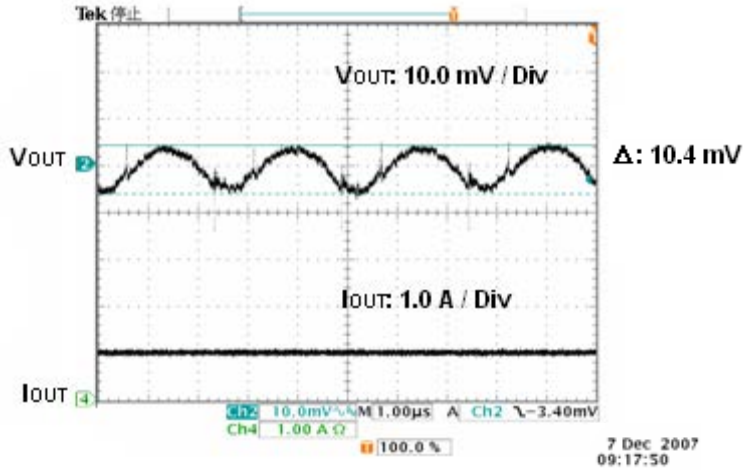


Figure 14. Output Ripple Voltage
(V_{IN}= 12V V_{OUT}= 3.3V L= 10µH C_{OUT} =22µF I_{OUT}= 1.0A)

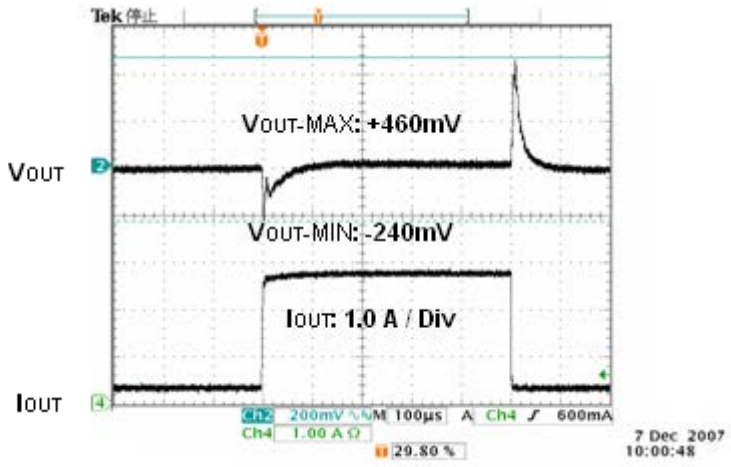


Figure 15. Transient Response
(V_{IN}= 12V V_{OUT}= 3.3V L= 10µH C_{OUT} =22µF I_{OUT}= 0.2-3.0A)

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Typical Waveforms - continued

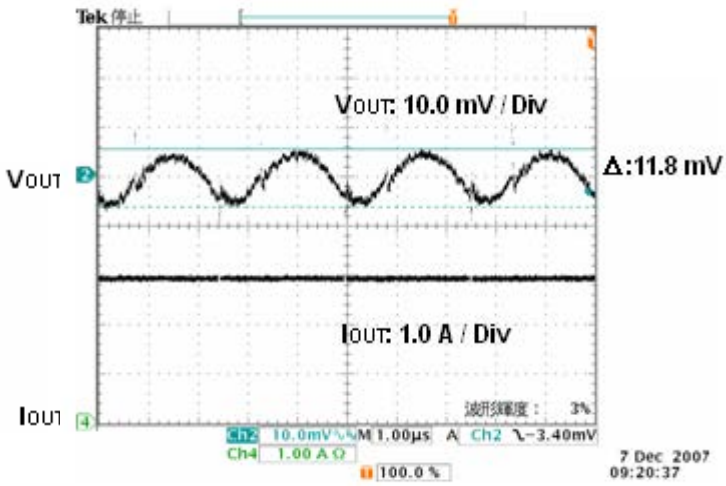


Figure 16. Output Ripple Voltage
(V_{IN}= 12V V_{OUT}= 3.3V L= 10µH C_{OUT} =22µF I_{OUT}= 3.0A)

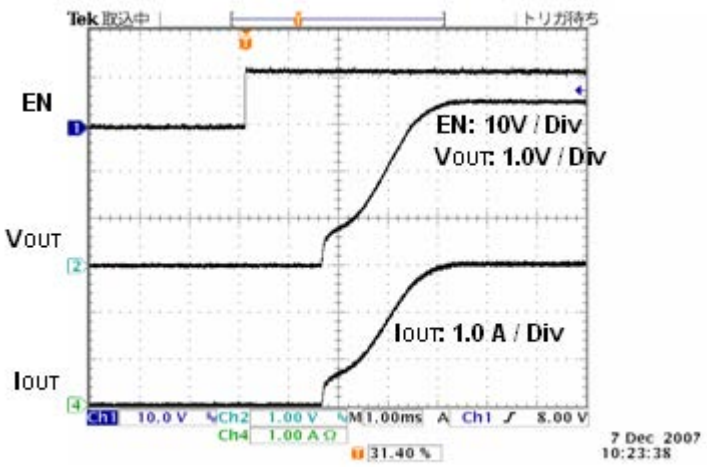


Figure 17. Start Up Waveform
(V_{IN}= 12V V_{OUT}= 3.3V L= 22µH C_{SS}= 0.1µF I_{OUT}= 0A)

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Application Information

1. Block Operation

(1) VREG
This block generates the constant-voltage needed for DC/DC boosting.

(2) VREF
This block generates the 2.9 V internal reference voltage of the Error Amp.

(3) TSD/UVLO
TSD (Thermal shutdown)/UVLO (Under Voltage Lockout) are protection circuit blocks. This circuit protects the device from damages due to excessive heat and power dissipation. When the TSD circuit is triggered by temperature exceeding the 175°C Maximum Junction Temperature, it shuts down the device. Once temperature falls below the threshold set by a hysteresis, the device resumes operation.

UVLO circuit prevents error in the device operation due to either excessive or insufficient power supply voltage. It monitors the voltage level at VIN pin and also the output of REG block. Once VIN voltage falls below 4.4V, the UVLO circuit disables the device and resets the Soft-Start circuit. Typical UVLO Hysteresis is 100 mV.

(4) Error Amp Block (ERR)
This circuit compares the reference voltage and the feedback of output voltage. The COMP pin voltage, which is the output of ERR block, determines the switching duty. During startup, the COMP pin voltage is limited by SS pin voltage since the soft start is operated by the SS pin voltage.

(5) Oscillator Block (OSC)
This block generates the internal oscillating frequency of the IC.

(6) SLOPE Block
This circuit is used to generate triangular waveform from the clock created by OSC block. This triangular waveform is sent to the PWM comparator.

(7) PWM Block
The COMP pin voltage, which is the output of ERR block, is compared to the SLOPE block's triangular waveform to determine the switching duty. Since the switching duty is limited by the maximum duty ratio which is determined internally, it does not become 100%.

(8) DRV Block
This circuit is a DC/DC driver block. A signal from the PWM serves as the input to drive the power FETs.

(9) OCP Block
OCP (Over-Current Protection) is a protection circuit block. The OCP block activates when the current flows through the FET is detected, and OCP starts when it reached 2.5 / 3.5 / 4.5A (min). After OCP, switching will turn OFF and SS capacitor will discharge. OCP is a self-recovery type (not latch).

(10) Soft Start Circuit
The soft-start feature reduces overshoot in the output by making the regulator reach steady-state gradually. The soft-start capacitor, C_{SS}, which is connected to SS (pin 8) and GND (pin4), sets the soft-start time, t_{SS}.
(Refer to Figure 23 to know how to set C_{SS}.)

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2. Selecting Application Components

(1) Output LC Constant (Buck Converter)
The inductance L to be used for the output is decided by the current rating I_{LR} and maximum input current value I_{OMAX} of the inductor.

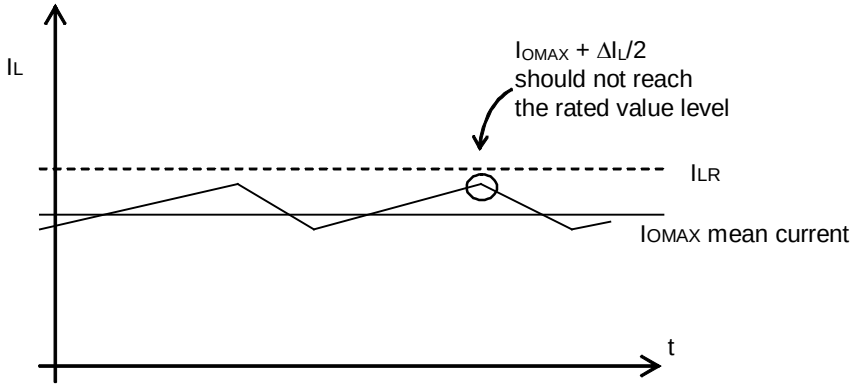


Figure 18

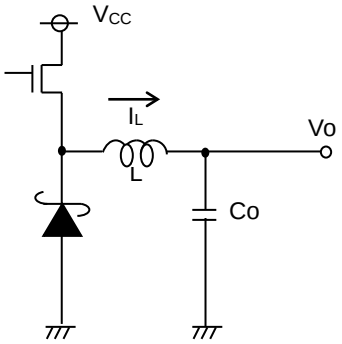


Figure 19

Adjust $I_{OMAX}+\Delta I_L/2$ so that it won't reach the current rating value I_{LR}. At this time, ΔI_L can be obtained by the following equation.

$$\Delta I_L = \frac{1}{L} \times (V_{CC} - V_O) \times \frac{V_O}{V_{CC}} \times \frac{1}{f} \quad [A]$$

Set with sufficient margin because the inductance L value may have a tolerance of ± 30%.

For output capacitor C, select a capacitor which has the larger value in the ripple voltage V_{PP} permissible value and the drop voltage permissible value at the time of sudden load change.

Output ripple voltage is decided by the following equation.

$$\Delta V_{PP} = \Delta I_L \times R_{ESR} + \frac{\Delta I_L}{2C_O} \times \frac{V_O}{V_{CC}} \times \frac{1}{f} \quad [V]$$

Perform setting so that the voltage is within the permissible ripple voltage range.
For the drop voltage V_{DR} during sudden load change, please perform the rough calculation by the following equation.

$$V_{DR} = \frac{\Delta I_L}{C_O} \times 10\mu s \quad [V]$$

However, 10µs is the rough calculation value of the DC/DC response speed.
Make Co settings so that these two values will be within the limit values.

(2) Loop Compensation
Choosing compensation Capacitor C1 and Resistor R3

The example of DC/DC converter application bode plot is shown in Figure 21. The compensation resistor R3 will set the cross over frequency F_C that decides the stability and response speed of DC/DC converter. So compensation resistor R3 has to be adjusted to adequate value for good stability and response speed.

The cross over frequency F_C can be adjusted by changing the compensation resistor R3 connected to COMP terminal. Higher cross over frequency achieves good response speed, but less stability, and the lower cross over frequency shows good stability, but worse response speed.
Usually, the 1/10 of DC/DC converter operating frequency is used for cross over frequency F_C. So please decide the compensation resistor and capacitor using the following formula on setting F_C to 1/10 of operating frequency at first.
After that, please measure and adjust the cross over frequency on your set (on the actual application) to meet the desired speed and phase-margin.

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(a) Choosing Phase Compensation Resistor R3

Please decide the compensation resistor R3 by following the formula below.

Compensation Resister $R3 = 5800 \times C_{OUT} \times fc \times V_{OUT}$ $[\Omega]$

Where
C_{OUT} is the Output capacitor connected to DC/DC output
V_{OUT} is the Output voltage
f_C is the Desired cross over frequency (38kHz)

The larger value of R3, value of fc increases (response better and stability worse).
The smaller value of R3, value of fc decreases (response worse and stability better).

(b) Choosing Phase Compensation Capacitor C1

The phase delay which is from output LC filter, needs to be cancelled to stabilize the DC/DC converter, this is done by inserting the phase lead.
The phase lead can be added by the zero introduced by the compensation resistor and capacitor.
The LC resonant frequency F_{LC} and the zero on compensation resistor and capacitor are expressed below.

LC Resonant Frequency $f_{LC} = \dfrac{1}{2\pi\sqrt{LC_{OUT}}}$ $[H_Z]$

Zero C1 and R3 $f_Z = \dfrac{1}{2\pi C_1 R_3}$ $[H_Z]$

Please choose C1 to make f_Z to 1 / 3 of f_{LC} .

Compensation Capacitor $C1 = \dfrac{3}{2\pi f_{LC} R_3}$ $[F]$

(c) The Condition of the Loop Compensation Stability
The stability of the DC/DC converter is important. To ensure the operating stability, please check the loop compensation if it has enough phase-margin. For the condition of loop compensation stability, the phase-lag must be less than 150 degrees when gain is 0 dB. Namely over 30 degrees phase-margin is needed.
Lastly, after the calculation above, find measures to adjust the phase-margin to more than 30 degrees.

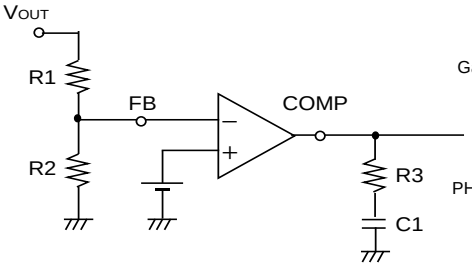


Figure 20

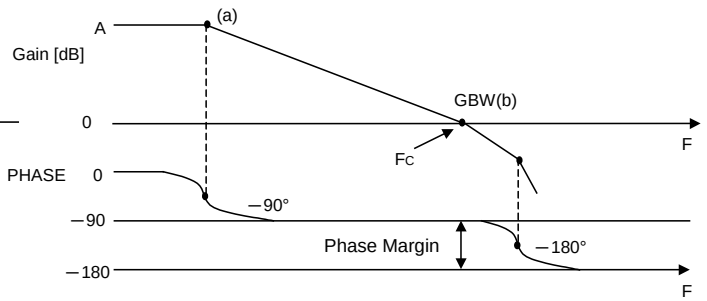
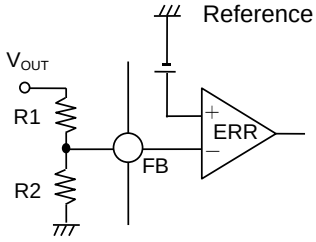


Figure 21

(3) Design of Feedback Resistance Constant

Set the feedback resistance as shown below.



$V_{OUT} = \dfrac{R1 + R2}{R2} \times$ Reference Voltage [V]

Figure 22

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(4) Soft Start Function

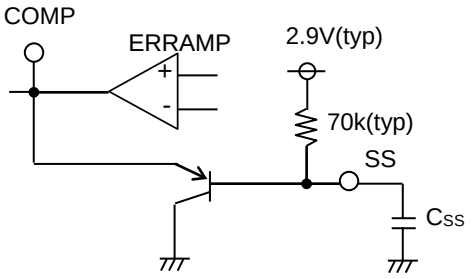


Figure 23

The buck converter has an adjustable Soft Start function to prevent high inrush current during start up.

The soft-start time is set by the external capacitor connected to SS pin.
The soft start time is given by;

$$tss = 16200 \times C_{SS} \quad [S]$$

Please confirm the overshoot of the output voltage and inrush current when deciding the SS capacitor value.

(5) EN Function

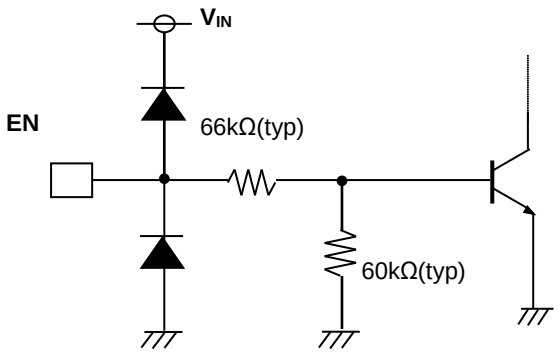


Figure 24. The Equivalent Internal Circuit

The EN terminal control the IC's shut down.
Leaving EN terminal open will shutdown the IC.
To start the IC, EN terminal should be connected to V_{IN} or the other power source output.
When the EN voltage exceed 1.2V (typ), the IC start operating.

3. Selecting Application Components

Two high pulsing current flowing loops exist in the buck regulator system.
The first loop, when FET is ON, starts from the input capacitors, to the VIN terminal, to the SW terminal, to the inductor, to the output capacitors, and then returns to the input capacitor through GND.
The second loop, when FET is OFF, starts from the Schottky diode, to the inductor, to the output capacitor, and then returns to the Schottky diode through GND.
To reduce the noise and improve the efficiency, please minimize these two loop area.
Especially input capacitor, output capacitor and Schottky diode should be connected to GND plane.
PCB Layout may affect the thermal performance, noise and efficiency greatly. So please take extra care when designing PCB Layout patterns.

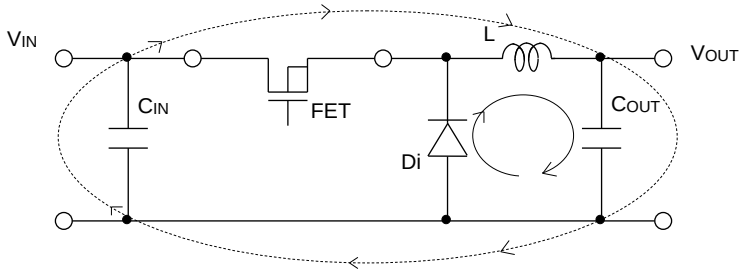


Figure 25. Current Loop in Buck Regulator System

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(1) The Thermal Pad on the back side of IC serves as heat sink for thermal conduction to the chip. Making the GND plane as broad and wide as possible can help in thermal dissipation. Adding a lot of thermal via is also effective for helping the spread of heat to the different layer.

(2) The input capacitors should be connected as close as possible to the VIN terminal.

(3) When there is unused area on PCB, please arrange the copper foil plane of DC nodes, such as GND, VIN and VOUT for helping heat dissipation of IC or circumference parts.

(4) Make the trace of the switching line as short and thick as possible to coil to avoid the noise influence of AC signals to combine with the other line.

(5) Keep sensitive signal traces such as trace connected FB and COMP away from SW pin.

(6) The inductor, the Schottky diode and the output capacitors should be placed close as possible to SW pin.

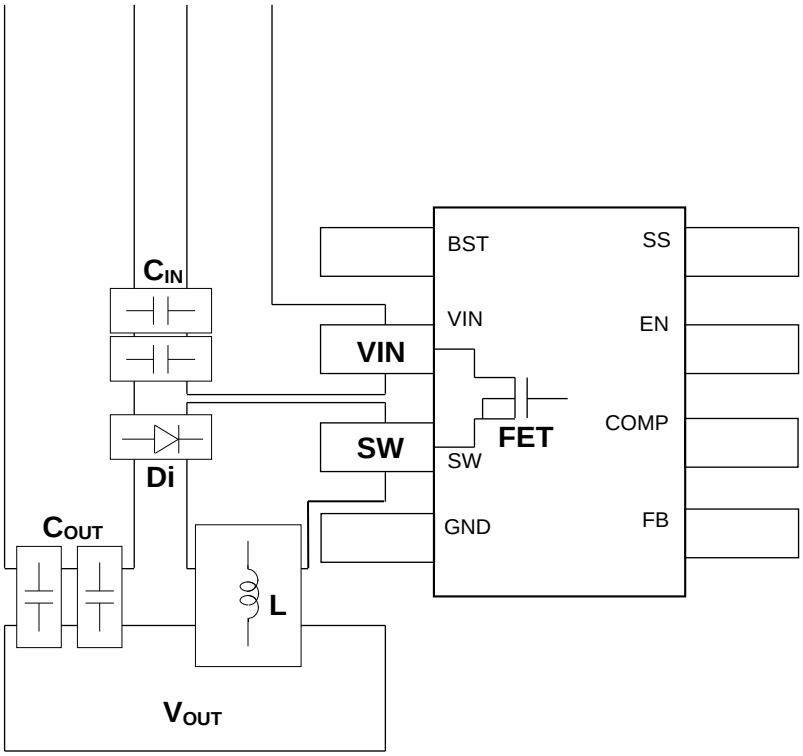
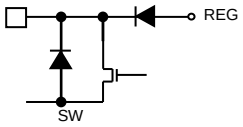
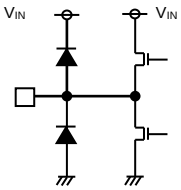
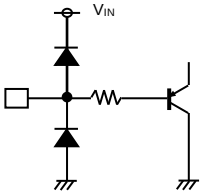
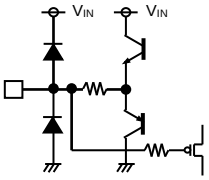
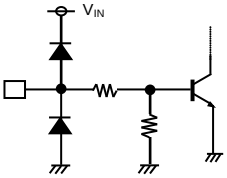
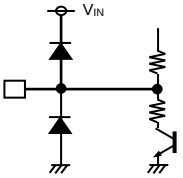


Figure 26. The Example of PCB Layout Pattern

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I/O Equivalence Circuit

1.BST	3.SW	5.FB
		
6.COMP	**7.EN**	**8.SS**
		

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Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Thermal Consideration**
   Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. The absolute maximum rating of the Pd stated in this specification is when the IC is mounted on a 70mm x 70mm x 1.6mm glass epoxy board. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.

6. **Recommended Operating Conditions**
   These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. **Operation Under Strong Electromagnetic Field**
   Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

10. **Inter-pin Short and Mounting Errors**
    Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

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Operational Notes – continued

11. Unused Input Pins

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

12. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

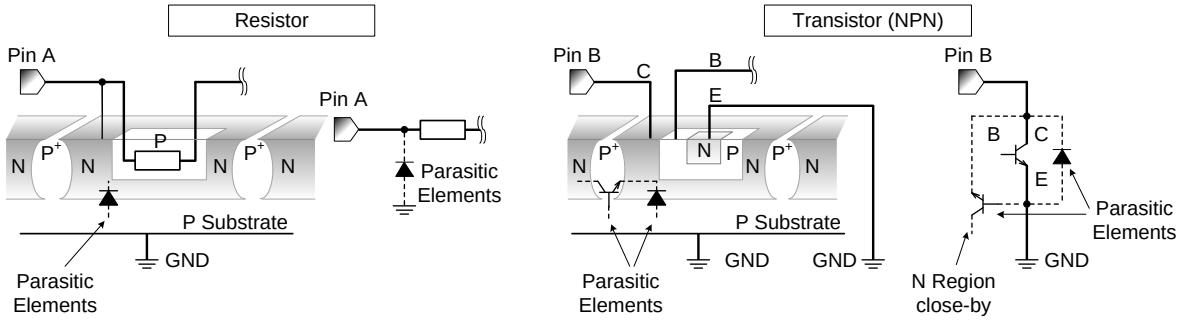


Figure 29. Example of monolithic IC structure

13. Thermal Shutdown Circuit(TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's power dissipation rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF all output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

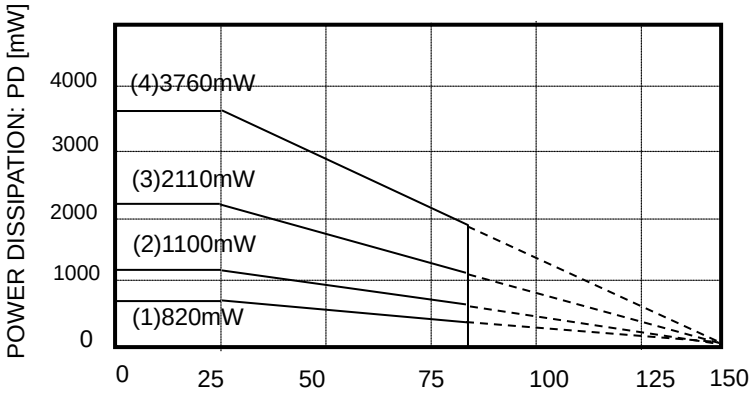
14. Over Current Protection Circuit (OCP)

This IC incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

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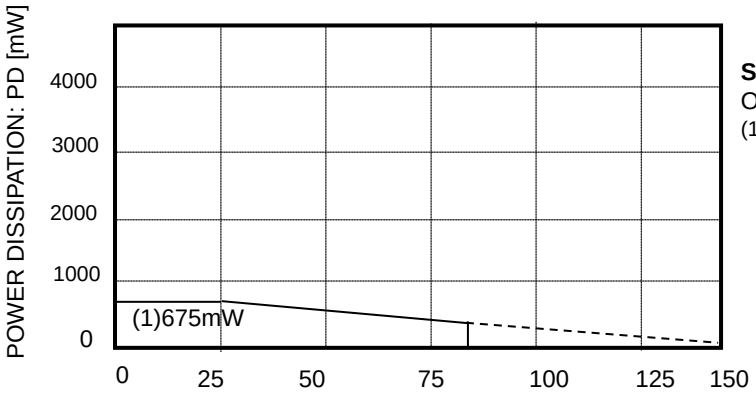
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Power Dissipation



HTSOP-J8 Package
On 70 × 70 × 1.6 mm glass epoxy PCB
(1) 1-layer board (Backside copper foil area 0 mm × 0 mm)
(2) 2-layer board (Backside copper foil area 15 mm × 15 mm)
(3) 2-layer board (Backside copper foil area 70 mm × 70 mm)
(4) 4-layer board (Backside copper foil area 70 mm × 70 mm)

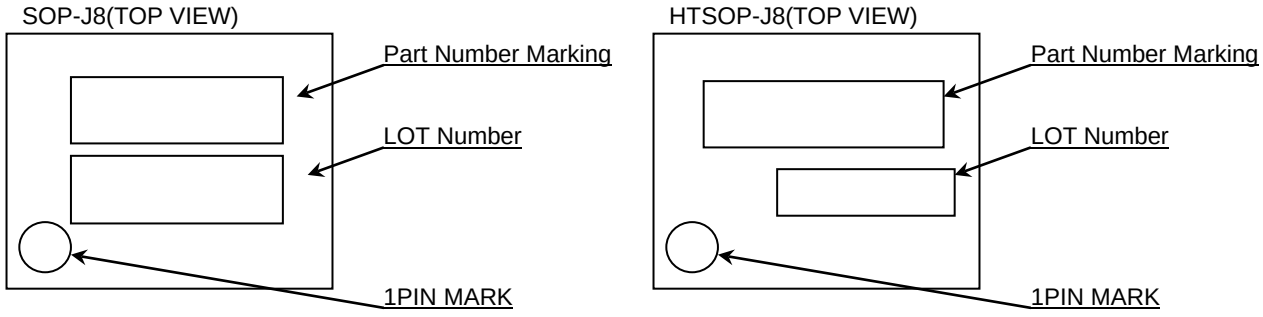
Figure 29. AMBIENT TEMPERATURE: Ta [°C]



SOP-J8 Package
On 70 × 70 × 1.6 mm glass epoxy PCB
(1) 1-layer board (Backside copper foil area 0 mm × 0 mm)

Figure 30. AMBIENT TEMPERATURE: Ta [°C]

Marking Diagrams



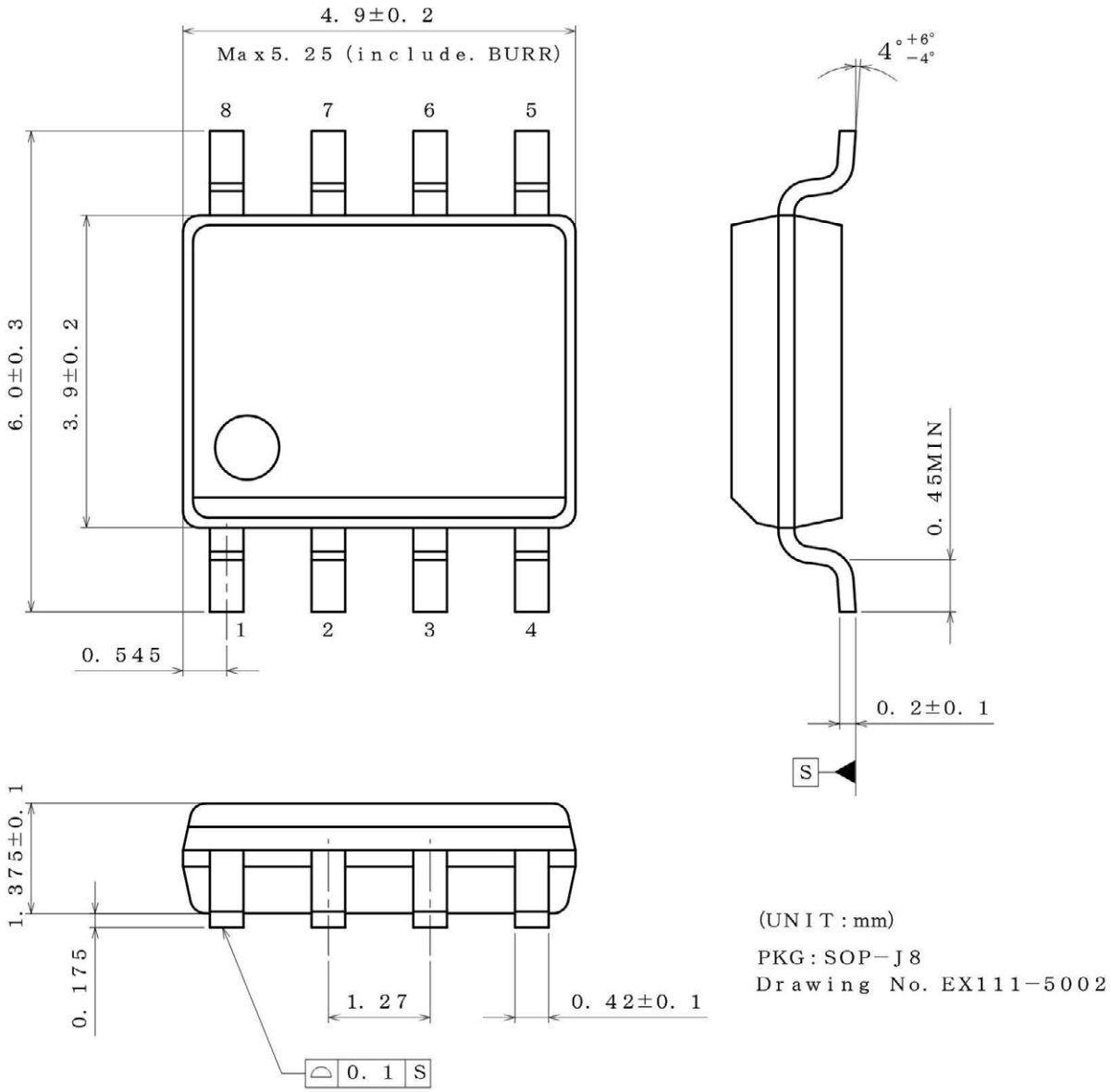
Part Number Marking	Package	Orderable Part Number
D9325	SOP-J8	BD9325FJ-LBE2
D9326	HTSOP-J8	BD9326EFJ-LBE2
D9327	HTSOP-J8	BD9327EFJ-LBE2

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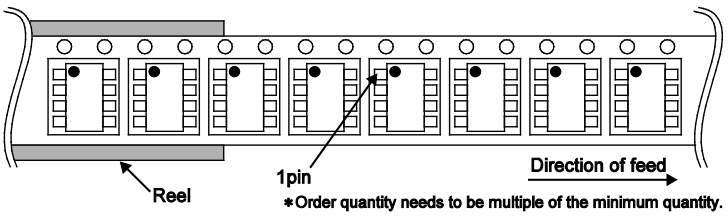
Physical Dimensions, Tape and Reel information

Package Name	SOP-J8



<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



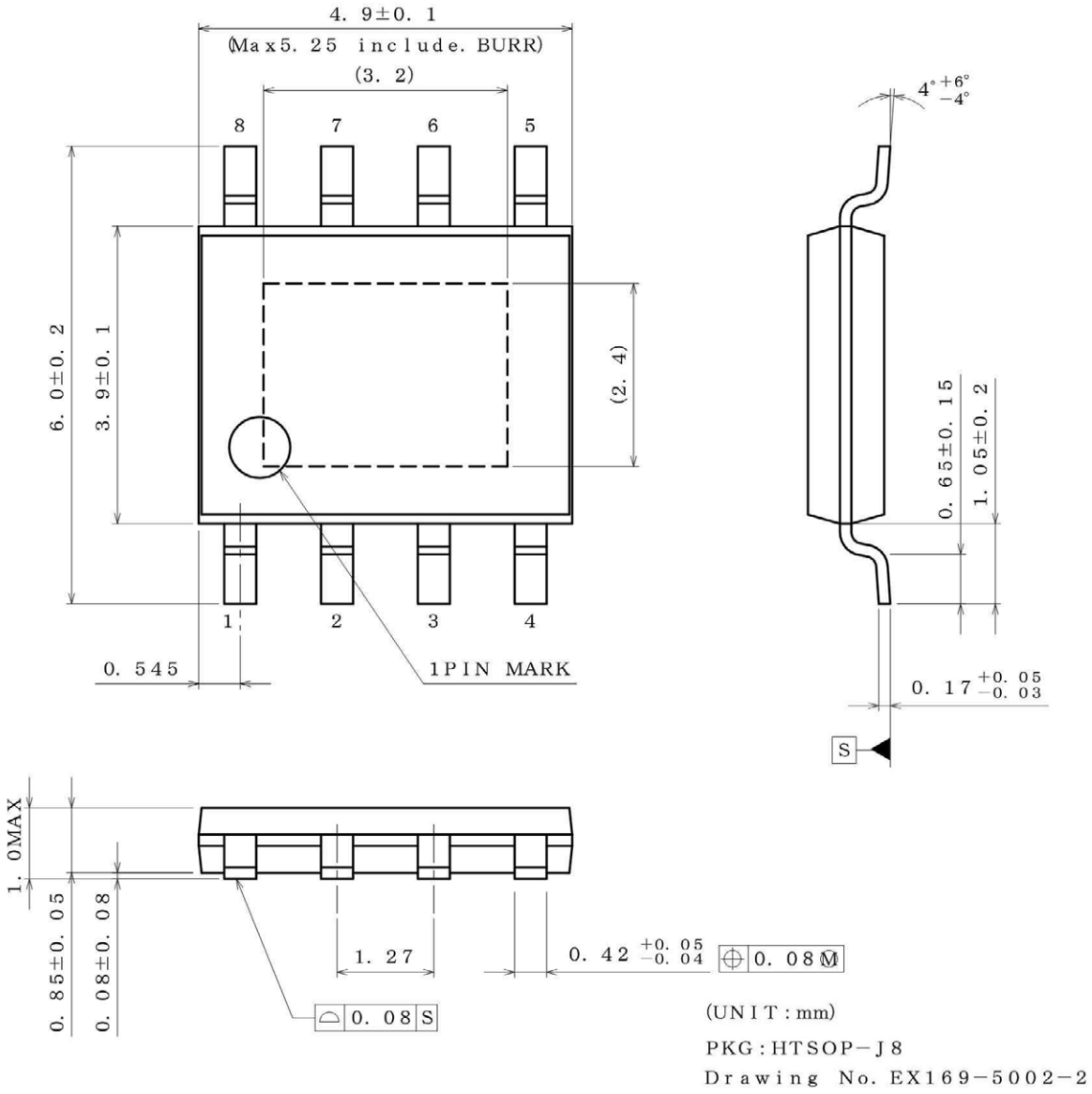
*Order quantity needs to be multiple of the minimum quantity.

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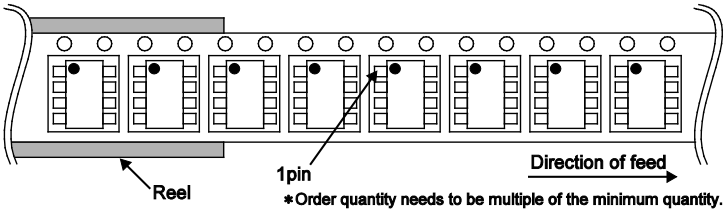
Physical Dimensions, Tape and Reel information - continued

Package Name	HTSOP-J8



<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



*Order quantity needs to be multiple of the minimum quantity.

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Revision History

Date	Revision	Changes
05.Aug.2013	001	New Release
27.Feb.2014	002	Delete sentence “and log life cycle” in General Description and Futures. Applied new style (“title” and “Physical Dimension Tape and Reel Information”).
09.Sep.2014	003	Applied the ROHM Standard Style and improved understandability in all pages.

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(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

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   [a] Installation of protection circuits or other protective devices to improve system safety
   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

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   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation (Pd) depending on Ambient temperature (Ta). When used in sealed area, confirm the actual ambient temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used; if flow soldering method is preferred, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   - [a] the Products are exposed to sea winds or corrosive gases, including Cl2, H2S, NH3, SO2, and NO2
   - [b] the temperature or humidity exceeds those recommended by ROHM
   - [c] the Products are exposed to direct sunshine or condensation
   - [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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Precaution for Disposition

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