

April 1988 Revised January 2004

74F30 8-Input NAND Gate

General Description

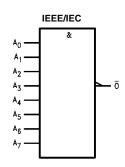
This device contains a single gate, which performs the logic NAND function.

Ordering Code:

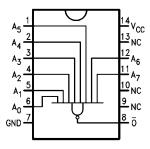
Order Number	Package Number	Package Description
74F30SC (Note 1)	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
74F30SJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74F30PC	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Note 1: Devices also available in Tape and Reel. Specify by appending the letter "X" to the ordering code.

Logic Symbol



Connection Diagram



Unit Loading/Fan Out

Din Namos	Description	U.L.	Input I _{IH} /I _{IL}		
riii Nailles	Description	HIGH/LOW	Output I _{OH} /I _{OL}		
A ₀ -A ₇	Inputs	1.0/1.0	20 μA/-0.6 mA		
ō	Output	50/33.3	-1 mA/20 mA		

Function Table

	Inputs							Output
A ₀	A ₁	A ₂	A ₃	A ₄	A ₅	A ₆	A ₇	ō
L	Χ	Χ	Χ	Χ	Χ	Х	Х	Н
Χ	L	X	Χ	Χ	Χ	X	X	Н
Х	Χ	L	Χ	Χ	Χ	Χ	Χ	Н
Х	Χ	Χ	L	Χ	Χ	Χ	Χ	Н
Х	Χ	Χ	Χ	L	Χ	Χ	Χ	Н
Х	Χ	Χ	Χ	Χ	L	Χ	Χ	Н
Х	Χ	Χ	Χ	Χ	Χ	L	Χ	Н
Х	Χ	Χ	Χ	Χ	Χ	Χ	L	Н
Н	Н	Н	Н	Н	Н	Н	Н	L

H = HIGH Voltage Level

L = LOW Voltage Level X = Immaterial

Absolute Maximum Ratings(Note 2)

-65°C to +150°C Storage Temperature -55°C to +125°C

Ambient Temperature under Bias Junction Temperature under Bias -55°C to +150C V_{CC} Pin Potential to Ground Pin -0.5V to +7.0V Input Voltage (Note 3) -0.5V to +7.0V Input Current (Note 3) -30 mA to +5.0 mA

Voltage Applied to Output in HIGH State (with $V_{CC} = 0V$)

Standard Output -0.5V to V_{CC} 3-STATE Output -0.5V to +5.5V

Current Applied to Output

in LOW State (Max) twice the rated I_{OL} (mA)

Recommended Operating Conditions

Free Air Ambient Temperature 0°C to +70°C Supply Voltage +4.5V to +5.5V

Note 2: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

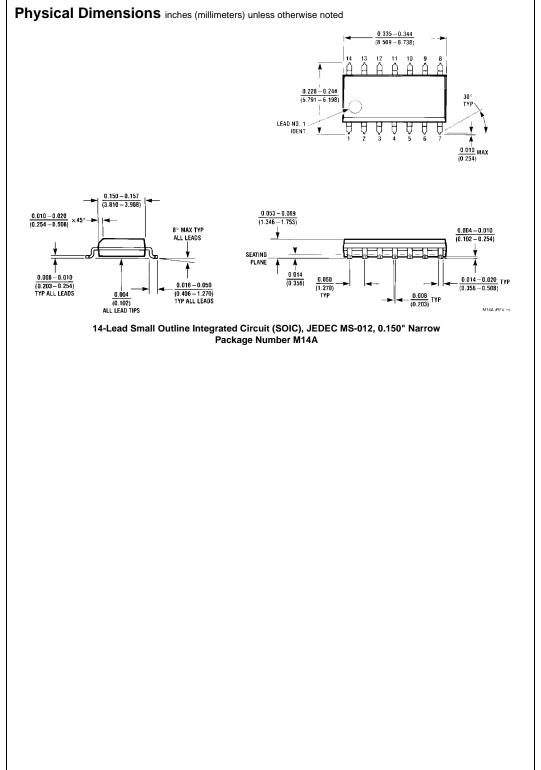
Note 3: Either voltage limit or current limit is sufficient to protect inputs.

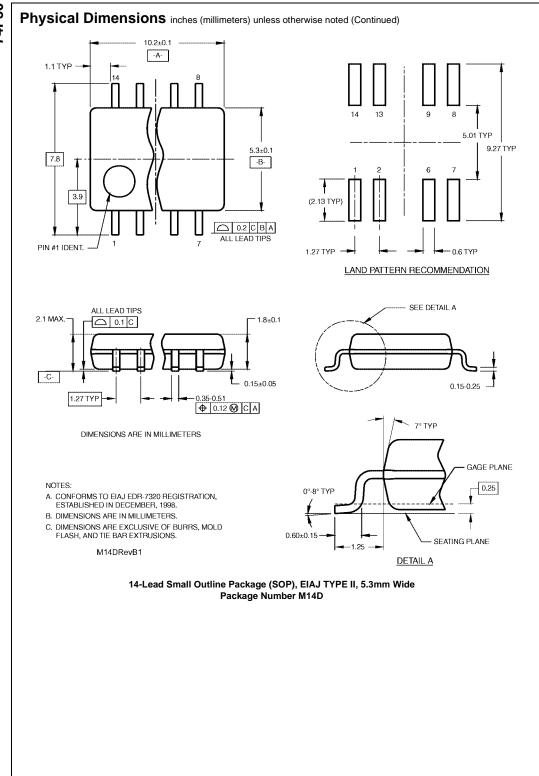
DC Electrical Characteristics

Symbol	bol Parameter		Min	Тур	Max	Units	v _{cc}	Conditions	
V _{IH}	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal	
V _{IL}	Input LOW Voltage				0.8	V		Recognized as a LOW Signal	
V _{CD}	Input Clamp Diode Voltage				-1.2	V	Min	$I_{IN} = -18 \text{ mA}$	
V _{OH}	Output HIGH	Output HIGH 10% V _{CC}				V	V Min	I _{OH} = -1 mA	
	Voltage	$5\% V_{CC}$	2.7			V	IVIIII	$I_{OH} = -1 \text{ mA}$	
V _{OL}	Output LOW Voltage	10% V _{CC}			0.5	V	Min	I _{OL} = 20 mA	
I _{IH}	Input HIGH Current				5.0	μА	Max	V _{IN} = 2.7V	
I _{BVI}	Input HIGH Current Breakdown Test				7.0	μА	Max	V _{IN} = 7.0V	
I _{CEX}	Output HIGH Leakage Current				50	μА	Max	V _{OUT} = V _{CC}	
V _{ID}	Input Leakage Test		4.75			V	0.0	$I_{ID} = 1.9 \mu\text{A}$ All Other Pins Grounded	
I _{OD}	Output Leakage Circuit Current				3.75	μА	0.0	V _{IOD} = 150 mV All Other Pins Grounded	
I _{IL}	Input LOW Current				-0.6	mA	Max	V _{IN} = 0.5V	
Ios	Output Short-Circuit Current		-60		-150	mA	Max	V _{OUT} = 0V	
I _{CCH}	Power Supply Current			0.5	1.5	mA	Max	V _O = HIGH	
I _{CCL}	Power Supply Current				4.5	mA	Max	$V_O = LOW$	

AC Electrical Characteristics

			$\textbf{T}_{\textbf{A}} = +25^{\circ}\textbf{C}$		$T_A = 0$ °C to +70°C			
Symbol	Parameter	$egin{aligned} V_{CC} = +5.0V \ C_L = 50 \ pF \end{aligned}$			V _{CC} = +5.0V C _L = 50 pF		Units	
		Min	Тур	Max	Min	Max		
t _{PLH}	Propagation Delay	1.0	3.7	5.0	1.0	5.5	ns	
t _{PHL}	A_n to \overline{O}	1.5	2.8	5.0	1.5	5.5	115	





Physical Dimensions inches (millimeters) unless otherwise noted (Continued) 0.740 - 0.770(18.80 - 19.56)0.090 (2.286) 14 13 12 11 10 9 8 14 13 12 0.250 ± 0.010 PIN NO. 1 IDENT PIN NO. 1 IDENT 1 2 3 4 5 6 7 1 2 3 $\frac{0.092}{(2.337)}$ DIA $\frac{0.030}{(0.762)}$ MAX OPTION 1 OPTION 02 $\frac{0.135 \pm 0.005}{(3.429 \pm 0.127)}$ 0.300 - 0.320 $\overline{(7.620 - 8.128)}$ 0.065 $\frac{0.145 - 0.200}{(3.683 - 5.080)}$ 0.060 4° TYP Optional (1.524) (1.651) $\frac{0.008 - 0.016}{(0.203 - 0.406)}$ TYP 0.020 (0.508) 0.125 - 0.150 0.075 ± 0.015 $\overline{(3.175 - 3.810)}$ 0.280 (1.905 ± 0.381) 0.014-0.023 TYP (7.112) MIN $\frac{0.100 \pm 0.010}{(2.540 \pm 0.254)} \text{ TYP}$ (0.356 - 0.584)

14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide Package Number N14A

 $\frac{0.050 \pm 0.010}{(1.270 - 0.254)} \text{ TYP}$

Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

- Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
- A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

 $0.325 + 0.040 \\ -0.015 \\ \hline (8.255 + 1.016) \\ -0.381)$

www.fairchildsemi.com

N144 (REV.E)