

Automotive 8 channels chip for advanced airbag applications



TQFP64 exposed pad down
(10x10x1.0 mm)

Features

- AEC-Q100 qualified 
- Squib/LEA deployment drivers
 - 8 channel HSD/LSD for squib load
 - 2 over 8 channels supporting LEA load
 - 2 channel couples supporting common-return connection
 - 18 V deployment voltage
 - Low, high and automatic dynamic deployment current profiles
 - R measure, STB, STG and leakage diagnostics
 - High and low side driver FET tests
 - LEA presence diagnostics
- Remote sensor interface and SYNC pulse supply voltage inputs and monitorings
- Two channel PSI-5 v2.3 remote sensor interface
- Two channel general purpose low side drivers with 0-100% PWM control
- Seven channel hall-effect, resistive or switch sensor interface
- System voltage diagnostics with integrated ADCs
- Temperature sensor
- 32 bit Global SPI bus interface
- 32 bit Remote Sensor SPI bus interface, SafeSPI v1.0 compatible
- Full ISO 26262 compliant, ASIL-D systems ready
- Packaging 64 pin

Product status link

[L9689E](#)

Product summary

Order code	Package	Packing
L9689E - TR	TQFP64EP 10x10x1.0 mm	Tape and reel

Description

The **L9689E** is an airbag extension chip, family compatible with L9691 and L9690 devices.

The IC includes eight deployment drivers, supporting both squib and low-energy actuator (LEA) loads (on two channels only). Additionally, it includes a two channels interface for PSI-5 remote sensors, a seven channels hall-effect/resistive sensor interface and two general purpose low-side driver outputs.

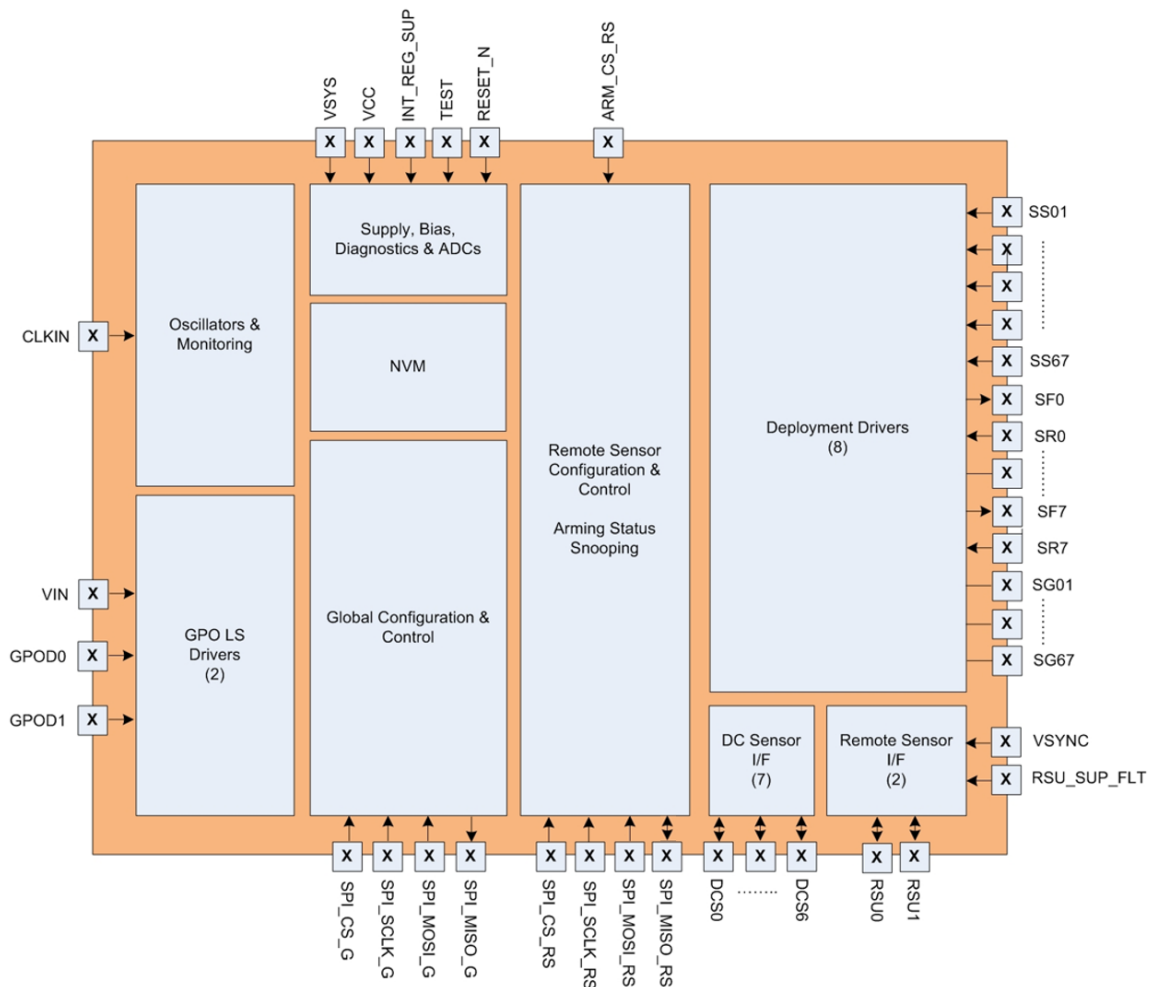
Dual SPI interfaces separate device global functions and remote sensors; all deployment loops are armed via snooping on the remote sensor SPI interface and an internal programmable mapping.

1 Block diagram and pin description

1.1 Block diagram

The L9689E IC is an application specific standard component for airbag system chip. Its main functions include deployment drivers (supporting both squib and low-energy actuator loads), remote sensor interfaces (supporting PSI-5 satellite sensors), diagnostics, deployment arming through remote sensor SPI communication snooping, hall-effect/switch sensor interfaces and general purpose output low-side drivers. A simplified block diagram for this IC is shown in the Figure 1.

Figure 1. Block diagram



1.2 Pin description

Figure 2. Device pinout

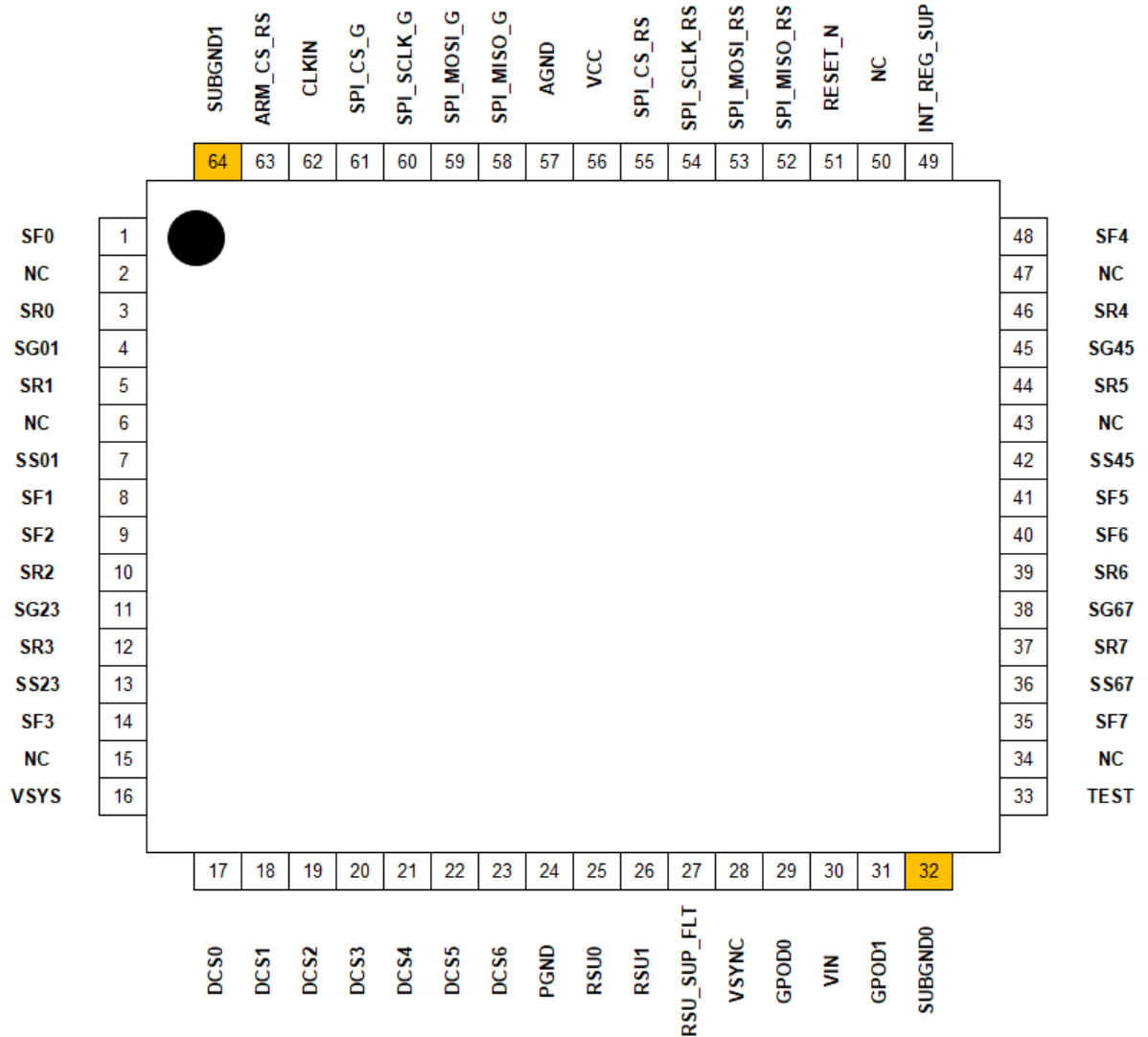


Table 1. Pin function

Pin #	Pin name	Description	I/O type	Class
1	SF0	Squib high-side channel 0	O	Global
2	NC	Not Connected	-	-
3	SR0	Squib low-side channel 0	O	Global
4	SG01	Squib low-side ground channel 0 and 1	S	Local
5	SR1	Squib low-side channel 1	O	Global
6	NC	Not Connected	-	-
7	SS01	Squib high-side supply channel 0 and 1	S	Local
8	SF1	Squib high-side channel 1	O	Global
9	SF2	Squib high-side channel 2	O	Global
10	SR2	Squib low-side channel 2	O	Global

Pin #	Pin name	Description	I/O type	Class
11	SG23	Squib low-side ground channel 2 and 3	S	Local
12	SR3	Squib low-side channel 3	O	Global
13	SS23	Squib high-side supply channel 2 and 3	S	Local
14	SF3	Squib high-side channel 3	O	Global
15	NC			
16	VSYS	Supply input voltage (DCS and deployment diagnostics)	S	Local
17	DCS0	DC sensor interface channel 0	O	Global
18	DCS1	DC sensor interface channel 1	O	Global
19	DCS2	DC sensor interface channel 2	O	Global
20	DCS3	DC sensor interface channel 3	O	Global
21	DCS4	DC sensor interface channel 4	O	Global
22	DCS5	DC sensor interface channel 5	O	Global
23	DCS6	DC sensor interface channel 6	O	Global
24	PGND	Power ground for GPOs and RSU	S	Local
25	RSU0	Remote sensor interface channel 0	O	Global
26	RSU1	Remote sensor interface channel 1	O	Global
27	RSU_SUP_FLT	RSU filtered supply input	S	Local
28	VSYNC	RSU SYNC pulse supply input	S	Local
29	GPOD0	General purpose drain output channel 0	O	Global
30	VIN	Battery input voltage (GPO diagnostic reference)	S	Global
31	GPOD1	General purpose drain output channel 1	O	Global
32	SUBGND0	Substrate ground 0 (fused with lead frame)	S	Local
33	TEST	Test-mode input	I	Local
34	NC	Not Connected	-	-
35	SF7	Squib/LEA high-side channel 7	O	Global
36	SS67	Squib/LEA high-side supply channel 6 and 7	S	Local
37	SR7	Squib/LEA low-side channel 7	O	Global
38	SG67	Squib/LEA low-side ground channel 6 and 7	S	Local
39	SR6	Squib/LEA low-side channel 6	O	Global
40	SF6	Squib/LEA high-side channel 6	O	Global
41	SF5	Squib high-side channel 5	O	Global
42	SS45	Squib high-side supply channel 4 and 5	S	Local
43	NC	Not Connected	-	-
44	SR5	Squib low-side channel 5	O	Global
45	SG45	Squib low-side ground channel 4 and 5	S	Local
46	SR4	Squib low-side channel 4	O	Global
47	NC	Not Connected	-	-
48	SF4	Squib high-side channel 4	O	Global
49	INT_REG_SUP	Internal regulator supply voltage pin	S	Local
50	NC	Not Connected	-	-
51	RESET_N	Reset input	I	Local

Pin #	Pin name	Description	I/O type	Class
52	SPI_MISO_RS	Remote sensor SPI data out/snooping input	I/O	Local
53	SPI_MOSI_RS	Remote sensor SPI data in	I	Local
54	SPI_SCLK_RS	Remote sensor SPI clock	I	Local
55	SPI_CS_RS	Remote sensor SPI chip select	I	Local
56	VCC	Digital supply input voltage	S	Local
57	AGND	Analog ground	S	Local
58	SPI_MISO_G	Global SPI data out	O	Local
59	SPI_MOSI_G	Global SPI data in	I	Local
60	SPI_SCLK_G	Global SPI clock	I	Local
61	SPI_CS_G	Global SPI chip select	I	Local
62	CLKIN	External clock input	I	Local
63	ARM_CS_RS	Arm status capture input (on remote sensor SPI)	I	Local
64	SUBGND1	Substrate ground 1 (fused with lead frame)	S	Local
-	Ex Pad Down	Substrate ground (backside)	S	Local

Legend: I = Input, O = Output, I/O = Input/Output, S = Supply or ground

2 Maximum ratings

2.1 Absolute maximum ratings

Maximum ratings are absolute ratings; exceeding any one of these values may cause permanent damage to the integrated circuit.

All voltages are related to the potential at substrate ground (SUBGND0 and SUBGND1).

Table 2. Absolute maximum ratings

Symbol	Parameter	Min	Typ	Max	Unit
SF0	Squib high-side channel 0	-1 ⁽¹⁾	-	40	V
NC	-	-	-	-	-
SR0	Squib low-side channel 0	-0.3	-	35	V
SG01	Squib low-side ground channel 0 and 1	-0.3	-	0.3	V
SR1	Squib low-side channel 1	-0.3	-	35	V
NC	-	-	-	-	-
SS01	Squib high-side supply channel 0 and 1	-0.3	-	40	V
SF1	Squib high-side channel 1	-1 ⁽¹⁾	-	40	V
SF2	Squib high-side channel 2	-1 ⁽¹⁾	-	40	V
SR2	Squib low-side channel 2	-0.3	-	35	V
[DOS_UR7E_0103010]SG23	Squib low-side ground channel 2 and 3	-0.3	-	0.3	V
SR3	Squib low-side channel 3	-0.3	-	35	V
SS23	Squib high-side supply channel 2 and 3	-0.3	-	40	V
SF3	Squib high-side channel 3	-1 ⁽¹⁾	-	40	V
NC	-	-	-	-	-
VSYS	Supply input voltage (DCS and deployment diagnostics)	-0.3	-	40	V
DCS0	DC sensor interface channel 0	-2	-	40	V
DCS1	DC sensor interface channel 1	-2	-	40	V
DCS2	DC sensor interface channel 2	-2	-	40	V
DCS3	DC sensor interface channel 3	-2	-	40	V
DCS4	DC sensor interface channel 4	-2	-	40	V
DCS5	DC sensor interface channel 5	-2	-	40	V
DCS6	DC sensor interface channel 6	-2	-	40	V
PGND	Power ground for GPOs and RSU	-0.3	-	0.3	V
RSU0	Remote sensor interface channel 0	-1	-	40	V
RSU1	Remote sensor interface channel 1	-1	-	40	V
RSU_SUP_FLT	RSU filtered supply input	-0.3	-	40	V
VSYNC	RSU SYNC pulse supply input	-0.3	-	40	V
GPOD0	General purpose drain output channel 0	-1	-	40	V
VIN	Battery input voltage (GPO diagnostic reference)	-1 ⁽²⁾	-	40	V
GPOD1	General purpose drain output channel 1	-1	-	40	V
SUBGND0	Substrate ground 0 (fused with lead frame)	-0.3	-	0.3	V
TEST	Test-mode input	-0.3	-	40	V

Symbol	Parameter	Min	Typ	Max	Unit
NC	-	-	-	-	-
SF7	Squib/LEA high-side channel 7	-1 ⁽¹⁾	-	40	V
SS67	Squib/LEA high-side supply channel 6 and 7	-0.3	-	40	V
SR7	Squib/LEA low-side channel 7	-0.3	-	35	V
SG67	Squib/LEA low-side ground channel 6 and 7	-0.3	-	0.3	V
SR6	Squib/LEA low-side channel 6	-0.3	-	35	V
SF6	Squib/LEA high-side channel 6	-1 ⁽¹⁾	-	40	V
SF5	Squib high-side channel 5	-1 ⁽¹⁾	-	40	V
SS45	Squib high-side supply channel 4 and 5	-0.3	-	40	V
NC	-	-	-	-	-
SR5	Squib low-side channel 5	-0.3	-	35	V
SG45	Squib low-side ground channel 4 and 5	-0.3	-	0.3	V
SR4	Squib low-side channel 4	-0.3	-	35	V
NC	-	-	-	-	-
SF4	Squib high-side channel 4	-1 ⁽¹⁾	-	40	V
RESET_N	Reset input	-0.3	-	min (VCC+0.3, 4.6)	V
SPI_MISO_RS	Remote sensor SPI data out	-0.3	-	min (VCC+0.3, 4.6)	V
SPI_MOSI_RS	Remote sensor SPI data in	-0.3	-	min (VCC+0.3, 4.6)	V
SPI_SCLK_RS	Remote sensor SPI clock	-0.3	-	min (VCC+0.3, 4.6)	V
SPI_CS_RS	Remote sensor SPI chip select	-0.3	-	min (VCC+0.3, 4.6)	V
VCC	VCC supply input voltage	-0.3	-	4.6	V
NC	-	-	-	-	-
INT_REG_SUP	Internal regulator supply voltage pin	-0.3	-	40	V
AGND	Analog ground	-0.3	-	0.3	V
SPI_MISO_G	Global SPI data out	-0.3	-	min (VCC+0.3, 4.6)	V
SPI_MOSI_G	Global SPI data in	-0.3	-	min (VCC+0.3, 4.6)	V
SPI_SCLK_G	Global SPI clock	-0.3	-	min (VCC+0.3, 4.6)	V
SPI_CS_G	Global SPI chip select	-0.3	-	min (VCC+0.3, 4.6)	V
CLKIN	External clock input	-0.3	-	min (VCC+0.3, 4.6)	V
ARM_CS_RS	Arm status capture input (on remote sensor SPI)	-0.3	-	min (VCC+0.3, 4.6)	V
SUBGND1	Substrate ground 1 (fused with lead frame)	-0.3	-	0.3	V
Ex Pad Down	Substrate ground (backside)	-0.3	-	0.3	V

1. In the case of deployment turn off the transient voltages on SS and SF pins can move away from each other until a maximum voltage of SS-SF < 45 V for a limited transient time (6.5 μ s maximum) with no damage on device. Additionally in this time transient, in worst case load condition (maximum load inductance 56 μ H) the peak energy that can be handled by the ESD protection on SF pin is 128 μ J within a maximum time of 6.5 μ s.
2. Valid in transient conditions only.

Table 3. ESD protection

Symbol	Parameter	Min	Typ	Max	Unit
All pins	HBM	-2	-	2	kV
All pins	CDM (values for corner pins in brackets)	-500/(-750)	-	500/(750)	V

Symbol	Parameter	Min	Typ	Max	Unit
Global pins	HBM	-4	-	4	kV

2.2 Temperature ranges and thermal data

Table 4. Temperature ranges and thermal data

Symbol	Parameter	Min	Max	Unit
T_{AMB}	Operating temperature (ECU environment)	-40	105	°C
T_J	Operating junction temperature	-40	175	°C
T_{STG}	Storage temperature	-55	150	°C
$R_{TH_J_CASE}$	Thermal resistance junction to case	-	2	°C/W

3 Device overview

3.1 Main features

- Dedicated INT_REG_SUP pin, providing supply voltage to the internal low voltage regulators
- Dedicated VCC pin, providing supply voltage to the digital I/Os and the internal low voltage regulator supplying the digital circuitry
- Dedicated VSYS pin, providing supply voltage to DC sensor interfaces and deployment diagnostic circuits
- Internal 16 MHz oscillator for timing generation
- Internal 10 MHz oscillator for monitoring
- Dedicated CLKIN pin to provide an external 4 MHz clock, 1% accurate, to improve timing accuracy (by FLL circuitry)
- RESET_N reset input pin
- Power-supply voltage and die average temperature monitoring by dedicated A/D converter
- Internal NVM, used for trimming

3.2 SPI interface

- One dedicated 32-bit SPI bus for global configuration and control
- One dedicated 32-bit SPI bus for remote sensor configuration and control, SafeSPI v1.0 compatible

3.3 Deployment drivers and diagnostics

- 8 high-side deployment drivers, 8 low side deployment drivers
- Low-energy actuator (LEA) support available on 2 channels (6 and 7)
- Common-return (CSRx) connection support available on 2 channel couples (2-3 and 4-5)
- Independently controlled high-side and low-side FETs
- User-programmable deployment options
 - Low current: 1.21 A minimum
 - High current: 1.76 A minimum
 - Programmable dwell time in 16 μ s increments
 - Automatic dynamic deployment current profile
- Configurable deployment current monitor feature
- Deployment interruption in case of high-side short to ground and/or supply overvoltage
- Squib/LEA resistance measurement
- High and low-side FET tests
- Open and shorts diagnostics, including between loop drivers
- LEA diode presence/integrity diagnostics

3.4 Remote sensor interfaces

- 2 channel receiver, PSI-5 v2.3 compatible with SYNC pulse
- Dedicated supply input pins for both satellite and SYNC pulse operation
- Current limit with short circuit protection diagnostics
- Auto-adjusting current trip points for each channel
- Satellite data with parity and CRC, 10 bit, 16 bit and 20 bit messages, 125 k or 189 kbps
- Satellite message error detection

3.5 DC sensor interfaces

- 7 integrated interfaces with current sense capability
- Compatible with Hall-effect, resistive and switch sensors
- Current limit protected output

- Capability to inhibit passenger airbag loops via monitoring of RS_SPI from System Basis device

3.6 General purpose low-side outputs

- 2 low-side drivers
- ON-OFF mode and PWM 0-100% fine control
- Diagnostics for short circuit protection and open load detection
- Current limit protected

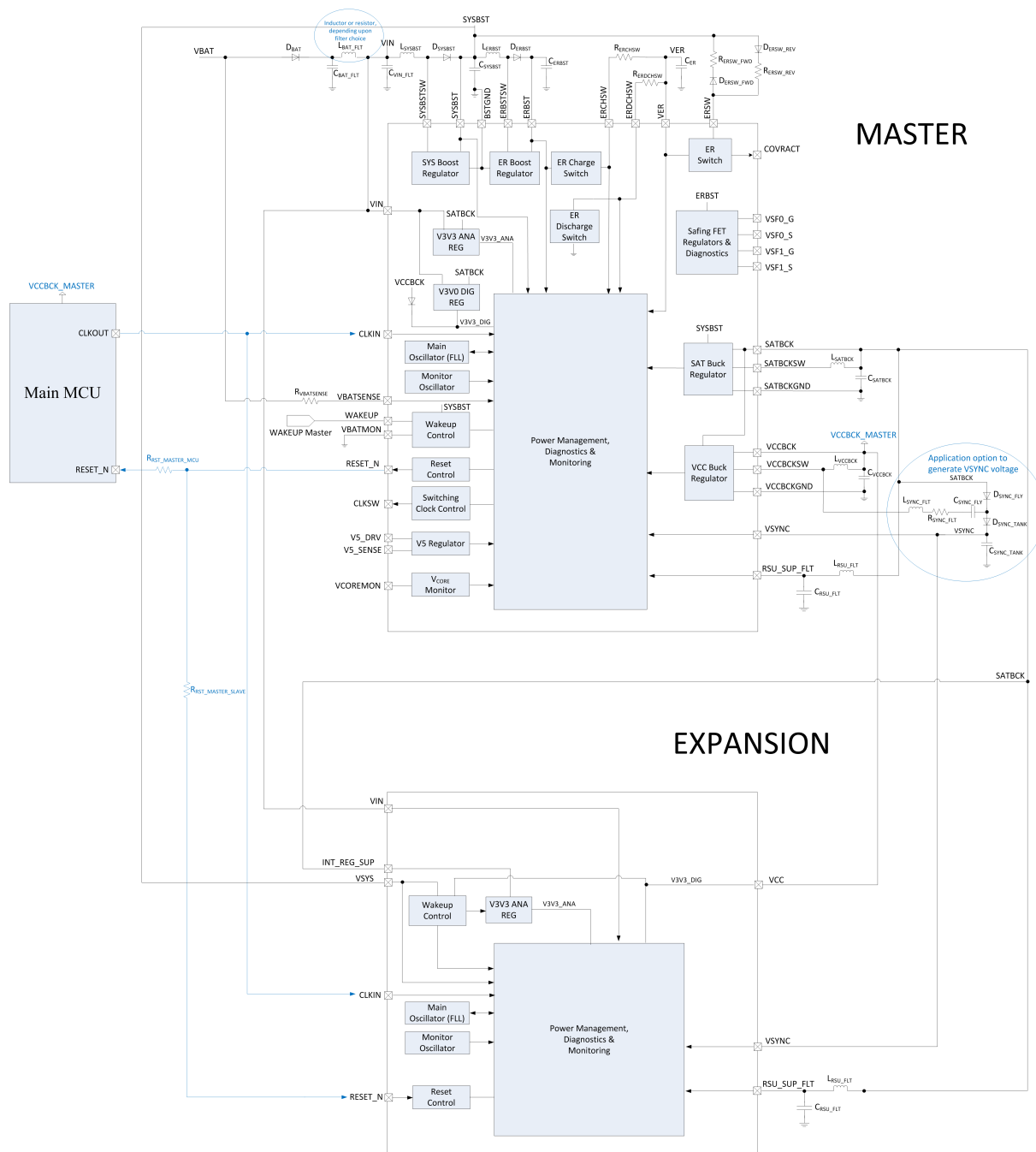
3.7 A/D converters

- One A/D converter dedicated to power-supply voltage and die average temperature monitoring, providing a 10 bit conversion via Global SPI and with the capability to handle a queue of 4 conversion requests
- One A/D converter dedicated to deployment circuitry voltage monitoring, providing a 10 bit conversion via Global SPI and with the capability to handle one conversion request per time
- One A/D converter dedicated to deployment leakage current diagnostic, providing a 10 bit conversion of the measured leakage current via Global SPI; this current A/D converter is shared among all 8 deployment channels
- 2 A/D converters dedicated to remote sensor interfaces, providing a 10 bit conversion of the sensor current value and used for sensor communication decoding; each RSU channel have a dedicated current A/D converter
- 2 A/D converters dedicated to DC sensor interfaces, one providing the voltage value (10 bit conversion) and the other one providing the current value (10 bit conversion); the 2 A/D converters are shared among all 7 DC sensor channels. Conversions are provided via Global SPI, with the capability to handle a queue of 4 conversion requests

4 Applicative circuit

A typical connection between L9689E Expansion device and L9691 Master device is shown in [Figure 3](#).

Figure 3. Example of dual chip/Master-Expansion scenario



5 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

5.1 TQFP64 (10X10X1.0 mm, 6.0x6.0 mm exp. pad down) package information

Figure 4. TQFP64 (10X10X1.0 mm, 6.0x6.0 mm exp. pad down) package outline

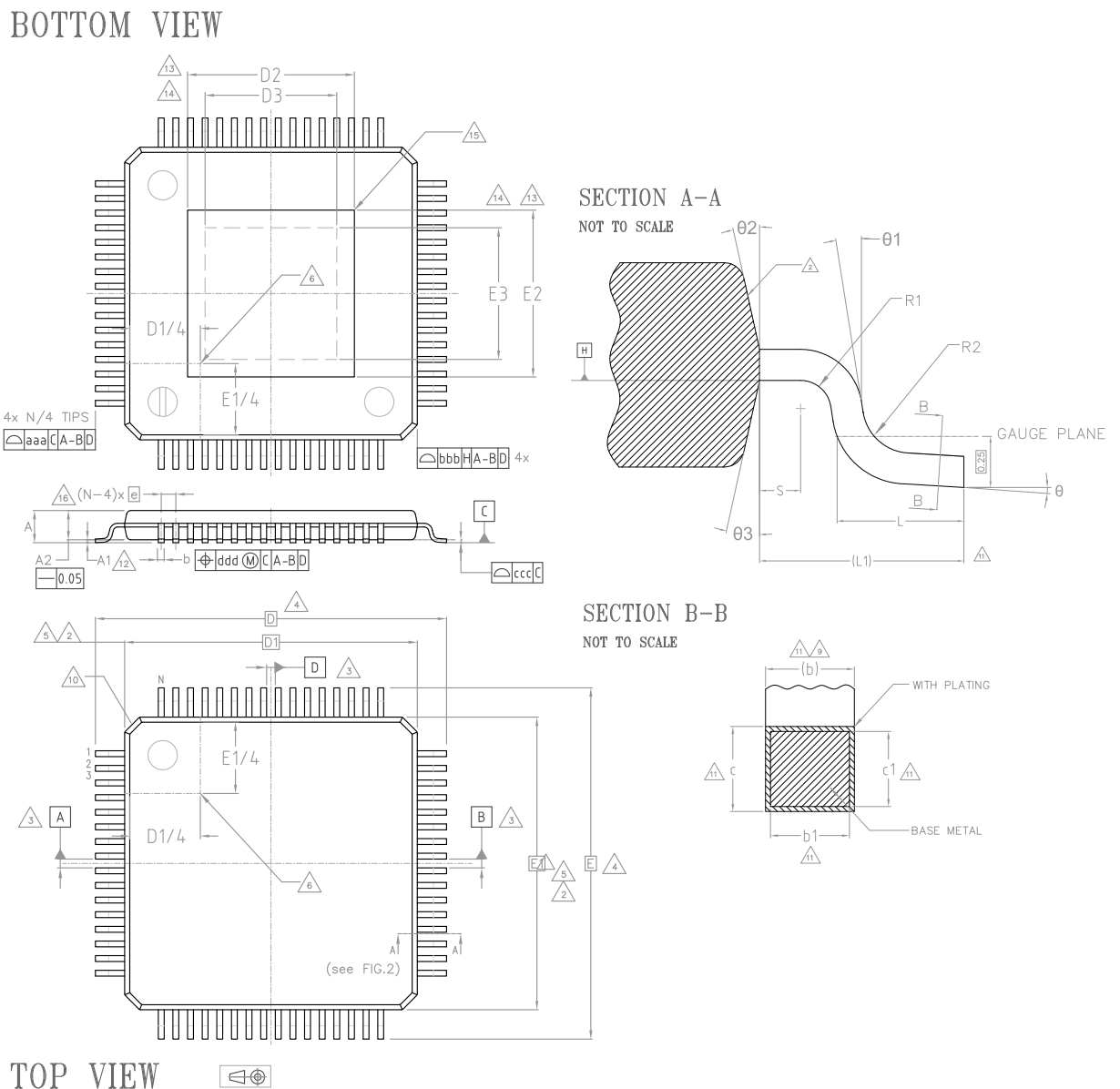


Table 5. TQFP64 (10X10X1.0 mm, 6.0x6.0 mm exp. pad down) package mechanical data

Symbol	Dimensions in mm		
	Min.	Typ.	Max.
θ	0°	3.5°	7°
θ_1	0°	-	-

Symbol	Dimensions in mm		
	Min.	Typ.	Max.
Ø2	10°	12°	14°
Ø3	10°	12°	14°
A	-	-	1.20
A1	0.05	-	0.15
A2	0.95	1.00	1.05
b	0.17	0.22	0.27
b1	0.17	0.20	0.23
c	0.09	-	0.20
c1	0.09	-	0.16
D	12.00 BSC		
D1	10.00 BSC		
D2 ⁽¹⁾	-	-	6.40
D3 ⁽²⁾	4.80	-	-
e	0.50 BSC		
E	12.00 BSC		
E1	10.00 BSC		
E2 ⁽¹⁾	-	-	6.40
E3 ⁽²⁾	4.80	-	-
L	0.45	0.60	0.75
L1	1.00 REF		
N	64		
R1	0.08	-	-
R2	0.08	-	0.20
S	0.20	-	-
Tolerance of form and position			
aaa	0.20		
bbb	0.20		
ccc	0.08		
ddd	0.08		

1. Dimensions D2 and E2 show the maximum exposed metal area on the package surface where the exposed pad is located (if present). It includes all metal protrusions from exposed pad itself. End user should verify D2 and E2 dimensions according to specific device application.
2. Dimensions D3 and E3 show the minimum solderable area, defined as the portion of exposed pad which is guaranteed to be free from resin flashes/bleeds, bordered by internal edge of inner groove.

Figure 1: Layout of the proposed 16x16 array. The diagram shows a central 16x16 array of thermal vias (n.20, pitch=1.5x1.0) surrounded by a 4x4 array of thermal pads (n.25, pitch=1.5x1.5). The layout includes dimensions for the array, pads, and vias, as well as labels for 'THERMAL PAD' and 'THERMAL VIA'.

This is a draft proposal only and it might be not in line with customer or pcb supplier design rules.

Revision history

Table 6. Document revision history

Date	Version	Changes
12-Aug-2022	1	Initial release.
06-Sep-2022	2	Updated title in cover page.

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