

TSM650P02CX

20V P-Channel Power MOSFET

SOT-23



Pin Definition:

1. Gate
2. Source
3. Drain

Note:

MSL 1 (Moisture Sensitivity Level) per J-STD-020

Key Parameter Performance

Parameter	Value	Unit
V_{DS}	-20	V
$R_{DS(on)}$ (max)	$V_{GS} = -4.5V$	65
	$V_{GS} = -2.5V$	85
	$V_{GS} = -1.8V$	130
Q_g	6.4	nC

Features

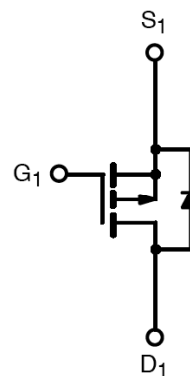
- Fast switching
- Suited for -1.8V gate drive applications
- Halogen-free

Ordering Information

Ordering code	Package	Packing
TSM650P02CX RFG	SOT-23	3kcs / 7" Reel

Note: Halogen-free according to IEC 61249-2-21 definition

Block Diagram



P-Channel MOSFET

Absolute Maximum Ratings ($T_c = 25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	-20	V
Gate-Source Voltage	V_{GS}	± 10	V
Continuous Drain Current	I_D	$T_c = 25^\circ C$	-4.1
		$T_c = 100^\circ C$	-2.6
Pulsed Drain Current (Note 1)	I_{DM}	-16.4	A
Power Dissipation @ $T_c = 25^\circ C$	P_D	1.56	W
Operating Junction Temperature	T_J	-55 to +150	$^\circ C$
Storage Temperature Range	T_{STG}	-55 to +150	$^\circ C$

Thermal Performance

Parameter	Symbol	Limit	Unit
Thermal Resistance - Junction to Ambient	$R_{\theta JA}$	80	$^\circ C/W$

Electrical Specifications (T_C = 25°C unless otherwise noted)

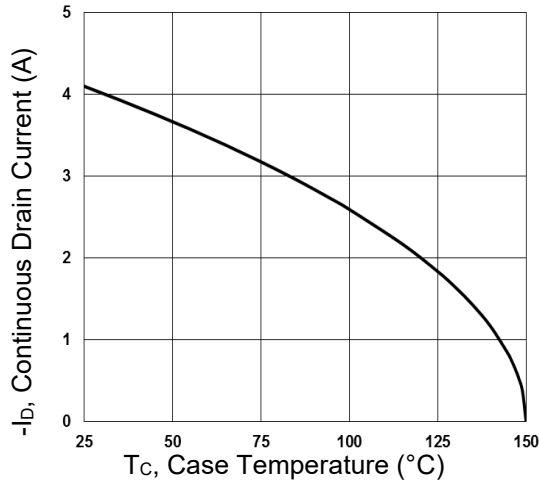
Parameter	Conditions	Symbol	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	V _{GS} = 0V, I _D = -250μA	BV _{DSS}	-20	--	--	V
Drain-Source On-State Resistance	V _{GS} = -4.5V, I _D = -3A	R _{DS(on)}	--	52	65	mΩ
	V _{GS} = -2.5V, I _D = -2A		--	73	85	
	V _{GS} = -1.8V, I _D = -1.5A		--	105	130	
Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = -250μA	V _{GS(TH)}	-0.4	-0.6	-0.8	V
Zero Gate Voltage Drain Current	V _{DS} = -20V, V _{GS} = 0V	I _{DSS}	--	--	-1	μA
	V _{DS} = -16V, T _J = 125°C		--	--	-10	
Gate Body Leakage	V _{GS} = ±10V, V _{DS} = 0V	I _{GSS}	--	--	±100	nA
Forward Transconductance (Note 2)	V _{DS} = -10V, I _D = -3A	g _{fs}	--	5.5	--	S
Dynamic						
Total Gate Charge (Note 2,3)	V _{DS} = -10V, I _D = -3A, V _{GS} = -4.5V	Q _g	--	6.4	--	nC
Gate-Source Charge (Note 2,3)		Q _{gs}	--	0.9	--	
Gate-Drain Charge (Note 2,3)		Q _{gd}	--	1.6	--	
Input Capacitance	V _{DS} = -10V, V _{GS} = 0V, f = 1.0MHz	C _{iss}	--	515	--	pF
Output Capacitance		C _{oss}	--	55	--	
Reverse Transfer Capacitance		C _{rss}	--	20	--	
Switching						
Turn-On Delay Time (Note 2,3)	V _{DD} = -10V, I _D = -1A, V _{GS} = -4.5V, R _{GEN} = 25Ω	t _{d(on)}	--	5	--	ns
Turn-On Rise Time (Note 2,3)		t _r	--	17.4	--	
Turn-Off Delay Time (Note 2,3)		t _{d(off)}	--	40.7	--	
Turn-Off Fall Time (Note 2,3)		t _f	--	11.4	--	
Source-Drain Diode Ratings and Characteristic						
Maximum Continuous Drain-Source Diode Forward Current	Integral reverse diode in the MOSFET	I _S	--	--	-4.1	A
Maximum Pulse Drain-Source Diode Forward Current		I _{SM}	--	--	-16.4	A
Diode-Source Forward Voltage	V _{GS} = 0V, I _S = -1A	V _{SD}	--	--	-1	V

Note:

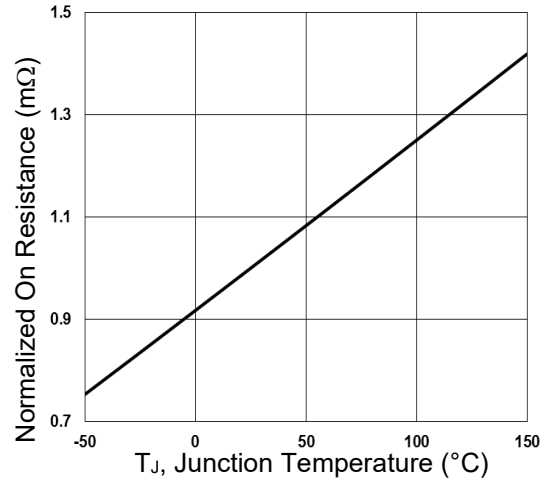
1. Pulse width limited by safe operating area
2. Pulse test: pulse width ≤ 300μs, duty cycle ≤ 2%
3. Switching time is essentially independent of operating temperature.

Electrical Characteristics Curve

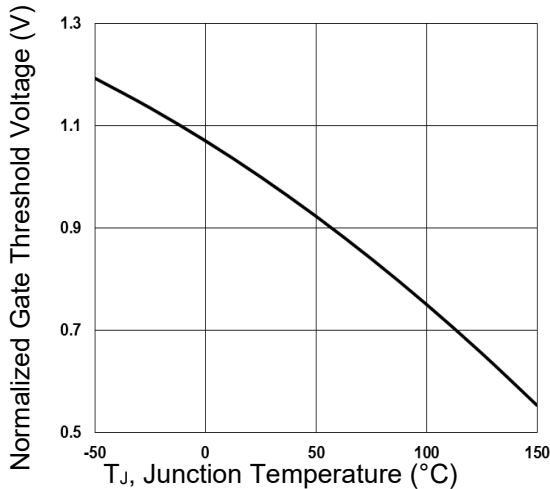
Continuous Drain Current vs. T_C



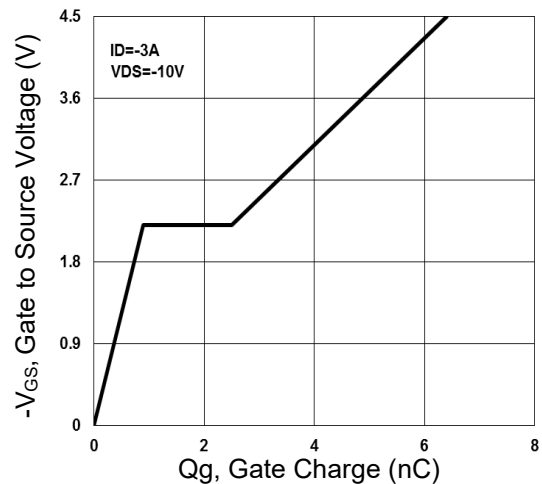
Normalized R_{DS(on)} VS. T_J



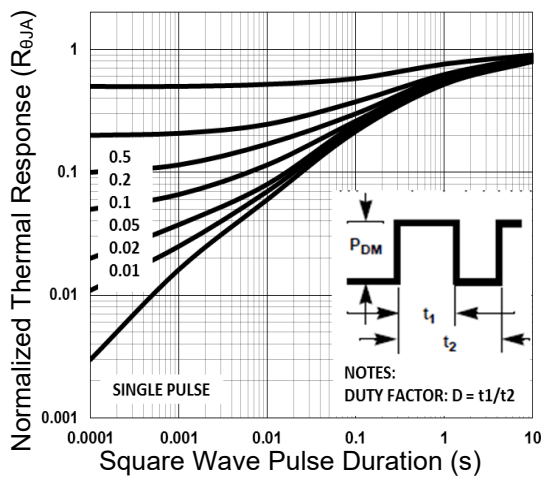
Threshold Voltage vs. Junction Temperature



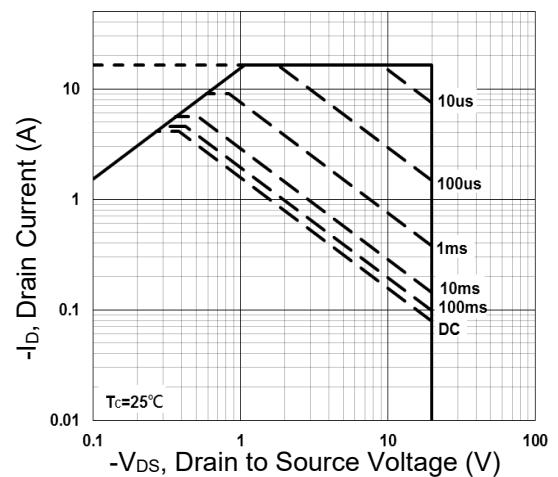
Gate Charge Waveform



Normalized Thermal Transient Impedance Curve

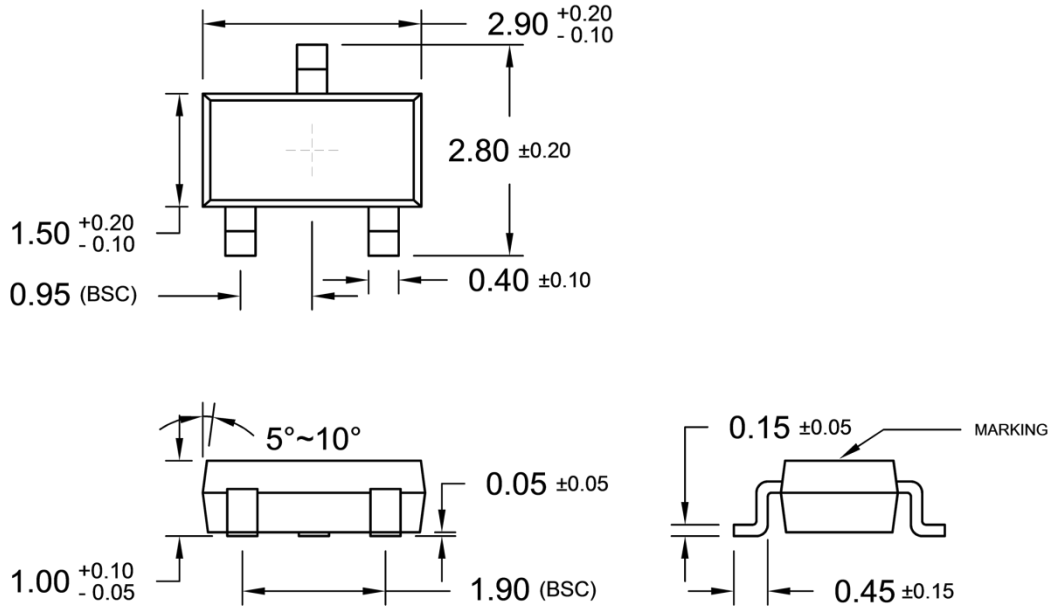


Maximum Safe Operating Area



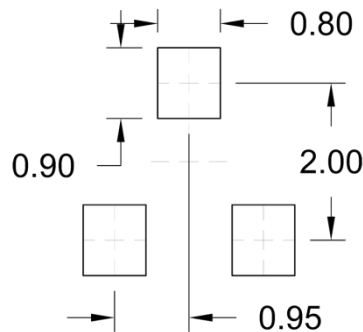


SOT-23 Mechanical Drawing

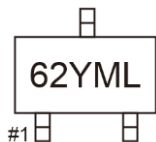


Unit: Millimeters

SUGGESTED PAD LAYOUT (Unit: Millimeters)



Marking Diagram



- 62** = Device Code
- Y** = Year Code
- M** = Month Code for Halogen Free Product
(**O**=Jan, **P**=Feb, **Q**=Mar, **R**=Apr, **S**=May, **T**=Jun, **U**=Jul, **V**=Aug, **W**=Sep, **X**=Oct, **Y**=Nov, **Z**=Dec)
- L** = Lot Code

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