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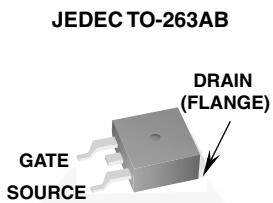
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www.onsemi.com

Please note: As part of the Fairchild Semiconductor integration, some of the Fairchild orderable part numbers will need to change in order to meet ON Semiconductor's system requirements. Since the ON Semiconductor product management systems do not have the ability to manage part nomenclature that utilizes an underscore (_), the underscore (_) in the Fairchild part numbers will be changed to a dash (-). This document may contain device numbers with an underscore (_). Please check the ON Semiconductor website to verify the updated device numbers. The most current and up-to-date ordering information can be found at www.onsemi.com. Please email any questions regarding the system integration to Fairchild_questions@onsemi.com.

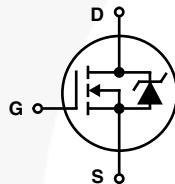
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N-Channel UltraFET Power MOSFET
100 V, 75 A, 14 mΩ

Packaging



Symbol



Absolute Maximum Ratings $T_C = 25^\circ\text{C}$, Unless Otherwise Specified

	HUFA75645S3S	UNITS
Drain to Source Voltage (Note 1)	V_{DSS}	V
Drain to Gate Voltage ($R_{GS} = 20\text{k}\Omega$) (Note 1)	V_{DGR}	V
Gate to Source Voltage	V_{GS}	± 20
Drain Current		
Continuous ($T_C = 25^\circ\text{C}$, $V_{GS} = 10\text{V}$) (Figure 2)	I_D	A
Continuous ($T_C = 100^\circ\text{C}$, $V_{GS} = 10\text{V}$) (Figure 2)	I_D	A
Pulsed Drain Current	I_{DM}	Figure 4
Pulsed Avalanche Rating	UIS	Figures 6, 14, 15
Power Dissipation	P_D	W
Derate Above 25°C		$W/\text{^\circ C}$
Operating and Storage Temperature	T_J , T_{STG}	$^\circ\text{C}$
Maximum Temperature for Soldering		
Leads at 0.063in (1.6mm) from Case for 10s.	T_L	$^\circ\text{C}$
Package Body for 10s, See Techbrief TB334	T_{pkg}	$^\circ\text{C}$

NOTES:

1. $T_J = 25^\circ\text{C}$ to 150°C .

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

HUFA75645S3S

Electrical Specifications $T_C = 25^\circ\text{C}$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS	
OFF STATE SPECIFICATIONS							
Drain to Source Breakdown Voltage	BV_{DSS}	$I_D = 250\mu\text{A}, V_{\text{GS}} = 0\text{V}$ (Figure 11)	100	-	-	V	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{\text{DS}} = 95\text{V}, V_{\text{GS}} = 0\text{V}$	-	-	1	μA	
		$V_{\text{DS}} = 90\text{V}, V_{\text{GS}} = 0\text{V}, T_C = 150^\circ\text{C}$	-	-	250	μA	
Gate to Source Leakage Current	I_{GSS}	$V_{\text{GS}} = \pm 20\text{V}$	-	-	± 100	nA	
ON STATE SPECIFICATIONS							
Gate to Source Threshold Voltage	$V_{\text{GS(TH)}}$	$V_{\text{GS}} = V_{\text{DS}}, I_D = 250\mu\text{A}$ (Figure 10)	2	-	4	V	
Drain to Source On Resistance	$r_{\text{DS(ON)}}$	$I_D = 75\text{A}, V_{\text{GS}} = 10\text{V}$ (Figure 9)	-	0.0115	0.014	Ω	
THERMAL SPECIFICATIONS							
Thermal Resistance Junction to Case	$R_{\theta\text{JC}}$	TO-263	-	-	0.48	$^\circ\text{C}/\text{W}$	
Thermal Resistance Junction to Ambient	$R_{\theta\text{JA}}$		-	-	62	$^\circ\text{C}/\text{W}$	
SWITCHING SPECIFICATIONS ($V_{\text{GS}} = 10\text{V}$)							
Turn-On Time	t_{ON}	$V_{\text{DD}} = 50\text{V}, I_D = 75\text{A}$ $V_{\text{GS}} = 10\text{V},$ $R_{\text{GS}} = 2.5\Omega$ (Figures 18, 19)	-	-	197	ns	
Turn-On Delay Time	$t_{\text{d(ON)}}$		-	14	-	ns	
Rise Time	t_r		-	117	-	ns	
Turn-Off Delay Time	$t_{\text{d(OFF)}}$		-	41	-	ns	
Fall Time	t_f		-	97	-	ns	
Turn-Off Time	t_{OFF}		-	-	207	ns	
GATE CHARGE SPECIFICATIONS							
Total Gate Charge	$Q_{\text{g(TOT)}}$	$V_{\text{GS}} = 0\text{V}$ to 20V	$V_{\text{DD}} = 50\text{V},$ $I_D = 75\text{A},$ $I_{\text{g(REF)}} = 1.0\text{mA}$ (Figures 13, 16, 17)	-	198	238	nC
Gate Charge at 10V	$Q_{\text{g(10)}}$	$V_{\text{GS}} = 0\text{V}$ to 10V		-	106	127	nC
Threshold Gate Charge	$Q_{\text{g(TH)}}$	$V_{\text{GS}} = 0\text{V}$ to 2V		-	6.8	8.2	nC
Gate to Source Gate Charge	Q_{gs}	-		14	-	nC	
Gate to Drain "Miller" Charge	Q_{gd}	-		41	-	nC	
CAPACITANCE SPECIFICATIONS							
Input Capacitance	C_{ISS}	$V_{\text{DS}} = 25\text{V}, V_{\text{GS}} = 0\text{V},$ $f = 1\text{MHz}$ (Figure 12)	-	3790	-	pF	
Output Capacitance	C_{OSS}		-	810	-	pF	
Reverse Transfer Capacitance	C_{RSS}		-	230	-	pF	

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage	V_{SD}	$I_{\text{SD}} = 75\text{A}$	-	-	1.25	V
		$I_{\text{SD}} = 35\text{A}$	-	-	1.00	V
Reverse Recovery Time	t_{rr}	$I_{\text{SD}} = 75\text{A}, dI_{\text{SD}}/dt = 100\text{A}/\mu\text{s}$	-	-	145	ns
Reverse Recovered Charge	Q_{RR}	$I_{\text{SD}} = 75\text{A}, dI_{\text{SD}}/dt = 100\text{A}/\mu\text{s}$	-	-	360	nC

Typical Performance Curves

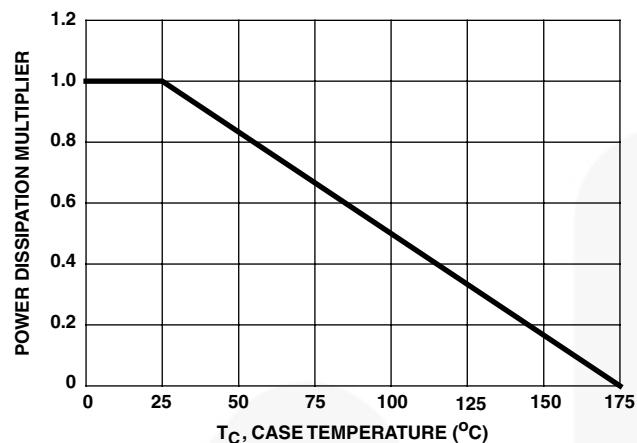


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

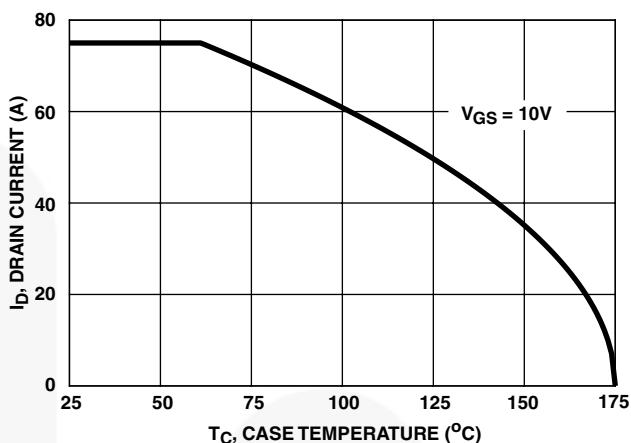


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

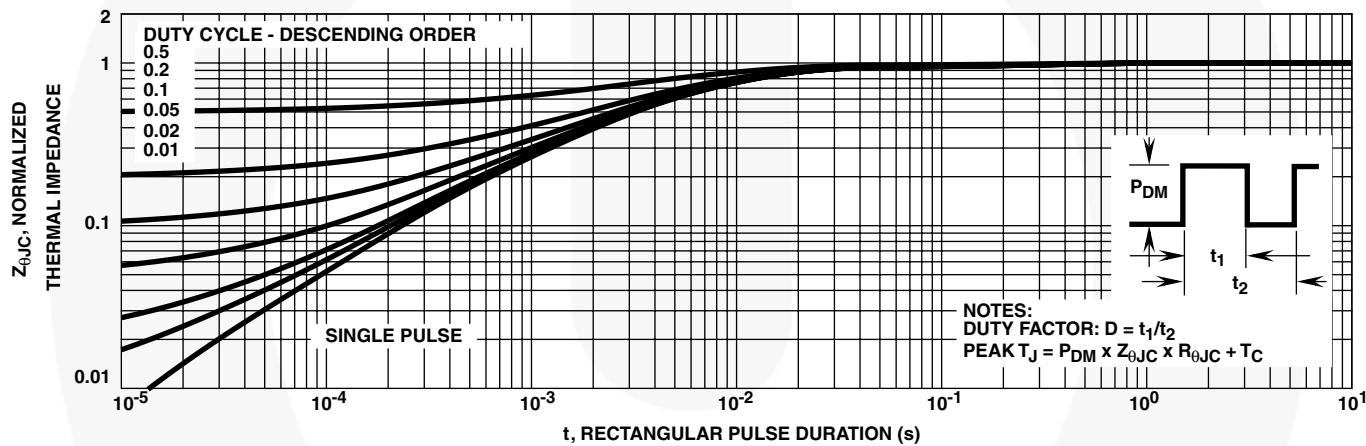


FIGURE 3. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

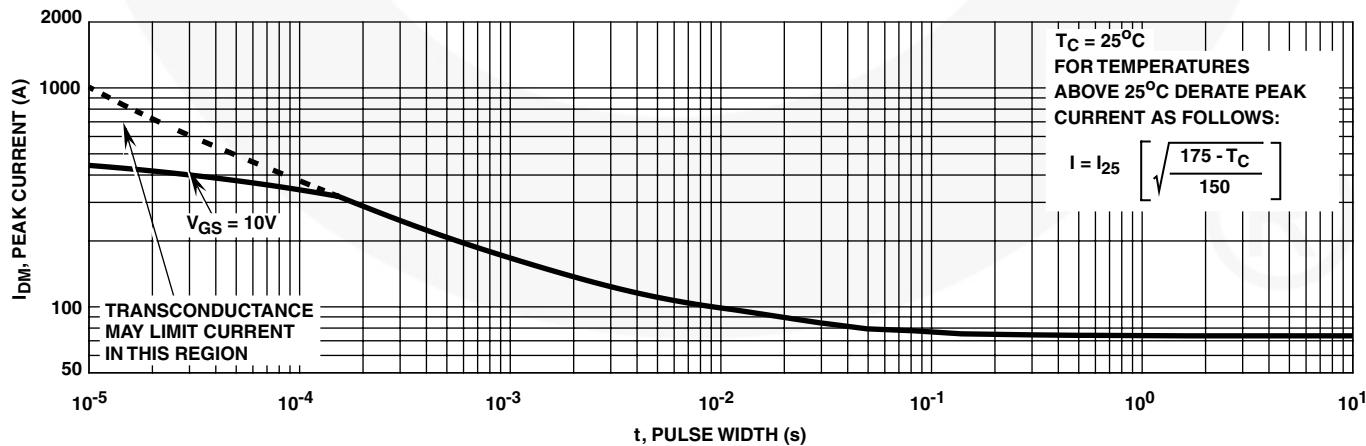


FIGURE 4. PEAK CURRENT CAPABILITY

Typical Performance Curves (Continued)

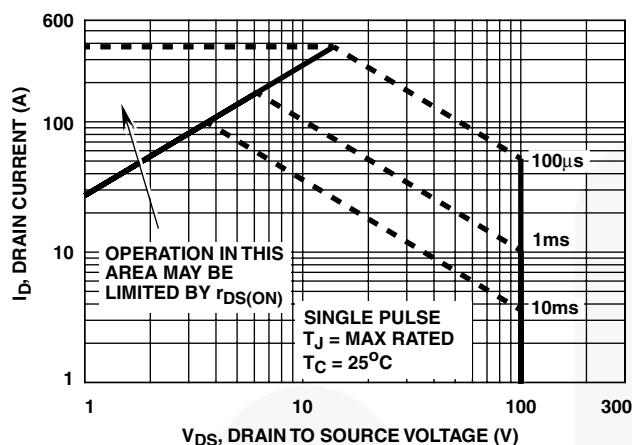
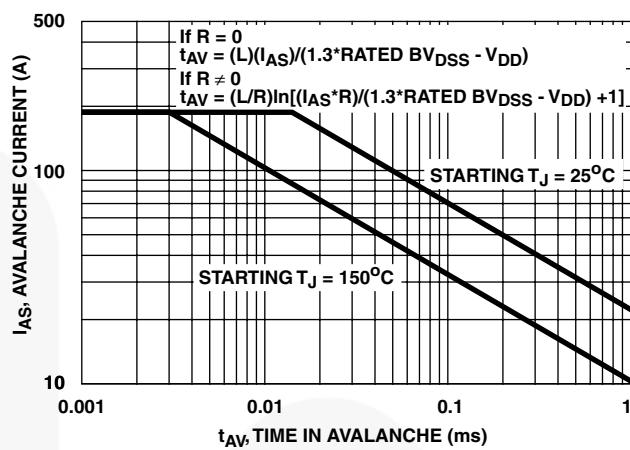


FIGURE 5. FORWARD BIAS SAFE OPERATING AREA



NOTE: Refer to Fairchild Application Notes AN9321 and AN9322.

FIGURE 6. UNCLAMPED INDUCTIVE SWITCHING CAPABILITY

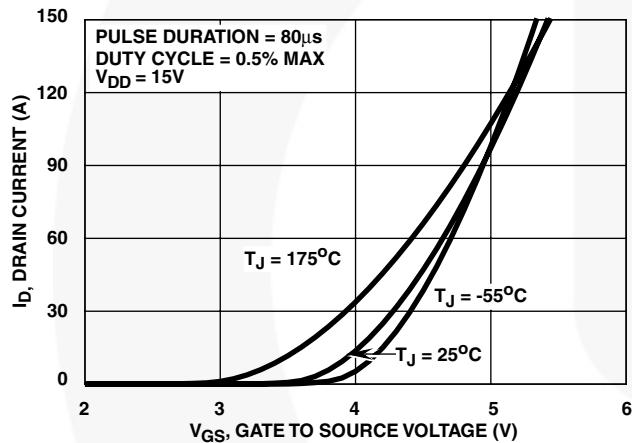


FIGURE 7. TRANSFER CHARACTERISTICS

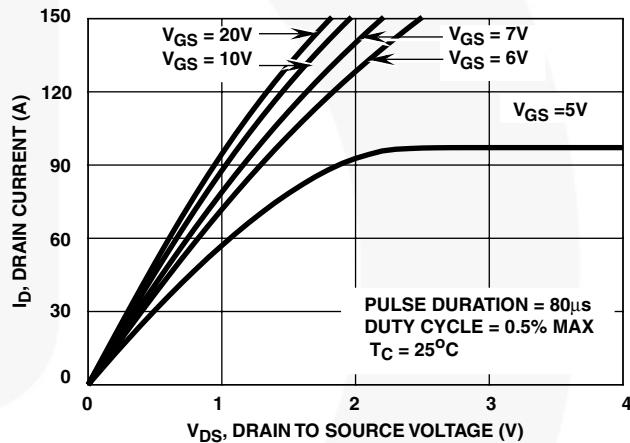


FIGURE 8. SATURATION CHARACTERISTICS

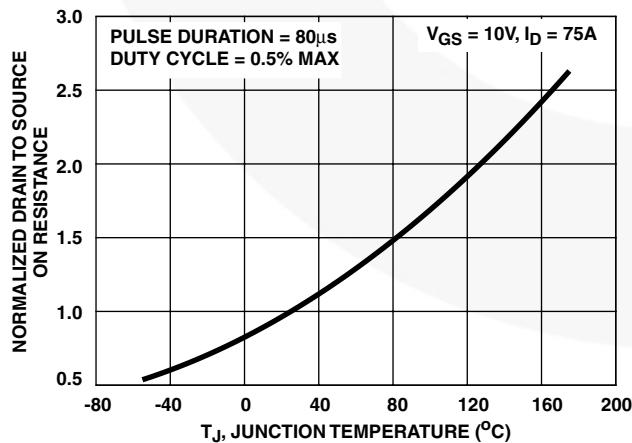


FIGURE 9. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

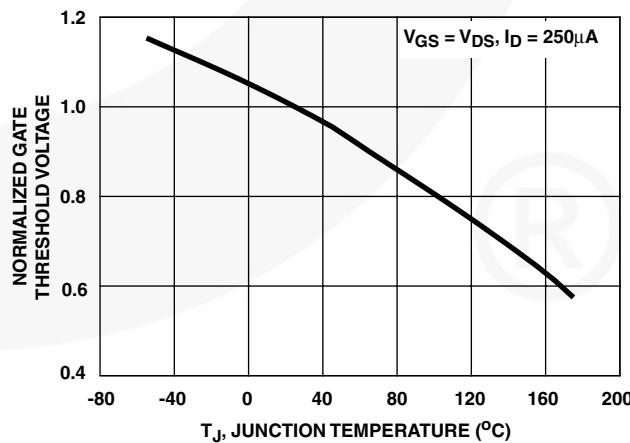


FIGURE 10. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

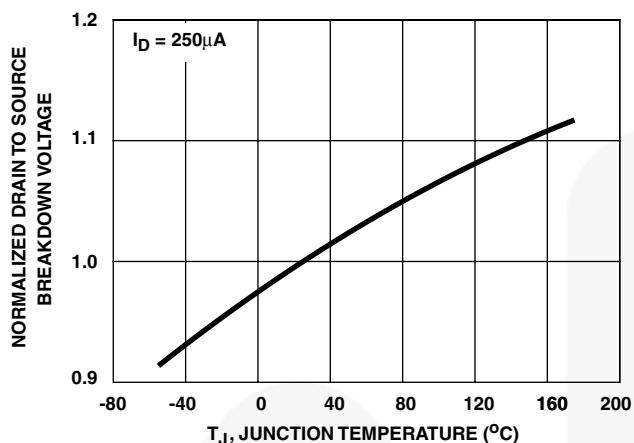
Typical Performance Curves (Continued)

FIGURE 11. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

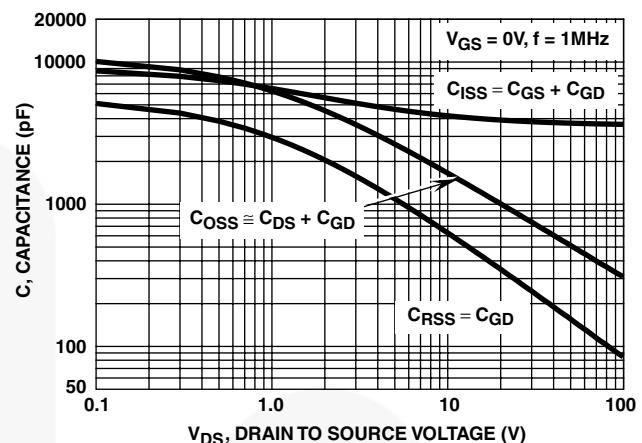
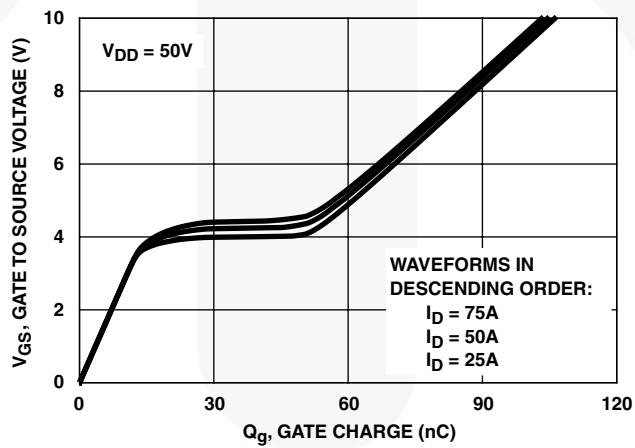


FIGURE 12. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE



NOTE: Refer to Fairchild Application Notes AN7254 and AN7260.

FIGURE 13. GATE CHARGE WAVEFORMS FOR CONSTANT GATE CURRENT

Test Circuits and Waveforms

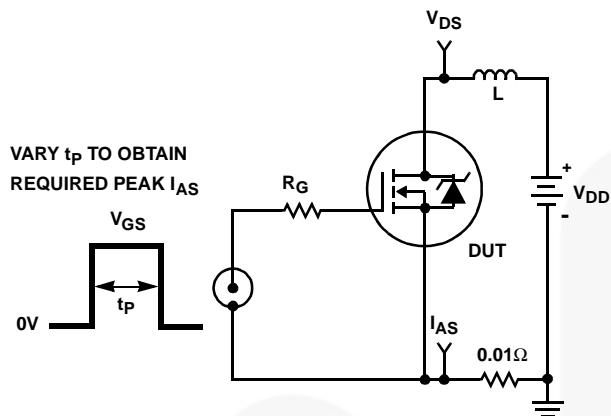


FIGURE 14. UNCLAMPED ENERGY TEST CIRCUIT

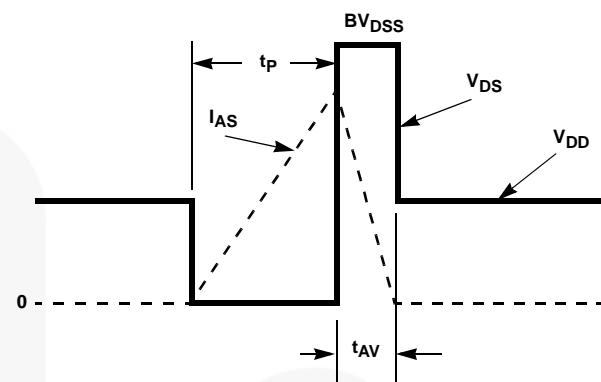


FIGURE 15. UNCLAMPED ENERGY WAVEFORMS

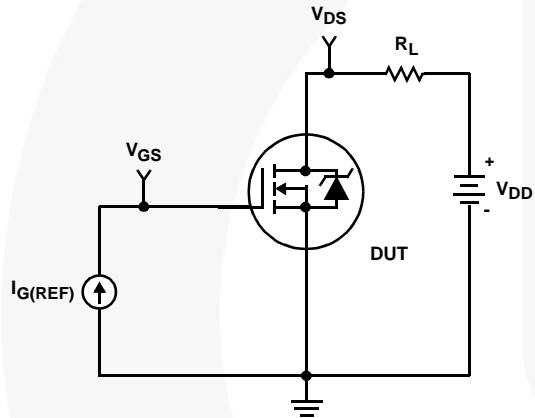


FIGURE 16. GATE CHARGE TEST CIRCUIT

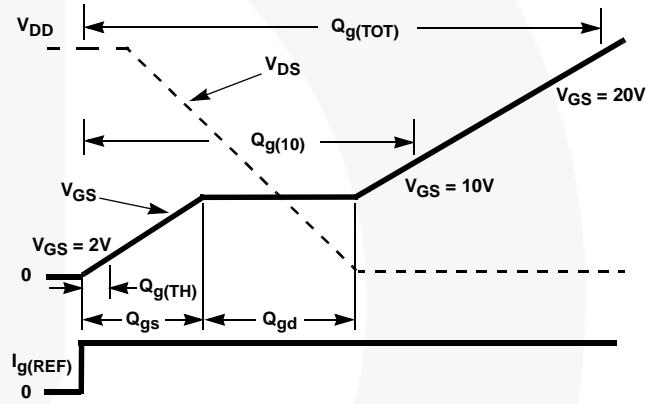


FIGURE 17. GATE CHARGE WAVEFORM

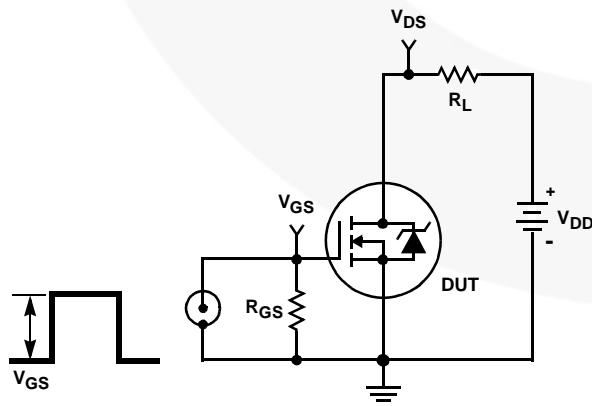


FIGURE 18. SWITCHING TIME TEST CIRCUIT

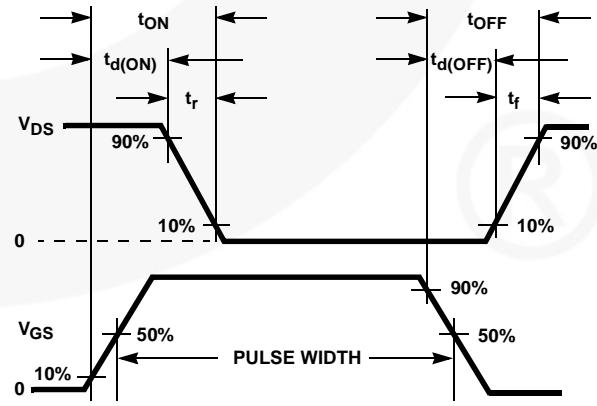


FIGURE 19. RESISTIVE SWITCHING WAVEFORMS

PSPICE Electrical Model

.SUBCKT HUFA75645 2 1 3 ; rev 21 May 1999

CA 12 8 5.31e-9
 CB 15 14 5.31e-9
 CIN 6 8 3.56e-9

DBODY 7 5 DBODYMOD
 DBREAK 5 11 DBREAKMOD
 DPLCAP 10 5 DPLCAPMOD

EBREAK 11 7 17 18 115.5
 EDS 14 8 5 8 1
 EGS 13 8 6 8 1
 ESG 6 10 6 8 1
 EVTHRES 6 21 19 8 1
 EVTEMP 20 6 18 22 1

IT 8 17 1

LDRAIN 2 5 1.0e-9
 LGATE 1 9 5.1e-9
 LSOURCE 3 7 4.4e-9

MMED 16 6 8 8 MMEDMOD
 MSTRO 16 6 8 8 MSTROMOD
 MWEAK 16 21 8 8 MWEAKMOD

RBREAK 17 18 RBREAKMOD 1
 RDRAIN 50 16 RDRAINMOD 7.80e-3
 RGATE 9 20 0.83
 RLDRAIN 2 5 10
 RLGATE 1 9 26
 RLSOURCE 3 7 11
 RSLC1 5 51 RSLC1MOD 1e-6
 RSLC2 5 50 1e3
 RSOURCE 8 7 RSOURCEMOD 1.65e-3
 RVTHRES 22 8 RVTHRESMOD 1
 RVTEMP 18 19 RVTEMPMOD 1

S1A 6 12 13 8 S1AMOD
 S1B 13 12 13 8 S1BMOD
 S2A 6 15 14 13 S2AMOD
 S2B 13 15 14 13 S2BMOD

VBAT 22 19 DC 1

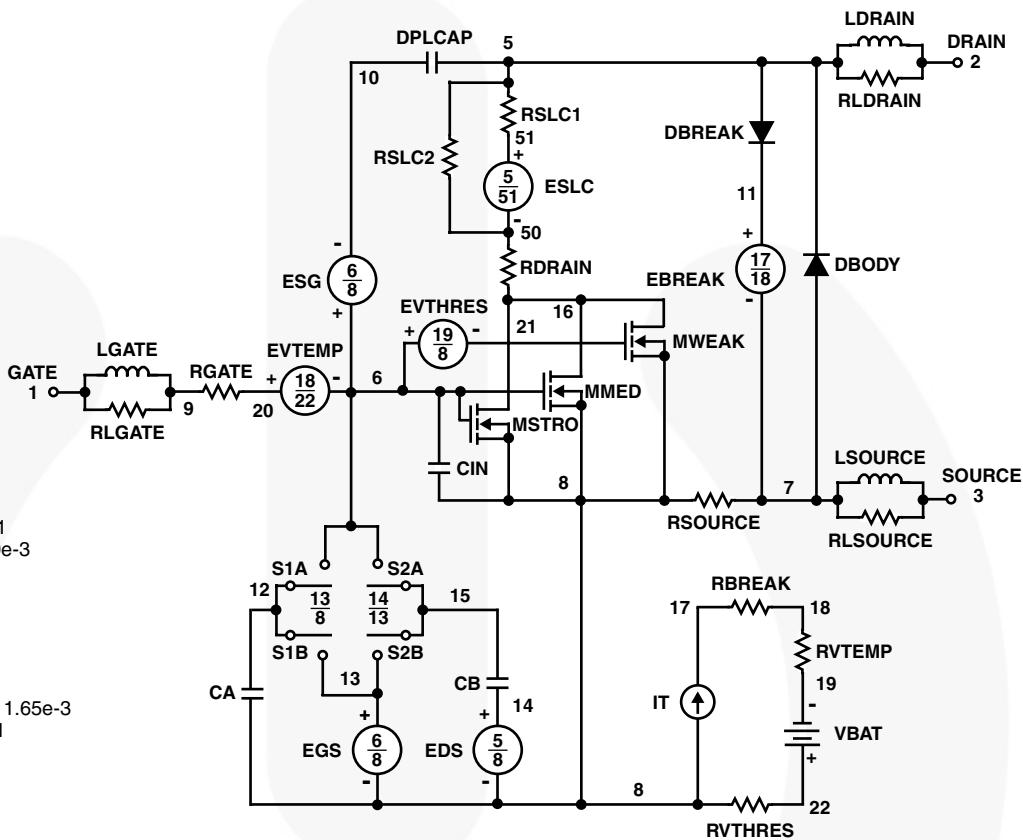
ESLC 51 50 VALUE={(V(5,51)/ABS(V(5,51)))*(PWR(V(5,51)/(1e-6*205),3.5))}

```
.MODEL DBODYMOD D (IS = 3.00e-12 IKF = 19 RS = 1.78e-3 XTI = 5 TRS1 = 2.25e-3 TRS2 = 1.00e-5 CJO = 5.32e-9 TT = 7.4e-8 M = 0.68)
.MODEL DBREAKMOD D (RS = 2.15e-1 IKF = 1 TRS1 = 8e-4 TRS2 = 3e-6)
.MODEL DPLCAPMOD D (CJO = 5.55e-9 IS = 1e-30 M = 0.98)
.MODEL MMEDMOD NMOS (VTO = 3.13 KP = 10 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u RG = 0.83)
.MODEL MSTROMOD NMOS (VTO = 3.51 KP = 93 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u)
.MODEL MWEAKMOD NMOS (VTO = 2.65 KP = 0.11 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u RG = 8.33 )
.MODEL RBREAKMOD RES (TC1 = 9.9e-4 TC2 = -1.3e-6)
.MODEL RDRAINMOD RES (TC1 = 9.40e-3 TC2 = 2.93e-5)
.MODEL RSLC1MOD RES (TC1 = 2.63e-3 TC2 = 1.05e-6)
.MODEL RSOURCEMOD RES (TC1 = 1e-3 TC2 = 1e-6)
.MODEL RVTHRESMOD RES (TC1 = -2.57e-3 TC2 = -7.05e-6)
.MODEL RVTEMPMOD RES (TC1 = -2.87e-3 TC2 = -2.21e-6)

.MODEL S1AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -6.2 VOFF = -2.4)
.MODEL S1BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -2.4 VOFF = -6.2)
.MODEL S2AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -1.8 VOFF = 0.5)
.MODEL S2BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = 0.5 VOFF = -1.8)

.ENDS
```

NOTE: For further discussion of the PSPICE model, consult **A New PSPICE Sub-Circuit for the Power MOSFET Featuring Global Temperature Options**; IEEE Power Electronics Specialist Conference Records, 1991, written by William J. Hepp and C. Frank Wheatley.



SABER Electrical Model

REV 21 May 1999

```

template ta75645 n2,n1,n3
electrical n2,n1,n3
{
var i iscl
d..model dbodymod = (is = 3.00e-12, cjo = 5.32e-9, tt = 7.4e-8, xti = 5, m = 0.68)
d..model dbreakmod = ()
d..model dplicapmod = (cjo = 5.55e-9, is = 1e-30, vj=1.0, m = 0.8)
m..model mmedmod = (type=_n, vto = 3.13, kp = 10, is = 1e-30, tox = 1)
m..model mstrongmod = (type=_n, vto = 3.51, kp = 93, is = 1e-30, tox = 1)
m..model mwweakmod = (type=_n, vto = 2.65, kp = 0.11, is = 1e-30, tox = 1)
sw_vcsp..model s1amod = (ron = 1e-5, roff = 0.1, von = -6.2, voff = -2.4)
sw_vcsp..model s1bmod = (ron = 1e-5, roff = 0.1, von = -2.4, voff = -6.2)
sw_vcsp..model s2amod = (ron = 1e-5, roff = 0.1, von = -1.8, voff = 0.5)
sw_vcsp..model s2bmod = (ron = 1e-5, roff = 0.1, von = 0.5, voff = -1.8)

```

$$\begin{aligned}
 c.ca \ n12 \ n8 &= 5.31e-9 \\
 c.cb \ n15 \ n14 &= 5.31e-9 \\
 c.cin \ n6 \ n8 &= 3.56e-9
 \end{aligned}$$

d.dbody n7 n71 = model=dbodymod
d.dbreak n72 n11 = model=dbreakmod
d.dplcap n10 n5 = model=dplcapmod

i.it n8 n17 = 1

$$\begin{aligned}I_{\text{drain}} &= n_2 n_5 = 1 \text{e-9} \\I_{\text{gate}} &= n_1 n_9 = 5.1 \text{e-9} \\I_{\text{source}} &= n_3 n_7 = 4.4 \text{e-9}\end{aligned}$$

m.mmed n16 n6 n8 n8 = model=mmedmod, l=1u, w=1u
m.mstrong n16 n6 n8 n8 = model=mstrongmod, l=1u, w=1u
m.mweak n16 n21 n8 n8 = model=mweakmod, l=1u, w=1u

```

res.rbreak n17 n18 = 1, tc1 = 9.9e-4, tc2 = -1.3e-6
res.rdbody n71 n5 = 1.78e-3, tc1 = 2.25e-3, tc2 = 1.e-5
res.rdbreak n72 n5 = 2.15e-1, tc1 = 8e-4, tc2 = 3e-6
res.rdrain n50 n16 = 7.8e-3, tc1 = 9.4e-3, tc2 = 2.93e-5
res.rgate n9 n20 = 0.83
res.rldrain n2 n5 = 10
res.rlgate n1 n9 = 26
res.rlsource n3 n7 = 11
res.rslc1 n5 n51 = 1e-6, tc1 = 2.63e-3, tc2 = 1.05e-6
res.rslc2 n5 n50 = 1e3
res.rsource n8 n7 = 1.65e-3, tc1 = 1e-3, tc2 = 1e-6
res.rvtemp n18 n19 = 1, tc1 = -2.87e-3, tc2 = -2.21e-6
res.rvthres n22 n8 = 1, tc1 = -2.57e-3, tc2 = -7.05e-6

```

```
spe.ebreak n11 n7 n17 n18 = 115.5
spe.eds n14 n8 n5 n8 = 1
spe.egs n13 n8 n6 n8 = 1
spe.esg n6 n10 n6 n8 = 1
spe.evtemp n20 n6 n18 n22 = 1
spe.evhres n6 n21 n19 n8 = 1
```

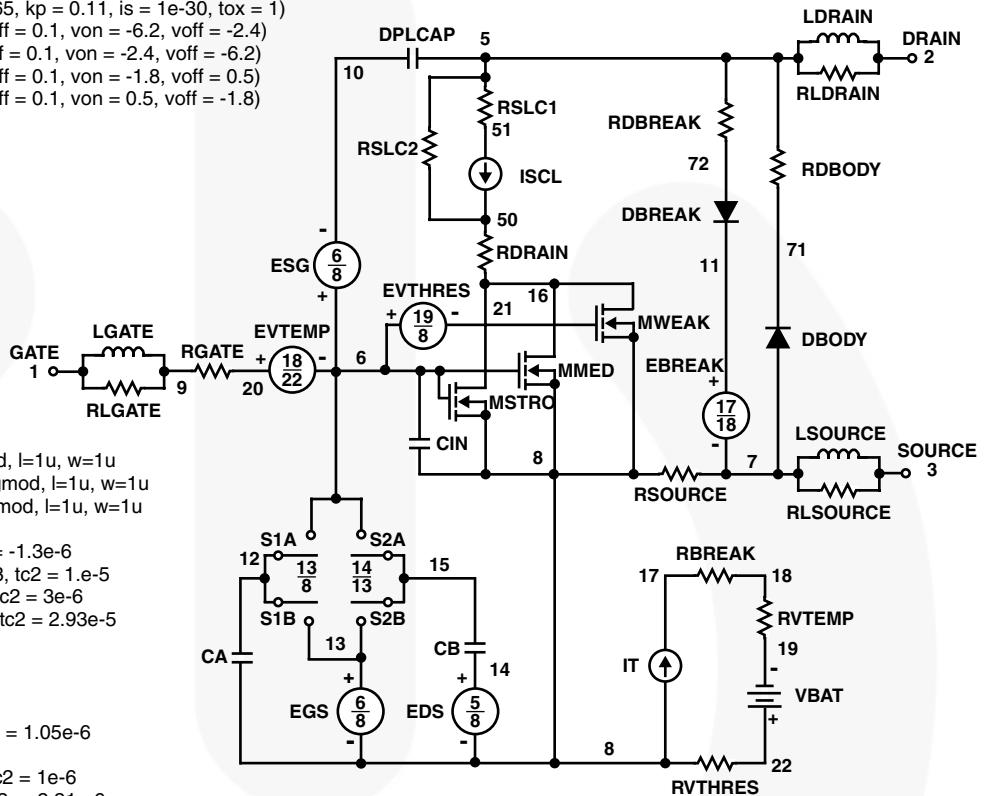
```
sw_vcsp.s1a n6 n12 n13 n8 = model=s1amod  
sw_vcsp.s1b n13 n12 n13 n8 = model=s1bmod  
sw_vcsp.s2a n6 n15 n14 n13 = model=s2amod  
sw_vcsp.s2b n13 n15 n14 n13 = model=s2bmod
```

v.vbat n22 n19 = dc=1

```

equations {
i(n51->n50) +=iscl
iscl: v(n51,n50) = ((v(n5,n51)/(1e-9+abs(v(n5,n51))))*((abs(v(n5,n51)*1e6/205))** 3.5))
}
}

```



SPICE Thermal Model

REV 28 July 1999

HUFA75645T

CTHERM1 th 6 8.80e-3
CTHERM2 6 5 2.50e-2
CTHERM3 5 4 2.70e-2
CTHERM4 4 3 3.70e-2
CTHERM5 3 2 4.40e-2
CTHERM6 2 tl 3.40e-1

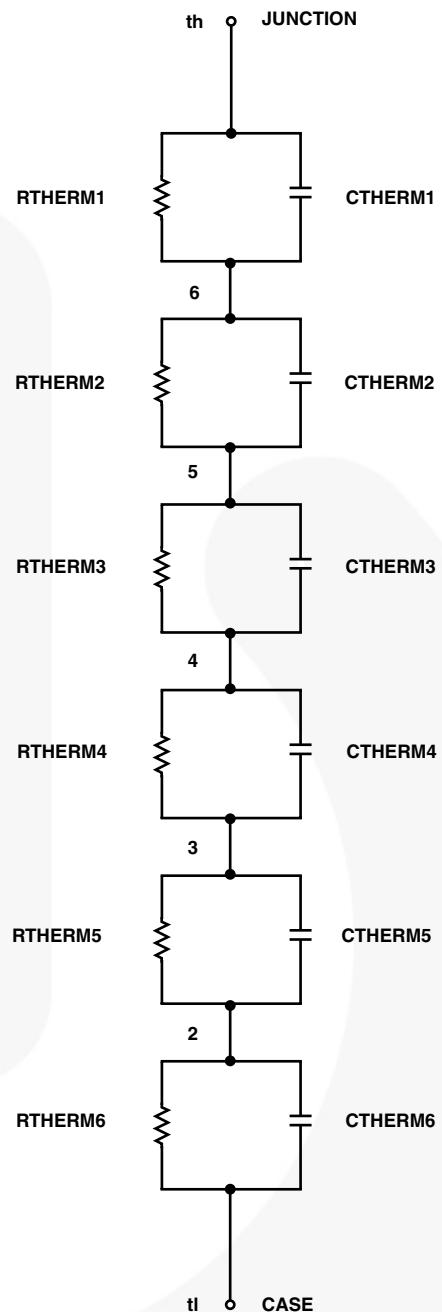
RTHERM1 th 6 1.20e-2
RTHERM2 6 5 3.00e-2
RTHERM3 5 4 4.30e-2
RTHERM4 4 3 8.80e-2
RTHERM5 3 2 9.90e-2
RTHERM6 2 tl 1.10e-1

SABER Thermal Model

SABER thermal model HUFA75645T

```
template thermal_model th tl
thermal_c th, tl
{
  ctherm.ctherm1 th 6 = 8.80e-3
  ctherm.ctherm2 6 5 = 2.50e-2
  ctherm.ctherm3 5 4 = 2.70e-2
  ctherm.ctherm4 4 3 = 3.70e-2
  ctherm.ctherm5 3 2 = 4.40e-2
  ctherm.ctherm6 2 tl = 3.40e-1

  rtherm.rtherm1 th 6 = 1.20e-2
  rtherm.rtherm2 6 5 = 3.00e-2
  rtherm.rtherm3 5 4 = 4.30e-2
  rtherm.rtherm4 4 3 = 8.80e-2
  rtherm.rtherm5 3 2 = 9.90e-2
  rtherm.rtherm6 2 tl = 1.10e-1
}
```





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Build it Now™	GreenBridge™	QFET®	TinyBuck®
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