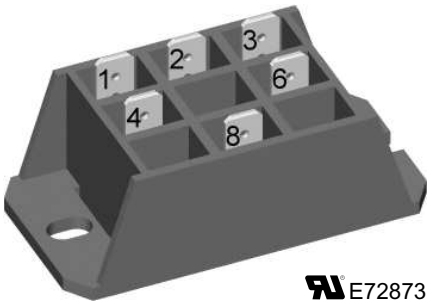
Half Controlled Single Phase Rectifier Bridge

with Freewheeling Diode

I_{dAVM} = 21 A
V_{RRM} = 800-1600 V

Part numbers

V_{RSM} V_{DSM}	V_{RRM} V_{DRM}	Type
V	V	
900	800	VHF 15-08io5
1300	1200	VHF 15-12io5
1700	1600	VHF 15-16io5



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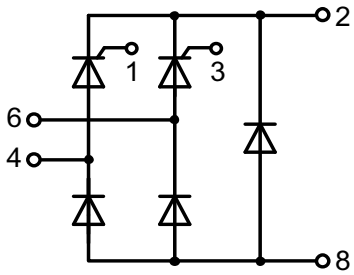

Features / Advantages:

- Planar passivated chips
- Space and weight savings
- Improved temperature & power cycling

Applications:

- Supply for DC power equipment
- DC motor control

Package: FO-F

- Isolation Voltage: 3600 V~
- DCB ceramic base plate
- 1/4" fast-on terminals
- Easy to mount with two screws
- RoHS compliant

Diodes

Symbol	Definitions	Conditions		Ratings min.	typ.	max.	Unit
I_{dAV}	*avarage DC output current*	module	T_K = 85°C			15	A
I_{dAVM}	*max. avarage DC output current*	for resistive load				21	A
I_{FRMS}, I_{TRMS}	*RMS forward current*	per leg				15	A
I_{FSM}, I_{TSM}	*max. surge forward current*	t = 1 0 ms (50 Hz), sine	T_{VJ} = 45°C			190	A
		t = 8.3 ms (60 Hz), sine; V_R = 0 V				210	A
		t = 1 0 ms (50 Hz), sine	T_{VJ} = 125°C			170	A
		t = 8.3 ms (60 Hz), sine; V_R = 0 V				190	A
I^2t	*I^2t value for fusing*	t = 1 0 ms (50 Hz), sine	T_{VJ} = 45°C			160	A^2s
		t = 8.3 ms (60 Hz), sine; V_R = 0 V				180	A^2s
		t = 1 0 ms (50 Hz), sine	T_{VJ} = 125°C			140	A^2s
		t = 8.3 ms (60 Hz), sine; V_R = 0 V				145	A^2s
$(di/dt)_{cr}$	*critical rate of rise of current*	f = 50 Hz, t_P = 200 µs, V_D = $^2/_3V_{DRM}$	T_{VJ} = 125°C				
		I_G = 0.3 A, di_G/dt = 0.3 A/µs					
			repetitive, I_T = 50 A			150	A/µs
			non repetitive, I_T = ½ I_{dAV}			500	A/µs
$(dv/dt)_{cr}$	*critical rate of rise of voltage*	V_D = $^2/_3V_{DRM}$	T_{VJ} = 125°C			1000	V/µs
		R_{GK} = ∞; method 1 (linear voltage rise)					
V_{RGM}	*max. reverse gate voltage*					10	V
P_{GM}	*max. gate power dissipation*	I_T = I_{TAVM}	t_p = 30 µs, T_{VJ} = 125°C			10	W
			t_p = 500 µs			5	W
			t_p = 10 ms			1	W
P_{GAVM}	*max. average gate power dissipation*					0.5	W

Thyristors

Symbol	Definitions	Conditions		Ratings min.	typ.	max.	Unit
I_R, I_D	*reverse, drain current*	V_R = V_{RRM}; V_D = V_{DRM}	T_{VJ} = 25°C			0,3	mA
			T_{VJ} = 125°C			5	mA
V_T, V_F	*forward voltage*	I_T, I_F = 45 A	T_{VJ} = 25°C			2.8	V
V_{T0}		For power-loss calculations only	T_{VJ} = 125°C		1.0		V
r_T					40		mΩ
V_{GT}	*gate trigger voltage*	V_D = 6 V	T_{VJ} = 25°C			1.0	V
			T_{VJ} = -40°C			1.2	V
I_{GT}	*gate trigger current*	V_D = 6 V	T_{VJ} = 25°C			65	mA
			T_{VJ} = -40°C			80	mA
			T_{VJ} = 125°C			50	mA
V_{GD}	*gate non-trigger voltage*	V_D = $^2/_3V_{DRM}$	T_{VJ} = 125°C			0.2	V
I_{GD}	*non-trigger gate current*					5	mA
I_L	*latching current*	I_G = 0.3 A, t_G = 30 µs	T_{VJ} = 25°C			150	mA
		di_G/dt = 0.3 A/µs	T_{VJ} = -40°C			200	mA
			T_{VJ} = 125°C			100	mA
I_H	*holding current*	V_D = 6 V, R_{GK} = ∞	T_{VJ} = 25°C			100	ns
t_{gd}	*gate controlled delay time*	V_D = ½V_{DRM}	T_{VJ} = 25°C		150		µs
		I_G = 0.3 A, di_G/dt = 0.3 A/µs					
t_q	*turn-off time*	I_T = 15 A, t_P = 300 µs, V_R = 100 V;	T_{VJ} = 125°C		150		µs
Q_r	*reverse recovery charge*	di/dt = -10 A/µs, dv/dt = 20 V/µs, V_D = $^2/_3V_{DRM}$			75		µC
R_{thJC}	*thermal resistance junction to case*	per thyristor (diode); DC current				2.4	K/W
		per module				0.6	K/W
R_{thJH}	*thermal resistance junction to heatsink*	per thyristor (diode); DC current			3.0		K/W
		per module			0.75		K/W

Data according to IEC 60747 and refer to a single thyristor/diode unless otherwise stated.

IXYS reserves the right to change limits, test conditions and dimensions.

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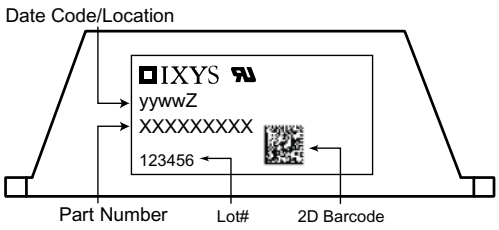
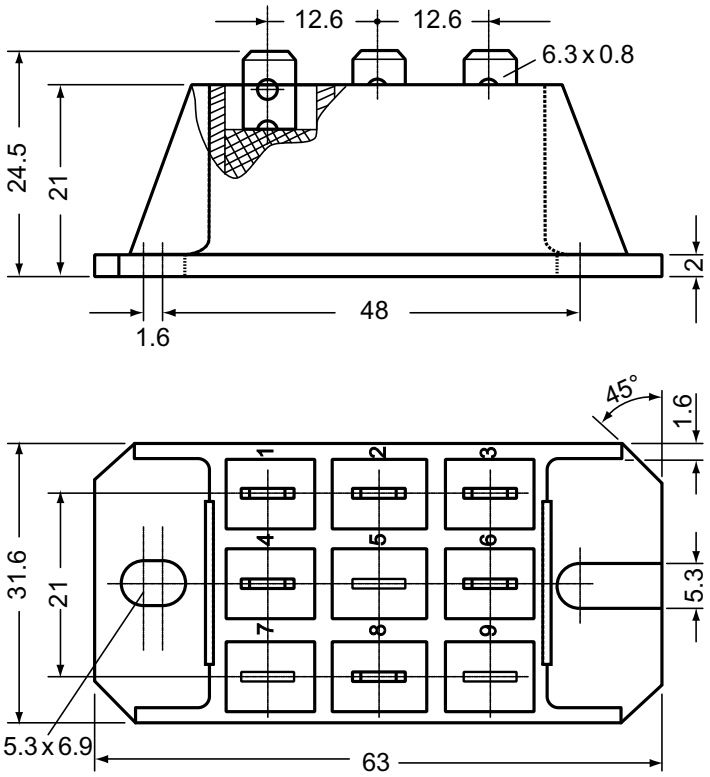
Package	FO-F				Ratings			
Symbol	Definitions	Conditions			min.	typ.	max.	Unit
I_{RMS}	*RMS current*	per terminal					100	A
T_{VJ}	*virtual junction temperature*				-40		125	°C
T_{op}	*operation temperature*				-40		100	°C
T_{stg}	*storage temperature*				-40		125	°C
Weight						45		g
M_D	*mounting torque*				2		2.5	Nm
$d_{Spp/App}$	*creepage distance on surface / striking distance through air*		*terminal to terminal*	18.0	6.0			mm
$d_{Spb/Apb}$			*terminal to backside*	26.0	20.0			mm
V_{ISOL}	*isolation voltage*	t = 1 second	50/60 Hz, RMS, $I_{ISOL} \leq 1$ mA		3600			V
		t = 1 minute			3000			V



Dimensions in mm (1 mm = 0.0394")



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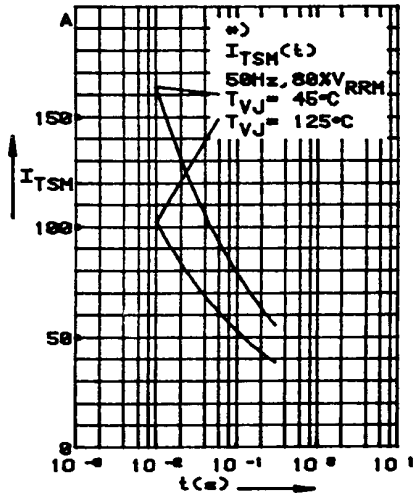

Fig. 1 Surge overload current per chip
I_{FSM}: Crest value, t: duration

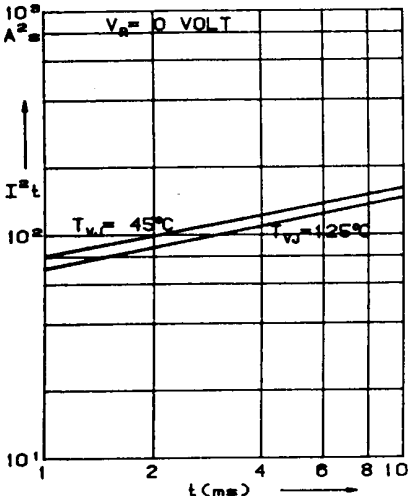

Fig. 2 I^2t versus time (1-10 ms) per chip

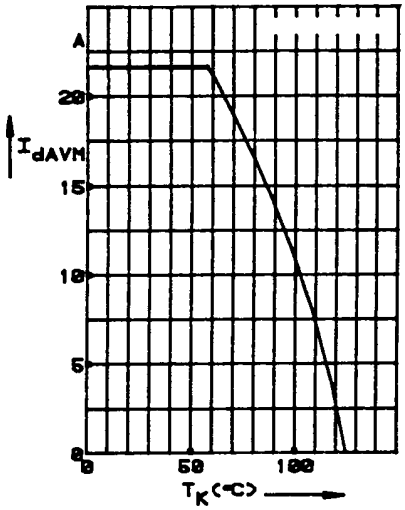

Fig. 3 Max. forward current at heatsink temperature

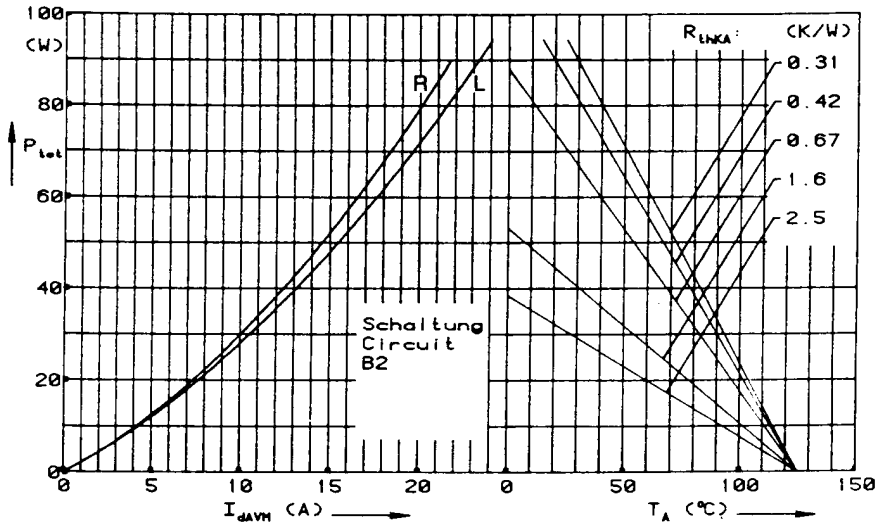

Fig. 4 Power dissipation versus direct output current and ambient temperature

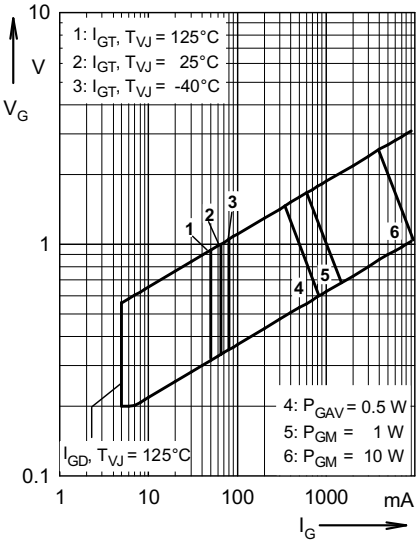

Fig. 5 Gate trigger range

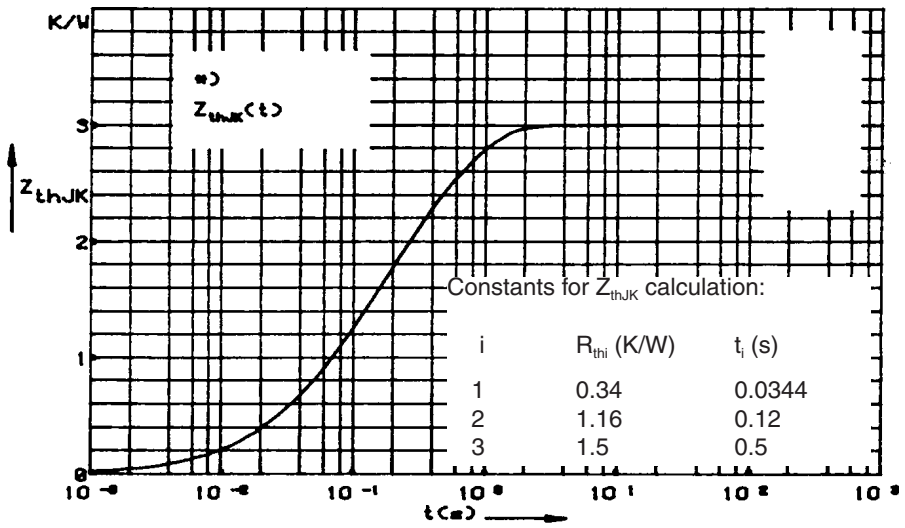

Fig. 6 Transient thermal impedance junction to heatsink per chip

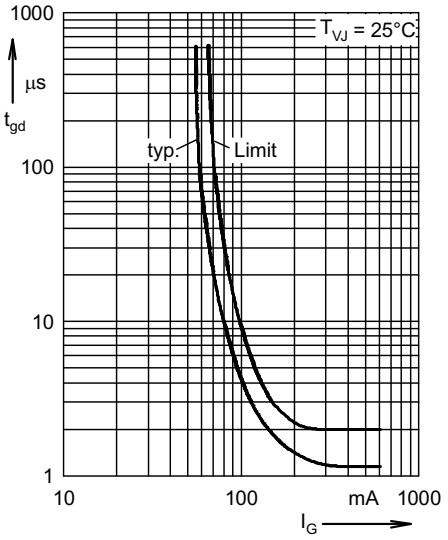

Fig. 7 Gate controlled delay time