XR21B1421

Enhanced 1-Ch Full-Speed USB HID to UART Bridge

General Description

The XR21B1421 is an enhanced Universal Asynchronous Receiver and Transmitter (UART) bridge to HID class USB interface. The USB interface is fully compliant to the USB 2.0 (Full-Speed) specification with 12 Mbps USB data transfer rate. The USB interface also supports USB suspend, resume and remote wakeup operations. The USB Vendor ID, Product ID, power mode, remote wakeup support, maximum power, and numerous other settings may be programmed in the no-chip OTP memory via the USB interface using either HID reports or MaxLinear-supplied OTP programming tools.

The XR21B1421 includes an internal oscillator and does not require an external crystal/oscillator. Any UART baud rate up to 12 Mbps may be generated with this internal clock and the fractional baud rate generator.

The UART pins for each port may also be configured as GPIO; direction, state, output driver type and input pull-up or pull-down resistors are programmed either through on chip OTP, or on the fly via memory mapped registers.

Large 512-byte TX and RX FIFOs prevent buffer overflow errors and optimize data throughput. Automatic half-duplex direction control and optional multi drop (9-bit) mode simplify both hardware and software in half-duplex RS-485 applications.

The XR21B1421 uses the native OS HID driver using HID reports. The HID reports perform a variety of functions, including device configuration, transmitting and receiving UART data, and programming of the on-chip OTP. MaxLinear provides a .dll as an easy to use programming interface to the HID reports.

The XR21B1421 operates from a single 5V or 3.3V power supply and is available in a 24 or 28 pin QFN package. When powered with 5V input, the XR21B1421 supplies a regulated 3.3V output. The 24 pin package has a separate V_{IO} supply voltage input for the Modem / GPIO pins. The 28 pin package has V_{IO} internally tied to 3.3V.

FEATURES

- ±15kV ESD on USBD+/USBD-
- USB 2.0 Compliant, Full-Speed (12Mbps)
- Unique pre-programmed USB serial number
- Internally generated 48MHz core clock
- Enhanced UART features
  - Baud rates up to 12 Mbps
  - Fractional Baud Rate Generator
  - 512-byte TX and 512-byte RX FIFOs
  - Auto Hardware / Software Flow Control
  - Multidrop and Half-Duplex Modes
  - Auto RS-485 Half-Duplex Control
  - Selectable GPIO or Modem I/O
- Up to 10 GPIOs
- 5V tolerant GPIO inputs
- Suspend state GPIO configuration
- Configurable clock output
- 24-pin or 28-pin QFN package
- Industrial -40°C to +85°C Temperature Range

APPLICATIONS

- Portable Medical Diagnostics
- Blood Glucose Meters
- Health and Fitness Wellness Monitors
- Uninterruptible Power Supplies
- Energy Management Consoles

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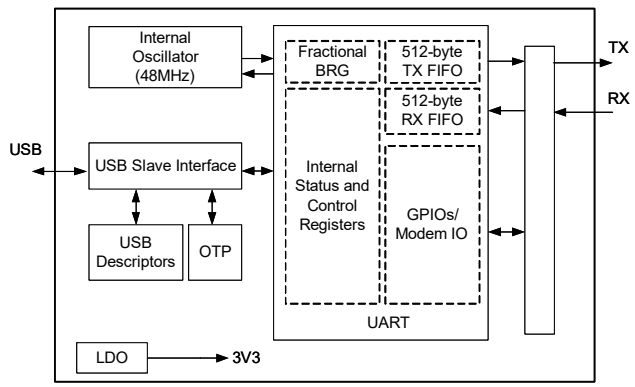
Block Diagram



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Absolute Maximum Ratings

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Maximum Rating condition for extended periods may affect device reliability and lifetime.

Supply Voltage (VCC_REG).....+5.75V

Supply Voltage (VCC, VIO).....+4V

Input Voltage (VBUS_SENSE).....-0.3 to +5.75V

Input Voltage (All other pins).....-0.3 to +5.6V

Junction Temperature.....125°C

Operating Conditions

Operating Temperature Range.....-40°C to +85°C

Electrical Characteristics

Unless otherwise noted: T_A = -40°C to +85°C, VCC_REG = 4.4V to 5.25V or 3.0V to 3.6V, VIO = 1.8V to 3.6V

Symbol	Parameter	Conditions		Min	Typ	Max	Units
Power							
I_{CC}	Power Supply Current	VCC_REG = +4.4V to +5.25V			13	19	mA
I_{SUSP}	Lowpower Mode Current				0.85	1.25	mA
V_{OUT}	Regulated Output Voltage (VCC pin)	VCC_REG = +4.4V to +5.25V. Maximum output current = 200 mA including the supply current of the XR21B1421.		3	3.3	3.6	V
UART, USB_STAT and GPIO Pins							
V_{IL}	Input Low Voltage			-0.3		0.25* VIO	V
V_{IH}	Input High Voltage			0.70* VIO		5.5	V
V_{OL}	Output Low Voltage	IOL = 1mA, VIO = +1.6V				0.3	V
		IOL = 4mA, VIO = +3.6V				0.5	V
V_{OH}	Output High Voltage	IOH = -400uA, VIO = +1.6V		1.3		VIO	V
		IOH = -1.5mA, VIO = +3.6V		2.8		VIO	V
I_{IL}	Input Low Leakage Current	VIO = +3V to +3.6V, VCC_REG = +4.4V to +5.25V, V_{INPUT} = 0V				±10	µA
I_{IH}	Input High Leakage Current	VIO = +3V to +3.6V, VCC_REG = +4.4V to +5.25V, V_{INPUT} = +3.3V				±10	µA
		VIO = +3V to +3.6V, VCC_REG = +4.4V to +5.25V, V_{INPUT} = +5.5V				±120	µA
C_{IN}	Input Pin Capacitance					5	pF

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Symbol	Parameter	Conditions		Min	Typ	Max	Units
USB I/O Pins							
V_{IL}	Input Low Voltage			-0.3		0.8	V
V_{IH}	Input High Voltage			2.0		5.5	V
V_{OL}	Output Low Voltage	External 15kΩ to GND on USBD+ and USBD- pins		0		0.3	V
V_{OH}	Output High Voltage	External 15kΩ to GND on USBD+ and USBD- pins		2.8		3.6	V
V_{DrvZ}	Driver Output Impedance			28		44	Ω

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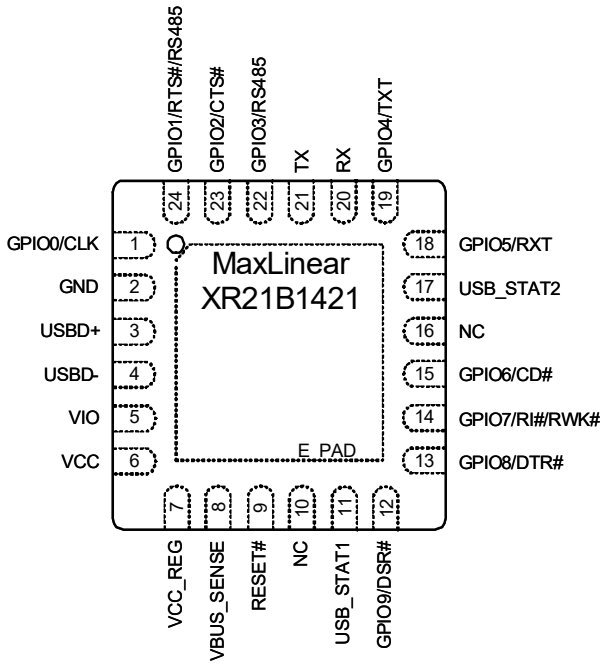
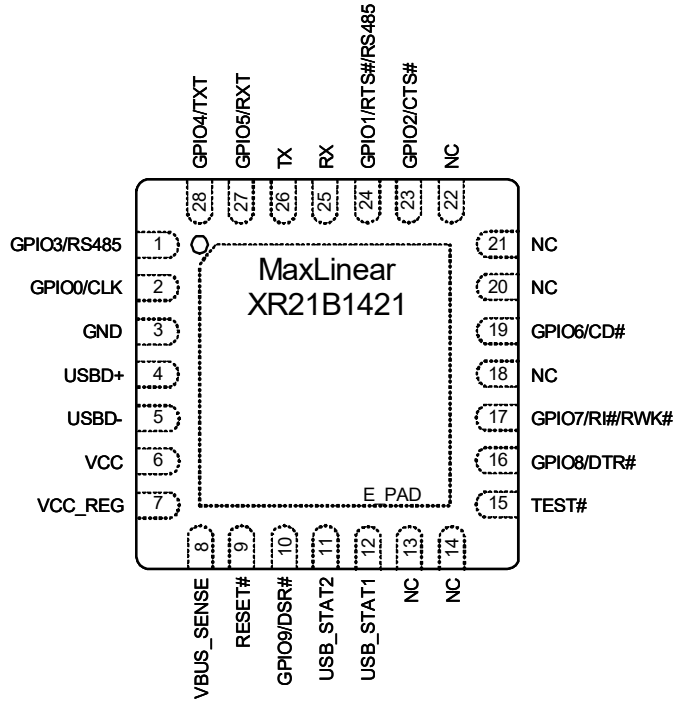
Pin Configuration



24-Pin
Top View



28-Pin
Top View

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Pin Assignments

24-pin QFN			
Pin No.	**Pin Name**	**Type**	**Description**
1	GPIO0/CLK	I/O	General purpose I/O, or clock or pulse output. Defaults to GPIO input with internal pull-up. See "GET / SET_GPIO_CONFIG" on page 28 and "GET / SET_PIN_CONFIG" on page 41.
2	GND	PWR	Power supply common, ground.
3	USBD+	I/O	USB port differential data positive input. This pin has internal pull-up resistor compliant to USB 2.0 specification. The ESD protection on this pin is +/-15 kV HBM.
4	USBD-	I/O	USB port differential data negative input. The ESD protection on this pin is +/-15 kV HBM.
5	VIO	PWR	Supply voltage for the UART and GPIO signals. The voltage range for VIO is + 1.8V to + 3.6V. In QFN28 package, the VIO is internally tied to core 3.3V. If VCC_REG is powered by 5V, VCC output 3.3V may be externally connected to VIO pin.
6	VCC	PWR	3.3V power to the device, or 3.3V power output from the device when 5V power is supplied to VCC_REG pin. 3.3V output power may source up to 200 mA maximum (including the device) and should be decoupled by minimum of 4.7 uF ceramic capacitor.
7	VCC_REG	PWR	5V or 3.3V power to the device. In bus-powered mode, connect VBUS power from the USB host to this pin and to the VBUS_SENSE pin. See Figure 1. In self-powered mode, connect on board 5V or 3.3V source to this pin and VBUS from the USB host to the VBUS_SENSE pin. See Figure 2 and Figure 3.
8	VBUS_SENSE	I	Must be connected to VBUS power from the USB host PC. This pin is used to disable the internal pull-up resistor on the USBD+ signal when VBUS is not present in self-powered mode.
9	RESET#	I/O OD	Active low open drain output. Asserted at power on or any time device is reset by either register or USB bus reset. As an input, must be asserted for at least 15 us to force a device reset. Reset pulse width input of shorter than 15 us will have unknown effects. A weak internal pull-up resistor provides noise immunity if left unconnected.
10	NC		No Connect
11	USB_STAT1	OD	The USB_STAT1 output pin may be used to indicate any of three USB status conditions: 1. USB_STAT1 is asserted when the USB host asserts USB reset. 2. USB_STAT1 is asserted when the USB host PC places the XR21B1421 device into the suspend state. 3. USB_STAT1 is asserted when it is not safe to draw the amount of current requested in the Device Maximum Power field of the Configuration Descriptor. a. For a low power device (<= 1 unit load or 100 mA, bMaxPower <= 0x32), USB_STAT1 will be asserted when the USB UART is in the suspend mode. b. For a high power device (bMaxPower > 0x32), USB_STAT1 will be asserted when the USB UART is in the suspend mode or when it is not yet configured. The assertion polarity and status condition are selectable via the PIN_CFG_STAT1 register. The USB_STAT pin will be de-asserted whenever the selected condition(s) is / are not met. The default output for this pin is active high polarity, asserted whenever the XR21B1421 is placed into a suspended state.
12	GPIO9/DSR#	I/O	General purpose I/O, or UART Data-Set-Ready input (active low). Defaults to GPIO push-pull output. See "Automatic DTR/DSR Hardware Flow Control" on page 16.
13	GPIO8/DTR#	I/O	General purpose I/O, or UART Data-Terminal-Ready push-pull output (active low). Defaults to GPIO push-pull output. See "Automatic DTR/DSR Hardware Flow Control" on page 16.
14	GPIO7/RI#/RWK#	I/O	General purpose I/O, or UART Ring-Indicator input (active low) or Remote Wakeup input (active low). Defaults to GPIO input with internal pull-up.

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24-pin QFN			
Pin No.	**Pin Name**	**Type**	**Description**
15	GPIO6/CD#	I/O	General purpose I/O, or UART Carrier-Detect input (active low). Defaults to GPIO input with internal pull-up.
16	NC		No Connect
17	USB_STAT2	OD	This pin has the same functionality as the USB_STAT1 pin. However, the default output for this pin is active low polarity, asserted whenever the XR21B1421 is placed into a suspended state. This default may be changed via the PIN_CFG_USB_STAT2 register.
18	GPIO5/RXT	I/O	General purpose I/O, or UART receive indicator. Defaults to receive indicator push-pull output. When configured as receive indicator, this pin will toggle at ~10 Hz intervals while the UART is receiving data.
19	GPIO4/TXT	I/O	General purpose I/O, or UART transmit indicator. Defaults to transmit indicator push-pull output. When configured as transmit indicator, this pin will toggle at ~10 Hz intervals during UART data transmission.
20	RX	I	UART Receive Data.
21	TX	O	UART Transmit Data.
22	GPIO3/RS485	I/O	General purpose I/O, or auto RS-485 half-duplex enable. Defaults to active high push-pull output Auto RS-485 half-duplex enable.
23	GPIO2/CTS#	I/O	General purpose I/O, or UART Clear-to-Send input (active low). Defaults to CTS input with internal pull-up. See “Automatic RTS/CTS Hardware Flow Control” on page 15.
24	GPIO1/RTS#/RS485	I/O	General purpose I/O, or UART Request-to-Send output (active low) or auto. RS-485 half-duplex enable. Defaults to open drain RTS output. See “GET / SET_GPIO_CONFIG” on page 28 and “GET / SET_PIN_CONFIG” on page 41.
Center Pad	GND	PWR	The center pad on the back side of the QFN package is metallic and should be connected to GND on the PCB. The thermal pad size on the PCB should be the approximate size of this center pad and should be solder mask defined. The solder mask opening should be at least 0.0025" inwards from the edge of the PCB thermal pad.

1. Pin type: I=Input, O=Push-pull Output, I/O= Input/output, PWR=Power, OD=Open Drain Output with weak internal pull-up

2. All GPIO pins as well as USB_STAT1 and USB_STAT2 may be configured for a variety of pin type options using the GPIO_MODE register or by writing to the OTP using XR_SET_OTP.

3. All enabled pull-up and pull-down resistors are maintained during USB suspend state.

4. Pin configurations set using XR_SET_OTP are enabled following the next power up reset and are permanent. During USB bus reset, resistors are disabled and re-enabled after bus reset is deasserted. Pin configurations set using the GPIO_MODE register will be lost after POR or USB bus reset.

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28-pin QFN			
Pin No.	**Pin Name**	**Type**	**Description**
1	GPIO3/RS485	I/O	General purpose I/O, or auto RS-485 half-duplex enable. Defaults to active high push-pull output Auto RS-485 half-duplex enable.
2	GPIO0/CLK	I/O	General purpose I/O, or clock or pulse output. Defaults to GPIO input with internal pull-up. See "GET / SET_GPIO_CONFIG" on page 28 and "GET / SET_PIN_CONFIG" on page 41.
3	GND	PWR	Power supply common, ground.
4	USBD+	I/O	USB port differential data positive input. This pin has internal pull-up resistor compliant to USB 2.0 specification. The ESD protection on this pin is +/-15 kV HBM.
5	USBD-	I/O	USB port differential data negative input. The ESD protection on this pin is +/-15 kV HBM.
6	VCC	PWR	3.3V power to the device, or 3.3V power output from the device when 5V power is supplied to VCC_REG pin. 3.3V output power may source up to 200 mA maximum and should be decoupled by minimum of 4.7 uF ceramic capacitor.
7	VCC_REG	PWR	5V or 3.3V power to the device. In bus-powered mode, connect VBUS power from the USB host to this pin and to the VBUS_SENSE pin. See Figure 1. In self-powered mode, connect on board 5V or 3.3V source to this pin and VBUS from the USB host to the VBUS_SENSE pin. See Figure 2 and Figure 3.
8	VBUS_SENSE	I	Must be connected to VBUS power from the USB host PC. This pin is used to disable the internal pull-up resistor on the USBD+ signal when VBUS is not present in self-powered mode.
9	RESET#	I/O OD	Active low open drain output. Asserted at power on or any time device is reset by either register or USB bus reset. As an input, must be asserted for at least 15 us to force a device reset. Reset pulse width input of shorter than 15 us will have unknown effects. A weak internal pull-up resistor provides noise immunity if left unconnected.
10	GPIO9/DSR#	I/O	General purpose I/O, or UART Data-Set-Ready input (active low). Defaults to GPIO push-pull output. See "Automatic DTR/DSR Hardware Flow Control" on page 16.
11	USB_STAT2	OD	This pin has the same functionality as the USB_STAT1 pin. However, the default output for this pin is active low polarity, asserted whenever the XR21B1421 is placed into a suspended state. This default may be changed via the PIN_CFG_USB_STAT2 register.
12	USB_STAT1	OD	The USB_STAT1 output pin may be used to indicate any of three USB status conditions: 1. USB_STAT1 is asserted when the USB host asserts USB reset. 2. USB_STAT1 is asserted when the USB host PC places the XR21B1421 device into the suspend state. 3. USB_STAT1 is asserted when it is not safe to draw the amount of current requested in the Device Maximum Power field of the Configuration Descriptor. a. For a low power device (<= 1 unit load or 100 mA, bMaxPower <= 0x32), USB_STAT1 will be asserted when the USB UART is in the suspend mode. b. For a high power device (bMaxPower > 0x32), USB_STAT1 will be asserted when the USB UART is in the suspend mode or when it is not yet configured. The assertion polarity and status condition are selectable via the PIN_CFG_STAT1 register. The USB_STAT pin will be de-asserted whenever the selected condition(s) is / are not met. The default output for this pin is active high polarity, asserted whenever the XR21B1421 is placed into a suspended state.
13	NC		No Connect
14	NC		No Connect
15	TEST#		Test mode. Must be left open or pulled high to VCC for normal operation.

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28-pin QFN			
Pin No.	**Pin Name**	**Type**	**Description**
16	GPIO8/DTR#	I/O	General purpose I/O, or UART Data-Terminal-Ready push-pull output (active low). Defaults to GPIO push-pull output. See "Automatic DTR/DSR Hardware Flow Control" on page 16.
17	GPIO7/RI#/RWK#	I/O	General purpose I/O, or UART Ring-Indicator input (active low) or Remote Wakeup input (active low). Defaults to GPIO input with internal pull-up.
18	NC		No Connect
19	GPIO6/CD#	I/O	General purpose I/O, or UART Carrier-Detect input (active low). Defaults to GPIO input with internal pull-up.
20	NC		No Connect
21	NC		No Connect
22	NC		No Connect
23	GPIO2/CTS#	I/O	General purpose I/O, or UART Clear-to-Send input (active low). Defaults to CTS input with internal pull-up. See "Automatic RTS/CTS Hardware Flow Control" on page 15.
24	GPIO1/RTS#/RS485	I/O	General purpose I/O, or UART Request-to-Send output (active low) or auto. RS-485 half-duplex enable. Defaults to open drain RTS output. See "GET / SET_GPIO_CONFIG" on page 28 and "GET / SET_PIN_CONFIG" on page 41.
25	RX	I	UART Receive Data.
26	TX	O	UART Transmit Data.
27	GPIO5/RXT	I/O	General purpose I/O, or UART receive indicator. Defaults to receive indicator push-pull output. When configured as receive indicator, this pin will toggle at ~10 Hz intervals while the UART is receiving data.
28	GPIO4/TXT	I/O	General purpose I/O, or UART transmit indicator. Defaults to transmit indicator push-pull output. When configured as transmit indicator, this pin will toggle at ~10 Hz intervals during UART data transmission.
Center Pad	GND	PWR	The center pad on the back side of the QFN package is metallic and should be connected to GND on the PCB. The thermal pad size on the PCB should be the approximate size of this center pad and should be solder mask defined. The solder mask opening should be at least 0.0025" inwards from the edge of the PCB thermal pad.

1. Pin type: I=Input, O=Push-pull Output, I/O= Input/output, PWR=Power, OD=Open Drain Output with weak internal pull-up

2. All GPIO pins as well as USB_STAT1 and USB_STAT2 may be configured for a variety of pin type options using the GPIO_MODE register or by writing to the OTP using XR_SET_OTP.

3. All enabled pull-up and pull-down resistors are maintained during USB suspend state.

4. Pin configurations set using XR_SET_OTP are enabled following the next power up reset and are permanent. During USB bus reset, resistors are disabled and re-enabled after bus reset is deasserted. Pin configurations set using the GPIO_MODE register will be lost after POR or USB bus reset.

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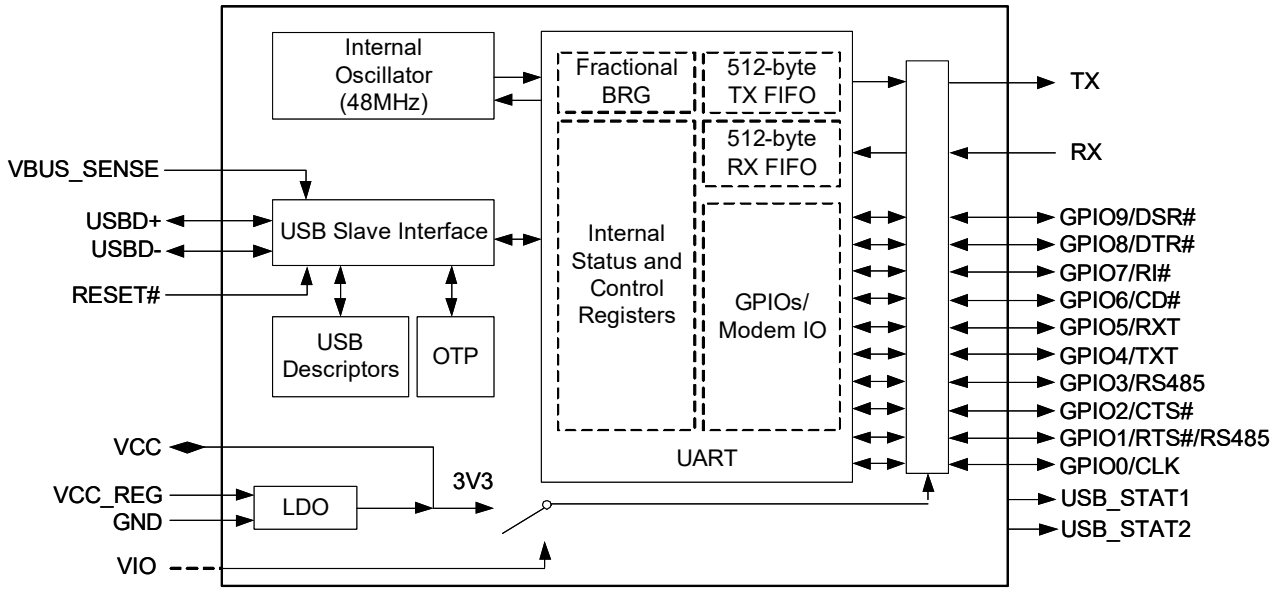
Functional Block Diagram



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Functional Description

USB Interface

The USB interface of the XR21B1421 is compliant with the USB 2.0 Full-Speed Specifications.

The XR21B1421 uses the following set of parameters:

- 1 Control Endpoint
  - Endpoint 0 as outlined in the USB specifications
- 1 Configuration is supported
- 1 HID Interface for the UART channel
  - Interrupt-in endpoint for UART receive data

Interrupt-out endpoint for UART transmit data

USB Vendor and Product IDs

Exar's USB Vendor ID is 0x04E2. This is the default Vendor ID that is used for the XR21B1421. Customers may obtain their own Vendor ID from USB.org. The default USB Product ID for the XR21B1421 is 0x1421. Upon request, MaxLinear will provide up to 8 PID values for use with Exar's VID. The VID and PID may be modified by the SET_USB_CONFIG HID report. However, the Exar VID and PID values will always be returned in the GET_CHIP_ID report (0x4F) irrespective of any changes to the VID and PID using the SET_USB_CONFIG report. Refer to Table 1.

USB Suspend

All USB peripheral devices must support the USB suspend mode. Per USB standard, the XR21B1421 device will begin to enter the suspend state if it does not detect any activity, (including Start of Frame or SOF packets) on its USB data lines for 3 ms. The peripheral device must then reduce power consumption from VBUS power within the next 7 ms to the allowed limit of 2.5 mA for the suspended state. Note that in this context, the "device" is all circuitry (including the XR21B1421) that draws power from the host VBUS.

Remote Wakeup

If the XR21B1421 device has been placed into suspend state by the USB host, the RI#/RWK# and / or RX pins may be used to request that the host exit the suspended state. By default the XR21B1421 device reports in its device attributes that it does not support remote wakeup. If remote wakeup is enabled via the OTP, the device will respond to a high to low transition on the RI#/RWK# pin if it is configured as an input, and remotely wake up the USB host. Note that Windows OS does not support remote wakeup for HID class devices that are not identified as either keyboard or mouse. RX pin remote wakeup is disabled by default and must also be separately enabled.

USB Strings

USB specifies three character string descriptors that are provided to the USB host during enumeration in string descriptors: the manufacturer, product and serial strings. The defaults manufacturer, and product strings for the XR21B1421 device are "Exar Corp." and, "Exar USB UART" respectively. The serial number string is a unique alpha-numeric string programmed into the device at the factory. All character strings use Unicode UTF-16LE format by default, but the Unicode language ID may be changed for the manufacturer and product strings. The default character string language ID is US English. If the language ID is modified via OTP, the serial number string should also be modified accordingly. However, note that USB.org requires any serial number string for a specific VID/PID combination to be unique for each device.

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Table 1: USB String Descriptor Defaults

Descriptor	Value
Exar USB Vendor ID	0x04E2
Exar USB Product ID	0x1421
Manufacturer String	Exar Corp.
Product String	Exar USB UART

Device Driver

The XR21B1421 device will utilize the native OS supplied HID driver. No other driver is required, however a custom dll supplied by MaxLinear provides a function library to any user that is developing applications that utilize the HID reporting capabilities. MaxLinear also supplies a sample GUI using the .dll as well as source code (upon request).

USB Power Modes

The XR21B1421 device may be configured in any one of three power modes: Bus-powered, Self-powered 5V, or Self-powered 3.3V. In all three modes, the VBUS power signal from the USB host must be connected to the VBUS_SENSE pin of the device.

The default power mode for the XR21B1421 is bus-powered. In this mode, a maximum power required for the USB device from the host must be specified. In this context, the USB device includes all components on the PCB that will draw power from the USB VBUS power. The default power request for the XR21B1421 is 100 mA but this may be changed using the Maxpower field of the SET_USB_CONFIG HID report.

Bus-Powered

In bus-powered mode, VBUS from the USB cable supplies 5V to the XR21B1421 device. The VCC pin will supply 3.3V output. The VIO pins may be externally connected to VCC or to an alternate voltage source.

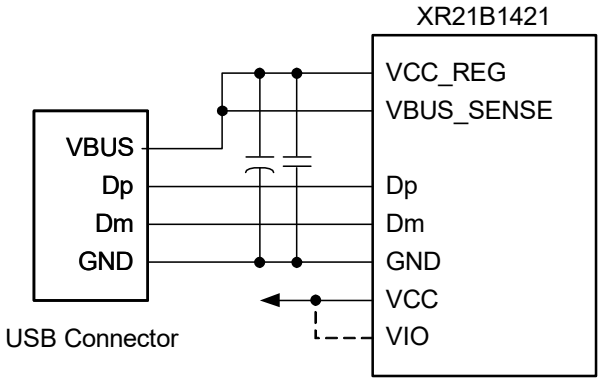

Figure 1: Bus-Powered Mode

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Self-Powered 5V

In self-powered 5V mode, a local source supplies 5V to the XR21B1421 device. The USB attributes should be changed using SET_USB_CONFIG to report self powered mode. The VCC pin will supply 3.3V output. VIO pins may be externally connected to VCC or to an alternate voltage source.

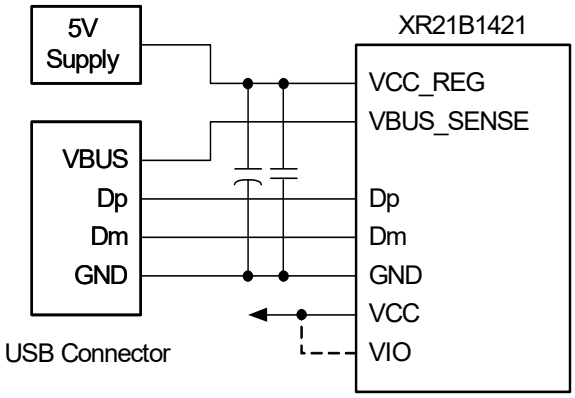

Figure 2: Self-Powered 5V Mode

Self-Powered 3.3V

In self-powered 3.3V mode, a local source supplies 3.3V to both the VCC_REG and VCC pins of the XR21B1421 device. The USB attributes should be changed using SET_USB_CONFIG to report self-powered mode. The VIO pin (on the QFN24 package) may be externally connected to VCC or to an alternate voltage source.

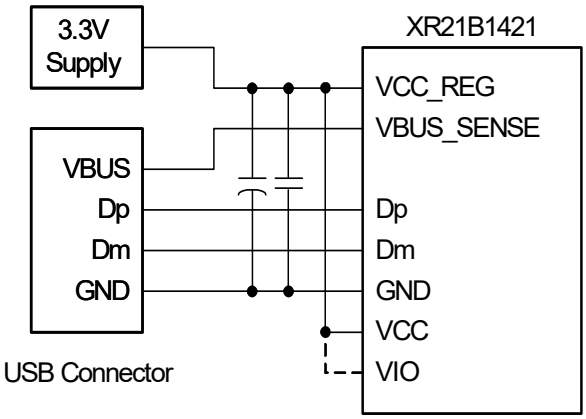

Figure 3: Self-Powered 3.3V Mode

Reset

The XR21B1421 has four different types of resets: power-on reset or POR, hardware reset, software reset and USB bus reset. The results of each of the four types of resets are listed in Table 2.

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Table 2: Device Resets

Reset Type	Device Actions
Power On Reset (POR)	Resets all registers and pins to default states including any OTP modifications. Locks OTP from further writes if Global Lock is set.
Hardware Reset	Resets all registers and pins to default states including any OTP modifications. Locks OTP from further writes if Global Lock is set.
Software Reset	Reset USB Interface, re-enumerate device, reset all internal states, clear UART FIFOs. Does not reset registers or pin configurations.
USB Bus Reset	Resets USB Interface, re-enumerate device, reset all internal states, clear UART FIFOs. Does not reset registers or pin configurations.

UART

The UART transmitter and receiver sections are described separately below. The UART may be configured via HID reports. Wide mode is discussed in “Wide Mode” on page 13.

Transmitter

The transmitter consists of a 512-byte TX FIFO and a Transmit Shift Register (TSR). Once a SET_TRANSMIT_DATA report using interrupt out packets has been received and is validated, the data bytes in that packet are written into the TX FIFO. Data from the TX FIFO is transferred to the TSR when the TSR is idle or has completed sending the previous data byte. The TSR shifts the data out onto the TX output pin at the selected baud rate. The transmitter sends the start bit followed by the data bits (starting with the LSB), inserts the proper parity-bit if enabled, and adds the stop-bit(s).

The transmitter may be configured for 5, 6, 7 or 8 data bits with or without parity or 9 data bits without parity. If 5, 6, 7 or 8 bit data with parity is selected, the TX FIFO contains 8 bits data and the parity bit is automatically generated and transmitted. If 9 bit data is selected, parity cannot be generated. The 9th bit will not be transmitted unless the wide mode is enabled.

Wide Mode

The XR21B1421 device may be configured for wide mode using the SET_TRANSFER_MODE (report 0x48). In wide mode the XR21B1421 checks each received character for parity, framing or overrun errors, and for break status. Note that although the GET_UART_STATUS (report 0x42), reports these same errors, they are historical or latched errors indicating that an error has occured at least once since the previous GET_UART_STATUS report. By comparison, in wide mode, each character is accompanied by real time error and status indicators.

Wide Mode Transmit

Wide mode may be selected with any (5, 6, 7, 8 or 9 bit) character size. For 5, 6 and 7 bit data, bits 5-7, 6-7, or 7 (respectively) are filled with ’0’. Two bytes from the USB host are used to form the data character which is serialized and transmitted. The least significant bit of the second byte contains the parity bit or the 9th bit of the character in 9 bit mode. The remaining 7 bits of the second byte are discarded.

Receiver

The receiver consists of a 512-byte RX FIFO and a Receive Shift Register (RSR). Data that is received in the RSR via the RX pin is transferred into the RX FIFO. Data from the RX FIFO is sent to the USB host by in response to a interrupt-in request. Depending on the mode, error / status information for that data character may or may not be stored in the RX FIFO with the data.

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Normal receive operation with 5, 6, 7 or 8-bit data

Received data is stored in the RX FIFO. Any parity, framing or overrun error or break status information related to the data is discarded. The receive data format is shown in Figure 4.

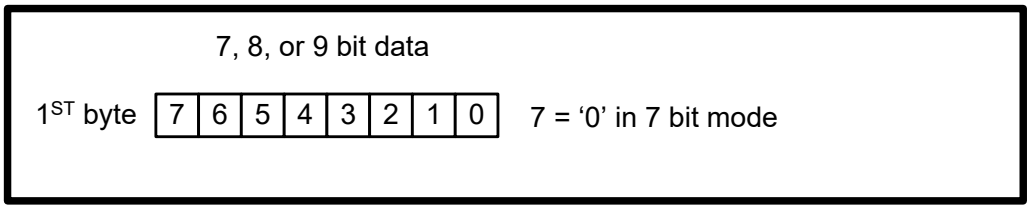

Figure 4: Normal Operation Receive Data Format

Normal receive operation with 9-bit data

The first 8 bits of data received is stored in the RX FIFO. The 9th bit as well as any parity, framing or overrun error or break status information related to the data is discarded.

Wide mode receive operation with 5, 6, 7 or 8-bit data

Two bytes of data are loaded into the RX FIFO for each byte of data received. The first byte is the received data. The second byte consists of the error bits and break status. The wide mode receive data format is shown in Figure 5.

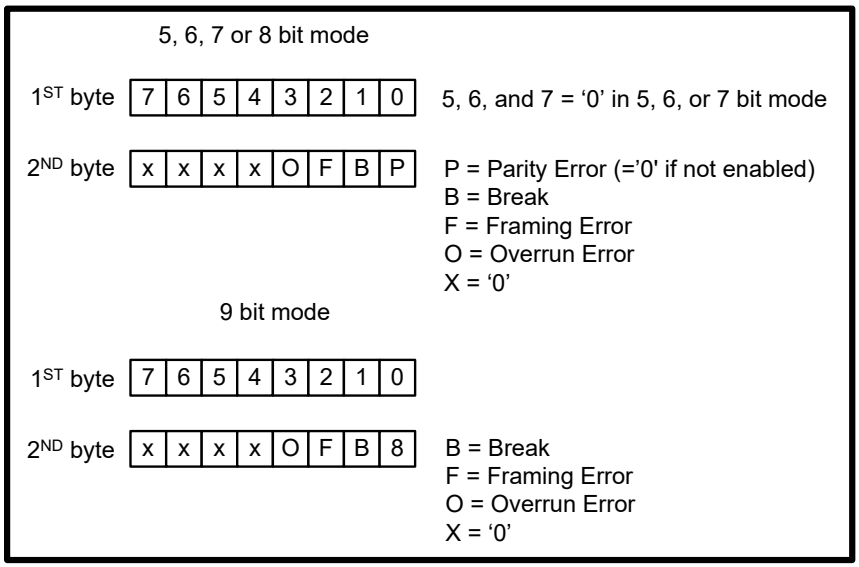

Figure 5: Wide Mode Receive Data Format

Wide mode receive operation with 9-bit data

Two bytes of data are loaded into the RX FIFO for each byte of data received. The first byte is the first 8 bits of the received data. The 9th bit received is stored in the bit 0 of the second byte. The parity bit is not received / checked. The remainder of the 2nd byte consists of the framing and overrun error bits and break status.

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RX FIFO Low Latency

In normal operation, all bulk-in transfers will be of maxPacketSize (64) bytes to improve throughput and to minimize host processing. When there are 64 bytes of data in the RX FIFO, the XR21B1421 will acknowledge a bulk-in request from the host and transfer the data packet. If there are less than 64 bytes in the RX FIFO, the XR21B1421 may respond to the bulk-in request with a NAK indicating that data is not ready to transfer at that time. However, if there are less than 64 bytes in the RX FIFO and no data has been received for more than 3 character times, the XR21B1421 will acknowledge the bulk-in request and transfer any data in the RX FIFO to the USB host.

In some cases, especially when the baud rate is low, this behavior may increase latency unacceptably. The low latency mode is automatically set whenever the baud rate is set to a value of less than 46921 bps. Additionally, a user may manually enable the low latency mode using the SET_TRANSFER_MODE report (0x48) to immediately transfer any received data in the RX FIFO to the USB host without waiting for 3 character times.

GPIO

Each UART has 10 GPIO pins in addition to the TX and RX pins. Each GPIO pin may also be configured for one or more special functions. Please refer to the pin descriptions for the default functionality of each of the general purpose I/Os.

Clock Out

The GPIO0/CLK pin may be configured as a clock output using the SET_PIN_CONFIG or SET_GPIO_CONFIG reports. The output frequency of the clock out may be programmed between 24 MHz and approximately 47 KHz. The duty cycle may also be programmed from 50/50 to single low or high going pulse. The default values of 0 for both DIV_HI and DIV_LO will result in a frequency of 24 MHz. For any non-zero values for DIV_HI and DIV_LO, the clock frequency is determined by the formula:

FREQ = 24 MHz / (DIV_HI + DIV_LO).

The duty cycle is determined by the ratio of DIV_HI to DIV_LO. GPIO0 will output this clock if is enabled in the GPIO_-MODE register.

Flow Control

The XR21B1421 is able to perform both hardware and software flow control. Both hardware and software flow control modes are configured via the SET_UART_CONFIG report. In both modes, flow control is asserted when the bytes in the RX FIFO reach the watermark set in the RX_THRESHOLD setting. Hardware flow control may either be RTS/CTS or DTR/DSR controlled. Note that although the default pin configuration for GPIO1/RTS# and GPIO2/CTS# are for RTS output and CTS input respectively, the hardware RTS/CTS flow control mode must be set in order to utilize the flow control functionality. Alternately, the pin configurations may be changed to GPIO functionality using the SET_PIN_CONFIG or SET_GPIO_-CONFIG reports for these pins to be used for GPIO functionality.

Automatic RTS/CTS Hardware Flow Control

Automatic RTS/CTS flow control is used to prevent data overrun errors in the local RX FIFO using the RTS signal to the remote UART. The RTS signal will be asserted (low) when there are less than 450 bytes in the receive FIFO. When the RX FIFO reaches the 450 byte threshold, the RTS pin will be deasserted. The CTS# input of the remote UART is monitored to suspend/restart the transmitter. Refer to Figure 6. Conversely, when the remote UART reaches its receive FIFO threshold, its RTS will be deasserted, and the XR21B1421 CTS input will cause the device to suspend data transmission.

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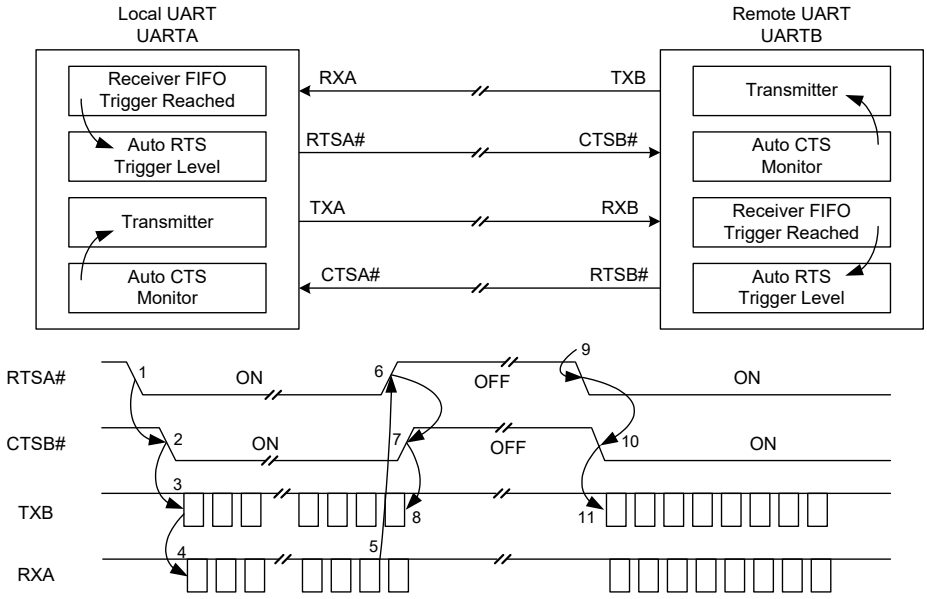

1) COM port opened, RX FIFO empty, RTSA# output is asserted
2) Signal propagated to CTSB# input
3) Data bytes enter TX FIFO, begin transmitting on TXB
4) Data propagates to Receiving device RXA
5) RX FIFO reaches threshold
6) RTSA# de-asserts
7) Signal propagates to CTSB# input
8) Transmission stops on TXB
9) USB Bulk-In empties RX FIFO below threshold, RTSA# is asserted
10) Signal propagated to CTSB# input
11) Data bytes resume transmitting on TXB

Figure 6: Auto RTS and CTS Flow Control Operation

Automatic DTR/DSR Hardware Flow Control

Auto DTR/DSR hardware flow control behaves the same as the Auto RTS/CTS hardware flow control described above except that it uses the DTR# and DSR# signals. GPIO8 and GPIO9 become DTR# and DSR#, respectively, when the SET_UART_CONFIG or SET_PIN_CONFIG report configures the device for DTR/DSR hardware flow control.

Automatic XON/XOFF Software Flow Control

When software flow control is enabled, the XR21B1421 compares the receive data characters with the programmed XON or XOFF characters. If the received character matches the programmed XOFF character, the XR21B1421 will halt transmission as soon as the current character has completed transmission. Data transmission is resumed when a received character matches the XON character.

In the receive data direction, the XOFF character will be sent when there are 450 bytes in the receive FIFO. When there are again less than 450 bytes in the RX FIFO, the XON character will be send. This threshold may be changed using the SET_FLOW_CTRL_THRESHOLD HID report.

Software flow control is enabled / disabled by the SET_UART_CONFIG report. Additionally, the SET_SW_FLOW_CONFIG report may be used to configure the start (XON) and stop (XOFF) characters.

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Multidrop mode with address matching

The XR21B1421 device has two address matching modes which are set by the SET_ADDR_MATCH_CONFIG report. These modes are intended for a multi-drop network application. In these modes, the UNI_ADD holds a unicast address and the MULTI_ADD holds a multicast address. An address match occurs when an address byte (9th bit or parity bit is '1') is received that matches the value stored in either the UNI_ADD or MULTI_ADD field. To send an address byte use 8 bit data with mark parity. To send data bytes, use 8 bit data with space parity.

Receiver

If an address match occurs in either of the address matching modes, the address byte will not be loaded into the RX FIFO, but all subsequent data bytes will be loaded into the RX FIFO. The UART Receiver will automatically be disabled when an address byte is received that does not match the values in the UNI_ADD or MULTI_ADD characters.

Transmitter

In flow control mode 3, the UART transmitter will transmit irrespective of the RX address match. In flow control mode 4, the UART will only transmit following an RX address match.

Programmable Turn-Around Delay

By default, the selected auto RS-485 half-duplex enable pin (either GPIO3/RS485 or GPIO1/RTS#/RS485) will be de-asserted immediately after the stop bit of the last byte has been shifted. However, this may not be ideal for systems where the signal needs to propagate over long cables. Therefore, the de-assertion of the auto RS-485 half-duplex enable may be delayed from 1 to 15 bit times via the SET_XCVR_EN_DELAY report to allow for the data to reach distant UARTs.

UART Half-Duplex Mode

In half-duplex mode, the UART will ignore any data on the RX input when the UART is transmitting data. The half-duplex mode may be configured using the SET_UART_CONFIG report.

IR Mode

The XR21B1421 supports IR mode at a maximum baud rate of 2.5 Mbaud with transmit pulses of 3/16th or 4/16th of a bit period and centered in the bit period. Receive data may be inverted to conform to some manufacturer's non-standard devices. IR mode is disabled by default but may be enabled by the SET_IR_MODE report 0x56.

USB_STAT Pins

The XR21B1421 has two USB_STAT output pins that may be used to indicate 3 different statuses in either positive or negative polarity. The SUSPEND status indicates that the XR21B1421 device has been placed into a suspended state by the USB host. This output may then be used by external circuitry, for example, to power down devices in order to meet USB power requirements for suspend mode. The LOW_POWER status is similar to the SUSPEND status, but LOW_POWER is also asserted for high power devices (any device that consume more than 100 mA of VBUS power from the USB host), before the device is configured during enumeration by the USB host. For low power devices (devices that consume 100 mA or less of VBUS power), SUSPEND and LOW_POWER status outputs are functionally the same. Lastly, the BUS_RST output status is asserted any time the XR21B1421 device is being reset by the USB host. This status output could be used, for example, by an FPGA or other logic device to reset this external logic.

Use Suspend

The USE_SUSPEND bit controls the GPIO pins when the XR21B1421 device is suspended by the USB host. If USE_SUSPEND is cleared to '0', GPIO pins retain their output states when the device is suspended. When USE_SUSPEND is set to '1', GPIO pins are assigned behavior defined by the SUSPEND_STATE and SUSPEND_MODE fields of SET_PIN_CONFIG or SET_SUSPEND_OUTPUT_CONFIG reports, with the following exceptions: GPIO0/CLK when configured as an output clock will always be driven low, i.e the clock output will stop, and GPIO1/RTS#/RS485 or GPIO3/RS485 when configured as a auto RS-485 half-duplex enable will always be deasserted.

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The SUSPEND_STATE field will set or clear the GPIO pin and the SUSPEND_MODE field will configure any GPIO output as open drain or push-pull output. Refer to “GET / SET_PIN_CONFIG” on page 41 or “GET / SET_SUSPEND_OUTPUT_CONFIG” on page 31. Configuration using the SET_SUSPEND_OUTPUT_CONFIG report will be lost at the next power cycle or bus reset of the device. Configuration using the SET_PIN_CONFIG report will be permanent.

TXT and RXT Pins

The Transmit toggle and Receive toggle pins "toggle" at a rate of approximately 10 Hz whenever the UART transmit and receive pins (respectively) are active.

OTP

The OTP is an on-chip non-volatile memory, that is incrementally one-time programmable via the USB interface. Some bits are pre-programmed at the factory and caution must be taken not to program any locations except those user defined addresses given in this data sheet. Some of the HID reports result in irreversible programming of the OTP. Once a specific report programs a portion of the OTP, the lock bit for that section of the OTP will be set and further changes to that section will not be allowed. Note that all OTP writes will take immediate effect, except for setting the global lock bit (report 0x68), which requires a hardware or power on reset to take effect.

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USB Control Commands

The following table shows all of the USB Control Commands that are supported by the XR21B1421. Commands include standard USB commands, CDC-ACM commands and custom MaxLinear commands.

Table 3: Supported USB Control Commands

Name	Request Type	Request	Value		Index		Length		Description
			LSB	MSB	LSB	MSB	LSB	MSB	
DEV GET_STATUS	0x80	0	0	0	0	0	2	0	Device: remote wake-up + self-powered
IF GET_STATUS	0x81	0	0	0	0	0	2	0	Interface: zero
EP GET_STATUS	0x82	0	0	0	0x0,0x4, 0x84	0	2	0	Endpoint: halted
DEV CLEAR_FEATURE	0x00	1	1	0	0	0	0	0	Device remote wake-up
EP CLEAR_FEATURE	0x02	1	0	0	0x0,0x4, 0x84	0	0	0	Endpoint halt
DEV SET_FEATURE	0x00	3	1	0	0	0	0	0	Device remote wake-up
DEV SET_FEATURE	0x00	3	2	0	0	test	0	0	Test mode - factory use only
EP SET_FEATURE	0x02	3	0	0	0x0,0x4, 0x84	0	0	0	Endpoint halt
SET_ADDRESS	0x00	5	addr	0	0	0	0	0	addr = 1 to 127
GET_DESCRIPTOR	0x80	6	0	1	0	0	len MSB	len MSB	Device descriptor
GET_DESCRIPTOR	0x80	6	0	2	LangID	LangID	len MSB	len MSB	Configuration descriptor
GET_DESCRIPTOR	0x80	6	0	3	0	0	len MSB	len MSB	String descriptor
GET_CONFIGURATION	0x80	8	0	0	0	0	1	0	
SET_CONFIGURATION	0x00	9	n	0	0	0	0	0	n = 0, 1
GET_INTERFACE	0x81	10	0	0	0	0	1	0	

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HID Reports

All of the functionality of the XR21B1421 device is controlled via HID reports. Some of these reports will program the on-chip OTP memory. All of the HID reports in the OTP customization section (reports 0x47 and 0x60 through 0x67) will permanently program the on-chip OTP. All other HID reports do not program the OTP. The SET_GPIO_CONFIG (report 0x49) dynamically configures the GPIO pins, but does not program the OTP as does the SET_PIN_CONFIG report.

Table 4: XR21B1421 HID Reports

Report ID	Report Name	Size
UART Data Transfer (Interrupt Transfers)		
0X1 - 0x3F	SET TRANSMIT DATA	2 - 64
0X1 - 0x3F	GET RECEIVE DATA	2 - 64
Device Configuration (Control Transfers)		
0x40	SET DEVICE RESET	2
0x41	GET / SET UART ENABLE	2
0x42	GET UART STATUS	7
0x43	SET CLEAR FIFOS	2
0x44	GET GPIO STATE	3
0x45	SET GPIO STATE	5
0x46	GET VERSION	3
0x48	GET / SET TRANSFER MODE	3
0x49	GET / SET GPIO CONFIG	13
0x4A	GET / SET SUSPEND OUTPUT CONFIG	5
0x4F	GET CHIP ID	7
UART Configuration (Control Transfers)		
0x50	GET / SET UART CONFIG	9
0x51	SET TRANSMIT LINE BREAK	2
0x52	SET STOP LINE BREAK	2
0x53	GET / SET SW FLOW CTRL CONFIG	3
0x54	GET / SET ADDR MATCH CONFIG	3
0x55	GET / SET LOOPBACK MODE	2
0x56	GET / SET IR MODE	2
0x57	GET / SET XCVR EN DELAY	2
0x58	GET / SET FLOW CTRL THRESHOLD	3
OTP Customization (Control Transfers)		
0x47	GET / SET OTP LOCK BYTE	3

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Table 4: XR21B1421 HID Reports

Report ID	Report Name	Size
0x60	GET / SET USB CONFIG	11
0x61	GET / SET VENDOR STRING 1	4 - 64
0x62	GET / SET VENDOR STRING 2	2 - 64
0x63	GET / SET PRODUCT STRING 1	4 - 64
0x64	GET / SET PRODUCT STRING 2	2 - 64
0x65	GET / SET SERIAL STRING	4 - 64
0x66	GET / SET PIN CONFIG	20
0x67	GET / SET LANG ID	3
0x68	GET / SET GLOBAL LOCK	2

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HID Report Descriptions

All of the functionality of the XR21B1421 device is controlled via HID reports. Some of these reports will program the on-chip OTP memory. All of the HID reports in the OTP customization section (reports 0x47 and 0x60 through 0x67) will permanently program the on-chip OTP. All other HID reports do not program the OTP. The SET_GPIO_CONFIG (report 0x49) dynamically configures the GPIO pins, but does not program the OTP as does the SET_PIN_CONFIG report.

SET_TRANSMIT_DATA

Transfer Type: Interrupt Out

Transfer Size: 2 - 64 bytes

The SET_TRANSMIT_DATA report transmits up to 63 bytes of data to the UART per transfer.

Field	Offset	Size	Value	Description
Report ID	0	1	0x01 - 0x3F	Indicates the size of the data transfer to be sent to the device from 1 (0x01) to 63 (0x3F) bytes excluding the report ID itself.
Data	1	1-63		Data from USB host to UART

GET_RECEIVE_DATA

Transfer Type: Interrupt In

Transfer Size: 2 - 64 bytes

The GET_RECEIVE_DATA report receives up to 63 bytes of data from the UART per transfer. This report is returned when the USB host polls the Interrupt-In endpoint at 1 ms intervals.

Field	Offset	Size	Value	Description
Report ID	0	1	0x01 - 0x3F	Indicates the size of the data transfer to be sent to the device from 1 (0x01) to 63 (0x3F) bytes excluding the report ID itself.
Data	1	1-63		Data from USB host to UART

SET_DEVICE_RESET

Transfer Type: Control Out

Transfer Size: 2 bytes

The SET_DEVICE_RESET report performs a software reset of the XR21B1421 device that resets the USB interface and clears the UART RX and TX FIFOs, but does not change any UART configuration settings or change any pin configurations. Any changes to on-chip OTP will not be reflected following the software reset. During software reset, the internal pull-up on the USBD+ pin will be disabled to signal the USB host that a detach event has occurred. Following reset, the pull-up resistor will be enabled to signal an attach event to the USB host.

Field	Offset	Size	Value	Description
Report ID	0	1	0x40	Force device hardware reset
Value	1	1		Set of any value forces reset

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GET / SET_UART_ENABLE

Transfer Type: Control In / Out

Transfer Size: 2 bytes

The GET / SET_UART_ENABLE report gets or sets the UART enable (default is disabled). Disable the UART and re-enable before sending or receiving UART data.

Field	Offset	Size	Value	Description
Report ID	0	1	0x41	Enable / disable UART
UART Enable	1	1	0x00 0x01	Disable(d) Enable(d) - default

GET_UART_STATUS

Transfer Type: Control In

Transfer Size: 7 bytes

The GET_UART_STATUS report returns the break and error status of the UART and number of bytes in RX and TX FIFOs. The TX and RX FIFOs hold a maximum of 512 bytes.

Field	Offset	Size	Value	Description
Report ID	0	1	0x42	Get status of historical error and status and RX and TX FIFO fill
TX FIFO MSB	1	1		Number of bytes in transmit FIFO
TX FIFO LSB	2	1		
RX FIFO MSB	3	1		Number of bytes in receive FIFO
RX FIFO LSB	4	1		
Error Status	5	1	Error Status	Receive Error / Break status Error Status indicates parity, overrun, and frame errors as well as break status for received data. Any error / break status will be latched until the status is read using the Get_UART_Status report. These bits will cleared when read. Bit 0 - parity error - '1' indicates parity error Bit 1 - overrun error - '1' indicates overrun Bit 2 - framing error - '1' indicates framing error Bit 3 - break status - '1' indicates break condition occured
Break Status	6	1	0x00 0x01	Receive - No Line Break Receive - Line Break Active

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SET_CLEAR_FIFOS

Transfer Type: Control Out

Transfer Size: 2 bytes

The SET_CLEAR_FIFOS report clears the selected FIFO buffers.

Field	Offset	Size	Value	Description
Report ID	0	1	0x43	Clear FIFO buffers
Clear	1	1	Value	Clears FIFOs Bit 0 - '1' clears TX FIFO (self-clearing) Bit 1 - '1' clears RX FIFO (self-clearing)

GET_GPIO_STATE

Transfer Type: Control In

Transfer Size: 3 bytes

The GET_GPIO_STATE report gets the actual state of the GPIO or flow control pins configured as either inputs or outputs.

Field	Offset	Size	Value	Description
Report ID	0	1	0x44	Get status of GPIO pins
State MSB	1	1		See Table 5
State LSB	2	1		

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Table 5: Get State Bit Positions

Bit	GPIO/Pin	Pin Name
15		Reserved
14	S1	USB_STAT1
13	9	GPIO9/DSR#
12	8	GPIO8/DTR#
11	7	GPIO7/RI#
10	6	GPIO6/CD#
9		Reserved
8	S2	USB/STAT2
7	5	GPIO5/RXT
6	4	GPIO4/TXT
5	RX	RX
4	TX	TX
3	3	GPIO3/RS485
2	2	GPIO2/CTS#
1	1	GPIO1/RTS#
0	0	GPIO0/CLK

SET_GPIO_STATE

Transfer Type: Control Out

Transfer Size: 5 bytes

The SET_GPIO_STATE report sets the state of pins configured as either GPIO or flow control outputs. Each bit position in the state value will be asserted to the specified ’1’ or ’0’ on the GPIO pin output if the direction for that IO pin is set to output and if the corresponding bit position in the mask is set to a ’1’.

Field	Offset	Size	Value	Description
Report ID	0	1	0x45	Set status of GPIO pins
State MSB	1	1		See Table 6
State LSB	2	1		
Mask MSB	3	1		Mask for output state changes
Mask LSB	4	1		

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Table 6: Set State Bit Positions

Bit	GPIO/Pin	Pin Name
15:14		Reserved
13	9	GPIO9/DSR#
12	8	GPIO8/DTR#
11	7	GPIO7/RI#
10	6	GPIO6/CD#
9:8		Reserved
7	5	GPIO5/RXT
6	4	GPIO4/TXT
5:4		Reserved
3	3	GPIO3/RS485
2	2	GPIO2/CTS#
1	1	GPIO1/RTS#
0	0	GPIO0/CLK

GET_VERSION

Transfer Type: Control In

Transfer Size: 7 bytes

The GET_VERSION report gets vendor, product and revision information.

Field	Offset	Size	Value	Description
Report ID	0	1	0x46	Get device version information
PID LSB	1	1	0x21	Least Significant Byte of PID
Revision	2	1	0x02	Manufacturer revision number

GET / SET_OTP_LOCK_BYTE

Transfer Type: Control In / Out

Transfer Size: 3 bytes

The GET / SET_OTP_LOCK_BYTE report gets or sets lock status of on-chip OTP values. Caution: OTP fields that are locked may not be unlocked or have any further modifications.

Field	Offset	Size	Value	Description
Report ID	0	1	0x47	Get device lock bytes
Lock Value MSB	1	1	0xFF	OTP programmed fields

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Field	Offset	Size	Value	Description
Lock Value LSB	2	1	0x8F	OTP programmed fields

Table 7 shows 13 distinct fields within the OTP. Each field may be individually locked by SET_LOCK_BYTE report by writing a '0' in the selected bit position to lock the field. Setting a value of 0x0 will lock all of the OTP fields from any further modifications.

Table 7: Lock State Bit Positions

Bit	Name
15	Vendor ID String2
14	Vendor ID String1
13	Auto Flush Buffers
12	Release Version
11	Power Mode
10	bMaxPower
9	PID
8	VID
7	Language ID
6:4	Reserved
3	Pin Config
2	Serial String
1	Product ID String2
0	Product ID String1

GET / SET_TRANSFER_MODE

Transfer Type: Control In / Out

Transfer Size: 3 bytes

The GET / SET_TRANSFER_MODE report reports or sets the UART wide mode.

Field	Offset	Size	Value	Description
Report ID	0	1	0x48	Get or set UART wide mode
TX Wide Enable	1	1	Bit 0 = 0	Disable TX wide mode - default
			Bit 0 = 1	Enable TX wide mode

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Field	Offset	Size	Value	Description
RX Wide Enable	2	1	Bit 0 = 0	Disable RX wide mode - default
			Bit 0 = 1	Enable RX wide mode
			Bit 1 = 0	Disable low latency
			Bit 1 = 1	Enable low latency - default

GET / SET_GPIO_CONFIG

Transfer Type: Control In / Out

Transfer Size: 13 bytes

The GET / SET_GPIO_CONFIG report contains several fields that may be used to get or set a variety of configurations for the GPIO pins, as detailed in Table 8. The direction field reports or sets pins configured as GPIO as inputs or outputs. The open drain field reports or sets GPIO outputs as either push-pull or open drain. The pull-up and pull-down field enables / disables weak pull-up or pull-down resistors on GPIO inputs. The clock divisor fields set the output clock frequency for GPIO0_CLK.

The default configuration for the XR21B1421 pins is defined by the Pin Config report (0x66). Note that the default direction and functionality of pins in the GET_GPIO_CONFIG report will not initially match that of the Pin Configuration report. Any changes to GPIO pins made via the SET_GPIO_CONFIG report will take effect immediately and will be lost following any subsequent power cycle or re-enumeration of the device. Pins configured for special functions, e.g. CLK, RTS#, etc. are not controlled by the direction, open drain, pull-up, or pull-down fields of this report.

Field	Offset	Size	Value	Description
Report ID	0	1	0x49	Get or set GPIO pin configuration (dynamic)
Direction MSB	1	1	See Table 8	Direction selection (input or output) 0: input 1: output
Direction LSB	2	1		
Open Drain MSB	3	1		Open drain selection 0: pin configured as an output will be open drain 1: pin configured as an output will be push-pull output
Open Drain LSB	4	1		
Pull-up MSB	5	1		Pull-up resistor enable 0: disables pull-up resistor on pin configured as an input 1: enables pull-up resistor on pin configured as an input
Pull-up LSB	6	1		
Pull-down MSB	7	1		Pull-down resistor enable 0: disables pull-down resistor on pin configured as an input 1: enables pull-down resistor on pin configured as an input, unless pull-up resistor is also enabled for same input pin
Pull-down LSB	8	1		
Clk div. High	9	1	See Table 9	Clock divider for high period
Clk div. Low	10	1	See Table 10	Clock divider for low period
GPIO Mode 0	11	1	See Table 11	Auto RS-485 half-duplex enable control
GPIO Mode 1	12	1	See Table 12	Clock and toggle controls

Table 8 shows the GPIO pins that may be controlled or queried by the GET / SET GPIO CONFIG report. A ’1’ or ’0’ in the appropriate bit position will control the direction, open drain selection and pull-up or pull-down for that GPIO pin.

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Table 8: GPIO Config Bit Positions

Bit	GPIO/Pin	Pin Name
15:14		Reserved
13	9	GPIO9/DSR#
12	8	GPIO8/DTR#
11	7	GPIO7/RI#
10	6	GPIO6/CD#
9:8		Reserved
7	5	GPIO5/RXT
6	4	GPIO4/TXT
5:4		Reserved
3	3	GPIO3/RS485
2	2	GPIO2/CTS#
1	1	GPIO1/RTS#
0	0	GPIO0/CLK

Table 9: Clock Divider High Bit Positions

Bit	Description
7:0	**High Period**

Table 10: Clock Divider Low Bit Positions

Bit	Description
7:0	**Low Period**

Output clock frequency is determined by the formula 24 MHz / (High period + Low period) unless both values are 0. For example, if both Clock Divider High and Clock Divider Low are set to a value of 1, the clock will be 12 MHz with a 50% duty cycle. If both high and low periods are set to 0 the clock frequency will be 24 MHz. This clock will be selected as an output if the SET_PIN_CONFIG or the SET_GPIO_CONFIG report selects the clock output.

Output clock must be enabled by GPIO_MODE1 CLK_EN field of this report.

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Table 11: GPIO Mode 0 Bit Positions

Bit	Description
7	**Reserved**
6:5	**RS485_SEL** 00: GPIO3/RS485 pin functions as GPIO 01: GPIO3/RS485 pin functions as auto RS-485 half-duplex enable (RS485_PIN = '1') 10: GPIO3/RS485 pin asserted during UART transmit only with address match (RS485_PIN = '1') 11: Reserved
4	**RS485_PIN** 0: Selected auto RS-485 half-duplex enable pin is GPIO1/RTS#/RS485, function determined by MODEM_SEL field 1: Selected auto RS-485 half-duplex enable pin is GPIO3/RS485, function determined by RS485_SEL field
3	**RS485_POL** 0: Auto RS-485 half-duplex enable active low 1: Auto RS-485 half-duplex enable active high
2:0	**MODEM_SEL** With MODEM_SEL = "001" for RTS/CTS flow control, H/W flow control must also be enabled in UART_CONFIG report (not default). 000: No GPIO pins used for either RTS/CTS or DTR/DSR hardware flow control 001: GPIO1 and GPIO2 used for hardware auto-RTS/CTS flow control - default 010: GPIO8 and GPIO9 used for hardware auto-DTR/DSR flow control 011: GPIO1/RTS#/RS485 pin asserted during UART transmit (RS485_PIN = '0') 100: GPIO1/RTS#/RS485 pin asserted during UART transmit only with address match (RS485_PIN = '0') 101 to 111: Reserved

Table 12: GPIO Mode 1 Bit Positions

Bit	Description
7	**RXT_EN** 0: Disable Receive toggle output function (pin reverts to GPIO functionality) 1: Enable Receive toggle output function
6	**TXT_EN** 0: Disable Transmit toggle output function (pin reverts to GPIO functionality) 1: Enable Transmit toggle output function
5:1	**Reserved**
0	**CLK_EN** 0: Disable Clock output function (pin reverts to GPIO functionality) 1: Enable Clock output function

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GET / SET_SUSPEND_OUTPUT_CONFIG

Transfer Type: Control In / Out

Transfer Size: 5 bytes

The GET / SET_SUSPEND_OUTPUT_CONFIG report gets or sets GPIO pins state and mode when the device is suspended by the USB host if the USE_SUSPEND bit is enabled. Suspend state is the value that is driven on the corresponding bit position in Table 13. Suspend mode configures the output to push-pull or open drain. Suspend state and suspend mode both default to 0x0000.

Field	Offset	Size	Value	Description
Report ID	0	1	0x4A	Get or Set output states and modes during suspend
Suspend state MSB	1	1	See Table 13	Asserted state in suspend mode 0: All GPIO pins are asserted low in USB Suspend state if USE_SUSPEND = '1' 1: All GPIO pins are asserted high in USB Suspend state if USE_SUSPEND = '1'
Suspend state LSB	2	1		
Suspend mode MSB	3	1		Output mode when in suspend mode 0: GPIO pin is Open Drain in USB Suspend state if USE_SUSPEND = '1' 1: GPIO pin is Push-pull in USB Suspend state if USE_SUSPEND = '1'
Suspend mode LSB	4	1		

Table 13: Suspend State Mode Bit Positions

Bit	GPIO/Pin	Pin Name
15		USE_SUSPEND
14		Reserved
13	9	GPIO9/DSR#
12	8	GPIO8/DTR#
11	7	GPIO7/RI#
10	6	GPIO6/CD#
9:8		Reserved
7	5	GPIO5/RXT
6	4	GPIO4/TXT
5:4		Reserved
3	3	GPIO3/RS485
2	2	GPIO2/CTS#
1	1	GPIO1/RTS#
0	0	GPIO0/CLK

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GET / SET_CHIP_ID

Transfer Type: Control In / Out

Transfer Size: 7 bytes

The GET / SET_CHIP_ID report reports MaxLinear's device manufacturer's USB Vendor and Product IDs (VID and PID) irrespective of any changes to the VID and PID using the SET_USB_CONFIG report. (However, values from the SET_USB_CONFIG report will be reported to the USB host during device enumeration.)

Field	Offset	Size	Value	Description
Report ID	0	1	0x4F	Get Chip ID
VID Chip LSB	1	1	0xE2	LSB of Exar Vendor VID
VID Chip MSB	2	1	0x04	MSB of Exar Vendor PID
PID Chip LSB	3	1	0x21	LSB of Exar Vendor PID
PID Chip MSB	4	1	0x14	MSB of Exar Vendor VID
Chip Revision	5	1	0x02	Device revision
Reserved	6	1	0x00	Reserved, return 0x00

GET / SET_UART_CONFIG

Transfer Type: Control In / Out

Transfer Size: 9 bytes

The GET / SET_UART_CONFIG report gets or sets baud rate, parity, flow control mode, and number of data and stop bits as well as controls auto-RS-485 half-duplex and hardware flow control modes.

Field	Offset	Size	Value	Description
Report ID	0	1	0x50	Get or set UART configuration
Baud Rate 3	1	1	Baud[31:24]	OTP programmed fields
Baud Rate 2	2	1	Baud[23:16]	Baud: Any integer value from 300 (0x0000012C) to 12,000,000 (0x00B71B00) is a valid baud rate. The default baud rate is 115,200 bps.
Baud Rate 1	3	1	Baud[15:8]	
Baud Rate 0	4	1	Baud[7:0]	
Parity	5	1	0x00	No Parity (Default)
			0x01	Even Parity
			0x02	Odd Parity
			0x03	Mark Parity
			0x04	Space Parity
Data Control	6	1	See Table 14	Control flow control mode, RS-485 half-duplex mode select and polarity, and duplex

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Field	Offset	Size	Value	Description
Data bits	7	1	0x00 or 0x05	5 data bits
			0x01 or 0x06	6 data bits
			0x02 or 0x07	7 data bits
			0x03 or 0x08	8 data bits (Default)
			0x04 or 0x09	9 data bits
Stop bits	8	1	0x00	1 stop bit (Default)
			0x01	1.5 if 5 bit data, 2 stop bits if 6, 7, 8 or 9 bit data

Table 14: Data Control Bit Positions

Bit	Description
7:4	**Reserved**
3	**HDUP** 0: Disable half-duplex mode (Default) 1: Enable half-duplex mode
2:0	**FLOW_CTL** 000: No flow control (Default) 001: Hardware flow control 010: Software flow control 011: Multidrop mode - Receive only after address match, Tx independent 100: Multidrop mode - Receive / transmit only after address match 101 to 111: Reserved

SET_TRANSMIT_LINE_BREAK

Transfer Type: Control Out

Transfer Size: 2 bytes

The SET_TRANSMIT_LINE_BREAK report asserts a line break until the set count value is decremented to 0.

Field	Offset	Size	Value	Description
Report ID	0	1	0x51	Set Line Break condition
Interval	1	1	Count	Count in ms Any integer value from 1 to 255 (0xFF) is a valid interval. A value of 0 will assert the line break condition until the SET_STOP_LINE_BREAK report 0x52 is received, or until any non-zero value is decremented to 0. Any data in the TX FIFO will be purged when the line break condition is asserted.

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SET_STOP_LINE_BREAK

Transfer Type: Control Out

Transfer Size: 2 bytes

The SET_STOP_LINE_BREAK report terminates any line break condition in progress.

Field	Offset	Size	Value	Description
Report ID	0	1	0x52	Set Stop Line Break condition
Value	1	1		Set using any value

GET / SET_SW_FLOW_CTL_CONFIG

Transfer Type: Control In / Out

Transfer Size: 3 bytes

The GET / SET_SW_FLOW_CTL_CONFIG report gets or sets the software flow control XON and XOFF values. The XOFF value is used by the receiver to stop transmission. If the received value matches the XOFF value with software flow control enabled, the transmitter will halt transmission until a received character matches the XON value. The default XON character is 0x11 and the default XOFF character is 0x13.

Field	Offset	Size	Value	Description
Report ID	0	1	0x53	Get / Set SW Flow Control Configuration
XON	1	1	Char1	Char1 is the XON
XOFF	2	1	Char2	Char2 is the XOFF

GET / SET_ADDR_MATCH_CONFIG

Transfer Type: Control In / Out

Transfer Size: 3 bytes

The GET / SET_ADDR_MATCH_CONFIG report gets or sets the multi-drop mode unicast and multicast address match values.

Field	Offset	Size	Value	Description
Report ID	0	1	0x54	Get / Set Address Matching Configuration
UNI_ADD	1	1	Char1	Unicast address (default value 0x11)
MULTI_ADD	2	1	Char2	Multicast address (default value 0x13)

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GET / SET_LOOPBACK_MODE

Transfer Type: Control In / Out

Transfer Size: 2 bytes

The GET / SET_LOOPBACK_MODE report gets or sets internal loopback of the UART data and flow control signals.

Field	Offset	Size	Value	Description
Report ID	0	1	0x55	Get / Set Internal UART Loopback
Loop	1	1	See Table 15	Loopback mode control

Table 15: Loopback Mode Bit Positions

Bit	Description
7:3	**Reserved**
2	**DTR_DSR** 0: Disable loopback (default) 1: Enable loopback
1	**RTS_CTS** 0: Disable loopback (default) 1: Enable loopback
0	**TX_RX** 0: Disable loopback (default) 1: Enable loopback

GET / SET_IR_MODE

Transfer Type: Control In / Out

Transfer Size: 2 bytes

The GET / SET_IR_MODE report gets or sets the infrared mode.

Field	Offset	Size	Value	Description
Report ID	0	1	0x56	Get / Set IR mode
IR mode	1	1	See Table 16	Infrared mode control

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Table 16: IR Mode Bit Positions

Bit	Description
7:3	**Reserved**
2	**TX_PULSE** 0: Transmit pulses are 3/16th of and centered in the bit period 1: Transmit pulses are 4/16th of and centered in the bit period
1	**RX_INVERT** 0: Standard IrDA receive data 1: Non-standard inverted receive data
0	**EN** 0: Disable IR mode 1: Enable IR mode

GET / SET_XCVR_EN_DELAY

Transfer Type: Control In / Out

Transfer Size: 2 bytes

The GET / SET_XCVR_EN_DELAY report gets or sets the delay in deasserting the or auto RS-485 half-duplex enable.

Field	Offset	Size	Value	Description
Report ID	0	1	0x57	Get / Set auto RS-485 half-duplex enable delay
Delay	1	1	See Table 17	Values from 0 - 15 baud times

Table 17: Delay Bit Positions

Bit	Description
7:4	**Reserved**
3:0	**Delay**

GET / SET_FLOW_CTRL_THRESHOLD

Transfer Type: Control In / Out

Transfer Size: 3 bytes

The GET / SET_FLOW_CTRL_THRESHOLD report gets or sets flow control threshold used in hardware and software flow control. The default flow control threshold is 0x1C2 or 450 decimal. For hardware flow control RTS or DTR will be deasserted (high) when the receive FIFO exceeds the flow control threshold and asserted low at or below the threshold. For software flow control the XOFF character is pushed into the transmit FIFO and transmitted to the remote UART above the threshold and the XON character is transmitted at the threshold setting.

Field	Offset	Size	Value	Description
Report ID	0	1	0x58	Get / Set auto RS-485 half-duplex enable delay

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Field	Offset	Size	Value	Description
Threshold MSB	1	1	See Table 18	Values from 0 - 511
Threshold LSB	2	1		

Table 18: Flow Control Threshold Bit Positions

Bit	Description
15:9	**Reserved**
8	**Threshold MSB**
7:0	**Threshold LSB**

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GET / SET_USB_CONFIG

Transfer Type: Control In / Out

Transfer Size: 11 bytes

The GET / SET_USB_CONFIG report gets or sets USB configuration data, including VID, PID, max power, attributes, device release number, as well as a UART FIFO flush control. Set permanently programs on-chip OTP. Six fields defined in the mask may be individually programmed. Once a field is programmed, any attempt to program that field again will be ignored.

Field	Offset	Size	Value	Description
Report ID	0	1	0x60	Get / Set Flow USB Configuration data
VID LSB	1	1	VID	USB Vendor ID Vendor ID obtained from USB.org. The default VID is Exar's assigned VID: 0x04E2.
VID MSB	2	1		
PID LSB	3	1	PID	USB Product ID Product ID specified by vendor. The default PID is Exar's assigned PID: 0x1421.
PID MSB	4	1		
MAXPOWER	5	1	bMaxPower	USB device bMaxPower in 2 mA units Must be less than or equal to 100 mA (0x32) for a low power device and 500 mA (0xFA) for a high power device. The default MAXPOWER is 0x32.
ATTRIBUTES	6	1	See Table 19	USB bmAttributes
REL_MAJOR	7	1		
REL_MINOR	8	1		
AUTO_FLUSH	9	1	See Table 20	
MASK	10	1	See Table 21	

Table 19: Attributes Bit Positions

Bit	Description
7:4	**Reserved**
3	**REM_WAKE_EN** 0: No remote wakeup support (Default) 1: Remote wakeup supported
2	**REM_WAKE_VALID** 0: REM_WAKE_EN bit not valid (Default) 1: REM_WAKE_EN bit valid
1:0	**POWER_MODE** 00: Bus Powered (Default) 01: Self Powered 10: Self Powered 11: Reserved

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Table 20: Auto Flush Bit Positions

Bit	Description
7:4	**Reserved**
3	**RX_CLOSE** 0: Do not automatically flush buffers on UART enable/disable condition. (Default) 1: Automatically flush buffers on UART enable/disable condition.
2	**RX_OPEN** 0: Do not automatically flush buffers on UART enable/disable condition. 1: Automatically flush buffers on UART enable/disable condition. (Default)
1	**TX_CLOSE** 0: Do not automatically flush buffers on UART enable/disable condition. (Default) 1: Automatically flush buffers on UART enable/disable condition.
0	**TX_OPEN** 0: Do not automatically flush buffers on UART enable/disable condition. 1: Automatically flush buffers on UART enable/disable condition. (Default)

Table 21: Mask Bit Positions

Bit	Description
7:6	**Reserved**
5	**AUTO_FLUSH**
4	**REL**
3	**POWER_MODE**
2	**ATTRIBUTES**
1	**PID**
0	**VID**

To program any of the fields, the corresponding mask bit must be set to a '1'. (Write only, will read back '0'.)

GET / SET_VENDOR_STRING1

Transfer Type: Control In / Out

Transfer Size: 64 bytes

The GET / SET_VENDOR_STRGIN report gets or sets up to 61 bytes (30 1/2 unicode characters) of vendor string.

Field	Offset	Size	Value	Description
Report ID	0	1	0x61	Get / Set Vendor string 1
LENGTH	1	1		String Length + 2 bytes

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Field	Offset	Size	Value	Description
DESC_TYPE	2	1	0x03	Descriptor type
STRING	3	61		61 ASCII / 30 1/2 Unicode Characters

GET / SET_VENDOR_STRING2

Transfer Type: Control In / Out

Transfer Size: 64 bytes

The GET / SET_VENDOR_STRING report gets or sets up to 63 bytes (31 1/2 unicode characters) of vendor string.

Field	Offset	Size	Value	Description
Report ID	0	1	0x62	Get / Set Product string 2
STRING	1	63		63 ASCII / 31 1/2 Unicode Characters

Vendor string 1 and string 2 combined may set a maximum of 124 ASCII or 62 Unicode UTF-16 characters.

GET / SET_PRODUCT_STRING1

Transfer Type: Control In / Out

Transfer Size: 4 - 64 bytes

The GET / SET_PRODUCT_STRING1 report gets or sets up to 61 bytes (30 1/2 unicode characters) of product string.

Field	Offset	Size	Value	Description
Report ID	0	1	0x63	Get / Set Product string 1
LENGTH	1	1		String Length + 2 bytes
DESC_TYPE	2	1	0x03	Descriptor type
STRING	3	61		61 ASCII / 30 1/2 Unicode Characters

GET / SET_PRODUCT_STRING2

Transfer Type: Control In / Out

Transfer Size: 2 - 64 bytes

The GET / SET_PRODUCT_STRING2 report gets or sets up to remaining 63 bytes (31 1/2 unicode characters) of product string.

Field	Offset	Size	Value	Description
Report ID	0	1	0x64	Get / Set Product string 2
STRING	1	63		63 ASCII / 31 1/2 Unicode Characters

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Product string 1 and string 2 combined may set a maximum of 124 ASCII or 62 Unicode UTF=16 characters.

GET / SET_SERIAL_STRING

Transfer Type: Control In / Out

Transfer Size: 4 - 64 bytes

The GET / SET_SERIAL_STRING report gets or sets a up to 61 bytes (30 1/2 unicode characters) of product string.

Field	Offset	Size	Value	Description
Report ID	0	1	0x65	Get / Set Product string 1
LENGTH	1	1		String Length + 2 bytes
DESC_TYPE	2	1	0x03	Descriptor type
STRING	3	61		61 ASCII / 30 1/2 Unicode Characters

GET / SET_PIN_CONFIG

Transfer Type: Control In / Out

Transfer Size: 20 bytes

The GET / SET_PIN_CONFIG report gets or sets Pin configurations, including selection of pin functionality, push-pull or open drain if pin is an output, pull-up and pull-down resistor controls, remote wakeup control, USB_STAT functionality selection, suspend configurations, and clock output duty cycle and frequency. The SET_PIN_CONFIG report may only be used once. All further attempts to use this report will be ignored by the device.

Field	Offset	Size	Value	Description
Report ID	0	1	0x66	Get / Set pin configurations
CLK	1	1	See Table 22	CLK pin configuration
RTS	2	1	See Table 23	RTS pin configuration
CTS	3	1	See Table 22	CTS pin configuration
RS485	4	1		RS485 pin configuration
TXT	5	1		TXT pin configuration
RXT	6	1		RXT pin configuration
CD	7	1	See Table 24	CD pin configuration
RI	8	1	See Table 25	RI pin configuration
DTR	9	1	See Table 23	DTR pin configuration
DSR	10	1	See Table 22	DSR pin configuration
UART_DATA	11	1	See Table 26	Rx / Tx pin configuration
USB_STAT1	12	1	See Table 27	USB_STAT1 pin configuration
USB_STAT2	13	1		USB_STAT2 pin configuration

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Field	Offset	Size	Value	Description
SUSPEND_STATE_MSB	14	1	See Table 28	GPIO State During Suspend (when USE_SUSPEND is set) 0: All GPIO pins asserted low in USB Suspend state 1: All GPIO pins asserted high in USB Suspend state
SUSPEND_STATE_LSB	15	1		
SUSPEND_MODE_MSB	16	1	See Table 29	GPIO Mode During Suspend (when USE_SUSPEND is set) 0: GPIO pin is Open Drain when is USB Suspend state 1: GPIO pin is Push-pull when is USB Suspend state
SUSPEND_MODE_LSB	17	1		
RS485_POL	18	1		Auto RS-485 half-duplex polarity Bit [0] 0: auto RS-485 half-duplex enable active low 1: auto RS-485 half-duplex enable active high Bits [7:1] Reserved
CLKOUT_DIV	19	1		Output clock frequency 8-bit value sets output clock frequency divider. Freq out = 24 MHz / 2 x CLKOUT_DIV. A value of 0 is undefined and not allowed.

Default configuration for each pin is shown in Table 30.

Table 22: CLK, CTS, RS485, TXT, RXT, DSR Pin Bit Positions

Bit	Description
7	**PULL_U** 0: disable pull-up resistor 1: enable pull-up resistor
6	**PULL_D** 0: disable pull-down resistor 1: enable pull-down resistor if pull-up is not enabled as well
5:2	**Reserved**
1:0	**CONFIG** 00: GPIO Input 01: GPIO Open drain output 10: GPIO Push-pull output 11: CLK, RS485, TXT, RXT functionality outputs, CTS, DSR functionality inputs If CTS or DSR functions are selected, RTS and DTR functions (respectively) must also be selected and DTR and RTS functions (respectively) must be configured as GPIOs.

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Table 23: RTS, DTR Pin Bit Positions

Bit	Description
7	**PULL_U** 0: disable pull-up resistor 1: enable pull-up resistor
6	**PULL_D** 0: disable pull-down resistor 1: enable pull-down resistor if pull-up is not enabled as well
5:3	**Reserved**
2:0	**CONFIG** 000: GPIO Input 001: GPIO Open drain output 010: GPIO Push-pull output 011: RTS, DTR Open drain output (default) 100: RTS, DTR Push-pull output 101 to 111: Reserved If RTS or DTR function is selected, CTS or DSR function (respectively) must also be selected and DSR and CTS function (respecively) must be configured as GPIOs.

Table 24: CD Pin Bit Positions

Bit	Description
7	**PULL_U** 0: disable pull-up resistor 1: enable pull-up resistor
6	**PULL_D** 0: disable pull-down resistor 1: enable pull-down resistor if pull-up is not enabled as well
5:2	**Reserved**
1:0	**CONFIG** 00: GPIO Input 01: GPIO Open drain output 10: GPIO Push-pull output 11: Reserved

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Table 25: RI Pin Bit Positions

Bit	Description
7	**PULL_U** 0: disable pull-up resistor 1: enable pull-up resistor
6	**PULL_D** 0: disable pull-down resistor 1: enable pull-down resistor if pull-up is not enabled as well
5	**RMTWK** 0: disable remote wakeup capability for RI pin 1: enable remote wakeup capability for RI pin. (Remote wakeup must be enabled in SET_USB_CONFIG [Attributes] report 0x60.)
4:2	**Reserved**
1:0	**CONFIG** 00: GPIO Input (default) 01: GPIO Open drain output 10: GPIO Push-pull output 11: RI input

Table 26: UART_DATA Pin Bit Positions

Bit	Description
7	**PULL_U** 0: disable Rx pull-up resistor 1: enable pull-up resistor
6	**PULL_D** 0: disable Rx pull-down resistor 1: enable pull-down resistor if pull-up is not enabled as well
5	**RMTWK** 0: disable remote wakeup capability for RX pin 1: enable remote wakeup capability for RX pin. (Remote wakeup must be enabled in SET_USB_CONFIG [Attributes] report 0x60.)
4:2	**Reserved**
1:0	**CONFIG** 00: Reserved 01: TX Open drain output 10: TX Push-pull output 11: Reserved

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Table 27: USB_STAT1 / USB_STAT2 Pin Configuration Bit Positions

Bit	Description
7:5	**Reserved**
4:2	**FXN** 000: USB_STAT1 asserted high, USB_STAT2 low during either suspend state or USB reset 001: SUSPEND: Asserted high when in USB suspend state 010: LOW_POWER: Asserted high when in USB suspend state or not yet configured 011: BUS_RST: Asserted high when USB bus reset is asserted 100: same as "000" 101: SUSPEND#: Asserted low when in USB suspend state 110: LOW_POWER#: Asserted low when in USB suspend state or not yet configured 111: BUS_RST#: Asserted low when USB bus reset is asserted
1:0	**CONFIG** 00: Reserved 01: USB_STAT1/2 Open drain output 10: USB_STAT1/2 Push-pull output 11: Reserved

Table 28: SUSPEND_STATE Bit Positions

Bit	GPIO/Pin	Pin Name
15:14		Reserved
13	9	GPIO9/DSR#
12	8	GPIO8/DTR#
11	7	GPIO7/RI#
10	6	GPIO6/CD#
9:8		Reserved
7	5	GPIO5/RXT
6	4	GPIO4/TXT
5:4		Reserved
3	3	GPIO3/RS485
2	2	GPIO2/CTS#
1	1	GPIO1/RTS#
0	0	GPIO0/CLK

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Table 29: SUSPEND_MODE Bit Positions

Bit	GPIO/Pin	Pin Name
15		USE_SUSPEND*
14		Reserved
13	9	GPIO9/DSR#
12	8	GPIO8/DTR#
11	7	GPIO7/RI#
10	6	GPIO6/CD#
9:8		Reserved
7	5	GPIO5/RXT
6	4	GPIO4/TXT
5:4		Reserved
3	3	GPIO3/RS485
2	2	GPIO2/CTS#
1	1	GPIO1/RTS#
0	0	GPIO0/CLK

* USE_SUSPEND is a control signal that controls the GPIO pins listed in Table 28 and Table 29 when the XR21B1421 device is suspended by the USB host. If USE_SUSPEND is cleared to '0', GPIO pins retain the same output states when the device is suspended as they had prior to suspend. When USE_SUSPEND is set to '1', GPIO pins are assigned behavior defined by the SUSPEND_STATE and SUSPEND_MODE fields of SET_PIN_CONFIG report, with the following exceptions: GPIO0/CLK when configured as an output clock will always be driven low, i.e the clock output will stop, and GPIO1/RTS#/ RS485 or GPIO3/RS485 when configured as a auto RS-485 half-duplex enable will always be deasserted.

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Table 30: Default Pin Configuration

Pin	Default Value	Default Configuration
RX		Rx Data Input (not configurable)
TX	0x02	Data P-P Output
GPIO0/CLK	0x00	GPIO Input
GPIO1/RTS#/RS485	0x03	RTS OD Output*
GPIO2/CTS#	0x03	CTS Input*
GPIO3/RS485	0x03	RS-485 half-duplex Ctrl PP
GPIO4/TXT	0x03	TX Toggle PP Output
GPIO5/RXT	0x03	RX Toggle PP Output
GPIO6/CD#	0x00	GPIO Input
GPIO7/RI#	0x00	GPIO Input
GPIO8/DTR#	0x02	GPIO PP Output
GPIO9/DSR#	0x02	GPIO PP Output
USB_STAT1	0xA	SUSPEND PP Output
USB_STAT2	0x1A	SUSPEND# PP Output

* Although GPOI1/RTS#/RS485 and GPIO2/CTS# have RTS# and CTS# functionality by default, H/W RTS/CTS flow control must be enabled before using this function.

GET / SET_LANGID

Transfer Type: Control In / Out

Transfer Size: 3 bytes

The GET / SET_LANGID report gets or sets unicode UTF-16 Language ID. Default Language ID code is 0x0409

Field	Offset	Size	Value	Description
Report ID	0	1	0x67	Get / Set Unicode Language ID
LANGID LSB	1	1	0x09	LSB of UTF-16LE Language ID code
LANGID MSB	2	1	0x04	MSB of UTF-16LE Language ID code

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GET / SET_GLOBAL_LOCK

Transfer Type: Control In / Out

Transfer Size: 2 bytes

The GET / SET_GLOBAL_LOCK report gets or sets unicode UTF-16 Language ID. Device must have either hardware or power on reset before the global lock takes effect.

Field	Offset	Size	Value	Description
Report ID	0	1	0x68	Get / Set Unicode Language ID
Global Lock	1	1	0x00	Set bit 0 to a '1' to set Global Lock

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Application Circuits

The GPIO inputs are 5V tolerant. However, when GPIO input voltage levels exceed VIO, an external clamp circuit is required to prevent VIO from increasing. Two examples of different application circuits are shown in Figure 7.

VIO Clamp Circuits

Figure 7: VIO Clamp Circuits

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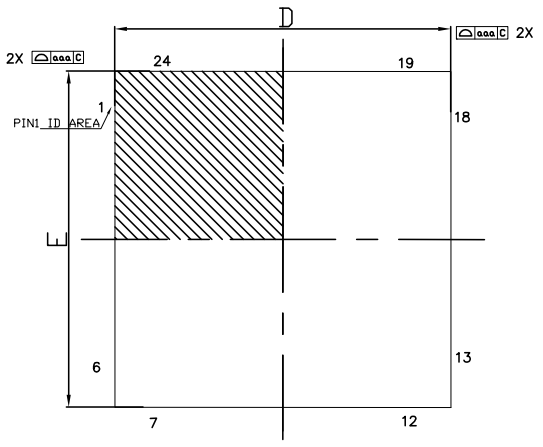
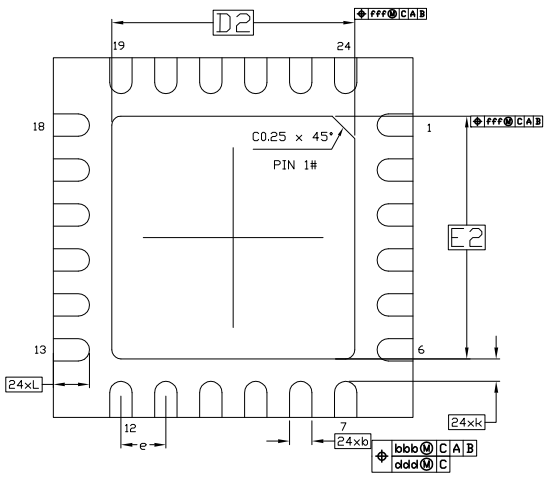
Mechanical Dimensions

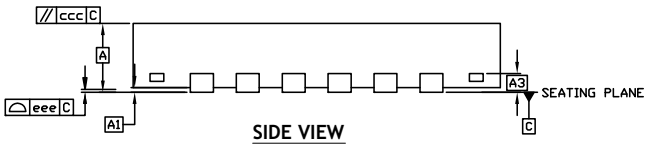
24-Pin QFN (Option 1)



TOP VIEW



BOTTOM VIEW



SIDE VIEW

DIM / SYMBOL	MIN	NOM	MAX
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
A3	---	0.20Ref	---
b	0.20	0.25	0.30
D		4.00 BSC	
E		4.00 BSC	
e		0.50 BSC	
D2	2.50	2.65	2.80
E2	2.50	2.65	2.80
L	0.35	0.40	0.45
K	0.20	–	–
aaa		0.15	
bbb		0.10	
ccc		0.10	
ddd		0.05	
eee		0.08	
fff		0.10	
N		24	

TERMINAL DETAILS

- ALL DIMENSIONS ARE IN MILLIMETERS, ANGLES AREA IN DEGREE.
- DIMENSIONS AND TOLERANCE PER JEDEC MO-220.

Drawing No.: POD-00000130

Revision: A

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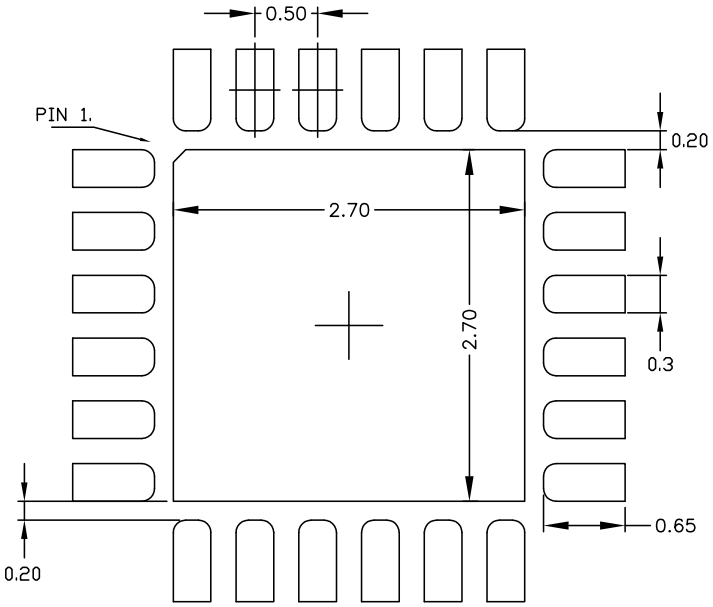
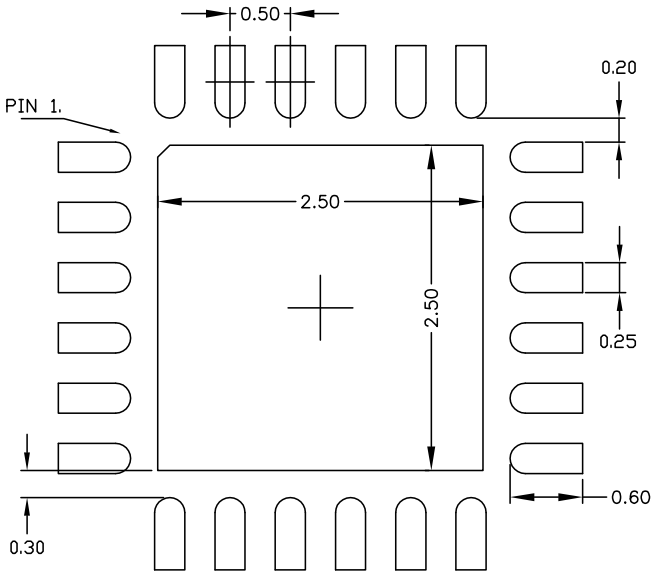
Recommended Land Pattern and Stencil Design

24-Pin QFN (Option 1)



TYPICAL RECOMMENDED LAND PATTERN



TYPICAL RECOMMENDED STENCIL

Drawing No.: POD-00000130

Revision: A

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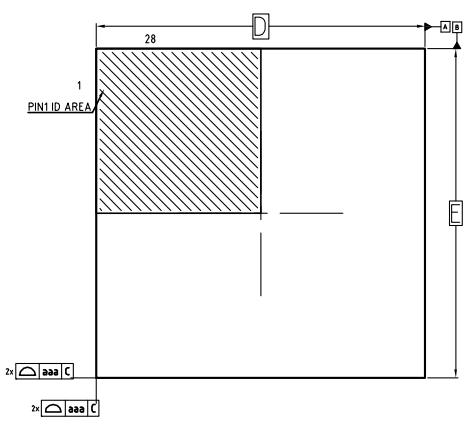
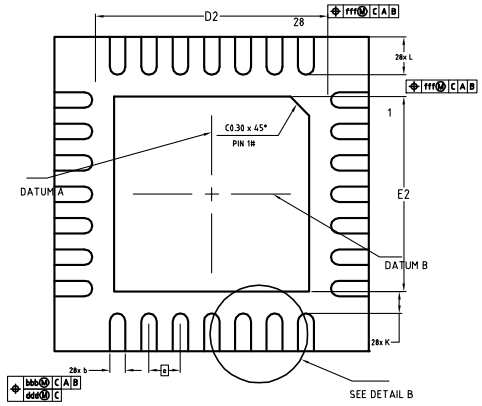
Mechanical Dimensions

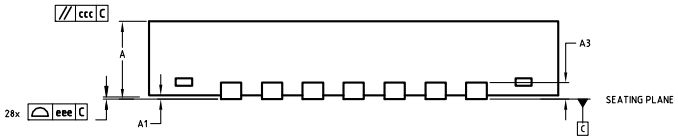
28-Pin QFN



TOP VIEW



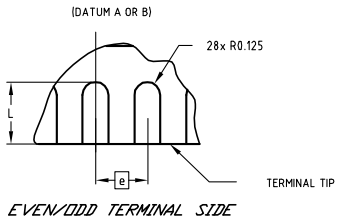
BOTTOM VIEW



SIDE VIEW

DIM / SYMBOL	MIN.	NOM.	MAX.
A	0.80	0.90	1.00
A1	0	0.02	0.05
A3	-	0.20 REF	-
b	0.20	0.25	0.30
D		5.00BSC	
E		5.00BSC	
D2	2.60	3.10	3.60
E2	2.60	3.10	3.60
e		0.50BSC	
L	0.55	0.60	0.65
K	0.20	-	-
aaa		0.15	
bbb		0.10	
ccc		0.10	
ddd		0.05	
eee		0.08	
fff		0.10	

TERMINAL DETAIL



DETAIL B

- ALL DIMENSIONS ARE IN MILLIMETERS, ANGLES AREA IN DEGREE.
- DIMENSIONS AND TOLERANCE PER JEDEC MO-220.

Drawing No.: POD-000000107

Revision: B

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Ordering Information[1]

Part Number	Operating Temperature Range	Lead-Free	Package	Packaging Method
XR21B1421IL24-F	-40°C to +85°C	Yes[2]	24-pin QFN	Tray
XR21B1421IL24TR-F[3]				Tape and Reel
XR21B1421IL28-F			28-pin QFN	Tray
XR21B1421IL28TR-F[3]				Tape and Reel
XR21B1421IL24-0A-EVB	24-pin QFN Evaluation Board for XR21B1421			
XR21B1421IL28-0A-EVB	28-pin QFN Evaluation Board for XR21B1421			

NOTE:

1. Refer to www.exar.com/XR21B1421 for most up-to-date Ordering Information.
2. Visit www.exar.com for additional information on Environmental Rating.
3. NRND - Not recommended for new designs.

Revision History

Revision	Date	Description
1A	April 2014	Initial release
1B	October 2014	Removed “contact factory” notice for 28 QFN package [ECN1442-07 I 10/14/2014]
1C	November 2017	Update package drawing per PCN # 17-0310-02. Corrected GET/SET_PIN_CONFIG offset 19 CLKOUT_DIV frequency and clarified value, clarified offset 18 RS485_POL bits. Corrected GET / SET_GLOBAL_LOCK Global Lock offset. Update to MaxLinear logo. Updated format and ordering information table.

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