8-BIT MICROCONTROLLER

Table of Contents-

1. GENERAL DESCRIPTION

The W78L365A is an 8-bit microcontroller which has an in-system programmable Flash EPROM for firmware updating. The instruction set of the W78L365A is fully compatible with the standard 8052. The W78L365A contains a 64K bytes of main ROM and a 4K bytes of auxiliary ROM which allows the contents of the 64KB main ROM to be updated by the loader program located at the 4KB auxiliary ROM; 256+1K bytes of on-chip RAM; four 8-bit bi-directional and bit-addressable I/O ports; an additional 4-bit port P4; three 16-bit timer/counters; a serial port. These peripherals are supported by a eight sources two-level interrupt capability. To facilitate programming and verification, the ROM inside the W78L365A allows the program memory to be programmed and read electronically. Once the code is confirmed, the user can protect the code for security.

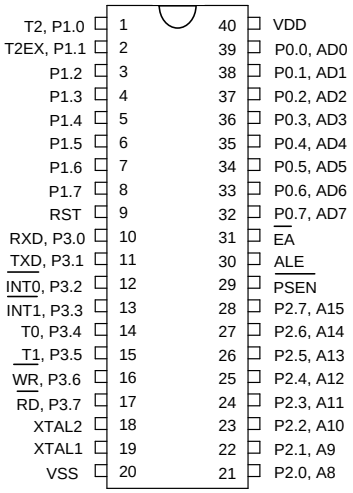
The W78L365A microcontroller has two power reduction modes, idle mode and power-down mode, both of which are software selectable. The idle mode turns off the processor clock but allows for continued peripheral operation. The power-down mode stops the crystal oscillator for minimum power consumption. The external clock can be stopped at any time and in any state without affecting the processor.

2. FEATURES

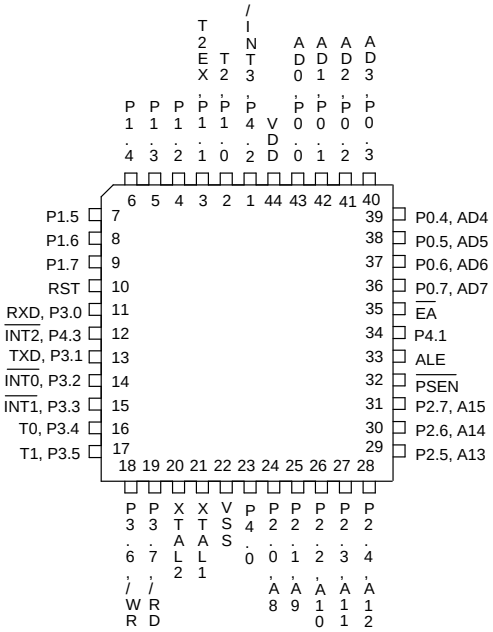
- Fully static design 8-bit CMOS microcontroller
- 64K bytes of in-system programmable Flash EPROM for Application Program (APROM)
- 4K bytes of auxiliary ROM for Loader Program (LDROM)
- 256+1K bytes of on-chip RAM. (Including 1K bytes of AUX-RAM, software selectable)
- Four 8-bit bi-directional ports
- One 4-bit multipurpose programmable port (I/O, interrupt, Chip select function)
- Three 16-bit timer/counters
- One full duplex serial port
- Watchdog timer
- Software Reset
- P1.0 T2 programmable clock out
- Eight-sources, two-level interrupt capability
- Up to 20 MHz
- Built-in power management
- Code protection
- Packaged in
  - Lead Free (RoHS) DIP 40: W78L365A24DL
  - Lead Free (RoHS) PLCC 44: W78L365A24PL
  - Lead Free (RoHS) QFP 44: W78L365A24FL
  - Lead Free (RoHS) LQFP 48: W78L365A24LL

3. PIN CONFIGURATIONS

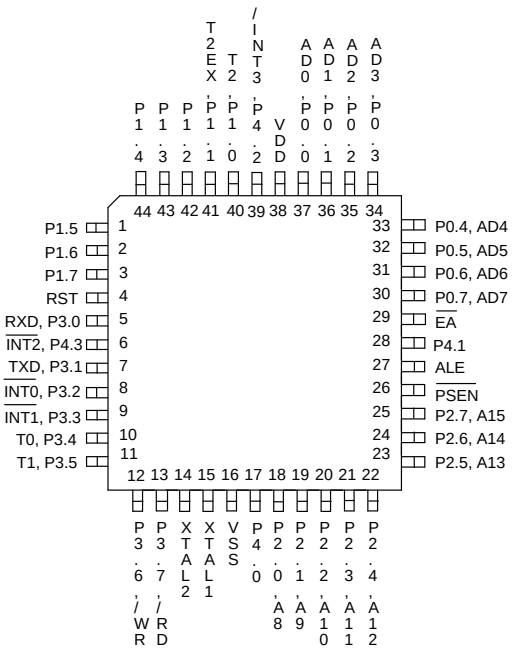
40-pin DIP



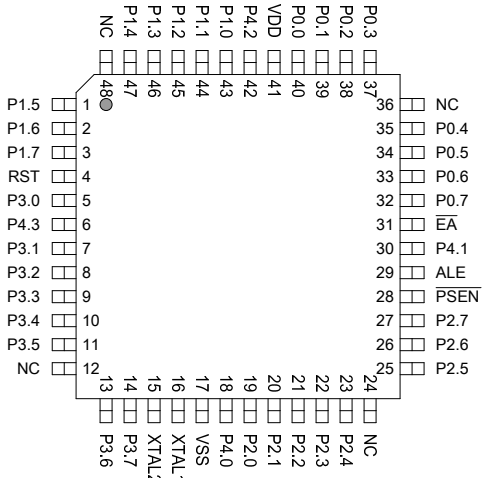
44-pin PLCC



44-pin PQFP



48-pin LQFP



4. PIN DESCRIPTION

SYMBOL	TYPE	DESCRIPTIONS
$\overline{EA}$	I	EXTERNAL ACCESS ENABLE: This pin forces the processor to execute the external ROM. The ROM address and data will not be presented on the bus if the $\overline{EA}$ pin is high.
$\overline{PSEN}$	O H	PROGRAM STORE ENABLE: $\overline{PSEN}$ enables the external ROM data in the Port 0 address/data bus. When internal ROM access is performed, no $\overline{PSEN}$ strobe signal outputs originate from this pin.
ALE	O H	ADDRESS LATCH ENABLE: ALE is used to enable the address latch that separates the address from the data on Port 0. ALE runs at 1/6th of the oscillator frequency.
RST	I L	RESET: A high on this pin for two machine cycles while the oscillator is running resets the device.
XTAL1	I	CRYSTAL 1: This is the crystal oscillator input. This pin may be driven by an external clock.
XTAL2	O	CRYSTAL 2: This is the crystal oscillator output. It is the inversion of XTAL1.
V_{SS}	I	GROUND: ground potential.
V_{DD}	I	POWER SUPPLY: Supply voltage for operation.
P0.0–P0.7	I/O D	PORT 0: Function is the same as that of standard 8052.
P1.0–P1.7	I/O H	PORT 1: Function is the same as that of standard 8052.
P2.0–P2.7	I/O H	PORT 2: Port 2 is a bi-directional I/O port with internal pull-ups. This port also provides the upper address bits for accesses to external memory. The P2.6 and P2.7 also provide the alternate function $\overline{REBOOT}$ which is H/W reboot from LD flash.
P3.0–P3.7	I/O H	PORT 3: Function is the same as that of the standard 8052.
P4.0–P4.7	I/O H	PORT 4: A bi-directional I/O. The P4.3 also provide the alternate function $\overline{REBOOT}$ which is H/W reboot from LD flash.

*** Note: TYPE** I: input, O: output, I/O: bi-directional, H: pull-high, L: pull-low, D: open drain

5. FUNCTIONAL DESCRIPTION

The W78L365A architecture consists of a core controller surrounded by various registers, four general purpose I/O ports, one special purpose programmable 4-bits I/O port, 256+1K bytes of RAM, three timer/counters, a serial port. The processor supports 111 different opcodes and references both a 64K program address space and a 64K data storage space.

5.1 RAM

The internal data RAM in the W78L365A is 256+1K bytes. It is divided into two banks: 256 bytes of scratchpad RAM and 1K bytes of AUX-RAM. These RAMs are addressed by different ways.

- RAM 0H–7FH can be addressed directly and indirectly as the same as in 8051. Address pointers are R0 and R1 of the selected register bank.
- RAM 80H–FFH can only be addressed indirectly as the same as in 8051. Address pointers are R0, R1 of the selected registers bank.
- AUX-RAM 0H–3FFH is addressed indirectly as the same way to access external data memory with the MOVX instruction. Address pointer are R0 and R1 of the selected register bank and DPTR register. An access to external data memory locations higher than 3FFH will be performed with the MOVX instruction in the same way as in the 8051. The AUX-RAM is **enabled** after a reset. Clearing the bit 4 in CHPCON register will disable the access to AUX-RAM. When executing from internal program memory, an access to AUX-RAM will not affect the Ports P0, P2, $\overline{WR}$ and $\overline{RD}$.

Example:

```
CHPENR    REG     F6H
CHPCON    REG     BFH
XRAMAH    REG     A1H

MOV     CHPENR, #87H
MOV     CHPENR, #59H
ORL     CHPCON, #00010000B  ; enable AUX-RAM
MOV     CHPENR, #00H
MOV     XRAMAH, #01H        ; internal high address
MOV     R0, #23H
MOV     A, #55H
MOVX    @R0, A              ; Write 55h data to 0123h AUX-RAM address.
MOV     XRAMAH, #02H
MOV     R1, #FFH            ; Read data from 02FFh AUX-RAM address.
MOVX    A, @R1
MOV     DPTR, #0134H
MOV     A, #78H
MOVX    @DPTR,A             ; Write 78h data to 0134h AUX-RAM address.
MOV     DPTR, #7FFFH
MOVX    A, @DPRT            ; Read data from the external  7FFFh address SRAM
```

5.2 Timers 0, 1 and 2

Timers 0, 1, and 2 each consist of two 8-bit data registers. These are called TL0 and TH0 for Timer 0, TL1 and TH1 for Timer 1, and TL2 and TH2 for Timer 2. The TCON and TMOD registers provide control functions for timers 0, 1. The T2CON register provides control functions for Timer 2. RCAP2H and RCAP2L are used as reload/capture registers for Timer 2. The operations of Timer 0 and Timer 1 are the same as in the W78C51. Timer 2 is a 16-bit timer/counter that is configured and controlled by the T2CON register. Like Timers 0 and 1, Timer 2 can operate as either an external event counter or as an internal timer, depending on the setting of bit C/T2 in T2CON. Timer 2 has three operating modes: capture, auto-reload, and baud rate generator. The clock speed at capture or auto-reload mode is the same as that of Timers 0 and 1.

5.2.1 Timer 2 Output

If set T2OE (T2MOD.1) bit and clear C/T2 (T2CON.1) bit at auto-reload mode, P1.0 will be toggled once overflow.

TIMER 2 Mode

Bit:	7	6	5	4	3	2	1	0
							T2OE	

Mnemonic: T2MOD Address: C9H

T2OE: Enable this bit to toggle P1.0 pin while Timer2 has been overflowed.

5.3 Clock

The W78L365A is designed with either a crystal oscillator or an external clock. Internally, the clock is divided by two before it is used by default. This makes the W78L365A relatively insensitive to duty cycle variations in the clock.

5.3.1 Crystal Oscillator

The W78L365A incorporates a built-in crystal oscillator. To make the oscillator work, a crystal must be connected across pins XTAL1 and XTAL2. In addition, a load capacitor must be connected from each pin to ground.

5.3.2 External Clock

An external clock should be connected to pin XTAL1. Pin XTAL2 should be left unconnected. The XTAL1 input is a CMOS-type input, as required by the crystal oscillator.

5.4 Power Management

5.4.1 Idle Mode

Setting the IDL bit in the PCON register enters the idle mode. In the idle mode, the internal clock to the processor is stopped. The peripherals and the interrupt logic continue to be clocked. The processor will exit idle mode when either an interrupt or a reset occurs.

5.4.2 Power-down Mode

When the PD bit in the PCON register is set, the processor enters the power-down mode. In this mode all of the clocks are stopped, including the oscillator. To exit from power-down mode is by a hardware reset or external interrupts $\overline{INT0}$ to $\overline{INT1}$ when enabled and set to level triggered.

5.4.3 Reduce EMI Emission

The W78L365A allows user to diminish the gain of on-chip oscillator amplifier by using programmer to clear the B7 bit of security register. Once B7 is set to 0, a half of gain will be decreased. Care must be taken if user attempts to diminish the gain of oscillator amplifier, reducing a half of gain may affect the external crystal operating improperly at high frequency. The value of C1 and C2 may need some adjustment while running at lower gain.

ALE OFF Function

Auxiliary Register

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	ALEOFF

Mnemonic: AUXR Address: 8EH

ALEOFF : Set this bit to disable ALE output.

5.5 Reset

The external RESET signal is sampled at S5P2. To take effect, it must be held high for at least two machine cycles while the oscillator is running. An internal trigger circuit in the reset line is used to deglitch the reset line when the W78L365A is used with an external RC network. The reset logic also has a special glitch removal circuit that ignores glitches on the reset line. During reset, the ports are initialized to FFH, the stack pointer to 07H, PCON (with the exception of bit 4) to 00H, and all of the other SFR registers except SBUF to 00H. SBUF is not reset.

5.5.1 W78L365A Special Function Registers (SFRs) and Reset Values

F8								
F0	+B 00000000						CHPENR 00000000	
E8								
E0	+ACC 00000000							
D8	+P4 11111111	PWMP 00000000	PWM0 00000000	PWM1 00000000	PWMCON1 00000000	PWM2 00000000	PWM3 00000000	
D0	+PSW 00000000							
C8	+T2CON 00000000	T2MOD 00000000	RCAP2L 00000000	RCAP2H 00000000	TL2 00000000	TH2 00000000	PWMCON2 00000000	PWM4 00000000
C0	+XICON 00000000		P4CONA 00000000	P4CONB 00000000	SFRAL 00000000	SFRAH 00000000	SFRFD 00000000	SFRCN 00000000
B8	+IP 00000000							CHPCON 00x11000
B0	+P3 11111111				P43AL 00000000	P43AH 00000000		
A8	+IE 00000000				P42AL 00000000	P42AH 00000000	P4CSIN 00000000	
A0	+P2 11111111	XRAMAH 00000000						
98	+SCON 00000000	SBUF xxxxxxxx						
90	+P1 11111111				P41AL 00000000	P41AH 00000000		
88	+TCON 00000000	TMOD 00000000	TL0 00000000	TL1 00000000	TH0 00000000	TH1 00000000	AUXR 00000000	WDTC 00000000
80	+P0 11111111	SP 00000111	DPL 00000000	DPH 00000000	P40AL 00000000	P40AH 00000000	POR 00000000	PCON 00110000

Notes:

1. The SFRs marked with a plus sign(+) are both byte- and bit-addressable.
2. The text of SFR with bold type characters are extension function registers.

5.6 Port 4

Port 4, address D8H, is a 8-bit multipurpose programmable I/O port. Each bit can be configured individually by software. The Port 4 has four different operation modes.

Mode 0: P4.0–P4.3 is a bi-directional I/O port which is same as port 1. P4.2 and P4.3 also serve as external interrupt $\overline{PSEN}$ and $\overline{INT2}$ if enabled.

Mode 1: P4.0–P4.3 are read strobe signals that are synchronized with $\overline{RD}$ signal at specified addresses. These signals can be used as chip-select signals for external peripherals.

Mode 2: P4.0–P4.3 are write strobe signals that are synchronized with $\overline{WR}$ signal at specified addresses. These signals can be used as chip-select signals for external peripherals.

Mode 3: P4.0–P4.3 are read/write strobe signals that are synchronized with $\overline{RD}$ or $\overline{WR}$ signal at specified addresses. These signals can be used as chip-select signals for external peripherals.

When Port 4 is configured with the feature of chip-select signals, the chip-select signal address range depends on the contents of the SFR P4xAH, P4xAL, P4CONA and P4CONB. The registers P4xAH and P4xAL contain the 16-bit base address of P4.x. The registers P4CONA and P4CONB contain the control bits to configure the Port 4 operation mode.

The high nibble of port4(P4.4 to P4.7) can be selected to serve to the direct LED display drive outputs by setting the HDx bit is set, the corresponding pin p4.x can sink about 20 mA current for driving LED display directly.

5.6.1 Port Options Register

Bit:	7	6	5	4	3	2	1	0
	-	-	-	HD47	HD46	HD45	HD44	P0UP

Mnemonic: POR Address: 86H

HD47-44: Enable pins P4.4 to P4.7 individually with high drive outputs.

P0UP: Enable Port 0 weak up. The pins of Port 0 can be configured with either the open drain or standart port with internal pull-up. By the default, Port 0 is an open drain bi-directional I/O port. When the P0UP bit in the POR register is set, the pins of port 0 will perform a bi-directional I/O port with internal pull-up that is structurally the same Port2.

5.6.2 $\overline{INT2}$ / $\overline{INT3}$

Two additional external interrupts, $\overline{INT2}$ and $\overline{INT3}$, whose functions are similar to those of external interrupt 0 and 1 in the standard 80C52. The functions/status of these interrupts are determined/shown by the bits in the XICON (External Interrupt Control) register. The XICON register is bit-addressable but is not a standard register in the standard 80C52. Its address is at 0C0H. To set/clear bits in the XICON register, one can use the "SETB ($\overline{CLR}$) bit" instruction. For example, "SETB 0C2H" sets the EX2 bit of XICON.

XICON - external interrupt control (C0H)

PX3	EX3	IE3	IT3	PX2	EX2	IE2	IT2

PX3: External interrupt 3 priority high if set

EX3: External interrupt 3 enable if set

IE3: If IT3 = 1, IE3 is set/cleared automatically by hardware when interrupt is detected/serviced

IT3: External interrupt 3 is falling-edge/low-level triggered when this bit is set/cleared by software

PX2: External interrupt 2 priority high if set

EX2: External interrupt 2 enable if set

IE2: If IT2 = 1, IE2 is set/cleared automatically by hardware when interrupt is detected/serviced

IT2: External interrupt 2 is falling-edge/low-level triggered when this bit is set/cleared by software

Eight-source interrupt information:

INTERRUPT SOURCE	VECTOR ADDRESS	POLLING SEQUENCE WITHIN PRIORITY LEVEL	ENABLE REQUIRED SETTINGS	INTERRUPT TYPE EDGE/LEVEL
External Interrupt 0	03H	0 (highest)	IE.0	TCON.0
Timer/Counter 0	0BH	1	IE.1	-
External Interrupt 1	13H	2	IE.2	TCON.2
Timer/Counter 1	1BH	3	IE.3	-
Serial Port	23H	4	IE.4	-
Timer/Counter 2	2BH	5	IE.5	-
External Interrupt 2	33H	6	XICON.2	XICON.0
External Interrupt 3	3BH	7 (lowest)	XICON.6	XICON.3

P4CONB (C3H)

BIT	NAME	FUNCTION
7, 6	P43FUN1 P43FUN0	00: Mode 0. P4.3 is a general purpose I/O port which is the same as Port1. 01: Mode 1. P4.3 is a Read Strobe signal for chip select purpose. The address range depends on the SFR P43AH, P43AL, P43CMP1 and P43CMP0. 10: Mode 2. P4.3 is a Write Strobe signal for chip select purpose. The address range depends on the SFR P43AH, P43AL, P43CMP1 and P43CMP0. 11: Mode 3. P4.3 is a Read/Write Strobe signal for chip select purpose. The address range depends on the SFR P43AH, P43AL, P43CMP1, and P43CMP0.

P4CONB (C3H), continued

BIT	NAME	FUNCTION
5, 4	P43CMP1 P43CMP0	Chip-select signals address comparison: 00: Compare the full address (16 bits length) with the base address register P43AH, P43AL. 01: Compare the 15 high bits (A15–A1) of address bus with the base address register P43AH, P43AL. 10: Compare the 14 high bits (A15–A2) of address bus with the base address register P43AH, P43AL. 11: Compare the 8 high bits (A15–A8) of address bus with the base address register P43AH, P43AL.
3, 2	P42FUN1 P42FUN0	The P4.2 function control bits which are the similar definition as P43FUN1, P43FUN0.
1, 0	P42CMP1 P42CMP0	The P4.2 address comparator length control bits which are the similar definition as P43CMP1, P43CMP0.

P4CONA (C2H)

BIT	NAME	FUNCTION
7, 6	P41FUN1 P41FUN0	The P4.1 function control bits which are the similar definition as P43FUN1, P43FUN0.
5, 4	P41CMP1 P41CMP0	The P4.1 address comparator length control bits which are the similar definition as P43CMP1, P43CMP0.
3, 2	P40FUN1 P40FUN0	The P4.0 function control bits which are the similar definition as P43FUN1, P43FUN0.
1, 0	P40CMP1 P40CMP0	The P4.0 address comparator length control bits which are the similar definition as P43CMP1, P43CMP0.

P4CSIN (AEH)

BIT	NAME	FUNCTION
7	P43CSINV	The active polarity of P4.3 when pin P4.3 is defined as read and/or write strobe signal. = 1: P4.3 is active high when pin P4.3 is defined as read and/or write strobe signal. = 0: P4.3 is active low when pin P4.3 is defined as read and/or write strobe signal.
6	P42CSINV	The similarity definition as P43SINV.
5	P41CSINV	The similarity definition as P43SINV.
4	P40CSINV	The similarity definition as P43SINV.
3	-	Reserve
2	-	Reserve
1	-	0
0	-	0

5.6.3 Port 4 Base Address Registers

P40AH, P40AL:

The Base address register for comparator of P4.0. P40AH contains the high-order byte of address, P40AL contains the low-order byte of address.

P41AH, P41AL:

The Base address register for comparator of P4.1. P41AH contains the high-order byte of address, P41AL contains the low-order byte of address.

P42AH, P42AL:

The Base address register for comparator of P4.2. P42AH contains the high-order byte of address, P42AL contains the low-order byte of address.

P43AH, P43AL:

The Base address register for comparator of P4.3. P43AH contains the high-order byte of address, P43AL contains the low-order byte of address.

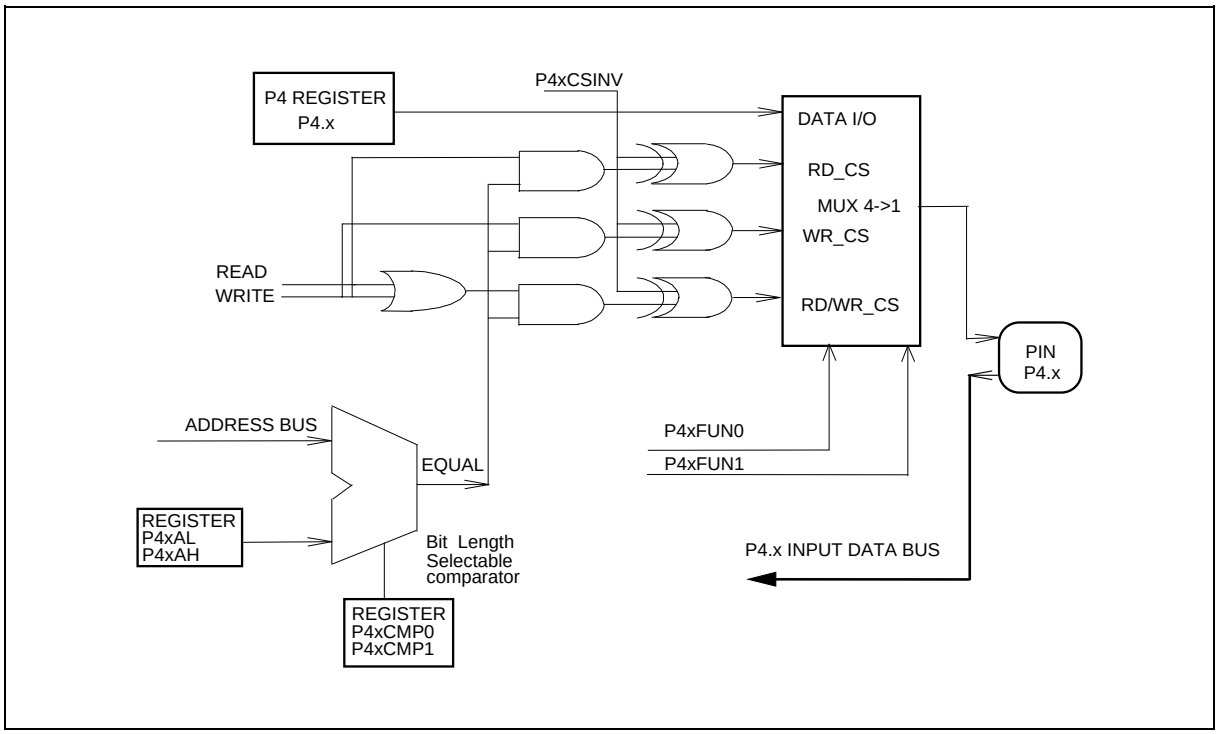
P4 (D8H)

BIT	NAME	FUNCTION
7	P47	I/O pin
6	P46	I/O pin.
5	P45	I/O pin.
4	P44	I/O pin.
3	P43	Port 4 Data bit which outputs to pin P4.3 at mode 0.
2	P42	Port 4 Data bit. which outputs to pin P4.2 at mode 0.
1	P41	Port 4 Data bit. which outputs to pin P4.1at mode 0.
0	P40	Port 4 Data bit which outputs to pin P4.0 at mode 0.

Here is an example to program the P4.0 as a write strobe signal at the I/O port address 1234H–1237H and positive polarity, and P4.1–P4.3 are used as general I/O ports. P4.4–P4.7 is only available for 48 pin package.

```
MOV  P40AH, #12H
MOV  P40AL, #34H          ; Base I/O address 1234H for P4.0
MOV  P4CONA, #00001010B   ; P4.0 a write strobe signal and address line A0 and A1 are masked.
MOV  P4CONB, #00H         ; P4.1–P4.3 as general I/O port which are the same as PORT1
MOV  P2ECON, #10H         ; Write the P40SINV = 1 to inverse the P4.0 write strobe polarity
                          ; default is negative.
```

Then any instruction MOVX @DPTR, A (with DPTR = 1234H–1237H) will generate the positive polarity write strobe signal at pin P4.0. And the instruction MOV P4, #XX will output the bit3 to bit1 of data #XX to pin P4.3–P4.1.



5.7 Pulse Width Modulated Outputs (PWM)

There are five pulse width modulated output channels to generate pulses of programmable length and interval. The repetition frequency is defined by an 8-bit prescaler PWMP, which supplies the clock for the counter. The prescaler and counter are common to both PWM channels. The 8-bit counter counts modular 255 (0–254). The value of the 8-bit counter compared to the contents of five registers: PWM0, PWM1, PWM2, PWM3 and PWM4. Provided the contents of either these registers is greater than the counter value, the corresponding PWM0, PWM1, PWM2, PWM3 or PWM4 output is set HIGH. If the contents of these registers are equal to, or less than the counter value, the output will be LOW. The pulse-width-ratio is defined by the contents of the registers PWM0, PWM1, PWM2, PWM3 and PWM4. The pulse-width-ratio is in the range of 0 to 1 and may be programmed in increments of 1/255. ENPWM0, ENPWM1, ENPWM2, ENPWM3 and ENPWM4 bit will enable or disable PWM output.

Buffered PWM outputs may be used to drive DC motors. The rotation speed of the motor would be proportional to the contents of PWM0/1/2/3/4. The repetition frequency f_{pwm}, at the PWM0/1/2/3/4 output is given by:

$$f_{pwm} = \frac{f_{osc}}{2 \times (1 + PWMP) \times 255}$$

Prescaler division factor = PWM + 1

PWMn high/low ratio of $\mathrm{PWMn} = \dfrac{(\mathrm{PWMn})}{255 - (\mathrm{PWMn})}$

This gives a repetition frequency range of 123 Hz to 31.4 KHz (f_{osc} = 16 MHz). By loading the PWM

registers with either 00H or FFH, the PWM channels will output a constant HIGH or LOW level, respectively. Since the 8-bit counter counts modulo 255, it can never actually reach the value of the PWM registers when they are loaded with FFH.

When a compare register (PWM0, PWM1, PWM2, PWM3, PWM4) is loaded with a new value, the associated output updated immediately. It does not have to wait until the end of the current counter period. There is weakly pulled high on PWM output.

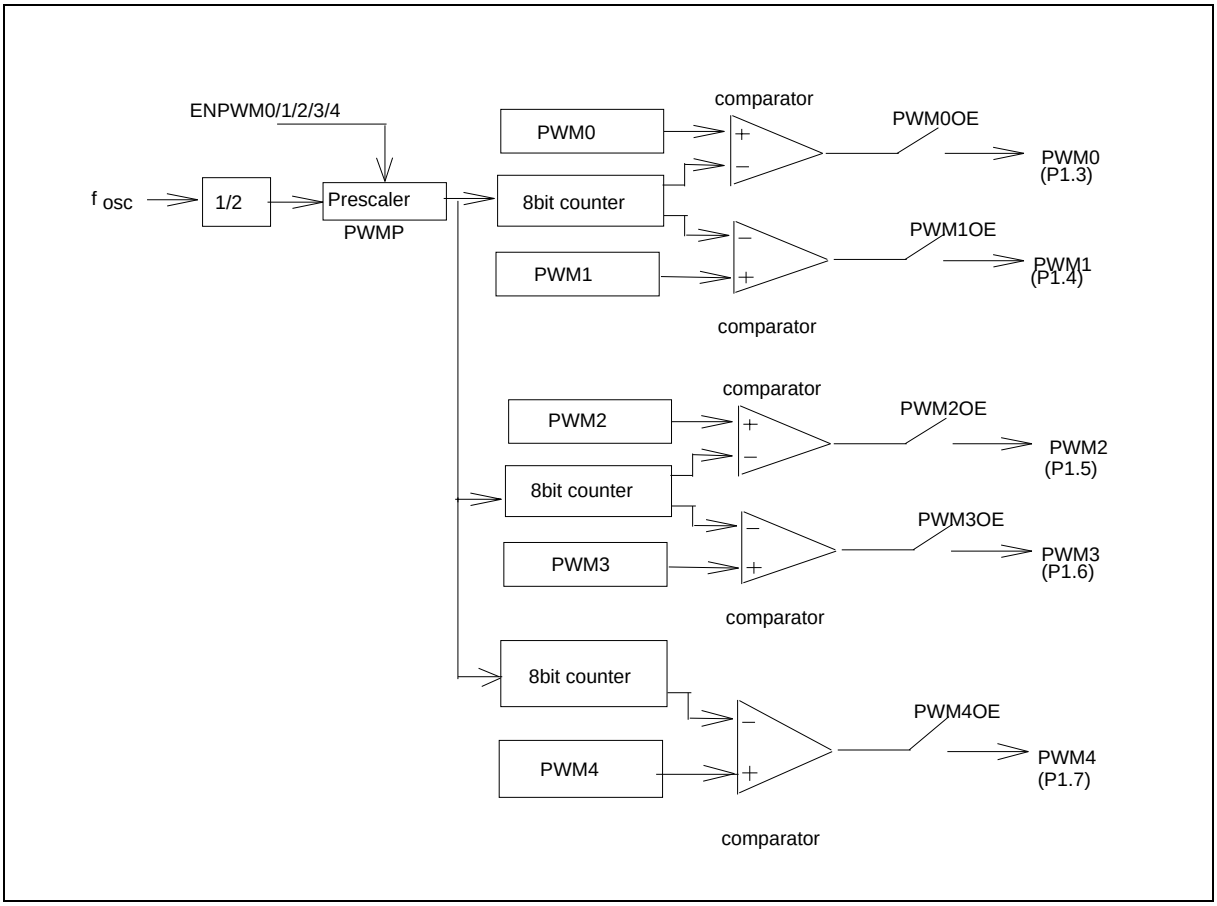


FIGURE 1 PWM DIAGRAM

Please refer as below code.

```
mov   pwmcon1, #00110011b    ; enable pwm3, 2, 1, 0
mov   pwmcon2, #00000101b    ; enable pwm4
mov   pwmp, #40h             ; Fpwm = XT/(2*(1+pwmp)*255)
jb    p1.3, $
mov   pwm0, #14h             ; duty cycle high/low = pwm0/(255-pmw0)
jb    p1.4, $
mov   pwm1, #18h
jb    p1.5, $
```

```
mov    pwm2, #20h
jb     p1.6, $
mov    pwm3, #b0h
jb     p1.7, $
mov    pwm4, #40h
mov    pwmcon1, #11111111b    ;output enable pwm3, 2, 1, 0
```

PWM3 Register

Bit:	7	6	5	4	3	2	1	0

Mnemonic: PWM3 Address: DEH

PWM2 Register

Bit:	7	6	5	4	3	2	1	0

Mnemonic: PWM2 Address: DDH

PWM Control 1 Register

Bit:	7	6	5	4	3	2	1	0
	PWM3OE	PWM2OE	ENPWM3	ENPWM2	PWM1OE	PWM0OE	ENPWM1	ENWPM0

Mnemonic: PWMCON1 Address: DCH

PWM3OE: Output enable for PWM3

PWM2OE: Output enable for PWM2

ENPWM3: Enable PWM3

ENPWM2: Enable PWM2

PWM1OE: Output enable for PWM1

PWM0OE: Output enable for PWM0

ENPWM1: Enable PWM1

ENPWM0: Enable PWM0

PWM1 Register

Bit:	7	6	5	4	3	2	1	0

Mnemonic: PWM1 Address: DBH

PWM0 Register

Bit:	7	6	5	4	3	2	1	0

Mnemonic: PWM0 Address: DAH

PWMP Register

Bit:	7	6	5	4	3	2	1	0

Mnemonic: PWMP Address: D9H

PWM4 Register

Bit:	7	6	5	4	3	2	1	0

Mnemonic: PWM4 Address: CFH

PWM Control 2 Register

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	PWM4OE	-	ENWPM4

Mnemonic: PWMCON2 Address: CEH

PWM4OE: Output enable for PWM4

ENPWM: Enable for PWM4

5.8 Watchdog Timer

The Watchdog timer is a free-running timer which can be programmed by the user to serve as a system monitor, a time-base generator or an event timer. It is basically a set of dividers that divide the system clock. The divider output is selectable and determines the time-out interval. When the time-out occurs, a system reset can also be caused if it is enabled. The main use of the Watchdog timer is as a system monitor. This is important in real-time control applications. In case of power glitches or electro-magnetic interference, the processor may begin to execute errant code. If this is left unchecked the entire system may crash. The watchdog time-out selection will result in different time-out values depending on the clock speed. The Watchdog timer will de disabled on reset. In general, software should restart the Watchdog timer to put it into a known state. The control bits that support the Watchdog timer are discussed below.

Watchdog Timer Control Register

Bit:	7	6	5	4	3	2	1	0
	ENW	CLRW	WIDL	-	-	PS2	PS1	PS0

Mnemonic: WDTC Address: 8FH

ENW : Enable watch-dog if set.

CLRW : Clear watch-dog timer and prescaler if set. This flag will be cleared automatically

WIDL : If this bit is set, watch-dog is enabled under IDLE mode. If cleared, watch-dog is disabled under IDLE mode. Default is cleared.

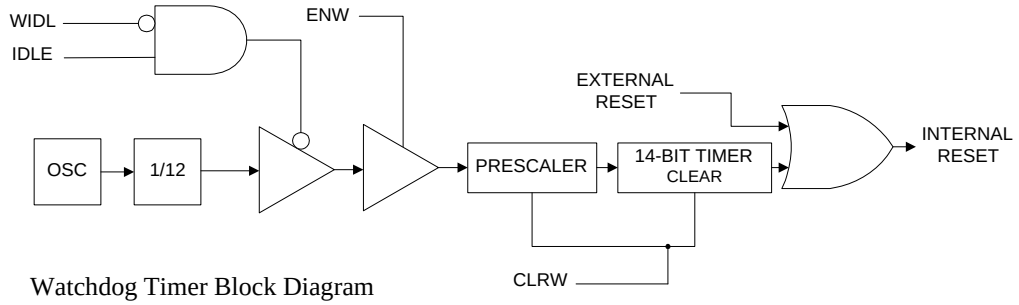
PS2, PS1, PS0: Watch-dog prescaler timer select. Prescaler is selected when set PS2–0 as follows:

PS2	PS1	PS0	PRESCALER SELECT
0	0	0	2
0	0	1	4
0	1	0	8
0	1	1	16
1	0	0	32
1	0	1	64
1	1	0	128
1	1	1	256

The time-out period is obtained using the following equation:

$$\frac{1}{OSC} \times 2^{14} \times PRESCALER \times 1000 \times 12 \text{ mS}$$

Before Watchdog time-out occurs, the program must clear the 14-bit timer by writing 1 to WDTC.6 (CLRW). After 1 is written to this bit, the 14-bit timer, prescaler and this bit will be reset on the next instruction cycle. The Watchdog timer is cleared on reset.



Watchdog Timer Block Diagram

Typical Watch-Dog time-out period when OSC = 20 MHz

PS2	PS1	PS0	WATCHDOG TIME-OUT PERIOD
0	0	0	19.66 mS
0	0	1	39.32 mS
0	1	0	78.64 mS
0	1	1	157.28 mS
1	0	0	314.57 mS
1	0	1	629.14 mS
1	1	0	1.25 S
1	1	1	2.50 S

5.9 In-System Programming (ISP) Mode

The W78L365A equips one 64K byte of main ROM bank for application program (called APROM) and one 4K byte of auxiliary ROM bank for loader program (called LDROM). In the normal operation, the microcontroller executes the code in the APROM. If the content of APROM needs to be modified, the W78L365A allows user to activate the In-System Programming (ISP) mode by setting the CHPCON register. **The CHPCON is read-only by default, software must write two specific values 87H, then 59H sequentially to the CHPENR register to enable the CHPCON write attribute. Writing CHPENR register with the values except 87H and 59H will close CHPCON register write attribute.** The W78L365A achieves all in-system programming operations including enter/exit ISP Mode, program, erase, read ... etc, during device in the idle mode. Setting the bit CHPCON.0 the device will enter in-system programming mode after a wake-up from idle mode. Because device needs proper time to complete the ISP operations before awaken from idle mode, software may use timer interrupt to control the duration for device wake-up from idle mode. To perform ISP operation for revising contents of APROM, software located at APROM setting the CHPCON register then enter idle mode, after awaken from idle mode the device executes the corresponding interrupt service routine in LDROM. Because the device will clear the program counter while switching from APROM to LDROM, the first execution of RETI instruction in interrupt service routine will jump to 00H at LDROM area. The device offers a software reset for switching back to APROM while the content of APROM has been updated completely. **Setting CHPCON register bit 0, 1 and 7 to logic-1 will result a software reset to reset the CPU**. The software reset serves as a external reset. This in-system programming feature makes the job easy and efficient in which the application needs to update firmware frequently. In some applications, the in-system programming feature make it possible to easily update the system firmware without opening the chassis.

SFRAH, SFRAL: The objective address of on-chip ROM in the in-system programming mode. SFRAH contains the high-order byte of address, SFRAL contains the low-order byte of address.

SFRFD: The programming data for on-chip ROM in programming mode.

SFRCN: The control byte of on-chip ROM programming mode.

SFRCN (C7)

BIT	NAME	FUNCTION
7	-	Reserve.
6	WFWIN	On-chip ROM bank select for in-system programming. = 0: 64K bytes ROM bank is selected as destination for re-programming. = 1: 4K bytes ROM bank is selected as destination for re-programming.
5	OEN	ROM output enable.
4	CEN	ROM chip enable.
3, 2, 1, 0	CTRL[3:0]	The flash control signals

MODE	WFWIN	CTRL<3:0>	OEN	CEN	SFRAH, SFRAL	SFRFD
Erase 64KB APROM	0	0010	1	0	X	X
Program 64KB APROM	0	0001	1	0	Address in	Data in
Read 64KB APROM	0	0000	0	0	Address in	Data out
Erase 4KB LDROM	1	0010	1	0	X	X
Program 4KB LDROM	1	0001	1	0	Address in	Data in
Read 4KB LDROM	1	0000	0	0	Address in	Data out

5.9.1 In-System Programming Control Register (CHPCON)

CHPCON (BFH)

BIT	NAME	FUNCTION
7	SWRESET	When this bit is set to 1, and both FBOOTSL and FPROGEN are set to 1. It will enforce microcontroller reset to initial condition just like power on reset.
6	-	Reserve.
5	LD/AP	This bit is read only. 1: CPU is running LDROM program. 0: CPU is running APROM program.
4	ENAUXRAM	1: Enable on-chip AUX-RAM. 0: Disable the on-chip AUX-RAM
3	1	Must be 1
2	-	Reserve.
1	FBOOTSL	When this bit is set to 1, and both SWRESET and FPROGEN are set to 1. It will enforce microcontroller reset to initial condition just like power on reset.
0	FPROGEN	When this bit is set to 1, and both SWRESET and FBOOTSL are set to 1. It will enforce microcontroller reset to initial condition just like power on reset.

This register is protected by CHPENR register. Please write as below procedures while you would like to write CHPCON register.

```
Mov  CHPENR, #87h
Mov CHPENR, #59h
Anl  CHPCON, #EFh  ;Disable AUX-RAM
Mov CHPENR, #0h
```

5.10 Software Reset

Set CHPCON = 0X83, timer and enter IDLE mode. CPU will reset and restart from APFLASH after time out.

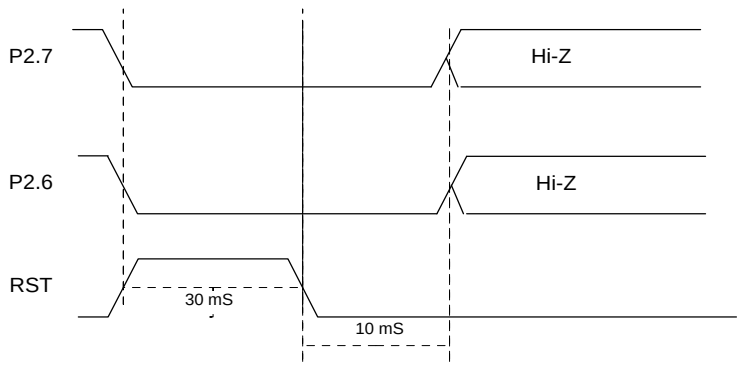
5.11 H/W Reboot Mode (Boot from LDROM)

By default, the W78L365A boots from APROM program after a power on reset. On some occasions, user can force the W78L365A to boot from the LDROM program via following settings. The possible situation that you need to enter H/W REBOOT mode when the APROM program can not run properly and device can not jump back to LDROM to execute in-system programming function. Then you can use this H/W REBOOT mode to force the W78L365A jumps to LDROM and executes in-system programming procedure. When you design your system, you may reserve the pins P2.6, P2.7 to switches or jumpers. For example in a CD-ROM system, you can connect the P2.6 and P2.7 to PLAY and EJECT buttons on the panel. When the APROM program fails to execute the normal application program. User can press both two buttons at the same time and then turn on the power of the personal computer to force the W78L365A to enter the H/W REBOOT mode. After power on of personal computer, you can release both buttons and finish the in-system programming procedure to update the APROM code. In application system design, user must take care of the P2, P3, ALE, $\overline{EA}$ and $\overline{PSEN}$ pin value at reset to prevent from accidentally activating the programming mode or H/W REBOOT mode. It is necessary to add 10K resistor on these P2.6, P2.7 and P4.3 pins.

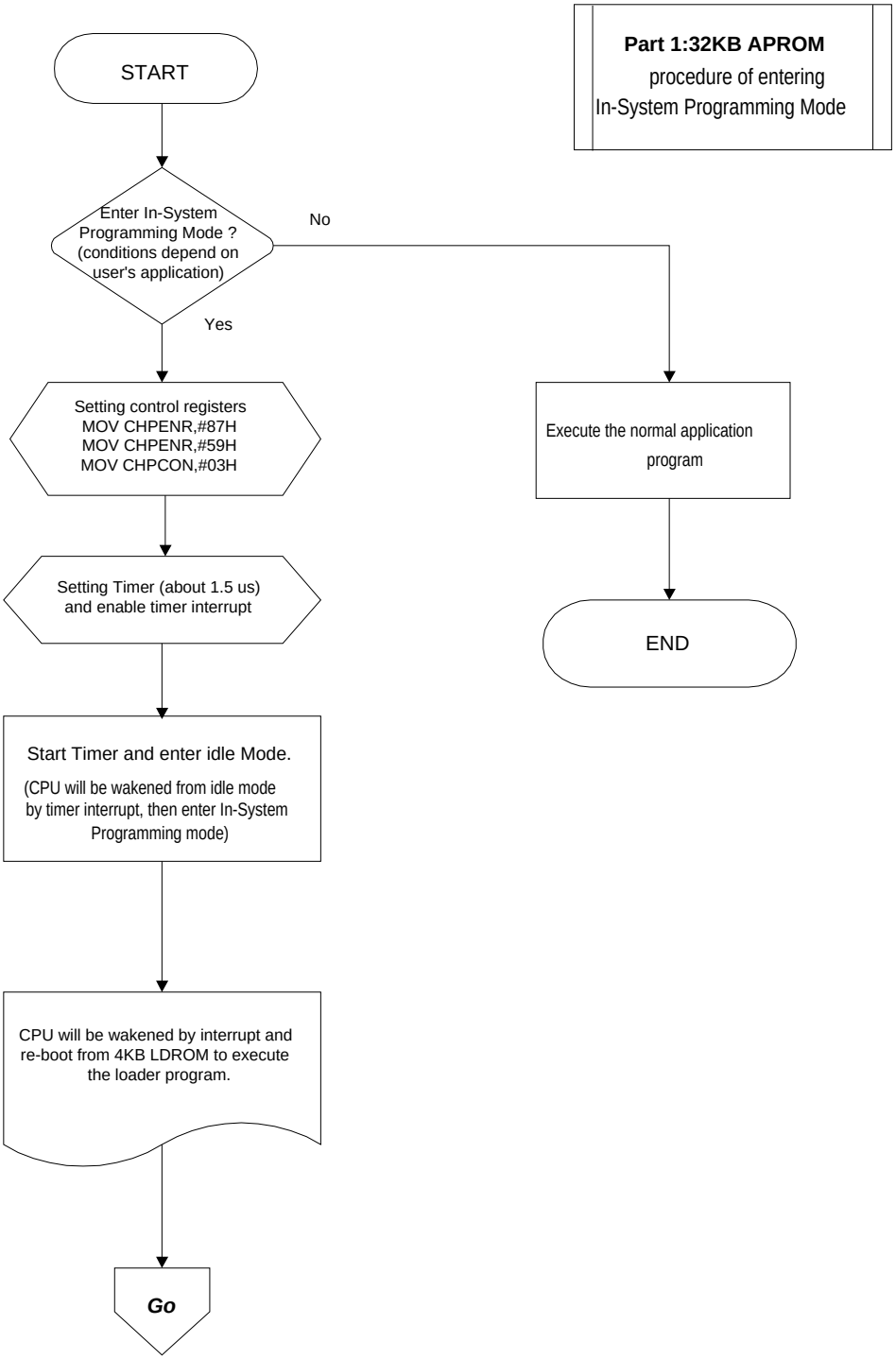
H/W Reboot MODE

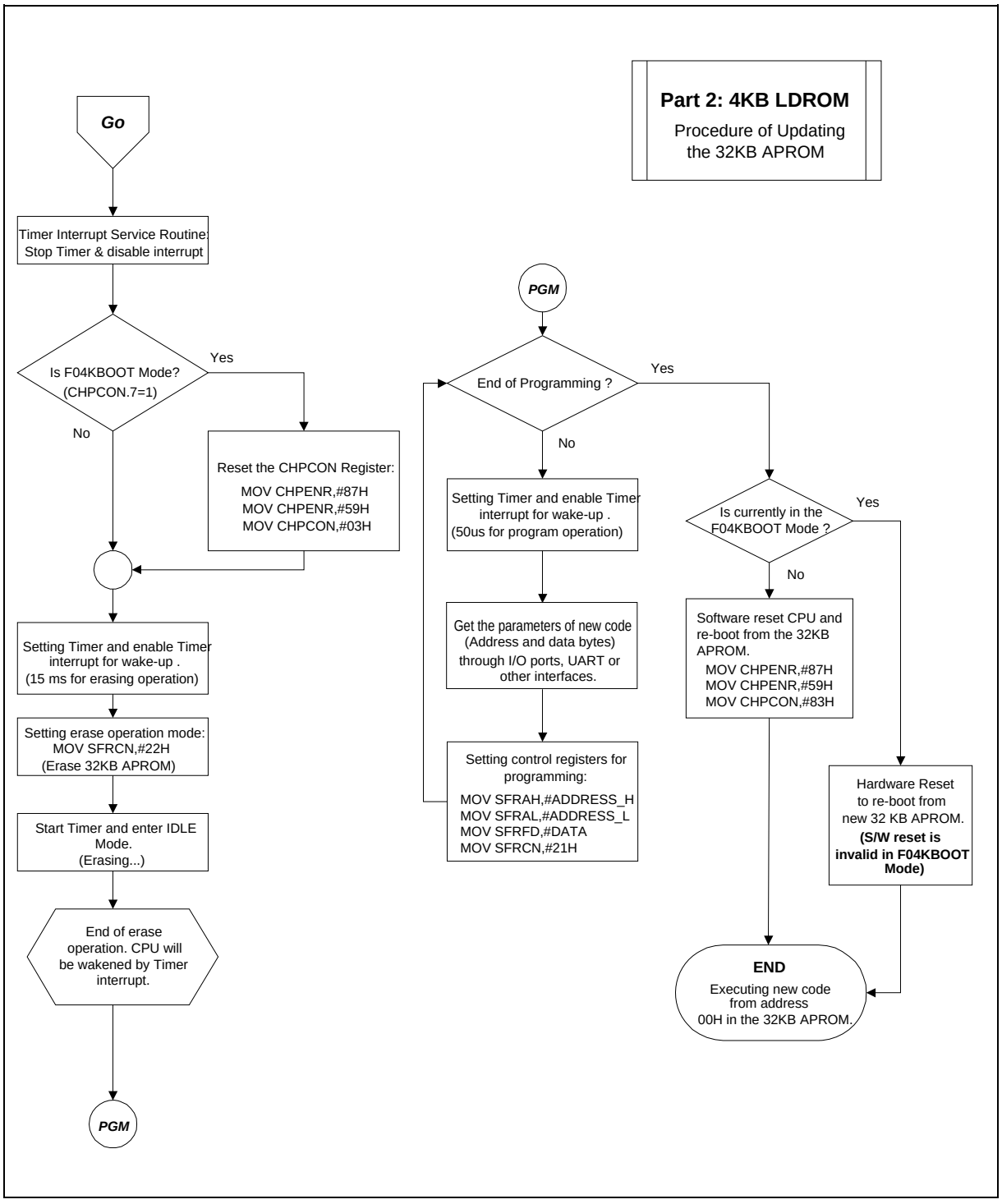
P4.3	P2.7	P2.6	MODE
X	L	L	REBOOT
L	X	X	REBOOT

The Reset Timing For Entering F04KBOOT Mode



The Algorithm of In-System Programming

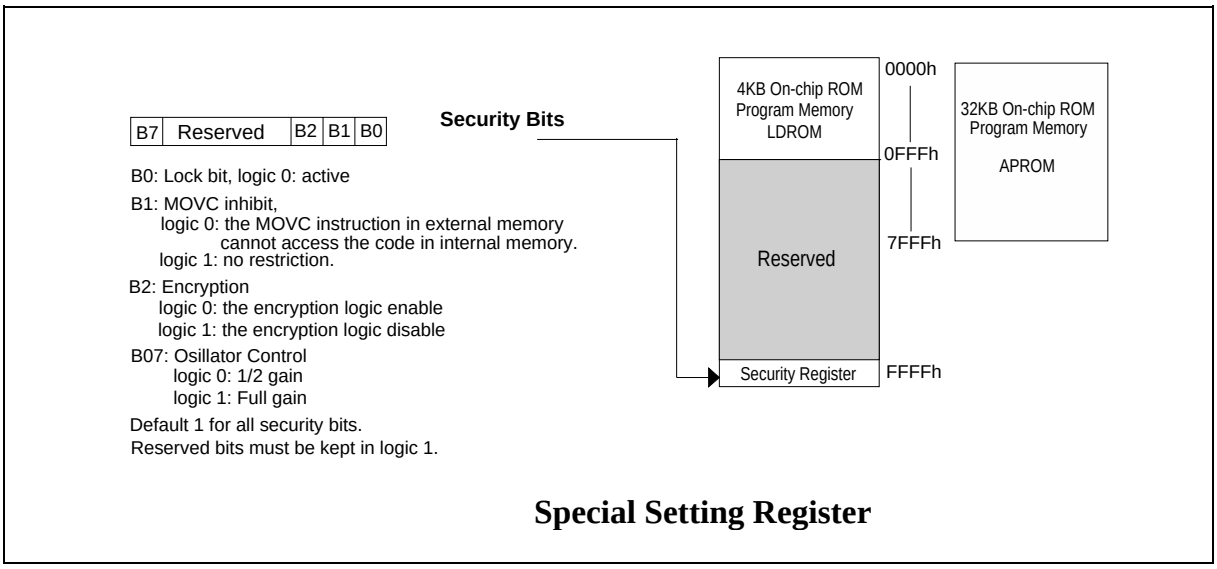




6. SECURITY

During the on-chip ROM programming mode, the ROM can be programmed and verified repeatedly. Until the code inside the ROM is confirmed OK, the code can be protected. The protection of ROM and those operations on it are described below.

The W78L365A has a Security Register that can be accessed in programming mode. Those bits of the Security Registers can not be changed once they have been programmed from high to low. They can only be reset through erase-all operation. The Security Register is located at the 0FFFFH of the LDROM space.



Special Setting Register

6.1 Lock Bit

This bit is used to protect the customer's program code in the W78L365A. It may be set after the programmer finishes the programming and verifies sequence. Once this bit is set to logic 0, both the ROM data and Security Register can not be accessed again.

6.2 MOVC Inhibit

This bit is used to restrict the accessible region of the MOVC instruction. It can prevent the MOVC instruction in external program memory from reading the internal program code. When this bit is set to logic 0, a MOVC instruction in external program memory space will be able to access code only in the external memory, not in the internal memory. A MOVC instruction in internal program memory space will always be able to access the ROM data in both internal and external memory. If this bit is logic 1, there are no restrictions on the MOVC instruction.

6.3 Encryption

This bit is used to enable/disable the encryption logic for code protection. Once encryption feature is enabled, the data presented on port 0 will be encoded via encryption logic. Only whole chip erase will reset this bit.

6.4 Oscillator Control

W78L365A/E516 allow user to diminish the gain of on-chip oscillator amplifier by using programmer to set the bit B7 of security register. Once B7 is set to 0, a half of gain will be decreased. Care must be taken if user attempts to diminish the gain of oscillator amplifier, reducing a half of gain may improperly affect the external crystal operation at high frequency above 20 MHz. The value of R and C1, C2 may need some adjustment while running at lower gain.

7. ELECTRICAL CHARACTERISTICS

7.1 Absolute Maximum Ratings

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
DC Power Supply	V_{DD}–V_{SS}	-0.3	+6.0	V
Input Voltage	V_{IN}	V_{SS} -0.3	V_{DD} +0.3	V
Operating Temperature	T_A	0	70	°C
Storage Temperature	T_{ST}	-55	+150	°C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

7.2 D.C. Characteristics

(V_{SS} = 0v, T_A = 25°C, unless otherwise specified.)

SYMBOL	PARAMETER	SPECIFICATION			TEST CONDITIONS
		MIN.	MAX.	UNIT	
V_{DD}	Operating Voltage	2.4	5.5	V	Without ISP
		2.7	5.5	V	With ISP
I_{DD}	Operating Current	-	20	mA	No load V_{DD} = 5.5V
			2.5	mA	No load V_{DD} = 2.4V
I_{IDLE}	Idle Current	-	6	mA	V_{DD} = 5.5V, Fosc = 20 MHz
			1	mA	V_{DD} = 2.4V, Fosc = 12 MHz
I_{PWDN}	Power Down Current	-	10	μA	V_{DD} = 5.5V, Fosc = 20 MHz
		-	10	μA	V_{DD} = 2.4V, Fosc = 12 MHz
I_{IN1}	Input Current P1, P2, P3, P4	-50	+10	μA	V_{DD} = 5.5V or 2.4V, V_{IN} = 0V or V_{DD}
I_{IN2}	Input Current RST	-10	+150	μA	V_{DD} = 5.5V, 0<V_{IN}<V_{DD}
		-10	50	μA	V_{DD} = 2.4V, 0<V_{IN}<V_{DD}
I_{LK}	Input Leakage Current P0, $\overline{EA}$	-10	+10	μA	V_{DD} = 5.5V or 2.4 V 0V<V_{IN}<V_{DD}
I_{TL}[*4]	Logic 1 to 0 Transition Current P1, P2, P3, P4	-500	-200	μA	V_{DD} = 5.5V, V_{IN} = 1.4V
		-50	-30	μA	V_{DD} = 2.4V, V_{IN} = 0.92V

D.C. Characteristics, continued

SYMBOL	PARAMETER	SPECIFICATION			TEST CONDITIONS
		MIN.	MAX.	UNIT	
V_{IL1}	Input Low Voltage	0	0.8	V	V_{DD} = 4.5V
	P0, P1, P2, P3, P4, RST, $\overline{EA}$	0	0.5	V	V_{DD} = 2.4V
V_{IL3}	Input Low Voltage	0	0.8	V	V_{DD} = 4.5V
	XTAL1[*4]	0	0.4	V	V_{DD} = 2.4V
V_{IH1}	Input High Voltage	2.4	V_{DD} +0.2	V	V_{DD} = 5.5V
	P0, P1, P2, P3, P4, $\overline{EA}$	1.4	V_{DD} +0.2	V	V_{DD} = 2.4V
V_{IH2}	Input High Voltage	3.5	V_{DD} +0.2	V	V_{DD} = 5.5V
	RST	1.7	V_{DD} +0.2	V	V_{DD} = 2.4V
V_{IH3}	Input High Voltage	3.5	V_{DD} +0.2	V	V_{DD} = 5.5V
	XTAL1[*4]	1.6	V_{DD} +0.2	V	V_{DD} = 2.4V
V_{OL}	Output Low Voltage	-	0.45	V	V_{DD} = 4.5V
	P1, P2, P3, P4, P0, ALE, $\overline{PSEN}$	-	0.4	V	V_{DD} = 2.4V
Isk1	Sink current	4	8	mA	V_{DD} = 4.5V, V_{OL} = 0.45V
	P1, P3, P4	2.5	4.5	mA	V_{DD} = 2.4V, V_{OL} = 0.4V
Isk2	Sink current	10	14	mA	V_{DD} = 4.5V, V_{OL} = 0.45V
	P0, P2, ALE, $\overline{PSEN}$	5	9	mA	V_{DD} = 2.4V, V_{OL} = 0.4V
V_{OH}	Output High Voltage	2.4	-	V	V_{DD} = 4.5V
	P1, P2, P3, P4, P0, ALE, $\overline{PSEN}$	1.4	-	V	V_{DD} = 2.4V
Isr1	Source current	-150	-200	μA	V_{DD} = 4.5V, V_{OH} = 2.4V
	P1, P2, P3, P4	-20	-60	μA	V_{DD} = 2.4V, V_{OH} = 1.4V
Isr2	Source current	-10	-14	mA	V_{DD} = 4.5V, V_{OH} = 2.4V
	P0, P2, ALE, $\overline{PSEN}$	-1.9	-3.8	mA	V_{DD} = 2.4V, V_{OH} = 1.4V

Notes:

*1. RST pin is a Schmitt trigger input.

*2. P0, ALE and $\overline{PSEN}$ are tested in the external access mode.

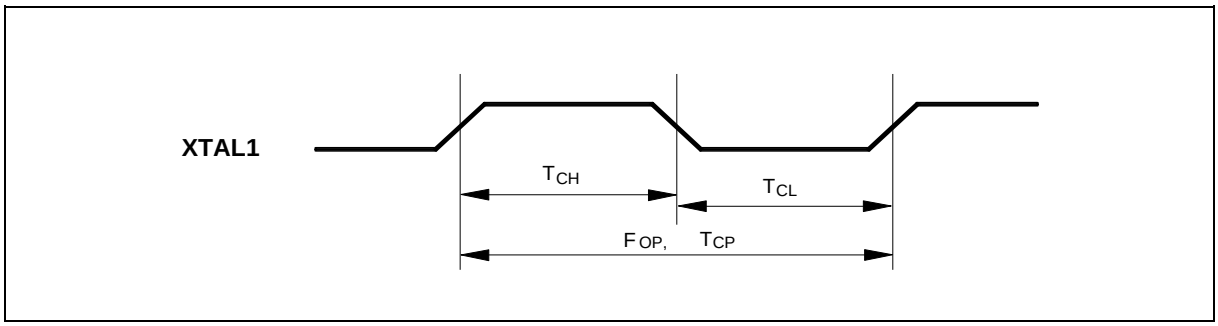
*3. XTAL1 is a CMOS input.

*4. Pins of P1, P2, P3, P4 can source a transition current when they are being externally driven from 1 to 0.

7.3 A.C. Characteristics

The AC specifications are a function of the particular process used to manufacture the part, the ratings of the I/O buffers, the capacitive load, and the internal routing capacitance. Most of the specifications can be expressed in terms of multiple input clock periods (T_{CP}), and actual parts will usually experience less than a ±20 nS variation.

Clock Input Waveform



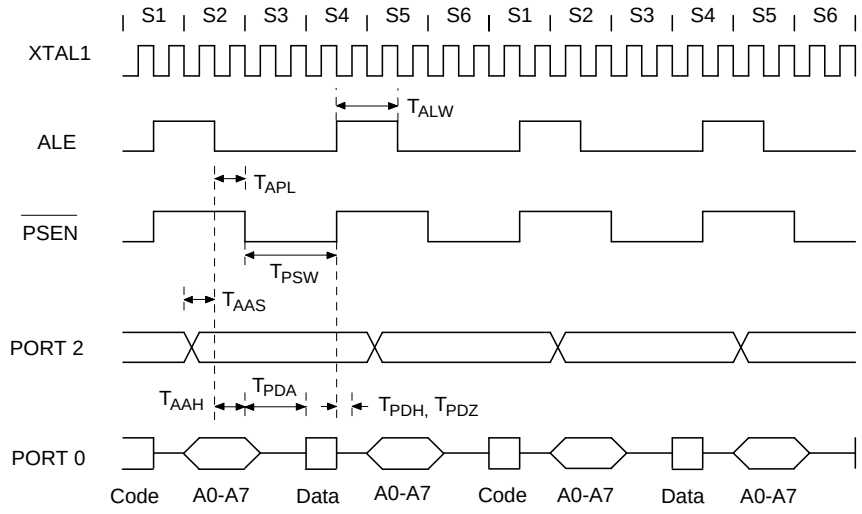
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTES
Operating Speed	F_{OP}	0	-	20	MHz	1
Clock Period	TCP	41.7	-	-	nS	2
Clock High	T_{CH}	20	-	-	nS	3
Clock Low	T_{CL}	20	-	-	nS	3

Notes:

1. The clock may be stopped indefinitely in either state.
2. The T_{CP} specification is used as a reference in other specifications.
3. There are no duty cycle requirements on the XTAL1 input.

8. TIMING WAVEFORMS

8.1 Program Fetch Cycle

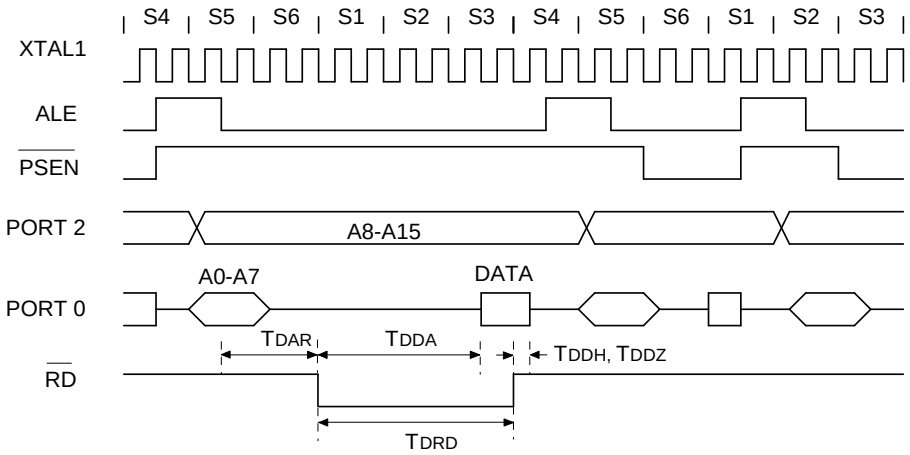


PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTES
Address Valid to ALE Low	T_{AAS}	1 T_{CP}-Δ	-	-	nS	4
Address Hold from ALE Low	T_{AAH}	1 T_{CP}-Δ	-	-	nS	1, 4
ALE Low to $\overline{PSEN}$ Low	T_{APL}	1 T_{CP}-Δ	-	-	nS	4
$\overline{PSEN}$ Low to Data Valid	T_{PDA}	-	-	2 T_{CP}	nS	2
Data Hold after $\overline{PSEN}$ High	T_{PDH}	0	-	1 T_{CP}	nS	3
Data Float after $\overline{PSEN}$ High	T_{PDZ}	0	-	1 T_{CP}	nS	
ALE Pulse Width	T_{ALW}	2 T_{CP}-Δ	2 T_{CP}	-	nS	4
$\overline{PSEN}$ Pulse Width	T_{PSW}	3 T_{CP}-Δ	3 T_{CP}	-	nS	4

Notes:

1. P0.0–P0.7, P2.0–P2.7 remain stable throughout entire memory cycle.
2. Memory access time is 3 T_{CP}.
3. Data have been latched internally prior to $\overline{PSEN}$ going high.
4. "Δ" (due to buffer driving delay and wire loading) is 20 nS.

8.2 Data Read Cycle

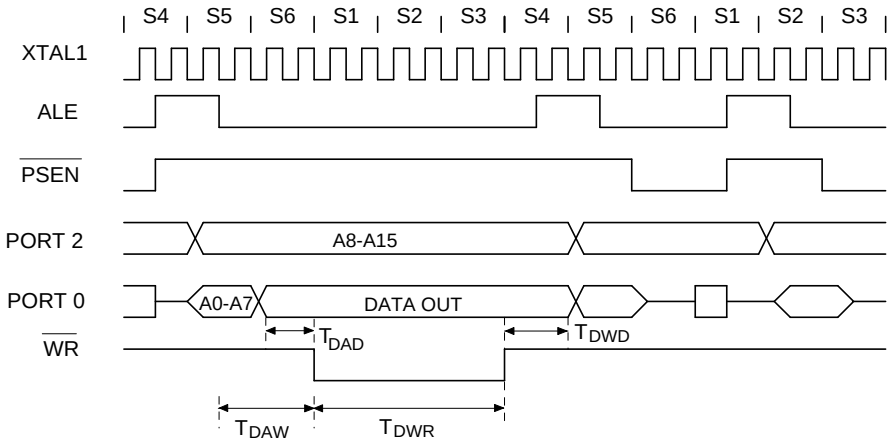


PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTES
ALE Low to $\overline{RD}$ Low	TDAR	3 TCP-Δ	-	3 TCP+Δ	nS	1, 2
$\overline{RD}$ Low to Data Valid	TDDA	-	-	4 TCP	nS	1
Data Hold from $\overline{RD}$ High	TDDH	0	-	2 TCP	nS	
Data Float from $\overline{RD}$ High	TDDZ	0	-	2 TCP	nS	
$\overline{RD}$ Pulse Width	TDRD	6 TCP-Δ	6 TCP	-	nS	2

Notes:

1. Data memory access time is 8 TCP.
2. "Δ" (due to buffer driving delay and wire loading) is 20 nS.

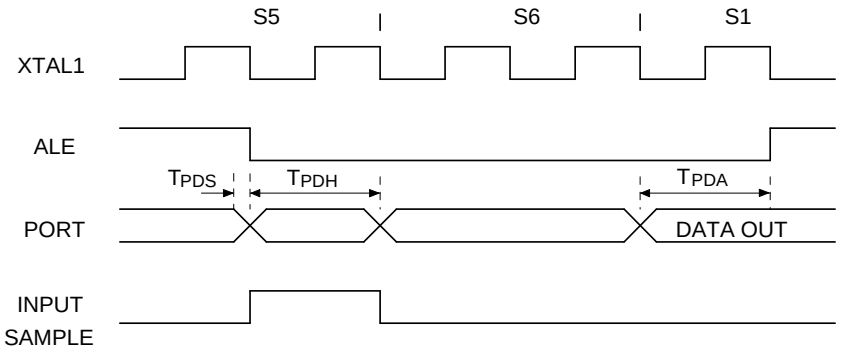
8.3 Data Write Cycle



PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
ALE Low to $\overline{WR}$ Low	TDAW	3 TCP-Δ	-	3 TCP+Δ	nS
Data Valid to $\overline{WR}$ Low	TDAD	1 TCP-Δ	-	-	nS
Data Hold from $\overline{WR}$ High	TDWD	1 TCP-Δ	-	-	nS
$\overline{WR}$ Pulse Width	TDWR	6 TCP-Δ	6 TCP	-	nS

Note: "Δ" (due to buffer driving delay and wire loading) is 20 nS.

8.4 Port Access Cycle



PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Port Input Setup to ALE Low	TPDS	1 TCP	-	-	nS
Port Input Hold from ALE Low	TPDH	0	-	-	nS
Port Output to ALE	TPDA	1 TCP	-	-	nS

Note: Ports are read during S5P2, and output data becomes available at the end of S6P2. The timing data are referenced to ALE, since it provides a convenient reference.

9. TYPICAL APPLICATION CIRCUIT

9.1 External Program Memory and Crystal

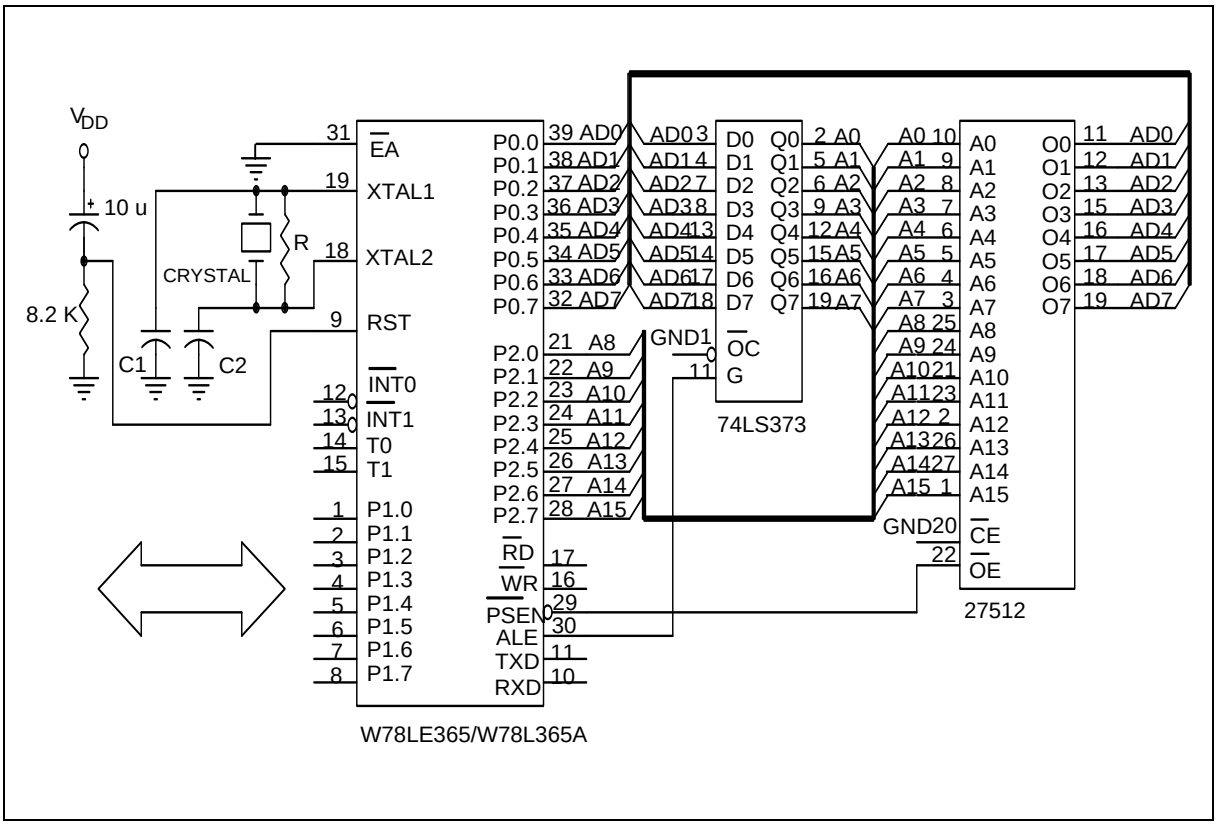


Figure A

CRYSTAL	C1	C2	R
6 MHz	47P	47P	-
16 MHz	30P	30P	-
20 MHz	15P	10P	-

Above table shows the reference values for crystal applications.

Notes:

1. C1, C2, R components refer to Figure A
2. Crystal layout must get close to XTAL1 and XTAL2 pins on user's application board.

9.2 Expanded External Data Memory and Oscillator

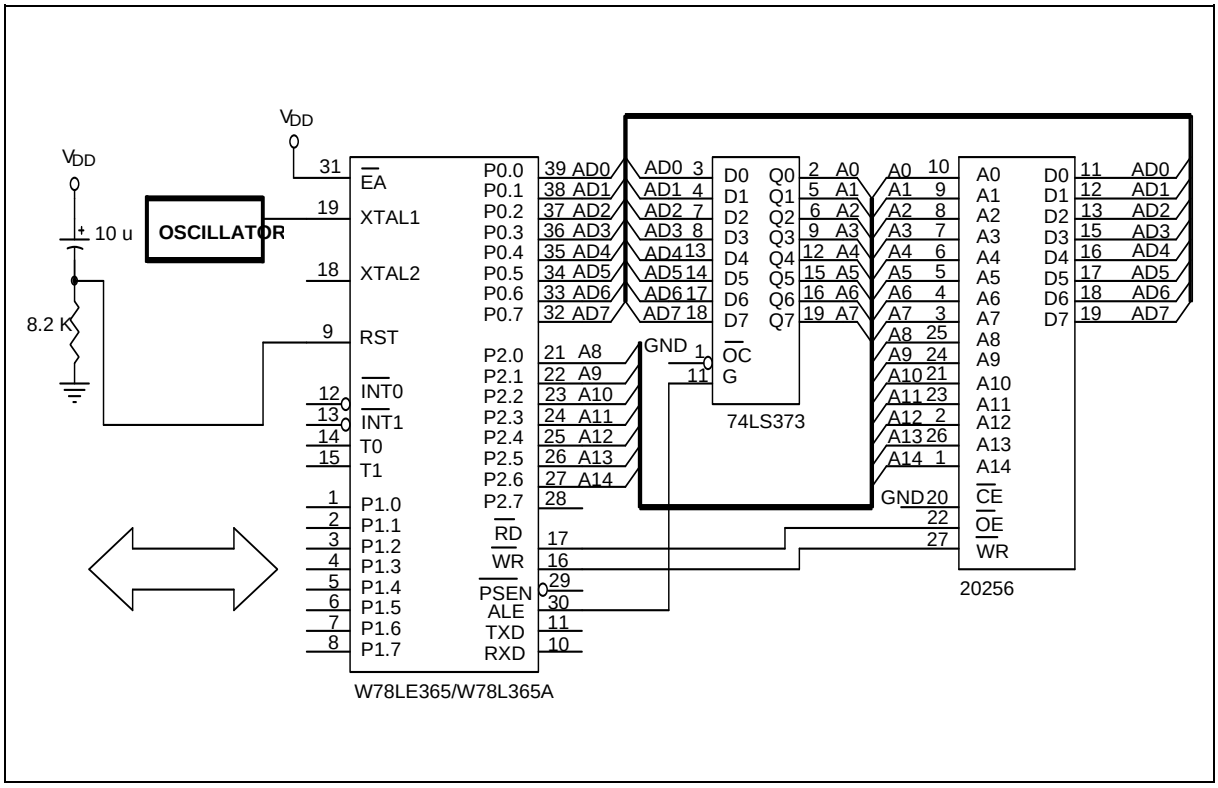
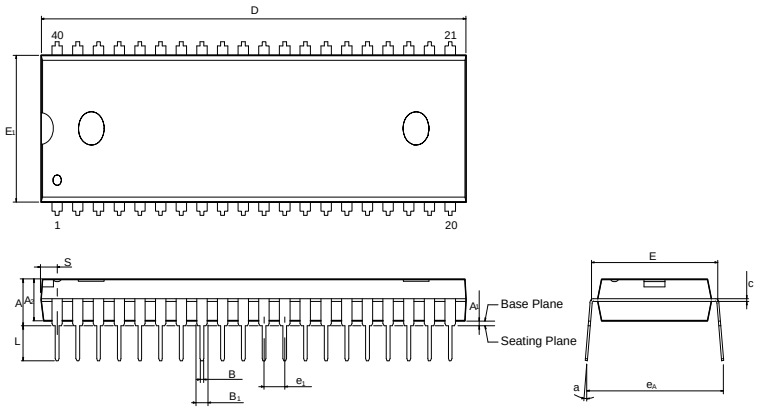


Figure B

10. PACKAGE DIMENSIONS

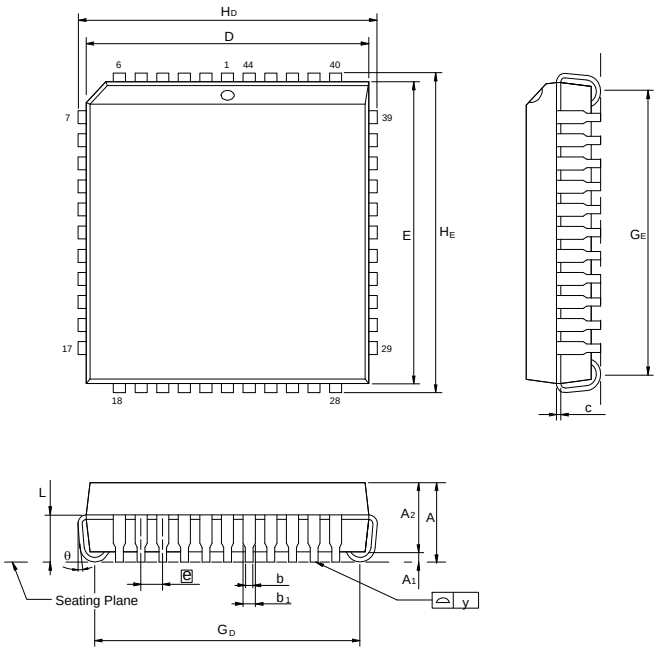
10.1 40-pin DIP



Symbol	Dimension in inch			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	0.210	—	—	5.334
A_1	0.010	—	—	0.254	—	—
A_2	0.150	0.155	0.160	3.81	3.937	4.064
B	0.016	0.018	0.022	0.406	0.457	0.559
B_1	0.048	0.050	0.054	1.219	1.27	1.372
c	0.008	0.010	0.014	0.203	0.254	0.356
D	—	2.055	2.070	—	52.20	52.58
E	0.590	0.600	0.610	14.986	15.24	15.494
E_1	0.540	0.545	0.550	13.72	13.84	13.97
e_1	0.090	0.100	0.110	2.286	2.54	2.794
L	0.120	0.130	0.140	3.048	3.302	3.556
a	0	—	15	0	—	15
e_A	0.630	0.650	0.670	16.00	16.51	17.01
S	—	—	0.090	—	—	2.286

Notes:
1. Dimension D Max. & S include mold flash tie bar burrs.
2. Dimension E1 does not include interlead fla
3. Dimension D & E1 include mold mismatch a are determined at the mold parting line
4. Dimension B1 does not include damba protrusion/intrusion.
5. Controlling dimension: Inches.
6. General appearance spec. should be based final visual inspection spec.

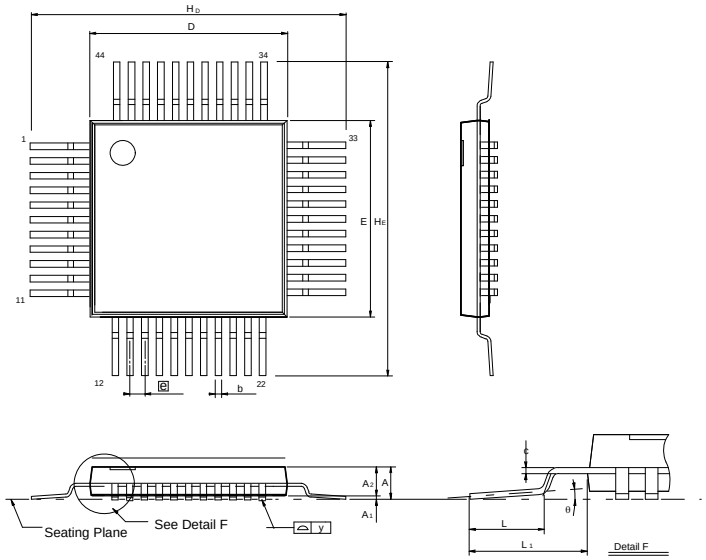
10.2 44-pin PLCC



Symbol	Dimension in inch			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	0.185	—	—	4.699
A_1	0.020	—	—	0.508	—	—
A_2	0.145	0.150	0.155	3.683	3.81	3.937
b_1	0.026	0.028	0.032	0.66	0.711	0.813
b	0.016	0.018	0.022	0.406	0.457	0.559
c	0.008	0.010	0.014	0.203	0.254	0.356
D	0.648	0.653	0.658	16.46	16.59	16.71
E	0.648	0.653	0.658	16.46	16.59	16.71
e	0.050 BSC			1.27 BSC		
G_D	0.590	0.610	0.630	14.99	15.49	16.00
G_E	0.590	0.610	0.630	14.99	15.49	16.00
H_D	0.680	0.690	0.700	17.27	17.53	17.78
H_E	0.680	0.690	0.700	17.27	17.53	17.78
L	0.090	0.100	0.110	2.296	2.54	2.794
y	—	—	0.004	—	—	0.10

Notes:
1. Dimension D & E do not include interlead flash.
2. Dimension b1 does not include dambar protrusion/intrusion.
3. Controlling dimension: Inches
4. General appearance spec. should be based on final visual inspection spec.

10.3 44-pin PQFP

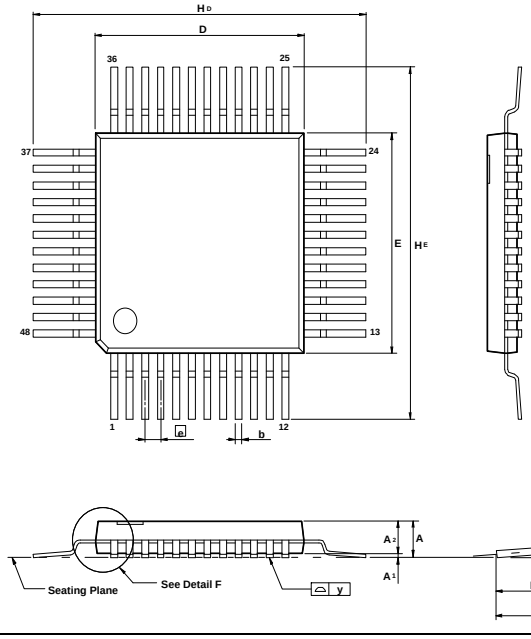


Symbol	Dimension in inch			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	---	---	---	---	---	---
A_1	0.002	0.01	0.02	0.05	0.25	0.5
A_2	0.075	0.081	0.087	1.90	2.05	2.20
b	0.01	0.014	0.018	0.25	0.35	0.45
c	0.004	0.006	0.010	0.101	0.152	0.254
D	0.390	0.394	0.398	9.9	10.00	10.1
E	0.390	0.394	0.398	9.9	10.00	10.1
e	0.025	0.031	0.036	0.635	0.80	0.952
H_D	0.510	0.520	0.530	12.95	13.2	13.45
H_E	0.510	0.520	0.530	12.95	13.2	13.45
L	0.025	0.031	0.037	0.65	0.8	0.95
L_1	0.051	0.063	0.075	1.295	1.6	1.905
y	—	—	0.003	—	—	0.08
θ	0°	—	7°	0°	—	7°

Notes:

1. Dimension D & E do not include interlead flash.
2. Dimension b does not include dambar protrusion/intrusion.
3. Controlling dimension: Millimeter
4. General appearance spec. should be based on final visual inspection spec.

10.4 48-pin LQFP



Symbol	Dimension in mm		
	Min.	Nom.	Max.
A	---	---	1.60
A_1	0.05	---	0.15
A_2	1.35	1.40	1.45
b	0.17	0.20	0.27
c	0.09	---	0.20
D		7.00	
E		7.00	
e		0.50	
H_D		9.00	
H_E		9.00	
L	0.45	0.60	0.75
L_1		1.00	
y	---	0.08	---
θ	0	3.5°	7

Notes:

1. **Dimensions D & E do not include interlead flash.**
2. **Dimension b does not include dambar protrusion/intrusion.**
3. **Controlling dimension: Millimeters**
4. **General appearance spec. should be based on final visual inspection spec.**

11. APPLICATION NOTE

11.1 In-system Programming Software Examples

This application note illustrates the in-system programmability of the Nuvoton W78E365 ROM microcontroller. In this example, microcontroller will boot from 64KB APROM bank and waiting for a key to enter in-system programming mode for re-programming the contents of 64KB APROM. While entering in-system programming mode, microcontroller executes the loader program in 4KB LDROM bank. The loader program erases the 64KB APROM then reads the new code data from external SRAM buffer (or through other interfaces) to update the 64KB APROM.

Example 1:

```
;*****************************************************************************************************************
;* Example of 64K APROM program: Program will scan the P1.0. if P1.0 = 0, enters in-system
;* programming mode for updating the content of APROM code else executes the current ROM code.
;* XTAL = 16 MHz
;*****************************************************************************************************************
        .chip 8052
        .RAMCHK OFF
        .symbols

        CHPCON    EQU    BFH
        CHPENR    EQU    F6H
        SFRAL     EQU    C4H
        SFRAH     EQU    C5H
        SFRFD     EQU    C6H
        SFRCN     EQU    C7H

        ORG    0H
        LJMP   100H                    ; JUMP TO MAIN PROGRAM
    ;*************************************************************************
    ;*  TIMER0 SERVICE VECTOR ORG = 000BH
    ;*************************************************************************
        ORG    00BH
        CLR    TR0                     ; TR0 = 0, STOP TIMER0
        MOV    TL0, R6
        MOV    TH0, R7
        RETI
    ;*************************************************************************
    ;*  64K APROM MAIN PROGRAM
    ;*************************************************************************
       ORG 100H

MAIN_64K:
        MOV A, P1                      ; SCAN P1.0
        ANL A, #01H
        CJNE A, #01H, PROGRAM_64K      ; IF P1.0 = 0, ENTER IN-SYSTEM PROGRAMMING MODE
        JMP NORMAL_MODE

PROGRAM_64K:
        MOV CHPENR, #87H               ; CHPENR = 87H, CHPCON REGISTER WRTE ENABLE
        MOV CHPENR, #59H               ; CHPENR = 59H, CHPCON REGISTER WRITE ENABLE
        MOV CHPCON, #03H               ; CHPCON = 03H, ENTER IN-SYSTEM PROGRAMMING MODE
        MOV TCON, #00H                 ; TR = 0 TIMER0 STOP
```

```
        MOV IP, #00H                ; IP = 00H
        MOV IE, #82H                ; TIMER0 INTERRUPT ENABLE FOR WAKE-UP FROM IDLE MODE
        MOV R6, #F0H                ; TL0 = F0H
        MOV R7, #FFH                ; TH0 = FFH
        MOV TL0, R6
        MOV TH0, R7
        MOV TMOD, #01H              ; TMOD = 01H, SET TIMER0 A 16-BIT TIMER
        MOV TCON, #10H              ; TCON = 10H, TR0 = 1, GO
        MOV PCON, #01H              ; ENTER IDLE MODE FOR LAUNCHING THE IN-SYSTEM
                                    ; PROGRAMMING
;*****************************************************************************
;* Normal mode 64KB APROM program: depending user's application
;*****************************************************************************
NORMAL_MODE:
        .                           ; User's application program
        .
        .
        .
```

Example 2:

```
;*************************************************************************************************************************
Example of 4 KB LDROM program: This loader program will erase the 64KB APROM first, then reads the new ;*
code from external SRAM and program them into 32 KB APROM bank. XTAL = 16 MHz
;*************************************************************************************************************************
    .chip 8052
    .RAMCHK OFF
    .symbols

    CHPCON    EQU    BFH
    CHPENR    EQU    F6H
    SFRAL     EQU    C4H
    SFRAH     EQU    C5H
    SFRFD     EQU    C6H
    SFRCN     EQU    C7H

      ORG    000H
      LJMP   100H             ; JUMP TO MAIN PROGRAM
  ;*************************************************************************
  ;* 1. TIMER0 SERVICE VECTOR ORG = 0BH
  ;*************************************************************************
      ORG 000BH
      CLR   TR0               ; TR0 = 0, STOP TIMER0
      MOV TL0, R6
      MOV TH0, R7
      RETI
  ;*************************************************************************
  ;*  4KB LDROM MAIN PROGRAM
  ;*************************************************************************
      ORG 100H
MAIN_4K:
```

```
        MOV SP, #C0H
        MOV CHPENR, #87H     ; CHPENR = 87H, CHPCON WRITE ENABLE.
        MOV CHPENR, #59H     ; CHPENR = 59H, CHPCON WRITE ENABLE.
        MOV CHPCON, #03H     ; CHPCON = 03H, ENABLE IN-SYSTEM PROGRAMMING.
        MOV CHPENR, #00H     ; DISABLE CHPCON WRITE ATTRIBUTE

        MOV TCON, #00H       ; TCON = 00H, TR = 0 TIMER0 STOP
         MOV TMOD, #01H      ; TMOD = 01H, SET TIMER0 A 16BIT TIMER
        MOV IP, #00H         ; IP = 00H
        MOV IE, #82H         ; IE = 82H, TIMER0 INTERRUPT ENABLED
        MOV R6, #F0H
        MOV R7, #FFH
        MOV TL0, R6
        MOV TH0, R7
        MOV TCON, #10H       ; TCON = 10H, TR0 = 1, GO
        MOV PCON, #01H       ; ENTER IDLE MODE

 UPDATE_64K:
        MOV TCON, #00H       ; TCON = 00H , TR = 0 TIM0 STOP
        MOV IP, #00H         ; IP = 00H
        MOV IE, #82H         ; IE = 82H, TIMER0 INTERRUPT ENABLED
        MOV TMOD, #01H       ; TMOD = 01H, MODE1
        MOV R6, #E0H         ; SET WAKE-UP TIME FOR ERASE OPERATION, ABOUT 15 mS. DEPENDING
                             ; ON USER'S SYSTEM CLOCK RATE.
        MOV R7, #B1H
        MOV TL0, R6
        MOV TH0, R7

ERASE_P_4K:
        MOV SFRCN, #22H      ; SFRCN(C7H) = 22H  ERASE 64K
        MOV TCON, #10H       ; TCON = 10H, TR0 = 1, GO
        MOV PCON, #01H       ; ENTER IDLE MODE (FOR ERASE OPERATION)

;*********************************************************************
;* BLANK CHECK
;*********************************************************************
        MOV SFRCN, #0H       ; READ 64KB APROM MODE
        MOV SFRAH, #0H       ; START ADDRESS = 0H
        MOV SFRAL, #0H
         MOV R6, #FEH        ; SET TIMER FOR READ OPERATION, ABOUT 1.5 μS.
        MOV R7, #FFH
        MOV TL0, R6
        MOV TH0, R7

BLANK_CHECK_LOOP:
        SETB TR0             ; ENABLE TIMER 0
        MOV PCON, #01H       ; ENTER IDLE MODE
        MOV A, SFRFD         ; READ ONE BYTE
        CJNE A, #FFH, BLANK_CHECK_ERROR
        INC SFRAL            ; NEXT ADDRESS
        MOV A, SFRAL
        JNZ BLANK_CHECK_LOOP
        INC SFRAH
        MOV A, SFRAH
        CJNE A, #80H, BLANK_CHECK_LOOP   ; END ADDRESS = 7FFFH
```

```
        JMP PROGRAM_64KROM

BLANK_CHECK_ERROR:
        MOV P1, #F0H
        MOV P3, #F0H
        JMP $

;*****************************************************************************
;* RE-PROGRAMMING 64KB APROM BANK
;*****************************************************************************
PROGRAM_64KROM:
        MOV DPTR, #0H       ; THE ADDRESS OF NEW ROM CODE
        MOV R2, #00H        ; TARGET LOW BYTE ADDRESS
        MOV R1, #00H        ; TARGET HIGH BYTE ADDRESS
        MOV DPTR, #0H       ; EXTERNAL SRAM BUFFER ADDRESS
        MOV SFRAH, R1       ; SFRAH, TARGET HIGH ADDRESS
        MOV SFRCN, #21H     ; SFRCN(C7H) = 21 (PROGRAM 64K)
        MOV R6, #BEH        ; SET TIMER FOR PROGRAMMING, ABOUT 50 μS.
        MOV R7, #FFH
        MOV TL0, R6
        MOV TH0, R7

PROG_D_64K:
        MOV SFRAL, R2       ; SFRAL(C4H) = LOW BYTE ADDRESS
        MOVX A, @DPTR       ; READ DATA FROM EXTERNAL SRAM BUFFER. BY ACCORDING USER?
                            ; CIRCUIT, USER MUST MODIFY THIS INSTRUCTION TO FETCH CODE
        MOV SFRFD, A        ; SFRFD(C6H) = DATA IN
        MOV TCON, #10H      ; TCON = 10H, TR0 = 1, GO
        MOV PCON, #01H      ; ENTER IDLE MODE (PRORGAMMING)
        INC DPTR
        INC R2
        CJNE R2, #0H, PROG_D_64K
        INC  R1
        MOV SFRAH, R1
        CJNE R1, #80H, PROG_D_64K

;*****************************************************************************
; * VERIFY 64KB APROM BANK
;*****************************************************************************
        MOV R4, #03H        ; ERROR COUNTER
        MOV R6, #FEH        ; SET TIMER FOR READ VERIFY, ABOUT 1.5 μS.
        MOV R7, #FFH
        MOV TL0, R6
        MOV TH0, R7
        MOV DPTR, #0H       ; The start address of sample code
        MOV R2, #0H         ; Target low byte address
        MOV R1, #0H         ; Target high byte address
        MOV SFRAH, R1       ; SFRAH, Target high address
        MOV SFRCN, #00H     ; SFRCN = 00 (Read ROM CODE)
```

```
READ_VERIFY_64K:
        MOV SFRAL, R2         ; SFRAL(C4H) = LOW ADDRESS
        MOV TCON, #10H        ; TCON = 10H, TR0 = 1,GO
        MOV PCON, #01H
        INC R2
        MOVX A, @DPTR
        INC DPTR
        CJNE A, SFRFD, ERROR_64K
        CJNE R2, #0H, READ_VERIFY_64K
        INC R1
        MOV SFRAH, R1
        CJNE R1, #80H, READ_VERIFY_64K

;*******************************************************************************
;* PROGRAMMING COMPLETLY, SOFTWARE RESET CPU
;*******************************************************************************
        MOV CHPENR, #87H      ; CHPENR = 87H
        MOV CHPENR, #59H      ; CHPENR = 59H
        MOV CHPCON, #83H      ; CHPCON = 83H, SOFTWARE RESET.

ERROR_64K:
        DJNZ R4, UPDATE_64K   ; IF ERROR OCCURS, REPEAT 3 TIMES.
        .                     ; IN-SYSTEM PROGRAMMING FAIL, USER'S PROCESS TO DEAL WITH IT.
        .
        .
        .
```

12. REVISION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A1	May 14, 2003	-	Initial Issued
A2	August, 2004	31	Revise the title of 9.1
A3	April 19, 2005	41	Add Important Notice
A4	July 1, 2005	3	Add lead free (RoHS) parts
A5	October 2, 2006		Remove block diagram Change operating frequency into 20MHz
A6	December 4, 2006	3	Remove all Leaded package parts
A7	January 10, 2007	3 4 36	Add 48-pin LQFP part. Add 48-pin LQFP package Add 48-pin LQFP package dimension
A8	April 28, 2008	9	Update P3 reset state
A9	July 15, 2008	6	Revise typo Incorrect: AUX-RAM is enable after a reset Correct: AUX-RAM is disabled after a reset
A10	January 12, 2009	6 9	Revise typo, on-chip AUX-RAM is enabled after a reset. (Ver A10 is incorrect) Revise CHPCON initial value from 0xx00000b to 00x11000b.

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