SX9324

Ultra Low Power, Smart Proximity Sensor for SAR

WIRELESS & SENSING

GENERAL DESCRIPTION

The SX9324 is a capacitive Specific Absorption Rate (SAR) controller.

The SX9324 can use two sensor inputs coupled to its smart engine for SAR to accurately discriminate between an inanimate object and human body.

The resulting detection is used in portable electronic devices to reduce and control radio-frequency (RF) emission power in the presence of a human body, enabling significant performance advantages for manufacturers of electronic devices with electro-magnetic radiation sources to meet stringent emission regulations' criteria and Specific Absorption Rate (SAR) standards.

Operating directly from an input supply voltage of 1.7 to 2V, the SX9324 outputs its data via I2C serial bus. The I2C serial communication bus port is compatible with 1.8V host control to report body detection/proximity and to facilitate parameter settings adjustment. Upon proximity detection, the NIRQ output asserts, enabling the user to either determine the relative proximity distance, or simply obtain an indication of detection.

The SX9324 includes an on-chip auto-calibration controller that regularly performs sensitivity adjustments to maintain peak performance over a wide variation of temperature, humidity and noise environments, providing simplified product development and enhanced performance.

KEY PRODUCT FEATURES

- ♦ **~1.8V Input Supply Voltage**
- ♦ **Up to 3 Capacitive Sensor Inputs**
  - ❖ Patented On-Chip Smart Engine For SAR
  - ❖ Capacitance Resolution down to 0.004fF
  - ❖ Capacitance Offset Compensation up to 200pF
  - ❖ Advanced Temperature Compensation
- ♦ **Automatic Calibration**
- ♦ **Ultra Low Power Consumption**
  - ❖ Active Mode: 22 uA
  - ❖ Doze Mode: 6 uA
  - ❖ Sleep Mode: 1.75 uA
- ♦ **400kHz I2C Serial Interface**
  - ❖ 2 Sub-Addresses Selectable by Pin.
- ♦ **Programmable Interrupt or Real-Time Status pin**
- ♦ **Two Reset Sources: POR, Soft Reset**
- ♦ **-40°C to +85°C Operation**
- ♦ **Compact Size: 0.92 x 1.69 mm WLCSP package**
- ♦ **Pb & Halogen Free, RoHS/WEEE compliant**

APPLICATIONS

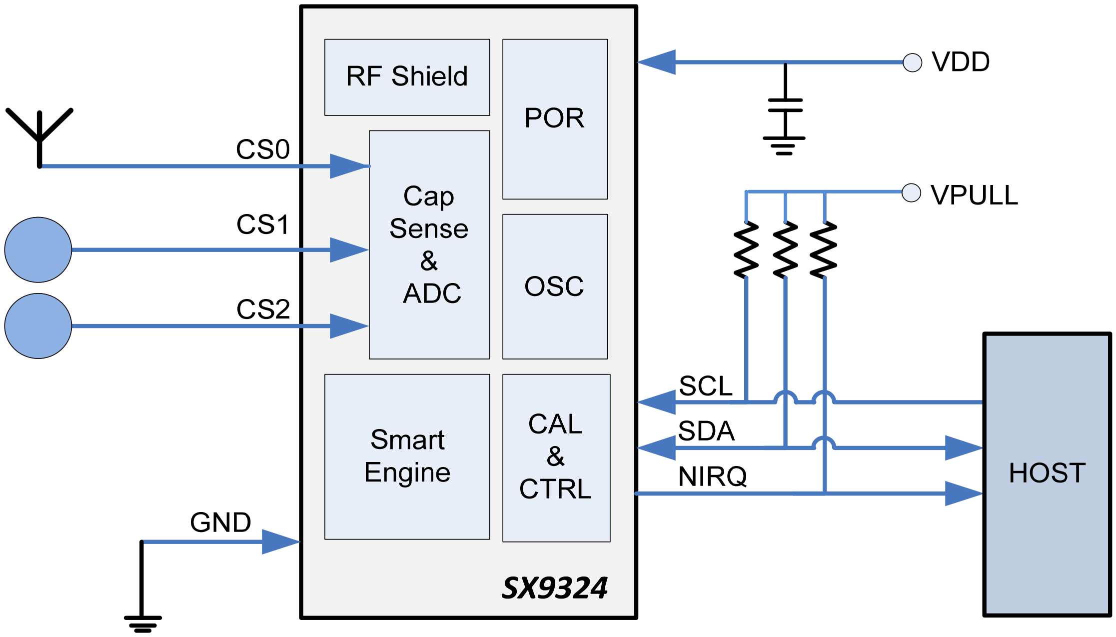
- Mobile Phones
- Tablets
- Notebooks

ORDERING INFORMATION

Part Number	Package	Marking
SX9324ICSTRT [1]	WLCSP-8	V4CP
SX9324EVKA	Eval. Kit	-

[1] 3000 Units/reel

TYPICAL APPLICATION CIRCUIT



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1 GENERAL DESCRIPTION

1.1 Pin Diagram

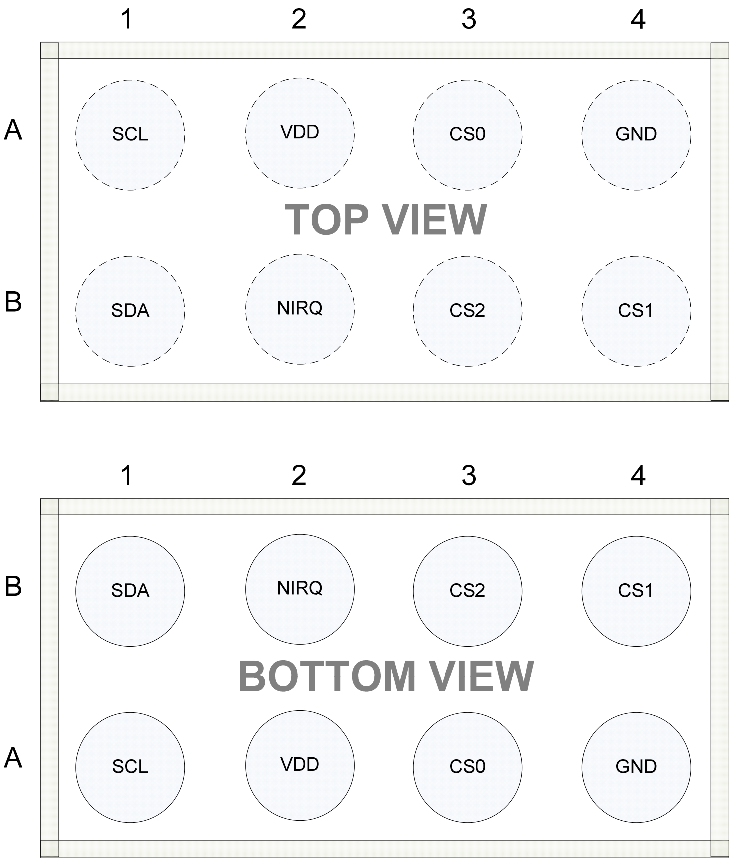

Figure 1: Pin Diagram

1.2 Marking Information

xxxx = Lot Number

Figure 2: Marking Information

1.3 Pin Description

Number	Name	Type	Description
A2	VDD	Power	Power Supply, requires decoupling capacitor.
A4	GND	Ground	Ground
A3	CS0	Analog	Secondary Capacitive Sensor Input
B4	CS1	Analog	Primary Capacitive Sensor Input
B3	CS2	Analog	Primary Capacitive Sensor Input **or** I2C Sub-Address Input.
A1	SCL	Digital Input	I2C Clock, requires pull-up resistor.
B1	SDA	Digital Input/Output	I2C Data, requires pull-up resistor.
B2	NIRQ	Digital Input/Output	Interrupt Output **and** Pause Input, requires pull-up resistor.

Table 1: Pin Description

2 ELECTRICAL CHARACTERISTICS

2.1 Absolute Maximum Ratings

Stresses above the values listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these, or any other conditions beyond the "Operating Conditions", is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability and proper functionality.

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{DD}	-0.5	2.2	V
Pull-up Voltage	V_{PULL}	-0.5	3.9	
Input Voltage (non-supply pins)	V_{IN}	-0.5	V_{DD}+0.3	
Input Current (non-supply pins)	I_{IN}	-10	10	mA
Operating Junction Temperature	T_{JCT}	-40	125	°C
Reflow Temperature	T_{RE}	-	260	
Storage Temperature	T_{STOR}	-50	150	
ESD HBM (ANSI/ESDA/JEDEC JS-001)	ESD_{HBM}	8	-	kV

Table 2: Absolute Maximum Ratings

2.2 Operating Conditions

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{DD}	1.7	2	V
Ambient Temperature	T_A	-40	85	°C

Table 3: Operating Conditions

Note: VDD and VPULL are fully independent, i.e. can be turned ON/OFF separately and in any sequence without creating any leakage current.

2.3 Thermal Characteristics

Parameter	Symbol	Typical	Unit
Thermal Resistance – Junction to Air (Static Airflow)	θ_{JA}	120	°C/W

Table 4: Thermal Characteristics

Note: θ_{JA} is calculated from a package in still air, mounted to 3" x 4.5", 4-layer FR4 PCB per JESD51 standards.

2.4 Electrical Specifications

All values are valid within the full operating conditions unless otherwise specified.
Typical values are given for T_A= +25°C, VDD=1.8V unless otherwise specified.

Parameter	Symbol	Conditions		Min	Typ.	Max	Unit
Current Consumption							
Sleep (no phase enabled)	I_{SLEEP}	Power down. (I2C listening) PHEN = 0000		-	1.75	5	uA
Doze	I_{DOZE}	SCANPERIOD = 400ms FREQ = 100kHz RESOLUTION = 64 PHEN = 0001		-	6	14	
Active	I_{ACTIVE}	SCANPERIOD = 30ms FREQ = 100kHz RESOLUTION = 64 PHEN = 0001		-	22	45	
Capacitive Sensing Interface							
Measurement Range	C_{RANGEL}	AGAIN=1000, GAIN01/23=001	ARANGE01/23 = 0/Small	-	+/-1.325	-	pF
	C_{RANGEH}		ARANGE01/23 = 1/Large	-	+/-2.65	-	pF
Measurement Resolution	N_{BIT}			-	16	-	bits
	C_{RESL}	AGAIN=0110, GAIN01/23=100	ARANGE01/23 = 0/Small	-	0.004	-	fF
	C_{RESH}		ARANGE01/23 = 1/Large	-	0.008	-	fF
Nominal Sampling Frequencies	F_S	Programmable with FREQ01/23		4.63	-	250	kHz
Nominal Scan Periods	T_{SCAN}	Programmable with SCANPERIOD		-*	-	4000	ms
Sampling & Scan Frequencies Trim Accuracy	F_{Trim}	Around Nominal Values. T_A = +25°C, VDD = 1.8V.		-4	-	+4	%
Sampling & Scan Frequencies Temperature Dependency	F_{Temp}	Around Trim Result. Full T_A range, VDD = 1.8V.		-	+/-1	-	%
Sampling & Scan Frequencies VDD Dependency	F_{VDD}	Around Trim Result. T_A = +25°C, Full VDD range.		-	+/-0.6	-	%
External DC Cap. to Ground per Measurement Phase	C_{DC}			-	-	200	pF
Temperature Sensor							
Temperature Sensor Slope	T_{SLOPE}	PROXUSEFUL, GAIN23=001		-	47.5	-	LSB/°C
Outputs: SDA, NIRQ							
Output Low Current	I_{OL04}	VOL ≤ 0.32V		3	-	-	mA
	I_{OL06}	VOL ≤ 0.6V		6	-	-	
Inputs: SCL, SDA, NIRQ							
Input High Voltage	V_{IH}			0.7 x V_{DD}	-	3.6	V
Input Low Voltage	V_{IL}			-0.5	-	0.3 x V_{DD}	
Input Leakage Current	I_L			-1	-	1	uA
Hysteresis	V_{HYS}			0.04 x V_{DD}	-	-	V
Miscellaneous							
Power-up Time	T_{POR}			-	-	1	ms

* Min is achieved when SCANPERIOD=00000 and determined by the total measurement time.

Table 5: Electrical Specifications

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
I2C Timing Specifications (Cf. figure below)						
SCL clock frequency	f_{SCL}		-	-	400	kHz
SCL low period	t_{LOW}		1.3	-	-	us
SCL high period	t_{HIGH}		0.6	-	-	
Data setup time	$t_{SU;DAT}$		0.1	-	-	
Data hold time	$t_{HD;DAT}$		0	-	-	
Repeated start setup time	$t_{SU;STA}$		0.6	-	-	
Start condition hold time	$t_{HD;STA}$		0.6	-	-	
Stop condition setup time	$t_{SU;STO}$		0.6	-	-	
Bus free time between stop and start	t_{BUF}		1.3	-	-	
Data valid time	$t_{VD;DAT}$		-	-	0.9	
Data valid acknowledge time	$t_{VD;ACK}$		-	-	0.9	
Input glitch suppression	t_{SP}	Note 1	-	-	50	ns

Note 1: Minimum glitch amplitude is $0.7V_{DD}$ at High level and Maximum $0.3V_{DD}$ at Low level.

Table 6: I2C Timing Specifications

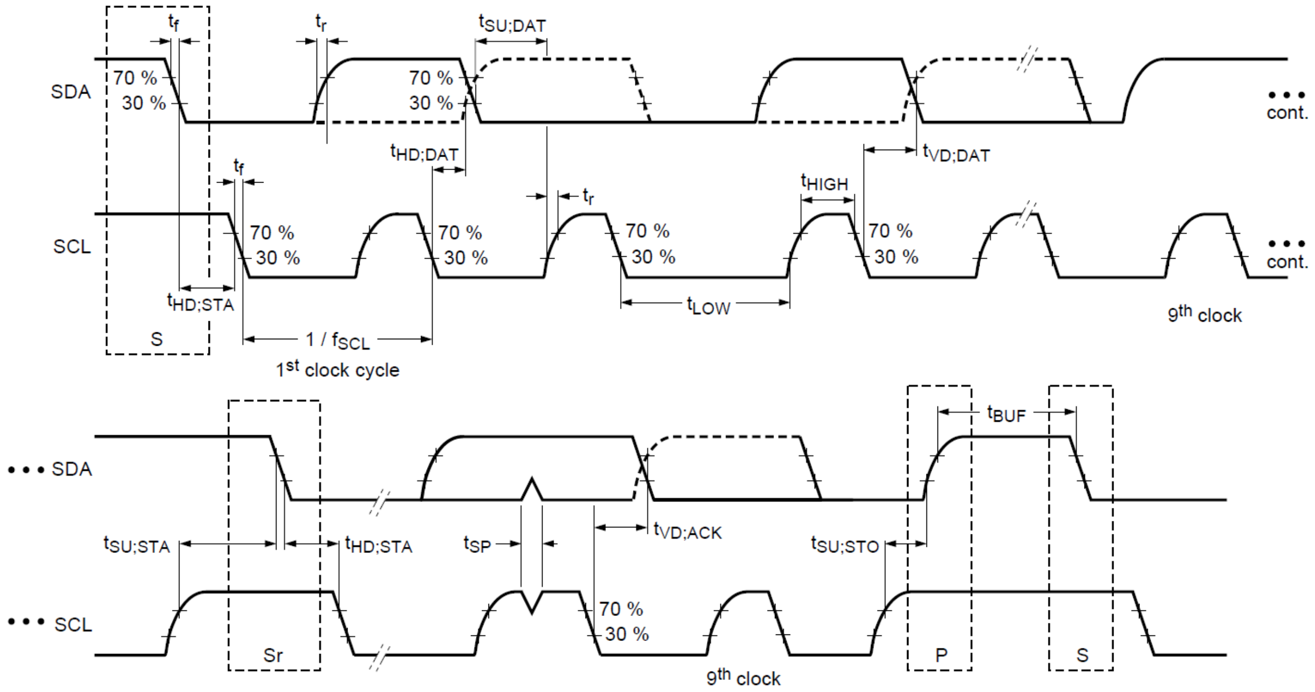

Figure 3: I2C Timing

3 PROXIMITY SENSING INTERFACE

3.1 Introduction

The purpose of the proximity sensing interface is to detect when a conductive object (usually a body part i.e. finger, palm, face, etc) is in the proximity of the system. Note that proximity sensing can be done through the air or through a solid (typically plastic) overlay (also called "touch" sensing).

The chip's proximity sensing interface is based on capacitive sensing technology. An overview is given the in figure below.

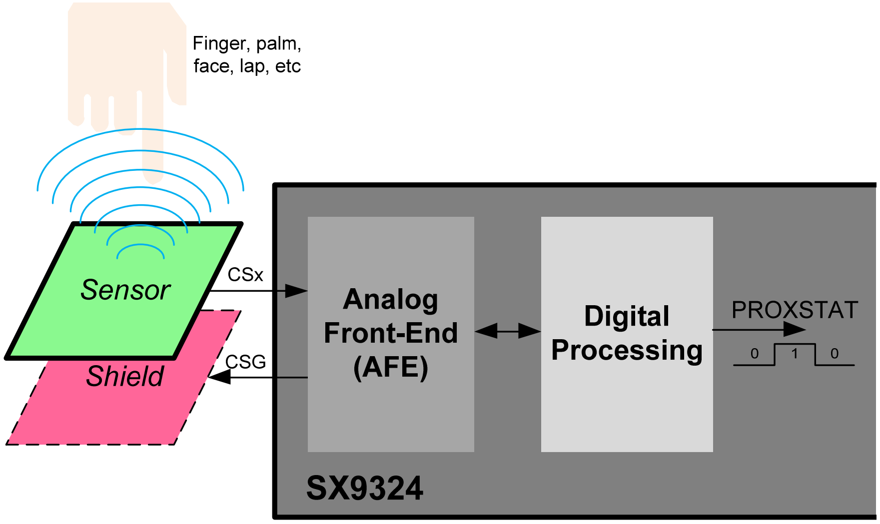

Figure 4: Proximity Sensing Interface Overview

- The sensor can be a simple copper area on a PCB or FPC for example. Its capacitance (to ground) will vary when a conductive object is moving in its proximity.
- The optional shield can also be a simple copper area on a PCB or FPC below/under/around the sensor. It is used to protect the sensor against potential surrounding noise sources and improve its global performance. It also brings directivity to the sensing, for example sensing objects approaching from top only.
- The analog front-end (AFE) performs the raw sensor's capacitance measurement and converts it into a digital value. It also controls the shield. See §3.3 for more details.
- The digital processing block computes the raw capacitance measurement from the AFE and extracts a binary information PROXSTAT corresponding to the proximity status, i.e. object is "Far" or "Close". It also triggers AFE operations (compensation, etc). See §3.4 for more details.

3.2 Scan Period

To save power and since the proximity event is slow by nature, the chip will awake regularly at every programmed scan period (SCANPERIOD) to first sense sequentially each of the enabled phases (PHEN, up to 4) and then process new proximity samples/info. The chip will be in idle mode most of the time. This is illustrated in figure below

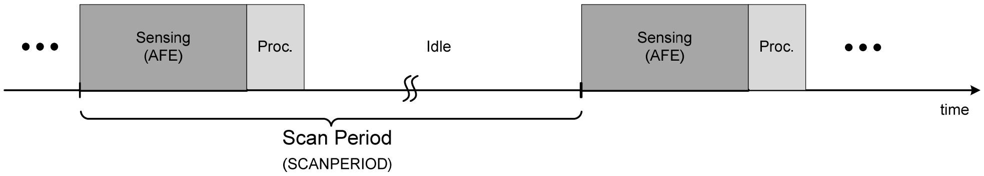

Figure 5: Proximity Sensing Sequencing

The sensing and processing durations vary with the number of phases enabled, the sampling frequency, and the resolution programmed. During the Idle state, the chip's analog circuits are turned off. Upon expiry of the idle timer, a new scan period cycle begins.

The scan period determines the minimum reaction time (actual/final reaction time also depends on debounce and filtering settings) and can be programmed from typ. 2ms to 4s.

3.3 Analog Front-End (AFE)

3.3.1 Capacitive Sensing Basics

Capacitive sensing is the art of measuring a small variation of capacitance in a noisy environment. As mentioned above, the chip's proximity sensing interface is based on capacitive sensing technology. In order to illustrate some of the user choices and compromises required when using this technology it is useful to understand its basic principles.

To illustrate the principle of capacitive sensing we will use the simplest implementation where the sensor is a copper plate on a PCB.

The figure below shows a cross-section and top view of a typical capacitive sensing implementation. The sensor connected to the chip is a simple copper area on top layer of the PCB. It is usually surrounded (shielded) by ground for noise immunity (shield function) but also indirectly couples via the ground areas of the rest of the system (PCB ground traces/planes, housing, etc). For obvious reasons (design, isolation, robustness …) the sensor is stacked behind an overlay which is usually integrated in the housing of the complete system.

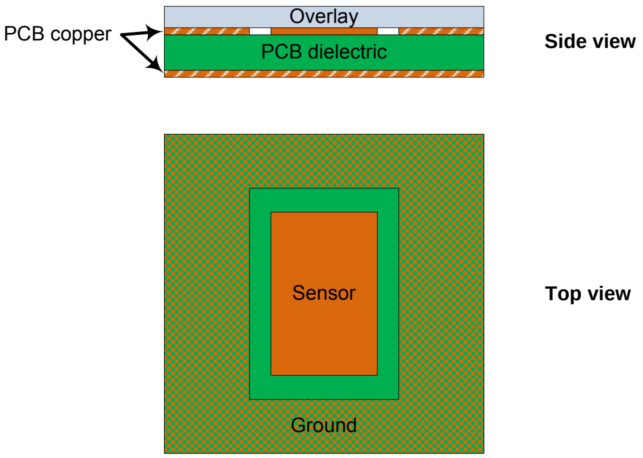

Figure 6: Typical Capacitive Sensing Implementation

When the conductive object to be detected (finger/palm/face, etc) is not present, the sensor only sees an inherent capacitance value C_{Env} created by its electrical field's interaction with the environment, in particular with ground areas.

When the conductive object (finger/palm/face, etc) approaches, the electrical field around the sensor will be modified and the total capacitance seen by the sensor increased by the user capacitance C_{User}. This phenomenon is illustrated in the figure below.

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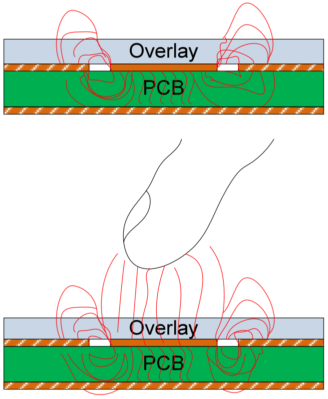


$C_{Sensor} = C_{Env}$

$C_{Sensor} = C_{Env} + C_{User}$

Figure 7: Proximity Effect on Electrical Field and Sensor Capacitance

The challenge of capacitive sensing is to detect this relatively small variation of C_{Sensor} (C_{User} usually contributes for a few percent only) and differentiate it from environmental noise (C_{Env} also slowly varies together with the environment characteristics like temperature, etc). For this purpose, the chip integrates an auto offset compensation mechanism which dynamically monitors and removes the C_{Env} component to extract and process C_{User} only. See §3.3.5 for more details.

In first order, C_{User} can be estimated by the formula below:

$$\boxed{C_{User} = \frac{\varepsilon_0 \cdot \varepsilon_r \cdot A}{d}}$$

A is the common area between the two electrodes hence the common area between the user's finger/palm/face and the sensor.

d is the distance between the two electrodes hence the proximity distance between the user and the system.

ε_0 is the free space permittivity and is equal to 8.85 10e-12 F/m (constant)

ε_r is the dielectric relative permittivity.

Typical permittivity of some common materials is given in the table below.

Material	Typical ε_r
Glass	8
FR4	5
Acrylic Glass	3
Wood	2
Air	**1**

Table 7: Typical Permittivity of Some Common Materials

From the discussions above we can conclude that the most robust and efficient design will be the one that minimizes C_{Env} value and variations while improving C_{User}.

3.3.2 AFE Block Diagram

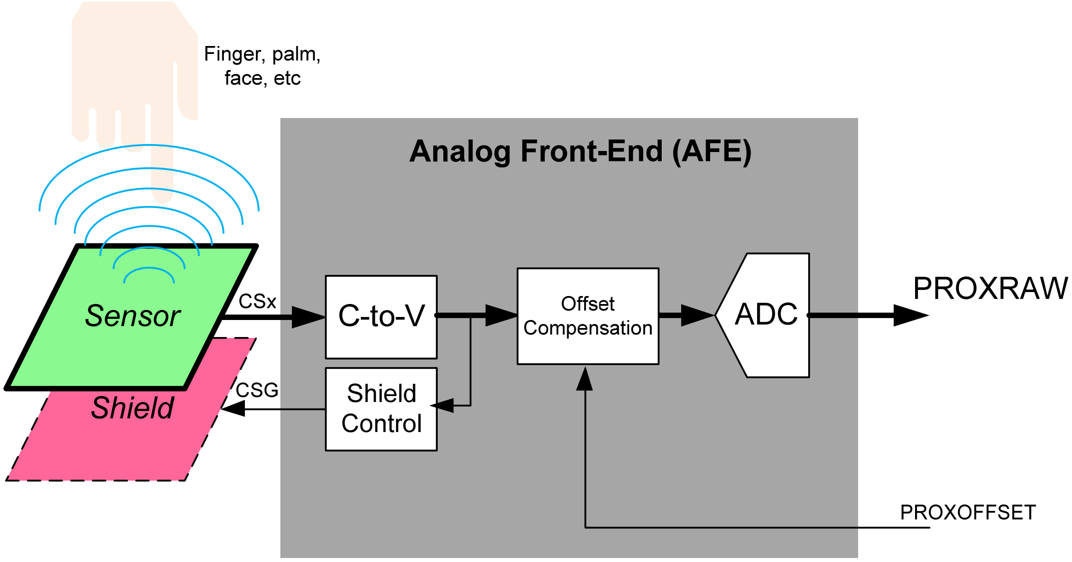


Figure 8: Analog Front-End Block Diagram

3.3.3 Capacitance-to-Voltage Conversion (C-to-V)

The sensitivity of the interface is determined by RANGE and GAIN parameters.

FREQ defines the operating frequency of the interface and should be set as high as possible for power consumption reasons.

3.3.4 Shield Control

When not being measured, any CSx pin can be used as a shield (CSG).

3.3.5 Offset Compensation

Offset compensation consists of performing a one-time measurement of C_{Env} and subtracting from the total capacitance C_{Sensor} in order to feed the ADC with the closest contribution of C_{User} only.

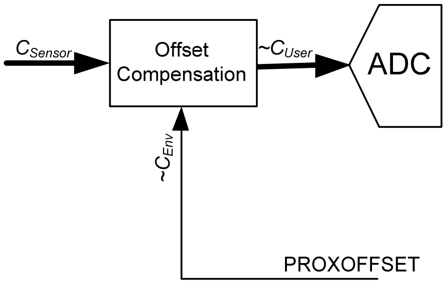


Figure 9: Offset Compensation Block Diagram

The ADC input C_{User} is the total capacitance C_{Sensor} to which C_{Env} is subtracted.

There are three possible compensation sources which are illustrated in the figure below. When set to 1 by any of these sources, COMPSTAT will only be reset once the compensation is completed.

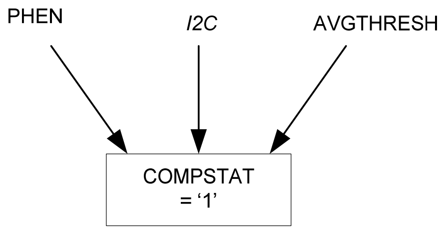


Figure 10: Compensation Request Sources

- PHEN: a compensation is automatically requested for a measurement phase on the rising edge of its PHEN bit.
- I2C: a compensation for one or more phases can be manually requested anytime by the host through I2C interface by writing a 1 into COMPSTAT bit(s).
- AVGTHRESH: a compensation for the relevant phase only, can be automatically requested if it is detected that C_{Env} has drifted beyond a predefined range programmed by the host.

Please note that the compensation request flag can be set anytime but the compensation itself is always done at the beginning of a scan period to keep all parameters coherent.
Also, when compensation occurs, PROXDIFF is reset and hence all compensated phases' PROXSTAT flags turn OFF (i.e. no proximity detected) independently from the user's potential actual presence (except if start-up detection is enabled).

3.3.6 Analog-to-Digital Conversion (ADC)

An ADC is used to convert the analog capacitance information into a digital word PROXRAW.

3.4 Digital Processing

3.4.1 Overview

The main purpose of the digital processing block is to convert the raw capacitance information coming from the AFE (PROXRAW) into a robust and reliable digital flag (PROXSTAT) indicating if something is within range of the proximity sensor.

The offset compensation performed in the AFE is a one-time measurement. However, the environment capacitance C_{Env} may vary with time (temperature, nearby objects, etc). Hence, in order to get the best estimation of C_{User} (PROXDIFF), the digital processing block dynamically tracks and subtracts C_{Env} variations. This is performed by filtering PROXUSEFUL to extract its slow variations (PROXAVG).

PROXDIFF is then compared to user programmable threshold (PROXTHRESH) to extract PROXSTAT flag.

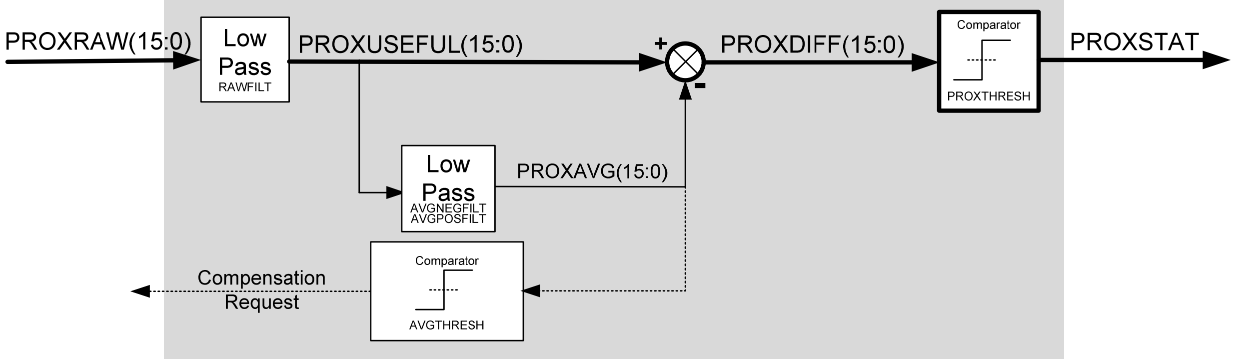


Figure 11: Digital Processing Block Diagram

The digital processor sequence (for all enabled channels) is illustrated in figure below. At every scan period wake-up, the block updates sequentially PROXRAW, PROXUSEFUL, PROXAVG, PROXDIFF and PROXSTAT before going back to Idle mode.

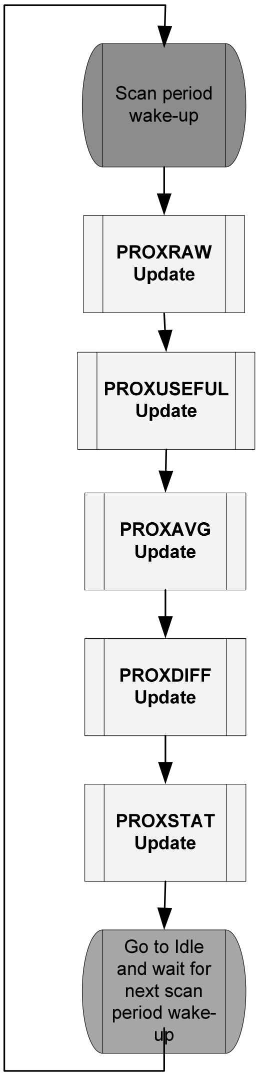


Figure 12: Digital Processor Sequence

The digital processing block also updates COMPSTAT (set when compensation is currently pending execution or completion).

3.4.2 PROXRAW Update

PROXRAW update consists mainly of starting the AFE and waiting for the new PROXRAW values (one for each phase) to be ready. If compensation was pending it is performed first.

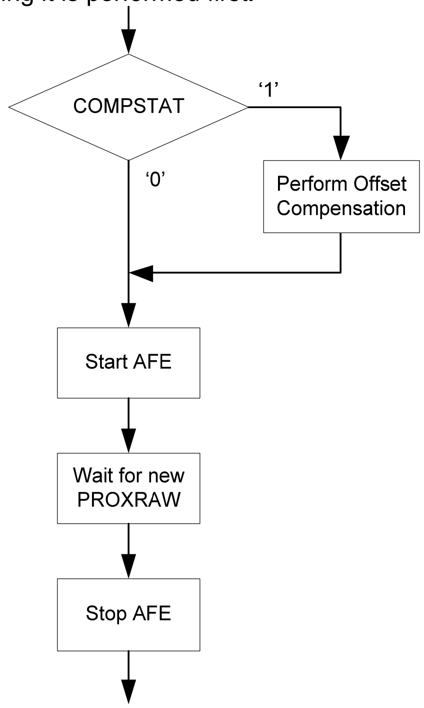


Figure 13: ProxRaw Update

Note that PROXRAW is not available in the "Phase Data Readback" section of the registers. If needed, it can be observed by disabling the raw filter (RAWFILT) and reading PROXUSEFUL.

3.4.3 PROXUSEFUL Update

PROXUSEFUL update consists of filtering PROXRAW upfront to remove its high frequencies components (system noise, interferer, etc) and extract only user activity (few Hz max) and slow environment changes.

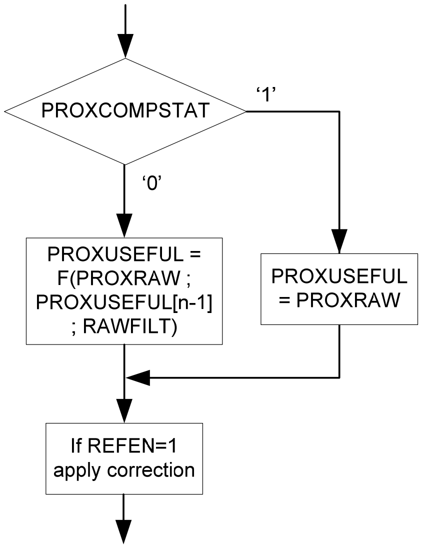


Figure 14: PROXUSEFUL Update

F(PROXRAW ; PROXUSEFUL[n-1] ; RAWFILT) = (1 - RAWFILT).PROXRAW + RAWFILT.PROXUSEFUL[n-1]

3.4.4 PROXAVG Update

PROXAVG update consists of averaging PROXUSEFUL to ignore its “fast” variations (i.e. user finger/palm/hand) and extract only the very slow variations of environment capacitance C_{Env}.

One can program a debounced threshold (AVGTHRESH/AVGDEB) to define a range within which PROXAVG can vary without triggering compensation (i.e. small acceptable environment drift).

Large positive values of PROXUSEFUL are considered as normal (user finger/hand/head) but large negative values are considered abnormal and should be compensated quickly. For this purpose, the averaging filter coefficient can be set independently for positive and negative variations via AVGPOSFILT and AVGNEGFILT. Typically, AVGPOSFILT > AVGNEGFILT to filter out (abnormal) negative events faster.

To prevent PROXAVG from being “corrupted” by user activity (it should only reflect environmental changes) it is frozen when proximity is detected.

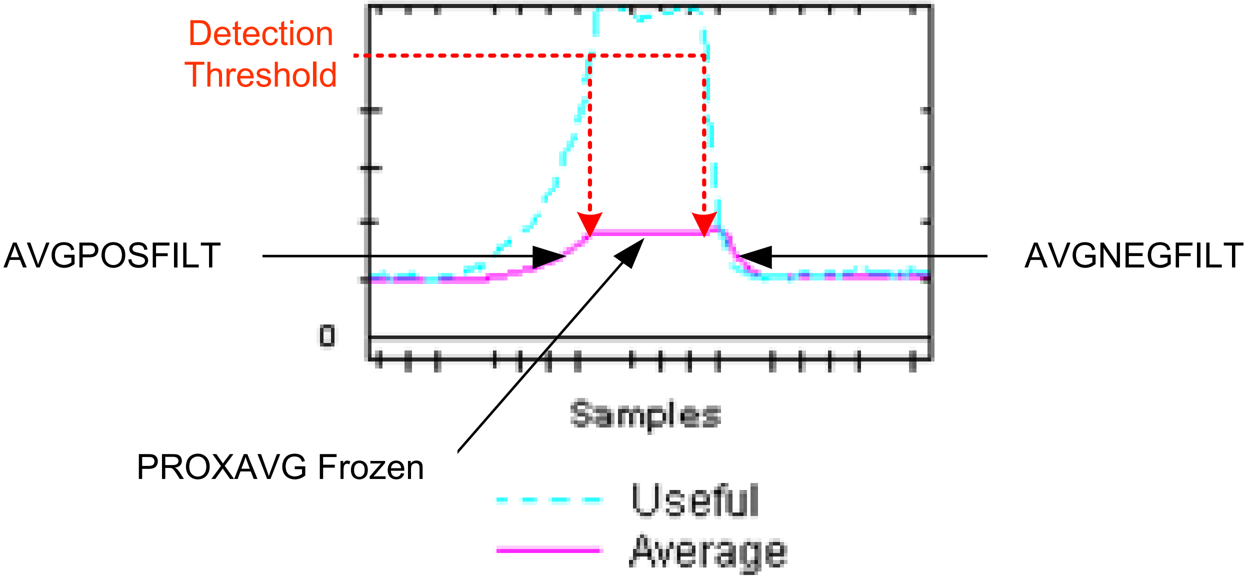


Figure 15: ProxAvg vs Proximity Event

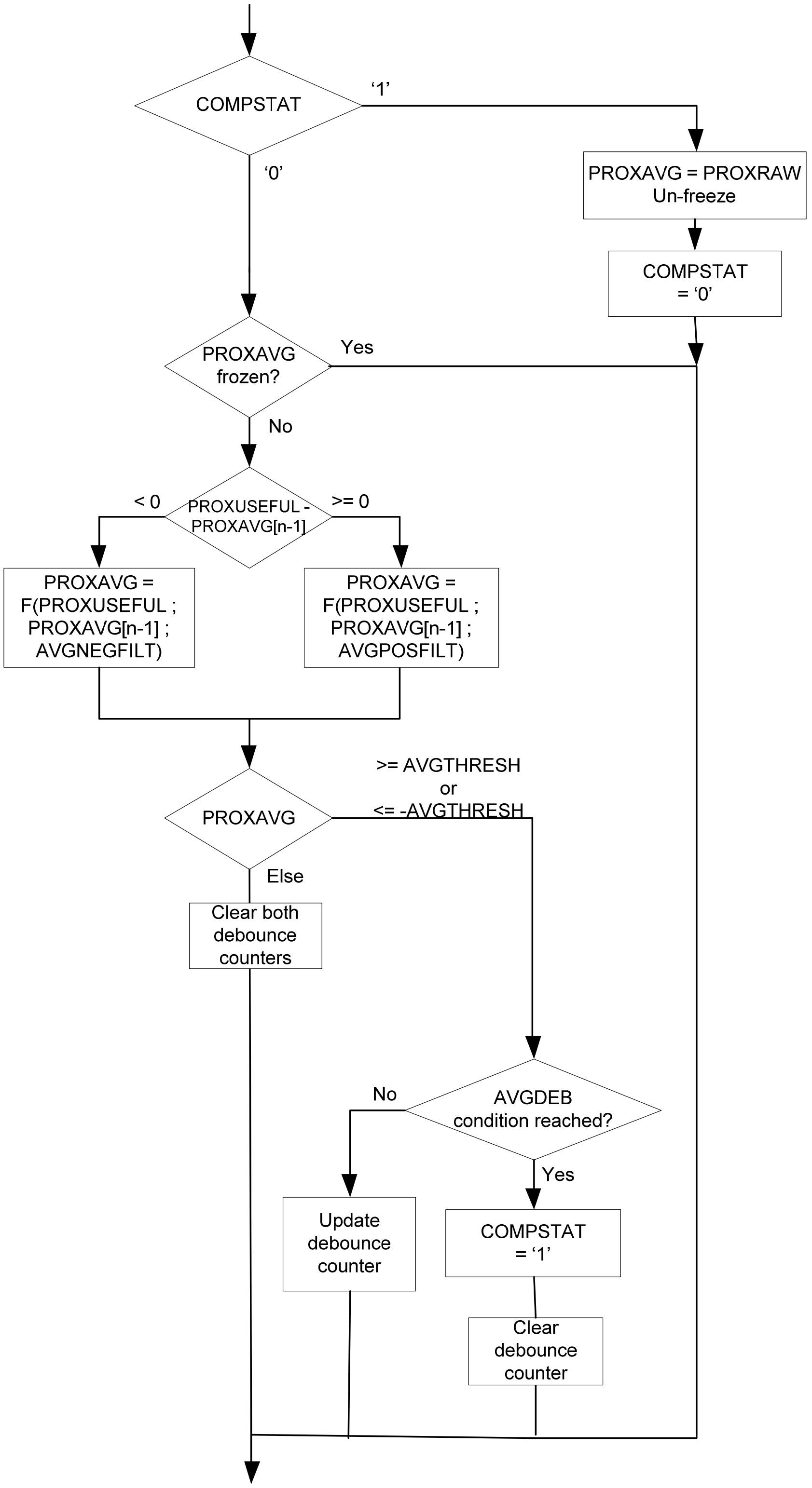


Figure 16: ProxAvg Update

F(PROXUSEFUL ; PROXAVG[n-1] ; AVGxxxFILT) = (1 - AVGxxxFILT).PROXUSEFUL + AVGxxxFILT.PROXAVG[n-1]

xxx = POS or NEG

3.4.5 PROXDIFF Update

PROXDIFF update consists of the complementary operation i.e. subtracting PROXAVG to PROXUSEFUL to ignore slow capacitances variations (C_{Env}) and extract only user related variations i.e. C_{User}.

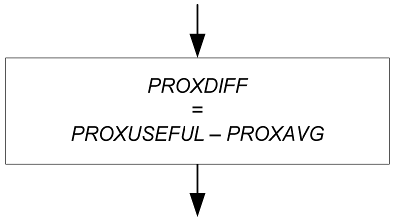


Figure 17: ProxDiff Update

3.4.6 PROXSTAT Update

PROXSTAT update consists of taking PROXDIFF information (C_{User}), comparing it with a user programmable threshold PROXTHRESH and finally updating PROXSTAT accordingly. When PROXSTAT=1, PROXAVG is typically frozen to prevent the user proximity signal from being absorbed into C_{Env}.

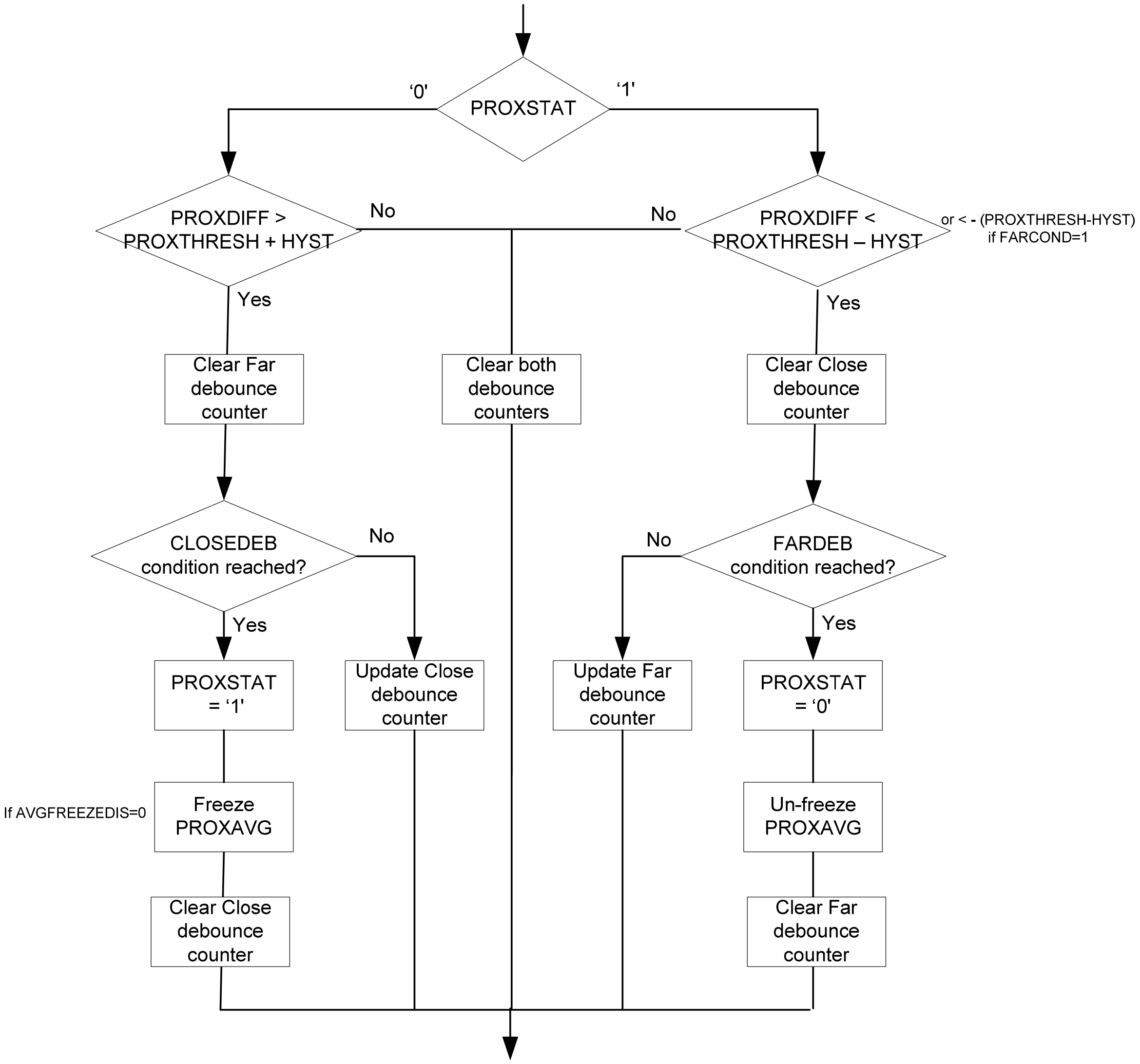


Figure 18: PROXSTAT Update

3.5 Host Operation

An interrupt can be triggered when the user is detected as “close” (in range), detected as “far” (out of range), or both (CLOSEANYIRQEN, FARANYIRQEN).

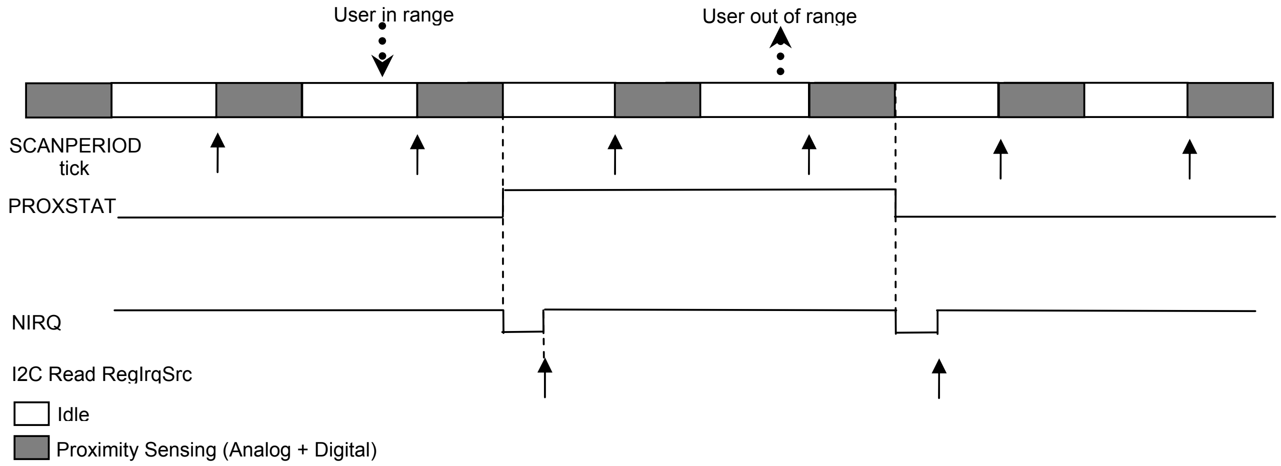


Figure 19: Proximity Sensing Host Operation (Monitoring Close/Far Events)

An interrupt can also be triggered at the end of each scan period’s conversion, indicating to the host when the proximity sensing block is running (CONVDONEIRQEN). This may be used by the host to synchronize noisy system operations or to read phase data (PROXUSEFUL, PROXAVG, and PROXDIFF) synchronously for monitoring purposes.

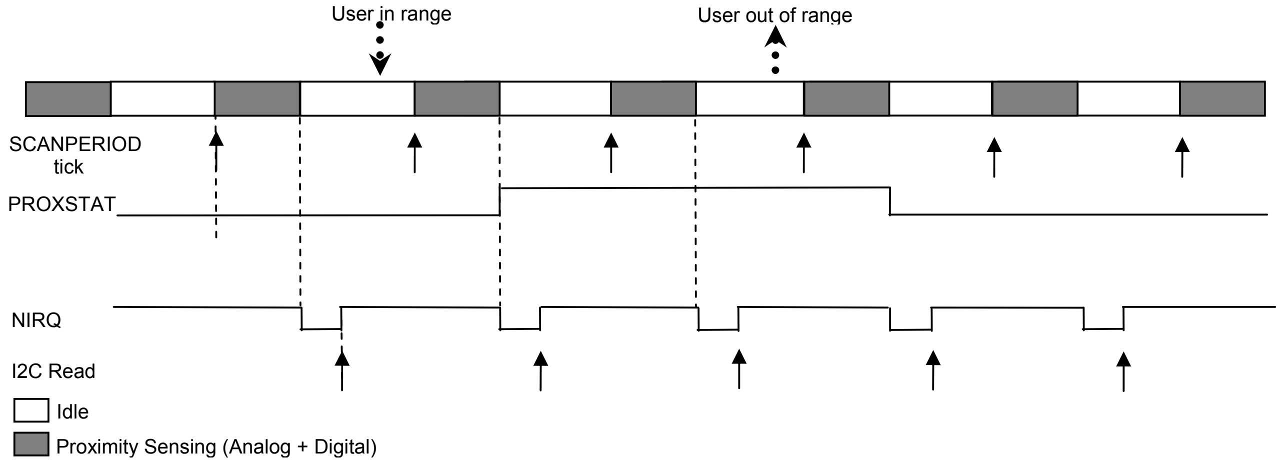


Figure 20: Proximity Sensing Host Operation (Monitoring Conversion Events)

In both cases above, an interrupt can also be triggered at the end of compensation (COMPDONEIRQEN).

3.6 Operational Modes

3.6.1 Active

Active mode has short scan periods, typically 100ms. In this mode, all enabled phases are scanned and information data is processed within this interval. The Active scan period is user configurable (SCANPERIOD).

3.6.2 Doze

In some applications, the reaction/sensing time needs to be fast when the user is present (proximity detected), but can be slow when no detection has occurred for some time.

The Doze mode, when enabled (DOZEPERIOD), allows the chip to automatically switch between a fast scan period (SCANPERIOD) during proximity detection and a slow scan period (DOZEPERIOD) when no proximity is detected. This enables a lower average power consumption at the expense of longer reaction times.

As soon as proximity is detected on any phase, the chip will automatically switch to Active mode. Conversely when it has not detected an object for DOZEPERIOD, it will automatically switch to Doze mode.

3.6.3 Sleep

Sleep mode can be entered by disabling all phases (PHEN=0000). It places the chip in its lowest power mode, with scanning completely disabled and idle period set to continuous. In this mode, only the I2C serial bus is active. Enabling any phase will make the chip leave Sleep mode (for Doze if enabled, else Active mode).

Additionally, Sleep mode can also be entered by using PAUSECTRL, PAUSEIRQEN and PAUSEPINEN.
But unlike using PHEN, this will not generate any compensation when Active mode is re-entered.

4 SMART ENGINE FOR SAR

4.1 Introduction

In addition to the proximity sensing interface, the SX9324 also embeds the world's first smart engine for SAR which is able to discriminate **at a distance** between proximity generated by low permittivity (table) and high permittivity objects (body).

This is typically useful for Specific Absorption Rate (SAR) applications in portable devices (tablets, cellphones, etc) where international regulations (FCC, ETSI, etc) impose RF power reductions in the presence of human body for safety reasons.

Typical capacitive sensing solutions are not able to discriminate between proximity detection generated when a tablet (for example) is sitting on a table (no need to reduce RF power) versus when it is sitting on the user's lap (need to reduce RF power) resulting in RF power and hence user's experience reduced significantly even when it is not needed.

The SX9324's smart engine for SAR enables RF power reduction only in the presence of body (high permittivity material) and hence offering significantly better user experience while still conforming to safety regulations.

4.2 Sensor Design

In order to use the SX9324's smart engine for SAR, the sensors design must follow a few rules which are described in this section.

A smart SAR sensor is physically made of two sensors (outer and inner) connected to pins CS1 and CS2. In the drawing below, the dark areas represent copper (conductor) and the light areas represents a non-conductor (spacing between the two copper areas).

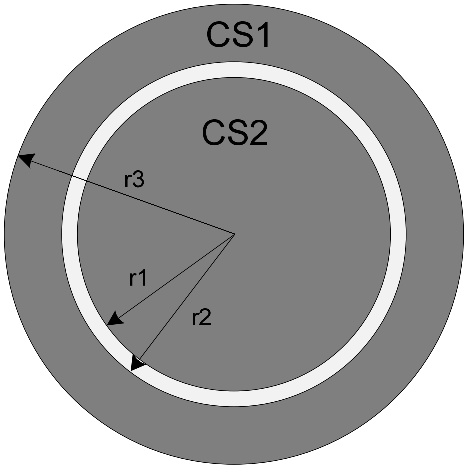


Figure 21: Typical Smart SAR Capacitive Sensor

IMPORTANT: For the Smart Engine for SAR to work properly, PH1 should be used/programmed for measuring the outer sensor, and PH2 for the inner sensor.

For best performance/robustness, the copper areas of CS1 and CS2 pads must be designed to be equal (as equal as the FPC/PCB technology tolerance allows).

The figure above illustrates an example of circular shape but smart SAR sensors can of course be designed in a variety of shapes (square, rectangular) depending on the physical/mechanical constraints of the system.

4.3 Processing

The smart engine for SAR is active when SAREN=1 and PROXSTAT1&2 (ignoring STEADYCOND impact) are set (i.e. both CS1 and CS2 sensors have detected proximity).

When active, the smart engine for SAR computes a real time SAR threshold value a*PH2+b and updates BODYSTAT1&2 accordingly (both set to 1 when PH1 > (SARSLOPE * PH2 + SAROFFSET) **OR** one of the two sensors is saturated i.e. > BODYTHRESH1/2).

Hysteresis and debounce mechanisms (SARHYST and SARDEB) can also be enabled on top of the threshold.

BODYSTAT1/2 (and TABLESTAT1/2, Cf. below) are **only** updated when PROXAVG is frozen (i.e. AVGFREEZEDIS=0, or AVGFREEZEDIS=1 up to 4xAVGDEB).

TABLESTAT1/2 are built from BODYSTAT1/2 and PROXSTAT1/2 accordingly:

- When PROXSTAT1/2=0 => Set to 0

- Else, set to [NOT BODYSTAT12]

5 I2C INTERFACE

5.1 Introduction

The I2C implemented on the chip and used by the host to interact with it is compliant with:

- Standard (100kb/s) and fast mode (400kb/s)
- Slave mode
- 7-bit address
  - Default is 0x28 (b0101000)
  - **Bit 2** will be set if CS2 is grounded during reset (power-up or software).

    Important: While CS2 is externally grounded, it cannot be used for capacitive sensing; **all** relevant bits in AFEPHx and CSIDLESLEEP should be set to HZ or GND.

The host can use the I2C to read and write data at any time, and these changes are effective immediately. Therefore the user may have to disable/enable phases(s) or perform a compensation for the new settings to apply properly.

5.2 I2C Write

The format of the I2C write is given in the figure below. After the start condition [S], the slave address (SA) is sent, followed by an eighth bit (‘0’) indicating a Write. The chip then Acknowledges [A] that it is being addressed, and the master sends an 8-bit Data Byte consisting of Register Address (RA). The Slave Acknowledges [A] and the master sends the appropriate 8-bit Data Byte (WD0). Again the Slave Acknowledges [A]. In case the master needs to write more data, a succeeding 8-bit Data Byte will follow (WD1), acknowledged by the slave [A]. This sequence will be repeated until the master terminates the transfer with the Stop condition [P].

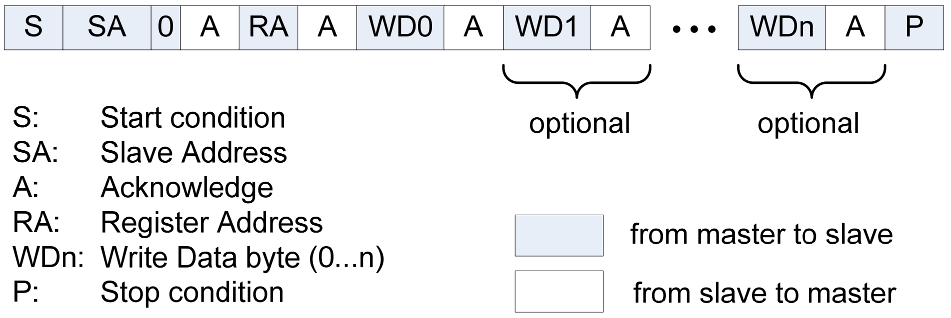


Figure 22: I2C Write

The register address is incremented automatically when successive register data (WD1...WDn) is supplied by the master.

5.3 I2C Read

The format of the main I2C read is given in the figure below. After the start condition [S], the slave address (SA) is sent, followed by an eighth bit (‘0’) indicating a Write. The SX9324 then Acknowledges [A] that it is being addressed, and the Master responds with an 8-bit Data consisting of the Register Address (RA). The Slave Acknowledges [A] and the master sends the Repeated Start Condition [Sr]. Once again, the slave address (SA) is sent, followed by an eighth bit (‘1’) indicating a Read. The SX9324 responds with an Acknowledge [A] and the read Data byte (RD0). If the master needs to read more data it will acknowledge [A] and the chip will send the next read byte (RD1). This sequence can be repeated until the master terminates with a NACK [N] followed by a stop [P].

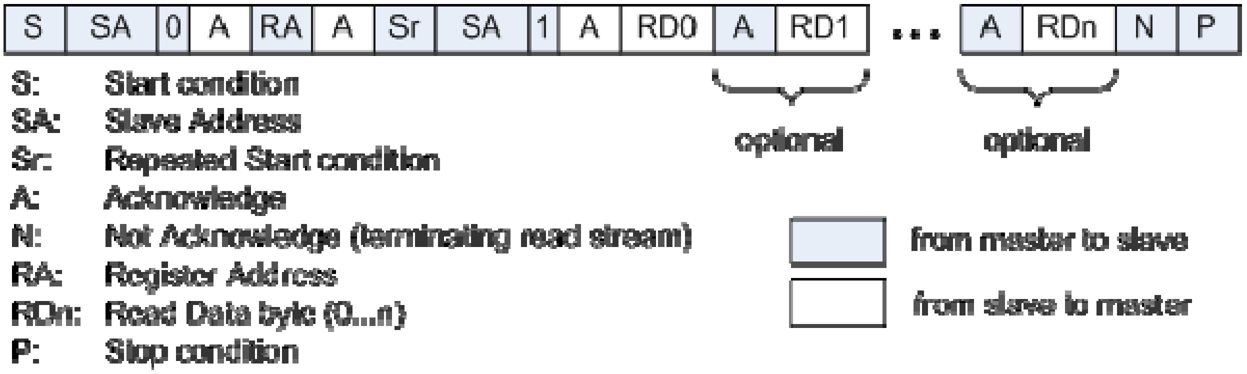


Figure 23: I2C Read

The register address is incremented automatically when successive register data (RD1...RDn) is retrieved by the master.

An “immediate” read can also be performed by the master. In this procedure data is transmitted from the slave to the master from the register address currently pointed to (last accessed from previous read or write). The slave address is sent followed by an eighth bit (‘1’) indicating a Read. The SX9324 responds with an Acknowledge [A] and the read Data byte (RD0). If the master needs to read more data it will acknowledge [A] and the chip will send the next read byte (RD1). This sequence can be repeated until the master terminates with a NACK [N] followed by a stop [P].

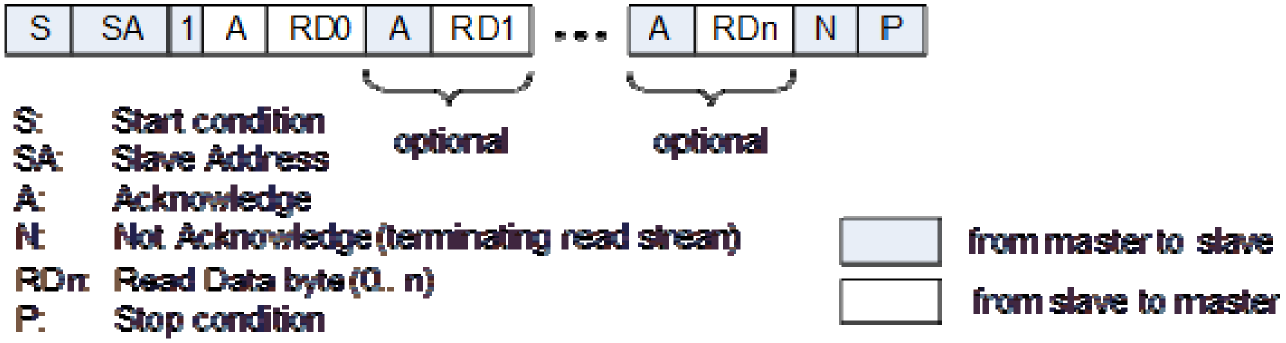


Figure 24: I2C Immediate Read

The register address is incremented automatically when successive register data (RD1...RDn) is retrieved by the master.

6 RESET

6.1 Power-up

During a power-up condition, and if IRQFUNCTION=00000, the NIRQ output is HIGH until V_{DD} has met its minimum input voltage requirements and a T_{POR} time has expired upon which, NIRQ asserts to a LOW condition indicating that the chip is initialized. The host must perform an I2C read of RegIrqSrc to clear this NIRQ status. The chip is then ready for normal I2C communication and is operational.

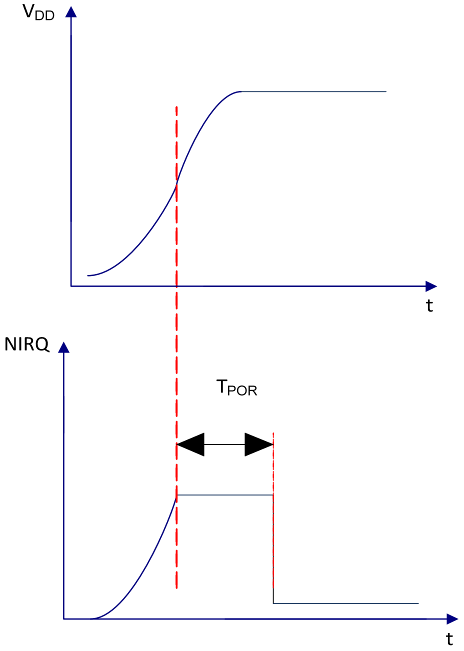


Figure 25: Power-up vs. NIRQ

6.2 Software Reset

The host can also perform a reset anytime by writing 0xDE into RegReset. The NIRQ output will be asserted LOW and the host is required to perform an I2C read to clear this NIRQ status.

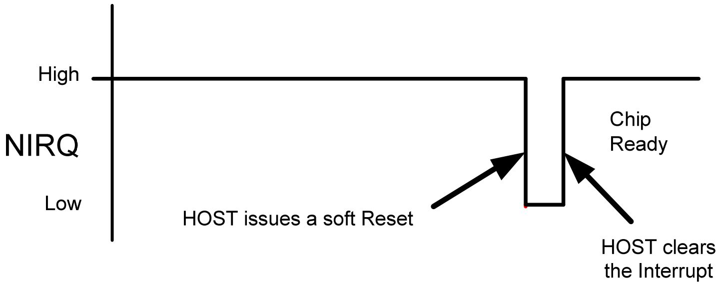


Figure 26: Software Reset

7 INTERRUPT

7.1 Power-up

During initial power-up, the NIRQ output is HIGH. Once the chip's internal power-up sequence has completed, NIRQ is asserted LOW, signaling that the chip is ready. The host must perform a read to RegIrqSrc to acknowledge and the chip will clear the interrupt and release the NIRQ line.

7.2 Assertion and Clearing

Except for Reset, the NIRQ pin can be asserted once per scan period in the processing phase. It will be automatically cleared after the host performs a read of RegIrqSrc (which content will be cleared as well).

8 REGISTERS

The registers below allow the user to do full parameter customization and their values must be set in accordance with the latest application notes available (please contact your Semtech representative).

Please note the following:
a) Addresses not listed above are reserved and should not be written.
b) Reserved bits should be left to their default value unless otherwise specified.

Addr	Name	Variable	Bits	RW	Default	Description
Interrupt and Status						
0x00	RegIrqSrc	RESETIRQ	7	R	1	Reset interrupt source status. (i.e. reset occurred)
		CLOSEANYIRQ	6	R	0	Close interrupt source status. (i.e. any PROXSTAT rising edge)
		FARANYIRQ	5	R	0	Far interrupt source status. (i.e. any PROXSTAT falling edge)
		COMPDONEIRQ	4	R	0	Compensation interrupt source status. (i.e. any COMPSTAT falling edge)
		CONVDONEIRQ	3	R	0	Conversion interrupt source status. (i.e. CONVSTAT falling edge)
		PROG2IRQ	2	R	0	As defined by PROG2IRQCFG.
		PROG1IRQ	1	R	0	As defined by PROG1IRQCFG.
		PROG0IRQ	0	R	0	As defined by PROG0IRQCFG.
0x01	RegStat0	STEADYSTAT	7:4	R	0000	Indicates if the Diff (or Useful, Cf. STEADYEN) value of the corresponding phase is steady. (i.e. set when value varied by max STEADYMAXVAR LSBs (peak-peak) within the last STEADYMINTIME sliding window; Cf. UNSTEADYDEB for clearing) [3:0] = [PH3, PH2, PH1, PH0]
		PROXSTAT	3:0	R	0000	Indicates if proximity is currently being detected for the corresponding phase. (i.e. set when phase's PROXDIFF value is above detection threshold; Cf. FARCOND for clearing) [3:0] = [PH3, PH2, PH1, PH0]
0x02	RegStat1	TABLESTAT	7:4	R	0000	When PROXSTAT=1 (ignoring STEADYCOND impact), indicates if the object detected by the current phase is recognized as a table. (i.e. phase's PROXDIFF value is within TABLETHRESH; HYST and CLOSEDEB/FARDEB apply). When PROXSTAT=0 (ignoring STEADYCOND impact), set to 0. [3:0] = [PH3, PH2, PH1, PH0]
		BODYSTAT	3:0	R	0000	When PROXSTAT=1 (ignoring STEADYCOND impact), indicates if the object detected by the current phase is recognized as a human body. (i.e. phase's PROXDIFF value exceeds BODYTHRESH; HYST and CLOSEDEB/FARDEB apply). When PROXSTAT=0 (ignoring STEADYCOND impact), set to 0. [3:0] = [PH3, PH2, PH1, PH0]
0x03	RegStat2	FAILSTAT	7:4	R	0000	Indicates if a failure (abnormal PROXOFFSET value,

						Cf. FAILTHRESH) is detected for the corresponding phase. [3:0] = [PH3, PH2, PH1, PH0]
		COMPSTAT	3:0	R	0000	Indicates which phase has compensation pending/running. [3:0] = [PH3, PH2, PH1, PH0] Writing a bit to 1 will trigger a compensation for the corresponding phase.
0x04	RegStat3	CONVSTAT	7	R	0	Set while new data is being measured.
		SMARTSARSTAT	6	R	0	Smart SAR flag as defined in SARSTATCONFIG.
		STARTUPSTAT	5	R	0	Set while start-up detection is forcing PROXSTAT=1.
		TEMPSTAT	4	R	0	Set while new temperature data is being measured.
		FAILSTATANY	3	R	0	Set while any of the FAILSTAT bits is set.
		STEADYSTATALL	2	R	0	Set while all enabled phases are steady.
		PROXSTATANY	1	R	0	Set while any of the PROXSTAT bits is set.
		PROXSTAT12	0	R	0	Set while both PROXSTAT1 and PROXSTAT2 are set.
0x05	RegIrqMsk	Reserved	7		0	
		CLOSEANYIRQEN	6	RW	1	Enables the close interrupt (Any).
		FARANYIRQEN	5	RW	1	Enables the far interrupt (Any).
		COMPDONEIRQEN	4	RW	0	Enables the compensation interrupt (Any).
		CONVDONEIRQEN	3	RW	0	Enables the conversion interrupt.
		PROG2IRQEN	2	RW	0	Enables the PROG2 interrupt.
		PROG1IRQEN	1	RW	0	Enables the PROG1 interrupt.
		PROG0IRQEN	0	RW	0	Enables the PROG0 interrupt.
0x06	RegIrqCfg0	Reserved	7		0	
		COMPSATIRQDIS	6	RW	0	0: Off 1: COMP interrupt is NOT issued (COMPSTAT not cleared) if PROXOFFSET is saturated.
		PROG2IRQCFG	5:4	RW	00	00: Any BODYSTAT/TABLESTAT rising or falling edge. 01: Any BODYSTAT/TABLESTAT/FAILSTAT rising or falling edge. 10: CONVSTAT rising edge. 11: TEMPSTAT falling edge.
		PROG1IRQCFG	3:2	RW	00	00: Any STEADYSTAT rising or falling edge. 01: Any STEADYSTAT rising edge. 10: Any STEADYSTAT falling edge. 11: STEADYSTATALL rising or falling edge.
		PROG0IRQCFG	1:0	RW	00	00: Any FAILSTAT rising or falling edge. 01: STARTUPSTAT rising or falling edge. 10: SMARTSARSTAT rising or falling edge. 11: PROXSTAT12 rising or falling edge.
0x07	RegIrqCfg1	FAILCOND	7	RW	1	0: Off 1: While any FAILSTAT bit is set, PROX/BODY/TABLE statuses for that phase are respectively set to 1/1/0 independently from their current value.

<table>
<tr><td></td><td></td><td>IRQPOLARITY</td><td>6</td><td>RW</td><td>0</td><td>Defines the NIRQ pin polarity:
0: Normal (Typ.)
1: Inverted

Normal polarity is “Active Low” when IRQFUNCTION=00000, else “Active High”.</td></tr>
<tr><td></td><td></td><td>IRQFUNCTION</td><td>5:0</td><td>RW</td><td>000000</td><td>Defines the NIRQ pin function:
000000: Interrupt (Typ.)
000001: PROXSTAT0
000010: PROXSTAT1
000011: PROXSTAT2
000100: PROXSTAT3
000101: STEADYSTAT0
000110: STEADYSTAT1
000111: STEADYSTAT2
001000: STEADYSTAT3
001001: TABLESTAT0
001010: TABLESTAT1
001011: TABLESTAT2
001100: TABLESTAT3
001101: BODYSTAT0
001110: BODYSTAT1
001111: BODYSTAT2
010000: BODYSTAT3
010001: FAILSTAT0
010010: FAILSTAT1
010011: FAILSTAT2
010100: FAILSTAT3
010101: COMPSTAT (Any)
010110: CONVSTAT
010111: SMARTSARSTAT
011000: STARTUPSTAT
011001: TEMPSTAT
011010: FAILSTATANY
011011: STEADYSTATALL
011100: PROXSTATANY
011101: PROXSTAT12
011110: High (not impacted by IRQPOLARITY)
011111: Low (not impacted by IRQPOLARITY)
100000: NOT(PROXSTATANY)
100001: PROXSTAT0 && [((NOT(TABLE1||TABLE2||BODY1||BODY2)) || ((NOT(STEADY1)&&BODY1)|| (NOT(STEADY2)&&BODY2))]
100010: PROXSTAT0 && [((NOT(TABLE1||TABLE2||BODY1||BODY2)) || ((BODY1)||(BODY2))]
100011: [NOT(STEADY1) && BODY1] || [NOT(STEADY2) && BODY2]
100100: BODY1 || BODY2
100101: PROXSTAT0 || PROXSTAT1
100110: PROXSTAT0 || PROXSTAT3</td></tr>
</table>

						100111: PROXSTAT0 || PROXSTAT2 101000: PROXSTAT0 || PROXSTAT1 || PROXSTAT2 101001: PROXSTAT2 || PROXSTAT3 Else: Reserved
0x08	RegIrqCfg2	Reserved	7:6		00	
		STEADYCOND23	5:3	RW	000	Enables steady condition for phases 2/3 status flags. [2:0]=[PROXSTAT2/3, BODYSTAT2/3, TABLESTAT2/3] 0: Off 1: On, prox/body/table status flags are set only if the corresponding STEADYSTAT is set also (logic AND). Note that bit2/MSB should not be set if STEADYEN=01
		STEADYCOND01	2:0	RW	000	Enables steady condition for phases 0/1 status flags. (Cf. STEADYCOND23)
General Control						
0x10	RegGnrlCtrl0	PAUSEIRQEN	7	RW	0	Enables automatic Sleep(pause) mode while NIRQ pin is set active(Cf. IRQPOLARITY) by our chip: 0: Off 1: On Note that before going to Sleep, any pending scan period measurements are completed (unlike PHEN). Also, no compensation is performed when Sleep mode is exited (unlike PHEN).
		DOZEPERIOD	6:5	RW	00	Enables Doze mode and defines its scan period: 00: Off 01: 4x SCANPERIOD 10: 8x SCANPERIOD 11: 16x SCANPERIOD When SCANPERIOD=0000, 30ms is used to calculate DOZEPERIOD.
		SCANPERIOD	4:0	RW	10110	Defines the Active scan period: 00000: Min (no idle time) 00001: 2 ms 00010: 4 ms 00011: 6 ms 00100: 8 ms 00101: 10 ms 00110: 14 ms 00111: 18 ms 01000: 22 ms 01001: 26 ms 01010: 30 ms 01011: 34 ms 01100: 38 ms 01101: 42 ms 01110: 46 ms 01111: 50 ms 10000: 56 ms 10001: 62 ms 10010: 68 ms 10011: 74 ms 10100: 80 ms

						10101: 90 ms 10110: 100 ms (Typ.) 10111: 200 ms 11000: 300 ms 11001: 400 ms 11010: 600 ms 11011: 800 ms 11100: 1 s 11101: 2 s 11110: 3 s 11111: 4 s Note that these are the nominal values, Cf. fTrim/fTemp/fVDD in electrical specifications. Low values will allow faster reaction time while high values will provide lower power consumption.
0x11	RegGnrlCtrl1	SCANPERIOD23	7:6	RW	00	Enables different Active scan period for phases 2/3: 00: Off (i.e. SCANPERIOD, same as phases 0/1) 01: 4x SCANPERIOD 10: 8x SCANPERIOD 11: 16x SCANPERIOD
		PAUSECTRL	5	RW	1	Allows to pause the chip manually via I2C: 1->0: Completes any pending scan period measurements and then goes to Sleep. 0->1: Resumes measurements normally at every scan period.
		PAUSEPINEN	4	RW	0	Enables automatic Sleep(pause) mode while NIRQ pin is set active(Cf. IRQPOLARITY) by our chip **OR by the host**: 0: Off 1: On Note that before going to Sleep, any pending scan period measurements are completed (unlike PHEN). Also, no compensation is performed when Sleep mode is exited (unlike PHEN).
		PHEN	3:0	RW	0000	Enables sensing/measurement phases. [3:0] = [PH3, PH2, PH1, PH0] When any PHEN bit is set a compensation (and start-up detection if enabled) is automatically performed for that phase. When SAREN =1, both PH1 and PH2 must be enabled.
0x14	RegI2cAddr	Reserved	7:2		000000	
		I2CADDR	1:0	RW	00	Defines bits [1:0] of the I2C address.
0x15	RegClkSprd	Reserved	7:5		000	
		CLKSPRDRNG	4	RW	0	Defines the range of the clock spreading: 0: Full 1: Reduced
		Reserved	3:1	RW	000	
		CLKSPRDEN	0	RW	0	Enables the sampling frequency clock spreading: 0: Off, fixed sampling frequency as defined by FREQ.

						1: On, dynamic sampling frequency automatically varying around FREQ value at every sampling period (8 steps, range defined by CLKSPRDRNG).
Analog-Front-End (AFE) Control						
0x20	RegAfeCtrl0	RINT	7:6	RW	00	Defines the internal resistor for compensation: 00: Lowest 01: Low 10: High 11: Highest
		CSIDLESLEEP	5:4	RW	00	Defines the status of the CSx pins during sleep mode and idle time: 0x: HZ (Typ.) 10: GND 11: VDD
		Reserved	3:0		0000	
0x21	RegAfeCtrl1	Reserved	7:0		0x10	
0x22	RegAfeCtrl2	Reserved	7:0		0x00	
0x23	RegAfeCtrl3	Reserved	7:1		0000000	
		ARANGE01	0	RW	0	Defines the analog range (full scale) for phases 0/1: 0: Small 1: Large
0x24	RegAfeCtrl4	FREQ01	7:3	RW	01000	Defines the sampling frequency for phases 0/1: 00000: 250 kHz 00001: 200 kHz 00010: 166.67 kHz 00011: 142.86 kHz 00100: 125 kHz 00101: 111.11 kHz 00110: 100 kHz 00111: 90.91 kHz 01000: 83.33 kHz (Typ.) 01001: 76.92 kHz 01010: 71.43 kHz 01011: 66.67 kHz 01100: 62.50 kHz 01101: 58.82 kHz 01110: 55.56 kHz 01111: 52.63 kHz 10000: 50 kHz 10001: 45.45 kHz 10010: 41.67 kHz 10011: 38.46 kHz 10100: 35.71 kHz 10101: 31.25 kHz 10110: 27.78 kHz 10111: 25 kHz 11000: 20.83 kHz 11001: 17.86 kHz 11010: 13.89 kHz 11011: 11.36 kHz 11100: 8.33 kHz

						11101: 6.58 kHz 11110: 5.43 kHz 11111: 4.63 kHz Note that these are the nominal values, Cf. fTrim/fTemp/fVDD in electrical specifications.
		RESOLUTION01	2:0	RW	100	Defines the measurement resolution/precision for phases 0/1: 000: 8 001: 16 010: 32 011: 64 100: 128 (Typ.) 101: 256 110: 512 111: 1024
0x25	RegAfeCtrl5	Reserved	7:0		0x00	
0x26	RegAfeCtrl6	Reserved	7:1		0000000	
		ARANGE23	0	RW	0	Defines the analog range (full scale) for phases 2/3. (Cf. ARANGE01)
0x27	RegAfeCtrl7	FREQ23	7:3	RW	01000	Defines the sampling frequency for phases 2/3. (Cf. FREQ01)
		RESOLUTION23	2:0	RW	100	Defines the resolution/precision for phases 2/3. (Cf. RESOLUTION01)
0x28	RegAfePh0	Reserved	7:6		00	
		AFEPH0	5:0	RW	101001	Defines the CS pins usage during phase 0: [5:4, 3:2, 1:0] = [CS2, CS1, CS0] 00: HZ 01: Measured Input 10: Dynamic Shield 11: GND Each CS setting is fully independent. Combined meas. can be achieved with several 01s. Default is CS0 measured while CS1/2 are shielded.
0x29	RegAfePh1	Reserved	7:6		00	
		AFEPH1	5:0	RW	100110	Defines CS pins usage during phase 1. (Cf. AFEPH0) Default is CS1 measured while CS0/2 are shielded.
0x2A	RegAfePh2	Reserved	7:6		00	
		AFEPH2	5:0	RW	011010	Defines CS pins usage during phase 2 (Cf. AFEPH0). Default is CS2 measured while CS0/1 are shielded.
0x2B	RegAfePh3	Reserved	7		0	
		TEMPEN	6	RW	0	Enables temperature sensing during phase 3: 0: Off 1: On, PROXUSEFUL of phase 3 now carries internal temperature sensor information. When set, AFEPH3 is ignored, all CS pins are HZ and all PH3 flags in RegStat0/1/2 are forced to 0.
		AFEPH3	5:0	RW	010110	Defines CS pins usage during phase 3. (Cf. AFEPH0)

						Default is CS1/2 measured while CS0 is shielded.
0x2C	RegAfeCtrl8	Reserved	7:4		0001	
		RESFILTIN	3:0	RW	0010	Defines the pre-charge input resistor (kOhm): 0000: 0/Off 0001: 2 0010: 4 (Typ.) 0011: 6 0100: 8 0101: 10 0110: 12 0111: 14 1000: 16 1001: 18 1010: 20 1011: 22 1100: 24 1101: 26 1110: 28 1111: 30
0x2D	RegAfeCtrl9	Reserved	7:4		0000	
		AGAIN	3:0	RW	1000	Defines the analog gain: 0110: x1.247 1000: x1 (Typ.) 1011: x0.768 1111: x0.552 Else: Reserved Note that these are the nominal values.
Main Digital Processing (Prox) Control						
0x30	RegProxCtrl0	Reserved	7:6		00	
		GAIN01	5:3	RW	001	Defines the digital gain for phases 0/1: 000: Reserved 001: Off (x1) 010: x2 011: x4 100: x8 Else: Reserved
		RAWFILT01	2:0	RW	001	Defines the PROXRAW filter strength for phases 0/1: 000: 0 (Off) 001: 1-1/2 (Typ.) 010: 1-1/4 011: 1-1/8 100: 1-1/16 101: 1-1/32 110: 1-1/64 111: 1-1/128 (Strongest)
0x31	RegProxCtrl1	Reserved	7:6		00	
		GAIN23	5:3	RW	001	Defines the digital gain for phases 2/3. (Cf. GAIN01)
		RAWFILT23	2:0	RW	001	Defines the PROXRAW filter strength for phases 2/3.

						(Cf. RAWFILT01)
0x32	RegProxCtrl2	AVGTHRESHINIT	7	RW	0	Defines the initial value used to calculate the average thresholds: 0: 0 1: Average value after compensation
		AVGCOMPMETHOD	6	RW	0	Defines the average compensation method: 0: Individual. Each phase triggers only its own compensation. 1: Common. Any phase triggers compensation for all phases.
		AVGNEGTHRESH	5:0	RW	100000	Defines the negative average threshold which will trigger compensation: All: AVGTHRESHINIT - (512*AVGNEGTHRESH) Typically set between -16384 and -24576 (i.e. ½ to ¾ of the system dynamic range). Phases are compensated individually or altogether depending on COMPMETHOD.
0x33	RegProxCtrl3	AVGDEB	7:6	RW	01	Defines the average debouncer applied to AVGPOSTHRESH/NEGTHRESH: 00: Off 01: 2 samples 10: 4 samples 11: 8 samples
		AVGPOSTHRESH	5:0	RW	100000	Defines the positive average threshold which will trigger compensation: 000000: Off, no automatic compensation; both from positive and negative thresholds. Else: AVGTHRESHINIT + (512*AVGPOSTHRESH) Typically set between +16384 and +24576 (i.e. ½ to ¾ of the system dynamic range). When AVGTHRESHINIT=0, should not be set below 100000 except to turn it OFF by setting it to 000000. When AVGTHRESHINIT=1, should not be set above 100000. Phases are compensated individually or altogether depending on COMPMETHOD.
0x34	RegProxCtrl4	Reserved	7		0	
		AVGFREEZEDIS	6	RW	0	Disables average freezing during prox: 0: On, as soon as prox is detected, average is frozen until prox is released. (Typ.) 1: Off, as soon as prox is detected, average is frozen for max 4xAVGDEB samples and then unfrozen (even if prox is not released). When SAREN=1, BODYSTAT1/2 and TABLESTAT1/2 are only updated while average is frozen. AVGFREEZEDIS=1 is typically used when FARCOND=1.
		AVGNEGFILT	5:3	RW	001	Defines the average negative filter strength: 000: 0 (Off) 001: 1-1/2 (Typ.)

						010: 1-1/4 011: 1-1/8 100: 1-1/16 101: 1-1/32 110: 1-1/64 111: 1 (Infinite)
		AVGPOSFILT	2:0	RW	100	Defines the average positive filter strength: 000: 0 (Off) 001: 1-1/16 010: 1-1/64 011: 1-1/128 100: 1-1/256 (Typ.) 101: 1-1/512 110: 1-1/1024 111: 1 (Infinite)
0x35	RegProxCtrl5	Reserved	7		0	
		FARCOND	6	RW	0	Defines the far/release/non-prox condition: 0 : PROXDIFF < (THRESH-HYST) (Typ.) 1 : PROXDIFF < **-** (THRESH-HYST) FARCOND=1 is typically used when AVGFREEZEDIS=1.
		HYST	5:4	RW	00	Defines the hysteresis applied to PROX/BODY/TABLETHRESH: 00: None 01: Small 10: Medium 11: High Small/Medium/High values correspond to a binary right shift of the threshold by respectively 4/3/2 bits, hence approximately +/- 6/12/25%.
		CLOSEDEB	3:2	RW	00	Defines the Close debouncer applied to PROX/BODY/TABLETHRESH: 00: Off 01: 2 samples 10: 4 samples 11: 8 samples
		FARDEB	1:0	RW	00	Defines the Far debouncer applied to PROX/BODY/TABLETHRESH: 00: Off 01: 2 samples 10: 4 samples 11: 8 samples
0x36	RegProxCtrl6	PROXTHRESH01	7:0	RW	00001000	Defines the proximity threshold for phases 0/1. 0x00: 0 0x01: 1 Else: int[$\text{PROXTHRESH}^2/2$] Default is 32. ($8^2/2$)
0x37	RegProxCtrl7	PROXTHRESH23	7:0	RW	0x08	Defines the proximity threshold for phases 2/3. (Cf. PROXTHRESH01)

Advanced Digital Processing Control						
0x40	RegAdvCtrl0	REFCALMSB	7:0	RW	0x00	Defines the reference calibration value. (Cf. REFINIT)
0x41	RegAdvCtrl1	REFCALLSB	7:0	RW	0x00	
0x42	RegAdvCtrl2	Reserved	7:5		000	
		REFEN	4	RW	0	Enables the reference correction: 0: Off, all phases work normally 1: On, the phase defined by REFPHASE is used to correct the other phases' measurements as defined by REFMETHOD.
		REFMETHOD	3	RW	0	Defines how the correction is applied: 0: Useful, all the time. Useful(n) = Useful(n) - REFCOEF* [RefUseful(n) – RefUseful0C] RefUseful0C corresponds to the value right after last compensation as defined by REFINIT. 1: Average, only when it is "frozen". Average(n) = Average0F + REFCOEF* [RefUseful(n) – RefUseful0F] Average0F and RefUseful0F correspond to the values right after Average has been frozen (i.e. right after prox detection)
		REFPHASE	2:1	RW	00	Defines which phase is used for reference: 00: PH0 01: PH1 10: PH2 11: PH3
		REFINIT	0	RW	0	Defines how RefUseful0C is initialized after a compensation (power-up or other): 0: If start-up detection is enabled, for STARTUPSENS phase, if PROXOFFSET=OFFSETTHRESH => REFCAL. Else RefUseful(n). 1: RefUseful(n)
0x43	RegAdvCtrl3	REFCOEF01	7:0	RW	0x00	Defines the reference coefficient for phases 0/1. Coded on 8 bits as XXX.YYYYY : 0x00: 0 (Off, no correction applied) 0x01: 0.03125 0x02: 0.0625 … 0x20: 1 … 0xFF: 7.96875 Note that when REFMETHOD=0, the exact coefficient applied depends on RAWFILT.
0x44	RegAdvCtrl4	REFCOEF23	7:0	RW	0x00	Defines the reference coefficient for phases 2/3. (Cf. REFCOEF01)
0x45	RegAdvCtrl5	Reserved	7:4		0000	
		STARTUPSENS	3:2	RW	01	Defines to which phase the start-up detection applies: 00: PH0 01: PH1 10: PH2

						11: PH3
		STARTUPFREQ	1	RW	0	Defines when the start-up detection is performed: 0: Only after PHEN compensation 1: After each compensation
		STARTUPMETH	0	RW	1	Defines the start-up detection method: 0: After the compensation is performed, PROXOFFSET (and PROXUSEFUL) of phase defined in STARTUPSENS, is compared with OFFSETTHRESH (and USEFULTHRESH if enabled). If [PROXOFFSET > OFFSETTHRESH] OR ([PROXOFFSET = OFFSETTHRESH] AND [PROXUSEFUL > USEFULTHRESH]) => Set PROXSTAT to 1 and set it back to 0 only when [PROXOFFSET < OFFSETTHRESH] OR ([PROXOFFSET = OFFSETTHRESH] AND [PROXUSEFUL < USEFULTHRESH]) Then start normal processing. Else => Set PROXSTAT to 0 and start normal processing. 1: After the compensation is performed, PROXOFFSET of phase defined in STARTUPSENS is temporarily forced to OFFSETTHRESH and PROXUSEFUL compared to USEFULTHRESH (PROXAVG and PROXDIFF frozen) If[PROXUSEFUL > USEFULTHRESH] => Set PROXSTAT to 1, and set it back to 0 only when [PROXUSEFUL < USEFULTHRESH], then run compensation and start normal processing. Else => Set PROXSTAT to 0, restore original PROXOFFSET and start normal processing. Important: PROXUSEFUL values used for start-up detection (and everything else) are the ones AFTER the reference correction (if enabled) has been applied.
0x46	RegAdvCtrl6	Reserved	7:6		00	
		OFFSETTHRESHMSB	5:0	RW	000000	Enables the start-up proximity detection and defines the offset threshold: 0x0000: Off, no start-up detection performed Else: Start-up detection offset threshold.
0x47	RegAdvCtrl7	OFFSETTHRESHLSB	7:0	RW	00000000	
0x48	RegAdvCtrl8	USEFULTHRESHMSB	7:0	RW	0x00	Defines the useful threshold for start-up detection. Signed, 2's complement format.
0x49	RegAdvCtrl9	USEFULTHRESHLSB	7:0	RW	0x00	
0x4A	RegAdvCtrl10	BODYTHRESH01	7:4	RW	0000	Defines the body threshold for phases 0/1: 0000: Off

						0001: 2048 0010: 4096 0011: 6144 0100: 8192 0101: 10240 0110: 12288 0111: 14336 1000: 16384 1001: 18432 1010: 20480 1011: 22528 1100: 24576 1101: 26624 1110: 28672 1111: 30720
		BODYTHRESH23	3:0	RW	0000	Defines the body threshold for phases 2/3. (Cf. BODYTHRESH01)
0x4B	RegAdvCtrl11	TABLETHRESHHIGH01	7:4	RW	0000	Defines the high table threshold for phases 0/1: 0000: Off (low table threshold must also be set Off) 0001: 2048 0010: 4096 0011: 6144 0100: 8192 0101: 10240 0110: 12288 0111: 14336 1000: 16384 1001: 18432 1010: 20480 1011: 22528 1100: 24576 1101: 26624 1110: 28672 1111: 30720
		TABLETHRESHLOW01	3:0	RW	0000	Defines the low table threshold for phases 0/1: 0000: Off (high table threshold must also be set Off) 0001: 2048 0010: 4096 0011: 6144 0100: 8192 0101: 10240 0110: 12288 0111: 14336 1000: 16384 1001: 18432 1010: 20480 1011: 22528 1100: 24576 1101: 26624 1110: 28672 1111: 30720

0x4C	RegAdvCtrl12	TABLETHRESHHIGH23	7:4	RW	0000	Defines the high table threshold for phases 2/3. (Cf. TABLETHRESHHIGH01)
		TABLETHRESHLOW23	3:0	RW	0000	Defines the low table threshold for phases 2/3. (Cf. TABLETHRESHLOW01)
0x4D	RegAdvCtrl13	Reserved	7		0	
		SAREN	6	RW	0	Enables smart engine for SAR: 0: Off, phases 1/2 are used for independent sensing. 1: On, phases 1/2 are used for smart SAR sensing.
		SARDEB	5:4	RW	00	Defines the debouncer applied to SAR threshold: 00: Off 01: 2 samples 10: 4 samples 11: 8 samples
		SARHYST	3:2	RW	00	Defines the hysteresis applied to SAR threshold: 00: None 01: Small 10: Medium 11: High Small/Medium/High values correspond to a binary right shift of the threshold by respectively 4/3/2 bits, hence approximately +/- 6/12/25%.
		SARSTATCONFIG	1:0	RW	00	Defines when SMARTSARSTAT flag is high: 00: (PROXSTAT12=0 && PROXSTATANY=1) || (PROXSTAT12=1 && BODYSTAT1=BODYSTAT2=1) 01: (PROXSTAT12=0 && PROXSTAT3=1) || (PROXSTAT12=1 && BODYSTAT1=BODYSTAT2=1) 10: (PROXSTAT12=0 && PROXSTAT0=1) || (PROXSTAT12=1 && BODYSTAT1=BODYSTAT2=1) 11: (PROXSTAT12=1 && BODYSTAT1=BODYSTAT2=1)
0x4E	RegAdvCtrl14	SARSLOPE	7:0	RW	0x80	Defines the slope for SAR threshold calculation. Coded on 8 bits as X.YYYYYYY: 0x00: 0 0x01: 0.0078125 0x02: 0.015625 … 0x80: 1 … 0xFF: 1.9921875
0x4F	RegAdvCtrl15	SAROFFSET	7:0	RW	0x0C	Defines the offset for SAR threshold calculation: 0x00: 0 0x01: 16 0x02: 32 … 0x0C: 192 … 0xFE: 4064 0xFF: 4080
0x50	RegAdvCtrl16	Reserved	7:6		00	
		STEADYEN	5:4	RW	00	Enables the steady detection, and defines to which signal it applies:

						00: Off 01: PROXDIFF, only when PROXSTAT=1. 10: PROXDIFF, all the time. 11: PROXUSEFUL, all the time. Note that setting 01 should not be used if STEADYCOND is set for PROXSTAT.
		STEADYWINDOW	3:2	RW	00	Defines the length of the steady window during which peak-peak variation is checked against STEADYMAXVAR. 00: 4 samples 01: 16 samples 10: 64 samples 11: 128 samples
		UNSTEADYDEB	1:0	RW	00	Defines the unsteady (STEADYSTAT falling edge) debouncer : 00: Off 01: 2 STEADYWINDOWs 10: 4 STEADYWINDOWs 11: 8 STEADYWINDOWs
0x51	RegAdvCtrl17	STEADYMAXVAR01	7:4	RW	0000	Defines the maximum tolerated peak-peak variation (LSBs) during each STEADYWINDOW for phases 0/1: 0000: 0 0001: 1 0010: 2 0011: 4 0100: 8 0101: 16 0110: 32 0111: 64 1000: 128 1001: 256 1010: 512 1011: 1024 1100: 2048 1101: 4096 1110: 8192 1111: 16384
		STEADYMAXVAR23	3:0	RW	0000	Defines the maximum tolerated peak-peak variation (LSBs) during each STEADYWINDOW for phases 2/3. (Cf. STEADYMAXVAR01)
0x52	RegAdvCtrl18	STEADYMINTIME01	7:4	RW	0000	Defines the number of consecutive and successful STEADYWINDOWs required to set STEADYSTAT0/1. 0000: 1 0001: 2 0010: 3 0011: 7 0100: 11 0101: 15 0110: 23 0111: 31 1000: 39

						1001: 55 1010: 71 1011: 87 1100: 119 1101: 151 1110: 183 1111: 247
		STEADYMINTIME23	3:0	RW	0000	Defines the number of consecutive and successful STEADYWINDOWs required to set STEADYSTAT2/3. (Cf. STEADYMINTIME01)
0x53	RegAdvCtrl19	FAILTHRESHHIGH01	7:4	RW	1111	Defines the high failure threshold for phases 0/1: 0000: Off, high failure detection disabled. 0001: 1024 0010: 2048 0011: 3072 0100: 4096 0101: 5120 0110: 6144 0111: 7168 1000: 8192 1001: 9216 1010: 10240 1011: 11264 1100: 12288 1101: 13312 1110: 14336 1111: Saturation (max or 0) Note that failure check is only performed after compensation or PROXOFFSET forced by I2C. (i.e. not when FAILTHRESH value is modified).
		FAILTHRESHLOW01	3:0	RW	0000	Defines the low failure threshold for phases 0/1: 0000: Off, low failure detection disabled. 0001: 1024 0010: 2048 0011: 3072 0100: 4096 0101: 5120 0110: 6144 0111: 7168 1000: 8192 1001: 9216 1010: 10240 1011: 11264 1100: 12288 1101: 13312 1110: 14336 1111: 15360 Note that failure check is only performed after compensation or PROXOFFSET forced by I2C. (i.e. not when FAILTHRESH value is modified).

0x54	RegAdvCtrl20	FAILTHRESHHIGH23	7:4	RW	1111	Defines the high failure threshold for phases 2/3. (Cf. FAILTHRESHHIGH01)
		FAILTHRESHLOW23	3:0	RW	0000	Defines the low failure threshold for phases 2/3. (Cf. FAILTHRESHHIGH23)
Phase Data Readback						
0x60	RegPhaseSel	Reserved	7:2		000000	
		PHASESEL	1:0	RW	00	Defines which phase's data will be available in registers RegUseMsb to RegOffsetLsb : 00: PH0 01: PH1 10: PH2 11: PH3
0x61	RegUseMsb	PROXUSEFULMSB	7:0	R	0x00	Useful current value. Signed, 2's complement format.
0x62	RegUseLsb	PROXUSEFULLSB	7:0	R	0x00	
0x63	RegAvgMsb	PROXAVGMSB	7:0	R	0x00	Average current value. Signed, 2's complement format.
0x64	RegAvgLsb	PROXAVGLSB	7:0	R	0x00	
0x65	RegDiffMsb	PROXDIFFMSB	7:0	R	0x00	Diff current value. Signed, 2's complement format.
0x66	RegDiffLsb	PROXDIFFLSB	7:0	R	0x00	
0x67	RegOffsetMsb	Reserved	7:6		00	Compensation offset current value. Unsigned. To force a value, MSB and LSB registers must be written in sequence and change is effective after LSB. LSB alone can be forced if needed. (MSB unchanged)
		PROXOFFSETMSB	5:0	RW	000000	
0x68	RegOffsetLsb	PROXOFFSETLSB	7:0	RW	0x00	
0x69	RegSarMsb	SARTHRESHMSB	7:0	R	0x00	SAR threshold current value. (SARSLOPE * PH2 + SAROFFSET) Signed, 2's complement format.
0x6A	RegSarLsb	SARTHRESHLSB	7:0	R	0x00	
Miscellaneous						
0x9F	RegReset	SOFTRESET	7:0	W	0x00	Writing 0xDE resets the chip.
0xFA	RegWhoAmI	WHOAMI	7:0	R	0x23	Chip Identification Number
0xFE	RegRev	REVISION	7:0	R	0x22	Chip Revision

Table 8: Registers Detailed Description

9 APPLICATION INFORMATION

9.1 Typical Application Circuit

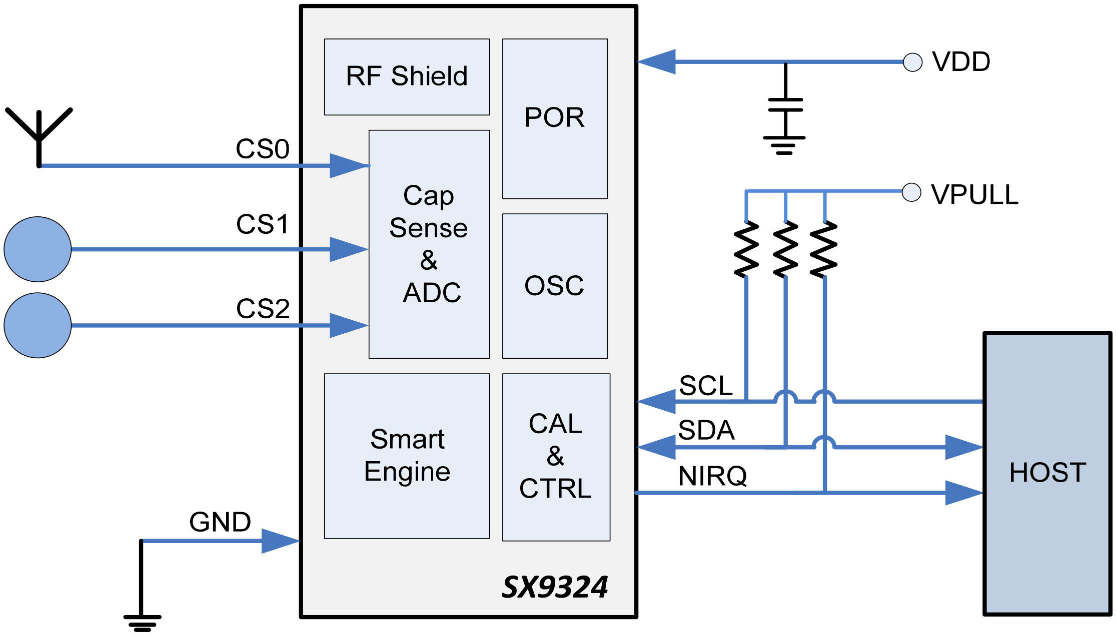


Figure 27: Typical Application Circuit

9.2 External Components Recommended Values

Symbol	Description	Note	Min	Typ.	Max	Unit
CDD	Supply Decoupling Capacitor	min X5R type, min 2.5V rating.	0.8	1	1.2	uF
RPULL	Host Interface Pull-ups		-	2.2	-	kΩ

Table 9: External Components Recommended Values

10 PACKAGING INFORMATION

10.1 Outline Drawing

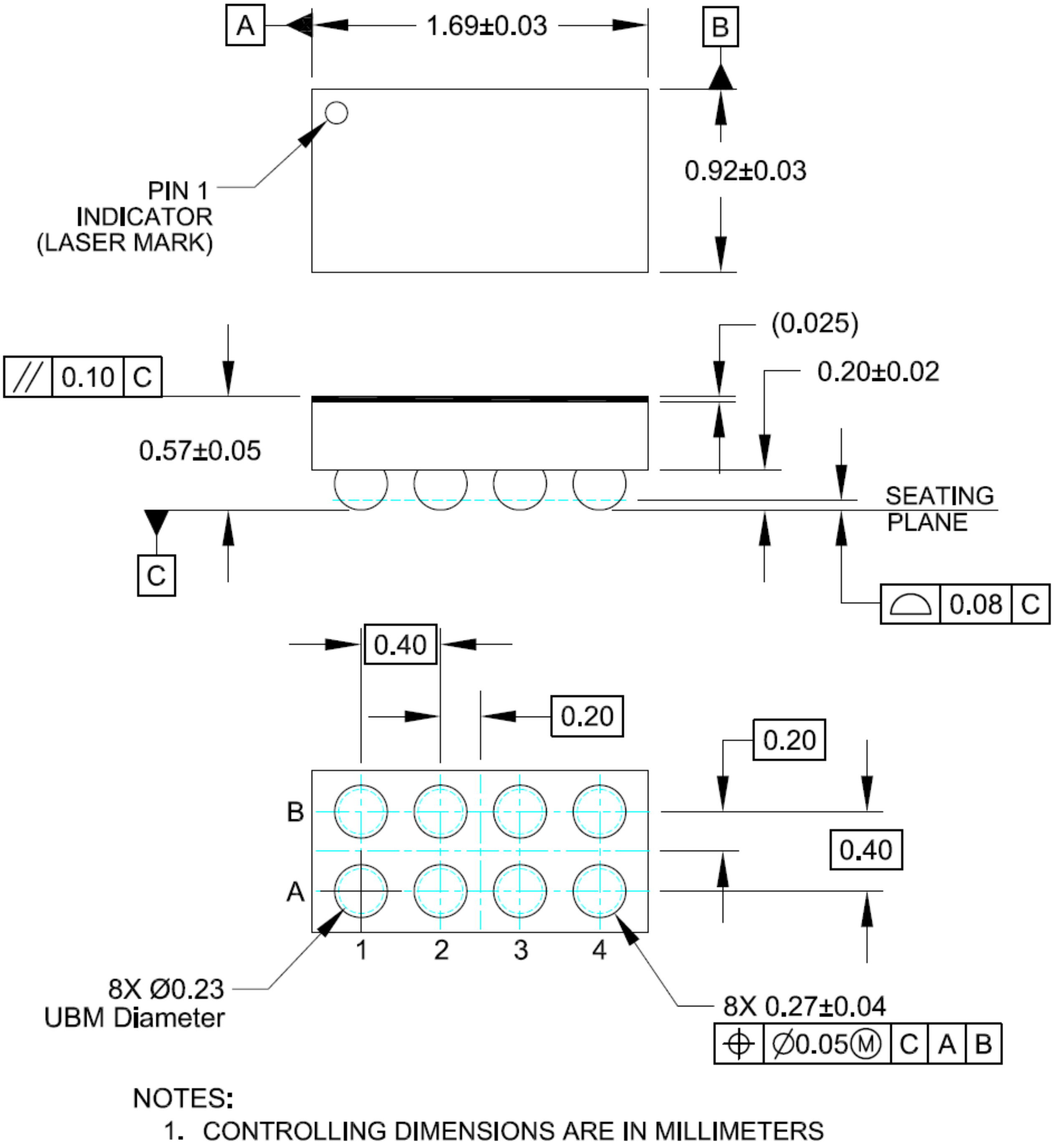
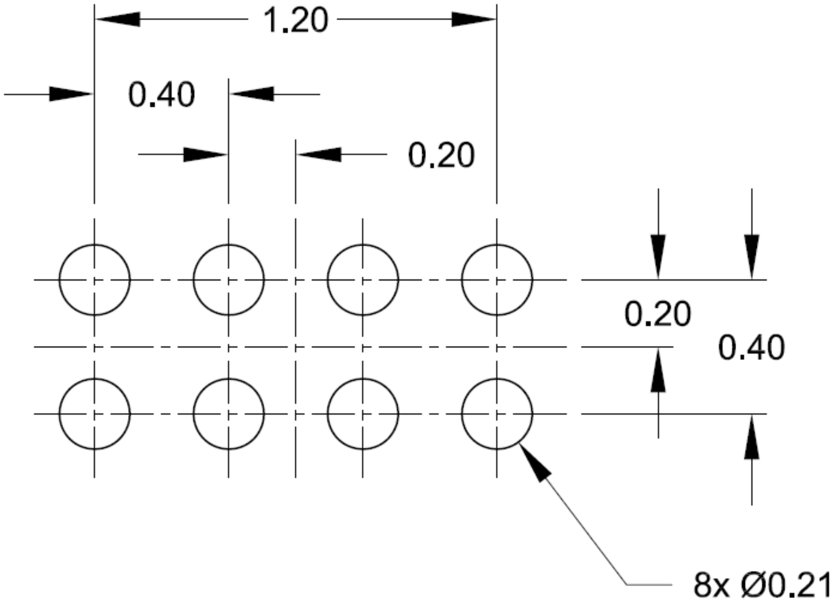


Figure 28: Outline Drawing

10.2 Land Pattern



NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS
2. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.

Figure 29: Land Pattern

WIRELESS & SENSING

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Contact Information

Semtech Corporation
Wireless and Sensing Products Division
200 Flynn Road, Camarillo, CA 93012
Phone: (805) 498-2111 Fax: (805) 498-3804

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