Middle Power Class-D Speaker Amplifier series

17W+17W Full Digital Speaker Amplifier with built-in DSP

BM28723AMUV

General Description

BM28723AMUV is a 17W+17W Class D stereo Speaker Amplifier with built-in DSP designed for TVs specifically for space-saving and low-power consumption.
BM28723AMUV features BCD (Bipolar, CMOS, DMOS) process technology to achieve high efficiency. In addition, BM28723AMUV is packaged in a compact back surface heatsink type power package to attain low power consumption, low heat generation without external heatsink. The package Max output power is only 17W+17W (When R_L=8Ω) as compared to 20W+20W (When R_L=8Ω) Max output power of package with external heat-sink.
The product satisfies all needs for drastic downsizing, low-profile structures and powerful high quality playback of sound systems.

Key Specifications

- Supply voltage range (V_{CCP1}, V_{CCP2}): 10V to 24V
- Speaker output power (V_{CCP1}, V_{CCP2}=18V, R_L=8Ω): 17W+17W (Typ)
- THD+N: 0.08[%] (Typ)

Applications

- TVs (LCD, OLED)
- Home Audio
- Desktop PC
- Amusement Equipment
- Electronic Music Equipment, etc.

Typical Application Circuit

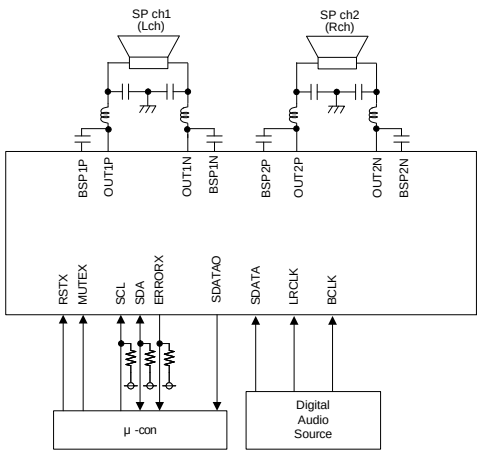


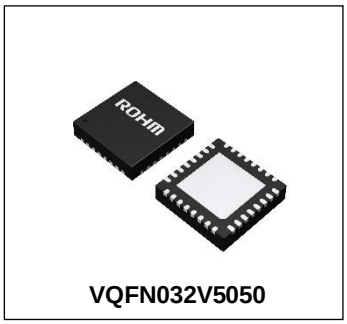
Figure 1. Typical Application Circuit

Features

- Built-in DSP (Digital Sound Processor) for Audio Signal Processing for TVs
  12-Band/ch BQ, 3-Band DRC, Pre-Scaler, Channel Mixer, Fine Master Volume, Hard Clipper, Level Meter, etc.
- Single Input System for Digital Audio Interface (No Master Clock Required)
  - I^2S/LJ/RJ Format
  - LRCLK: 32kHz/44.1kHz/48kHz
  - BCLK: 32fs/48fs/64fs
  - SDATA: 16bit/20bit/24bit
- Single Output System for Digital Audio Interface
  - I^2S Format
  - SDATA: 16bit/20bit/24bit
- No Snubber Circuit Required (V_{CCP1}, V_{CCP2}≤22V) because of Slew Rate Control
- Output Feedback Circuit which prevents decrease of sound quality caused by change of power supply voltage, achieves low noise and low distortion, so no large electrolytic-capacitors for V_{CC} bypass is required.
- Wide Range of Power Supply Input Voltage
- The monaural output reduces the number of external parts needed.
- High Efficiency and Low Heat Dissipation allowing Miniaturization, Slim Design, and also Power Saving of the System
- Eliminates pop-noise generated during the power supply ON/OFF. High quality muting performance is achieved using the soft-muting technology.
- Built-in with Various Protection Functions for Highly Reliability Design
  - High Temperature Protection
  - Under Voltage Protection
  - Output Short Protection
  - DC Voltage Protection for speaker
  - Clock Stop Protection
- Small Package, it reduces surface mount area

Package

	W(Typ) x D(Typ) x H(Max)
VQFN032V5050	5.00mm x 5.00mm x 1.00mm



VQFN032V5050

○Product structure: Silicon integrated circuit ○This product has no designed protection against radioactive rays

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Pin Configuration and Block Diagram

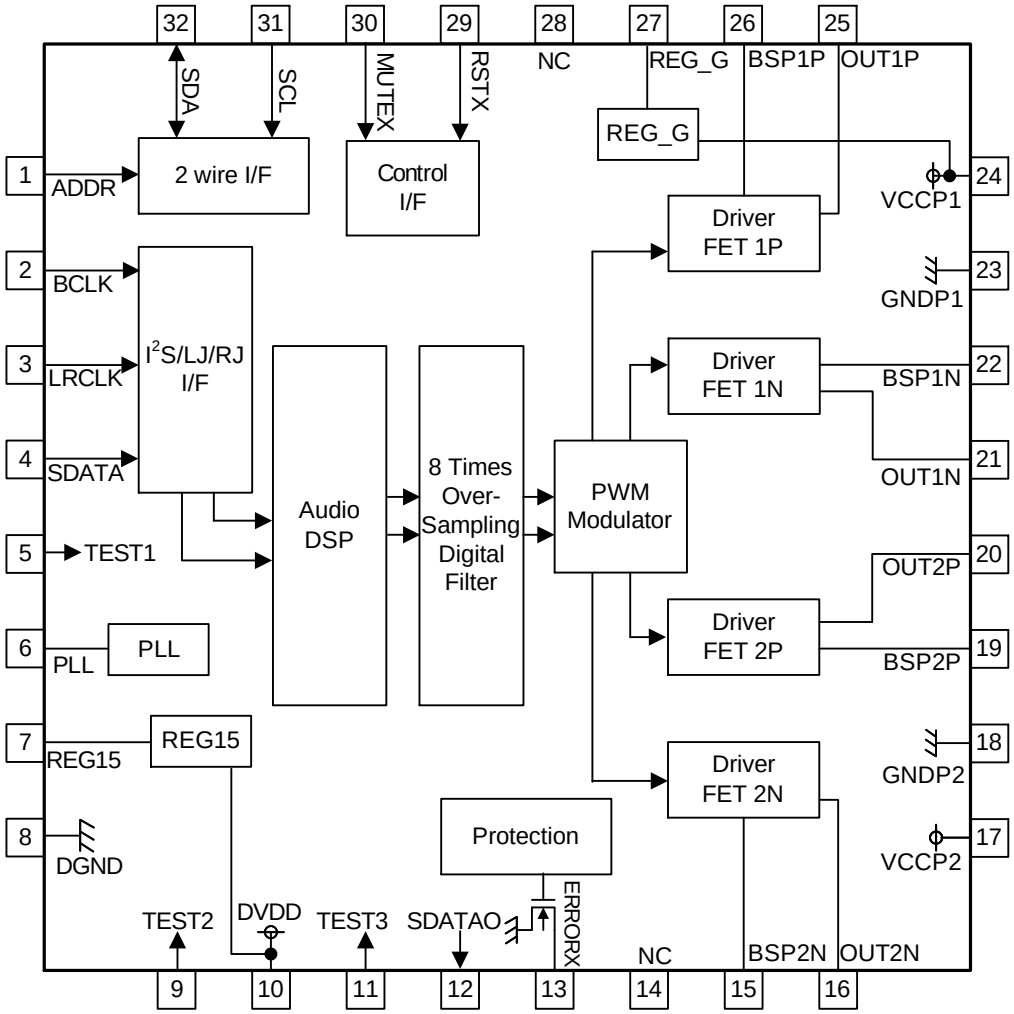


Figure 2. Pin Configurations and Block Diagram (Top View)

Pin Description

No.	Name	I/O	No.	Name	I/O	No.	Name	I/O	No.	Name	I/O
1	ADDR	I	9	TEST2	I	17	VCCP2	-	25	OUT1P	O
2	BCLK	I	10	DVDD	-	18	GNDP2	-	26	BSP1P	I
3	LRCLK	I	11	TEST3	I	19	BSP2P	I	27	REG_G	O
4	SDATA	I	12	SDATAO	O	20	OUT2P	O	28	NC	-
5	TEST1	I	13	ERRORX	O	21	OUT1N	O	29	RSTX	I
6	PLL	I/O	14	NC	-	22	BSP1N	I	30	MUTEX	I
7	REG15	O	15	BSP2N	I	23	GNDP1	-	31	SCL	I
8	DGND	-	16	OUT2N	O	24	VCCP1	-	32	SDA	I/O

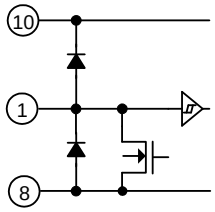
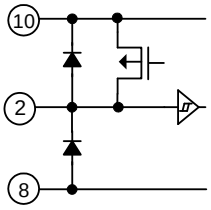
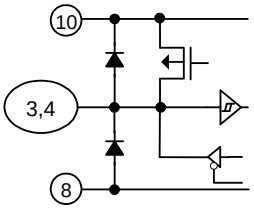
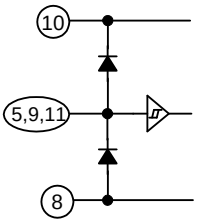
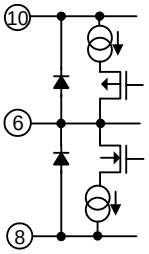
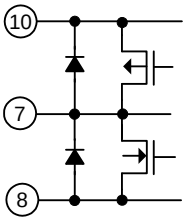
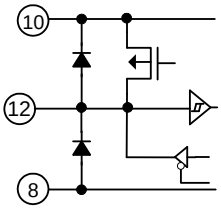
I: input, O: output, -: others

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I/O Equivalence Circuits

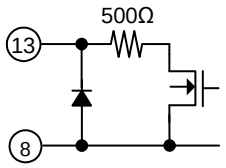
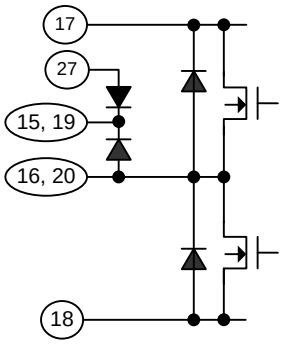
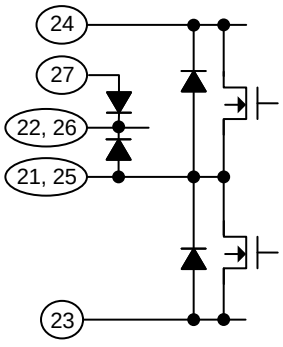
Caution: The numerical value of I/O equivalence circuit is typical value, not guaranteed.

Pin No.	Pin Name	Pin Voltage	Pin Explanation	I/O Equivalence Circuit
1	ADDR	0V	2 wire Bus control slave address select pin Select LSB data of slave address for 2 wire Bus control. Input High level to set LSB=1. Input Low level to set LSB=0. Select pull-down resistor after DVDD is applied.	
2	BCLK	3.3V	Digital audio signal input pin Input bit clock of digital audio signal. Select pull-up resistor after DVDD is applied.	
3 4	LRCLK SDATA	3.3V	Digital audio signal input pin Input LR clock of digital audio signal to LRCLK. Input data of digital audio signal to SDATA. Select pull-up resistor after DVDD is applied.	
5 9 11	TEST1 TEST2 TEST3	- - -	Test pin Connect to DGND.	
6	PLL	1V	PLL filter pin Connect filter circuit for PLL.	
7	REG15	1.5V	Internal power supply pin for digital circuit Connect capacitor. ***Caution:*** The REG15 of BM28723AMUV should not be used as an external supply and cannot support voltage load from external source. Therefore, do not connect anything except capacitor for stabilization.	
8	DGND	0V	GND pin for Digital I/O	-
10	DVDD	3.3V	Power supply pin for Digital I/O. Connect capacitor.	-
12	SDATAO	3.3V	Digital audio signal output pin Output data of digital audio signal. Select pull-up resistor after DVDD is applied.	

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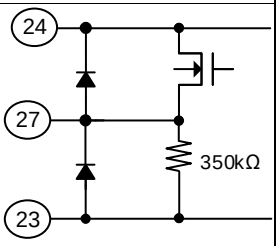
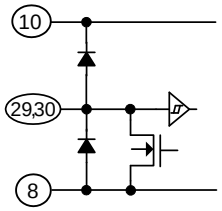
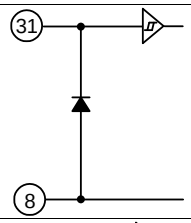
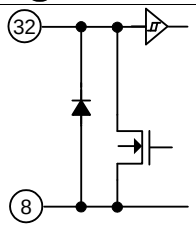
I/O Equivalence Circuits – continued

Pin No.	Pin Name	Pin Voltage	Pin Explanation	I/O Equivalence Circuit
13	ERRORX	3.3V	Error flag pin Connect pull-up resistor. High: Normal operation Low: Error ***Caution:*** An error flag is indicated when Output Short Protection, DC Voltage Protection for speaker, and High Temperature Protection are activated. The flag shows the LSI condition during operation. Don't use for the protection except this product.	
14 28	NC	-	No-Connection Pin Don't connect anything.	-
15	BSP2N	-	Boot strap pin, CH2 negative Connect a capacitor from pin to OUT2N.	
16	OUT2N	V_{CCP2} to 0V	PWM output pin, CH2 negative Connect pin to output LPF. ***Caution 1:*** If this pin is shorted to GND, the LSI may break. ***Caution 2:*** When Reset ON or Mute ON, all output transistors are OFF and output pins are pulled down by 10kΩ (Typ).	
17	VCCP2	V_{CCP2}	Power supply pin for CH2	
18	GNDP2	0V	Power GND pin for CH2	
19	BSP2P	-	Boot strap pin, CH2 positive Connect a capacitor from pin to OUT2P.	
20	OUT2P	V_{CCP2} to 0V	PWM output pin, CH2 positive Connect pin to output LPF. ***Caution 1*:** If this pin is shorted to GND, the LSI may break. ***Caution 2*:** When Reset ON or Mute ON, all output transistors are OFF and output pins are pulled down by 10kΩ (Typ).	
21	OUT1N	V_{CCP1} to 0V	PWM output pin, CH1 negative Connect pin to output LPF. ***Caution 1*:** If this pin is shorted to GND, the LSI may break. ***Caution 2*:** When Reset ON or Mute ON, all output transistors are OFF and output pins are pulled down by 10kΩ (Typ).	
22	BSP1N	-	Boot strap pin, CH1 negative Connect a capacitor from pin to OUT1N.	
23	GNDP1	0V	Power GND pin for ch1	
24	VCCP1	V_{CCP1}	Power supply pin for ch1	
25	OUT1P	V_{CCP1} to 0V	PWM output pin, CH1 positive Connect to output LPF. ***Caution 1*:** If this pin is shorted to GND, the LSI may break. ***Caution 2*:** When Reset ON or Mute ON, all output transistors are OFF and output pins are pulled down by 10kΩ (Typ).	
26	BSP1P	-	Boot-strap pin of ch1 positive Connect a capacitor from pin to OUT1P.	

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I/O Equivalence Circuits - continued

Pin No.	Pin Name	Pin Voltage	Pin Explanation	I/O Equivalence Circuit
27	REG_G	5.7V	Internal power supply pin for gate driver Connect capacitor ***Caution:*** The REG_G pin of BM28723AMUV should not be used as an external supply and cannot support voltage load from external source. Therefore, do not connect anything except capacitor for stabilization.	
29	RSTX	0V	Reset pin for Digital circuit High: Reset OFF Low: Reset ON Select pull-down resistor after DVDD is applied.	
30	MUTEX	0V	Speaker output mute control pin High: Mute OFF Low: Mute ON Select pull-down resistor after DVDD is applied.	
31	SCL	-	2 wire Bus control transmit clock input pin Input the transmit clock to this pin for 2 wire Bus control. ***Caution:*** This pin is not corresponding to threshold tolerance of 5V. Refer to Absolute Maximum Ratings, Input voltage 1	
32	SDA	-	2 wire Bus control data input/output pin Input the transmit data to this pin for 2 wire Bus control. ***Caution:*** This pin is not corresponding to threshold tolerance of 5V.Refer to Absolute Maximum Ratings, Input voltage 1	
-	EXP-PAD	-	There is no problem when EXP-PAD is left unconnected. However, connecting it to ground is recommended because the radiation performance will be degraded. The connection to any place except for the ground is prohibited.	-

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Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Limit	Unit	Conditions
Supply Voltage	V_{CCMAX}	30	V	Pin 17, 24*(Note 1) (Note 2)*
	$V_{DVDDMAX}$	4.5	V	Pin 10*(Note 1)*
Input Voltage 1	V_{IN1}	-0.3 to V_{DVDD}+0.3*(Note 2)*	V	Pin 1 to 5, 9, 11, 29 to 32*(Note 1)*
Pin Voltage 1	V_{PIN1}	-0.3 to +7.0	V	Pin 27*(Note 1)*
Pin Voltage 2	V_{PIN2}	-0.3 to +V_{CCMAX}	V	Pin 16, 20, 21, 25*(Note 1) (Note 4)*
Pin Voltage 3	V_{PIN3}	-0.3 to V_{OUT1P}+7	V	Pin 26*(Note 1) (Note 5)*
		-0.3 to V_{OUT1N}+7		Pin 22*(Note 1) (Note 5)*
		-0.3 to V_{OUT2P}+7		Pin 19*(Note 1) (Note 5)*
		-0.3 to V_{OUT2N}+7		Pin 15*(Note 1) (Note 5)*
Pin Voltage 4	V_{PIN4}	-0.3 to +2.1	V	Pin 7*(Note 1)*
Open-drain Pin Voltage	V_{ERR}	-0.3 to +7.0	V	Pin 13*(Note 1)*
Operating Temperature Range	Topr	-25 to +85	°C	
Storage Temperature Range	Tstg	-55 to +150	°C	
Junction Temperature Range	Tj	-40 to +150	°C	

Caution 1: *Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.*

Caution 2: *Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB with thermal resistance taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.*

(Note 1) The voltage that can be applied reference to GND (Pin 8, 18, 23).
(Note 2) Do not exceed Tj=150°C.
(Note 3) Refer to Recommended Operating Ratings for V_{DVDD}.
(Note 4) This LSI should be used within AC peak limits at all conditions. Overshoot should be ≤30V with reference to GND.
Undershoot should be ≤10ns and ≤30V with reference to V_{CCP1} and V_{CCP2}. (Refer to Figure 3-1)
(Note 5) This LSI should be used in lower than this rating by all means.
Undershoot should be ≤10ns and ≤ (V_{OUT1P} or V_{OUT1N} or V_{OUT2P} or V_{OUT2N}) +7V. (Refer to Figure 3-2)

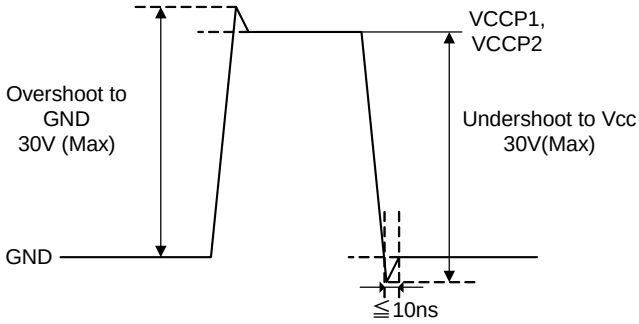


Figure 3-1

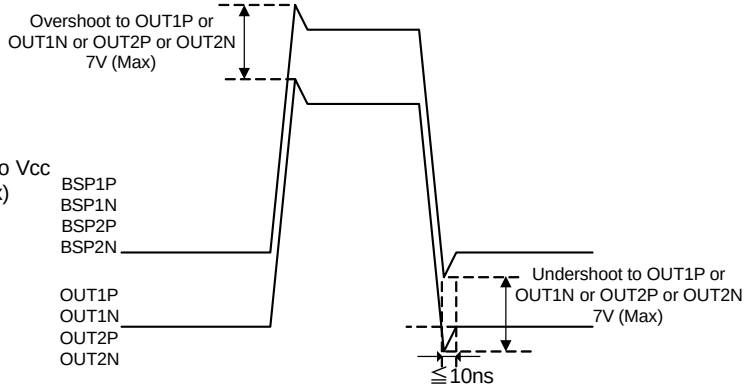


Figure 3-2

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Thermal Resistance(Note 6)

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s(Note 8)	2s2p(Note 9)	
VQFN032V5050				
Junction to Ambient	θ_{JA}	138.9	39.1	°C/W
Junction to Top Characterization Parameter(Note 7)	Ψ_{JT}	11	5	°C/W

(Note 6) Based on JESD51-2A (Still-Air)
(Note 7) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.
(Note 8) Using a PCB board based on JESD51-3.
(Note 9) Using a PCB board based on JESD51-5, 7.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3mm x 76.2mm x 1.57mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70µm

Layer Number of Measurement Board	Material	Board Size	Thermal Via(Note 10)	
			Pitch	Diameter
4 Layers	FR-4	114.3mm x 76.2mm x 1.6mmt	1.20mm	Φ0.30mm

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70µm	74.2mm x 74.2mm	35µm	74.2mm x 74.2mm	70µm

(Note 10) This thermal via connects with the copper pattern of all layers.

Recommended Operating Conditions (Ta=-25°C to +85°C)

Parameter	Symbol	Limit	Unit	Conditions
Supply voltage	V_{CCP1}	10 to 24	V	Pin 24(Note 1) (Note 2)
	V_{CCP2}	10 to 24	V	Pin 17(Note 1) (Note 2)
	V_{DVDD}	3.0 to 3.6	V	Pin 10 (Note 1)
Minimum load impedance	R_L	6.4	Ω	$21V<V_{CCP1}$, $V_{CCP2}\leq 24V$(Note 2)
		4.8	Ω	$14V<V_{CCP1}$, $V_{CCP2}\leq 21V$(Note 2)
		3.6	Ω	V_{CCP1}, $V_{CCP2}\leq 14V$(Note 2)

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Electrical Characteristics

(Unless otherwise specified Ta=25°C, V_{CCP1}, V_{CCP2}=18V, V_{DVDD}=3.3V, V_{RSTX}=3.3V, V_{MUTEX}=3.3V, f=1kHz, fs=48kHz, R_L=8Ω, DSP: Through, Driver Gain (G_{DRV}) =26dB, LC Filter: L=10μH, C_g=0.47μF, Without Snubber circuit)

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
Total Circuit						
Circuit Current 1 (Normal mode)	I_{CC1}	-	45	90	mA	Pin 17, 24, -infinity dBFS input, No load
	I_{DD1}	-	9	19	mA	Pin 10, -infinity dBFS input, No load
Circuit Current 2 (Reset mode)	I_{CC2}	-	110	400	μA	Pin 17, 24, -infinity dBFS input, No load, V_{RSTX}=0V, V_{MUTEX}=0V
	I_{DD2}	-	2.5	7.0	mA	Pin 10, -infinity dBFS input, No load V_{RSTX}=0V, V_{MUTEX}=0V
Open-drain Pin Low Level Voltage	V_{ERR}	-	-	0.8	V	Pin 13, I_{OUT}=0.5mA
High Level Input Voltage	V_{IH}	2.5	-	3.3	V	Pin 1 to 5, 9, 11, 29 to 32
Low Level Input Voltage	V_{IL}	0	-	0.8	V	Pin 1 to 5, 9, 11, 29 to 32
Input Pull-up Resistance	R_{UP}	22	33	-	kΩ	Pin 2 to 4, V_{IN}=0V
Input Pull-down Resistance	R_{DN}	31	47	-	kΩ	Pin 1, 29, 30, V_{IN}=3.3V
Input Current (SCL, SDA pin)	I_{IL}	-1	0	-	μA	Pin 31, 32, V_{IN}=0V
Input Current (SCL, SDA pin)	I_{IH}	-	0	1	μA	Pin 31, 32, V_{IN}=3.3V
Speaker Amplifier Output						
Maximum Output Power 1*(Note 11)*	P_{O1}	-	10	-	W	V_{CCP1}, V_{CCP2}=13V, THD+N=10%
Maximum Output Power 2*(Note 11)*	P_{O2}	-	15	-	W	V_{CCP1}, V_{CCP2}=16V, THD+N=10%
Total Harmonic Distortion*(Note 11)*	THD	-	0.08	-	%	V_{CCP1}, V_{CCP2}=12V, P_O=1W, BW=AES17 (20Hz -22kHz) With snubber circuit
Crosstalk*(Note 11)*	CT	60	90	-	dB	P_O=1W, 1kHz BPF
PSRR*(Note 11)*	PSRR	-	60	-	dB	V_{ripple}=1V_{rms}, f=1kHz
Output Noise Voltage*(Note 11)*	V_{NO}	-	150	-	μVrms	-Infinity dBFS input, BW=A-Weight
PWM (Pulse Width Modulation) Frequency	f_{PWM1}	-	256	-	kHz	f_S=32 kHz
	f_{PWM2}	-	352.8	-	kHz	f_S=44.1 kHz
	f_{PWM3}	-	384	-	kHz	f_S=48 kHz

(Note 11) These Parameters show the typical performance of device and depend on board layout, parts, and power supply. The standard value is in mounting device and parts on surface of ROHM's board directly.

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Typical Performance Curves

Unless otherwise specified Ta=25°C, V_{CCP1}, V_{CCP2}=18V, V_{DVDD}=3.3V, V_{RSTX}=3.3V, V_{MUTEX}=3.3V, f=1kHz, fs=48kHz, R_L=8Ω, DSP: Through, Driver Gain (G_{DRV}) =26dB
Measured by ROHM designed 4 layers board *(Note 12)*

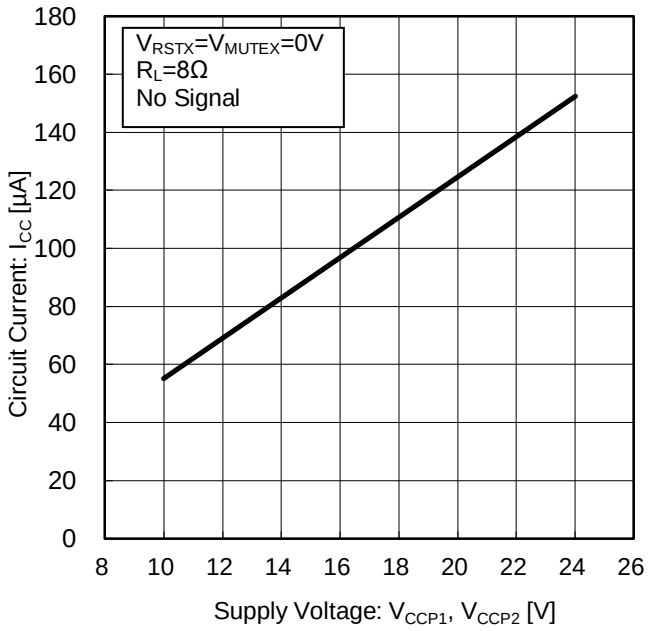


Figure 4. Circuit Current vs Supply Voltage

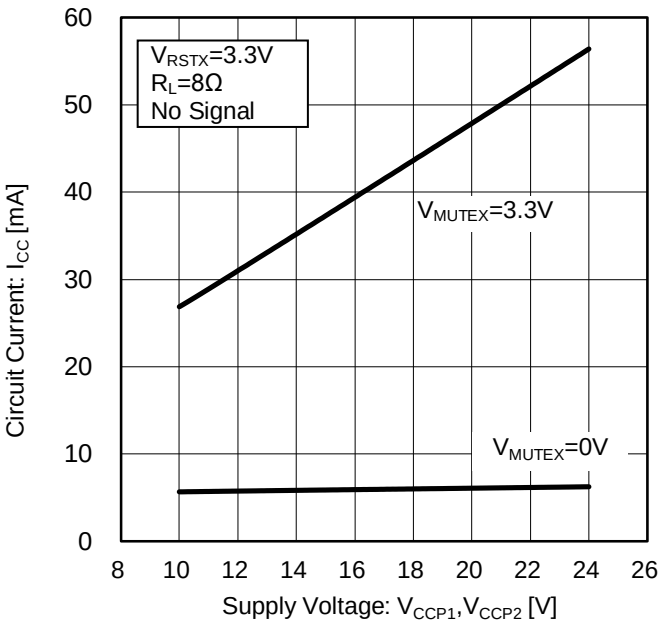


Figure 5. Circuit Current vs Supply Voltage

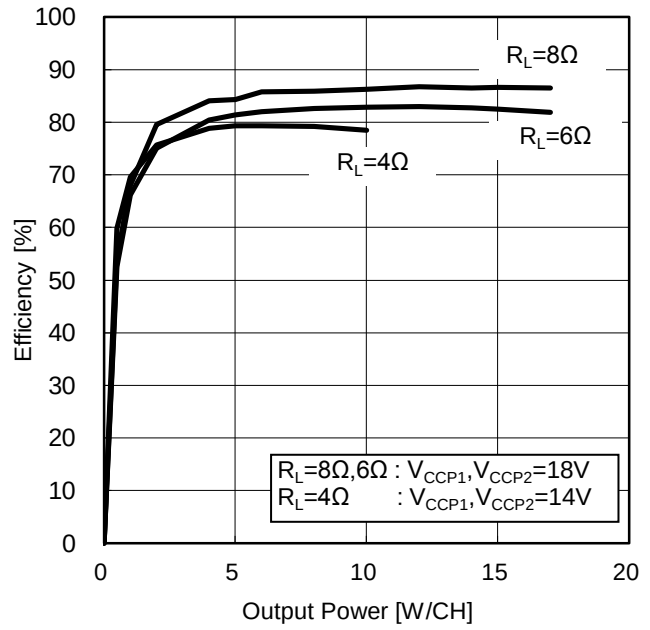


Figure 6. Efficiency vs Output Power

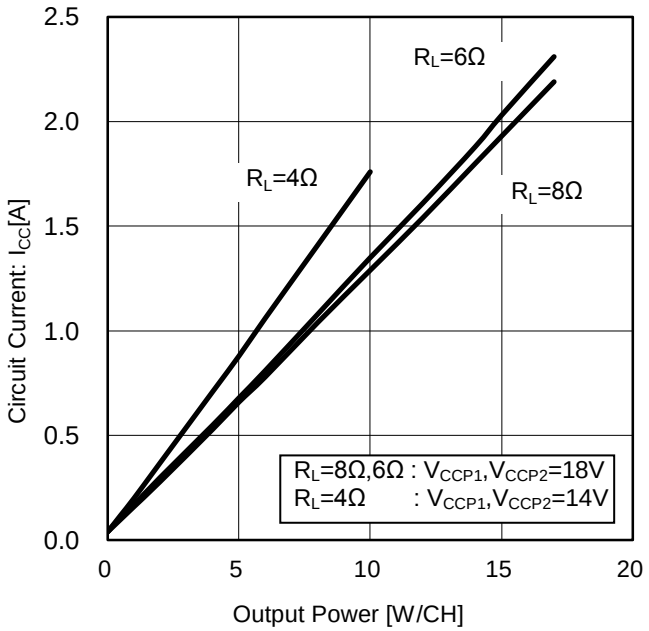


Figure 7. Circuit Current vs Output Power

(Note 12) 100mmx100mmx1.6mm FR4 4-layer glass epoxy board Cu Thickness 35μm/70μm/70μm/35μm For Application Evaluation Board

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Typical Performance Curves - continued

Unless otherwise specified Ta=25°C, V_{CCP1}, V_{CCP2}=18V, V_{DVDD}=3.3V, V_{RSTX}=3.3V, V_{MUTEX}=3.3V, f=1kHz, fs=48kHz, R_L=8Ω, DSP: Through, Driver Gain (G_{DRV}) =26dB
Measured by ROHM designed 4 layers board*(Note 12)*

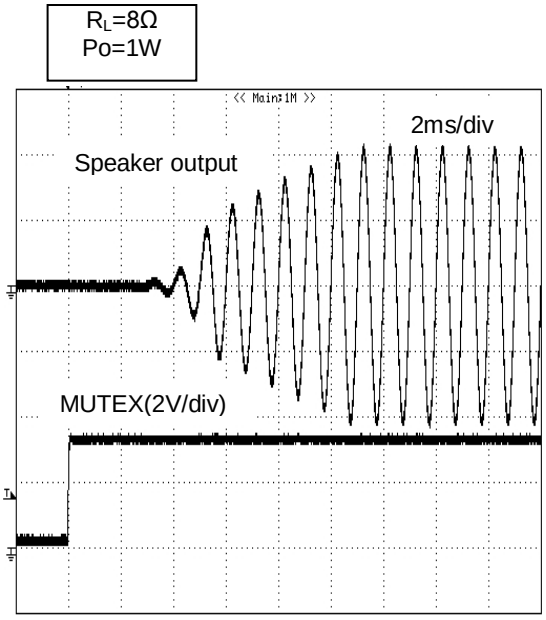


Figure 8. Waveform at soft start

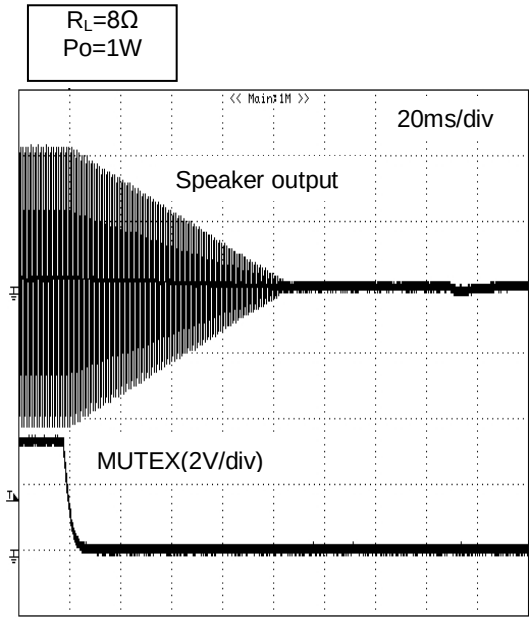


Figure 9. Waveform at soft mute

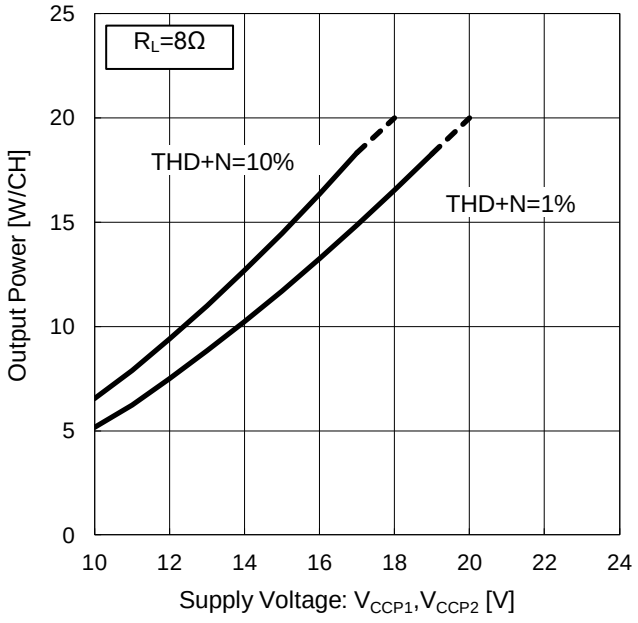


Figure 10. Output Power vs Supply Voltage

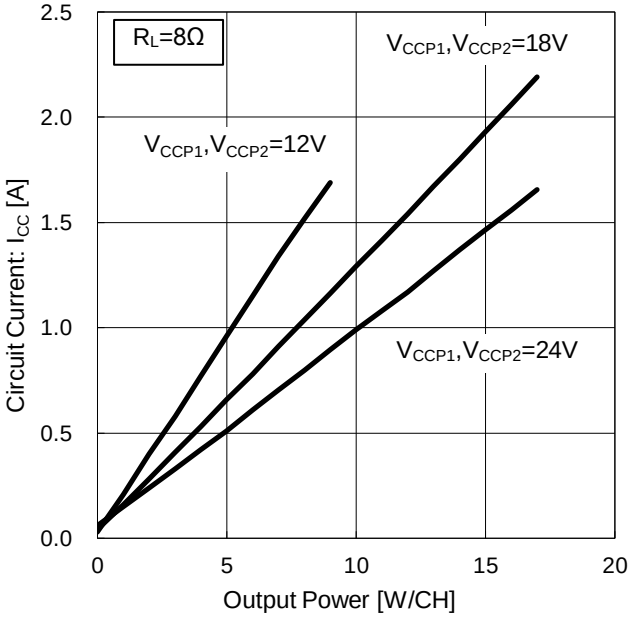


Figure 11. Circuit Current vs Output Power

Caution 1: Dotted line means exceeding maximum junction temperature.In that case heat dissipation measures such as the heat sink are necessary separately.
Caution 2: Use this LSI in 20W or less output power even with heat dissipation measures.

(Note 12) 100mmx100mmx1.6mm FR4 4-layer glass epoxy board Cu Thickness 35µm/70µm/70µm/35µm For Application Evaluation Board

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Typical Performance Curves - continued

Unless otherwise specified Ta=25°C, V_{CCP1}, V_{CCP2}=18V, V_{DVDD}=3.3V, V_{RSTX}=3.3V, V_{MUTEX}=3.3V, f=1kHz, fs=48kHz,
DSP: Through, Driver Gain (G_{DRV}) =26dB
Measured by ROHM designed 4 layers board*(Note 12)*

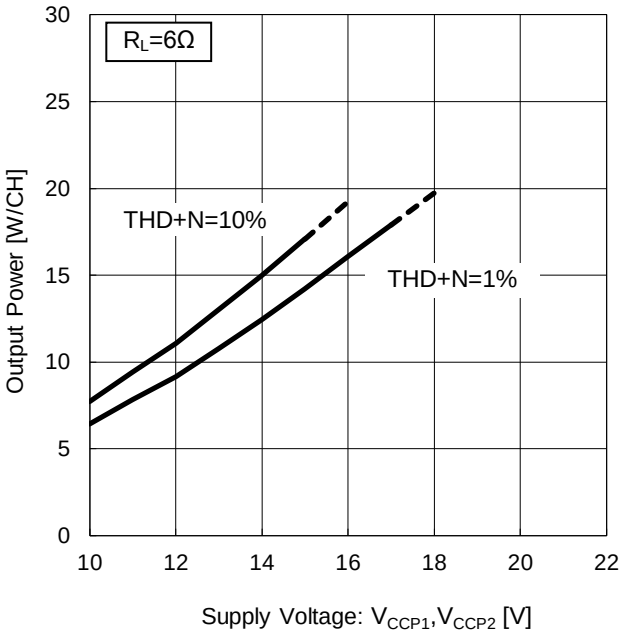


Figure 12. Output Power vs Supply Voltage

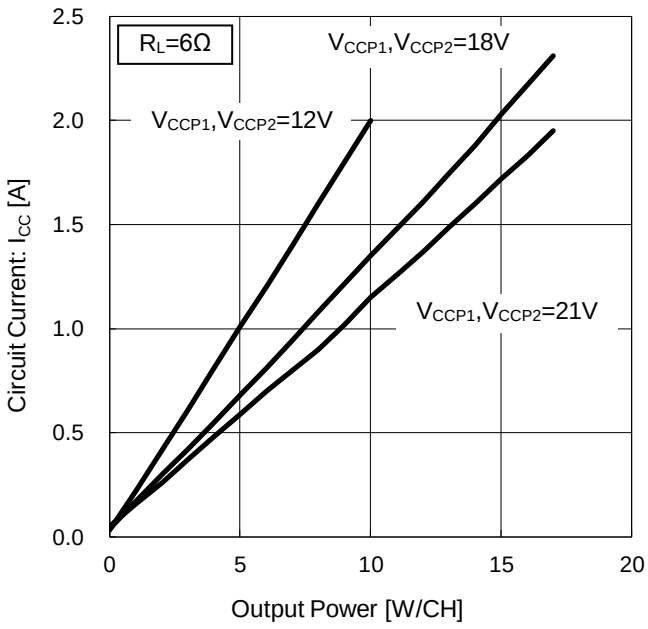


Figure 13. Circuit Current vs Output Power

Caution 1: Dotted line means exceeding maximum junction temperature.In that case heat dissipation measures such as the heat sink are necessary separately.
Caution 2: Use this LSI in 20W or less output power even with heat dissipation measures.

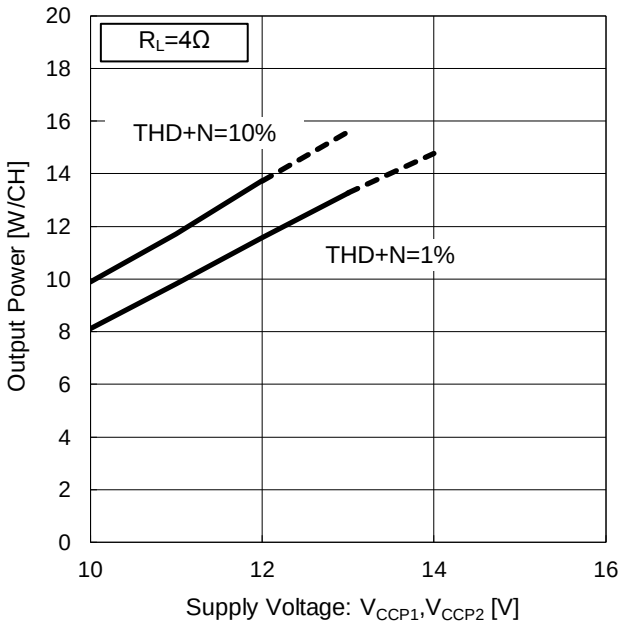


Figure 14. Output Power vs Supply Voltage

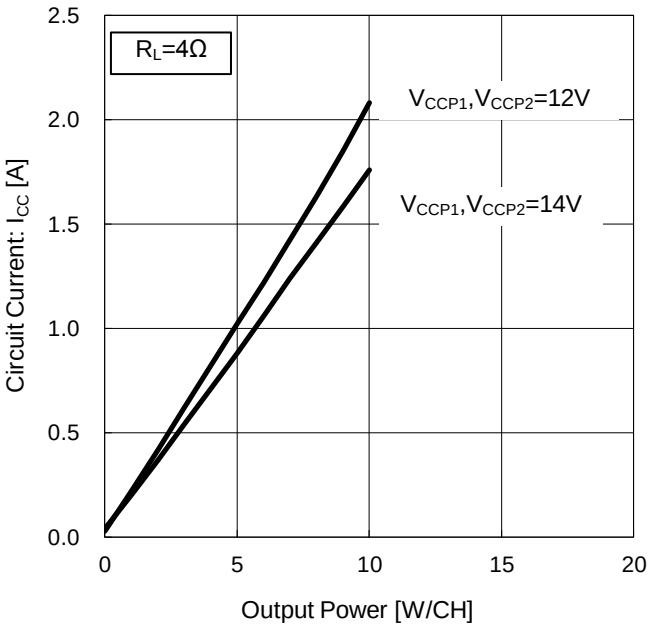


Figure 15. Circuit Current vs Output Power

Caution 1: Dotted line means exceeding maximum junction temperature.In that case heat dissipation measures such as the heat sink are necessary separately.
Caution 2: Use this LSI in 15W or less output power even with heat dissipation measures.

(Note 12) 100mmx100mmx1.6mm FR4 4-layer glass epoxy board Cu Thickness 35µm/70µm/70µm/35µm For Application Evaluation Board

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Typical Performance Curves - continued

Unless otherwise specified Ta=25°C, V_{CCP1}, V_{CCP2}=18V, V_{DVDD}=3.3V, V_{RSTX}=3.3V, V_{MUTEX}=3.3V, f=1kHz, fs=48kHz, R_L=8Ω, DSP: Through, Driver Gain (G_{DRV}) =26dB
Measured by ROHM designed 4 layers board *(Note 12)*

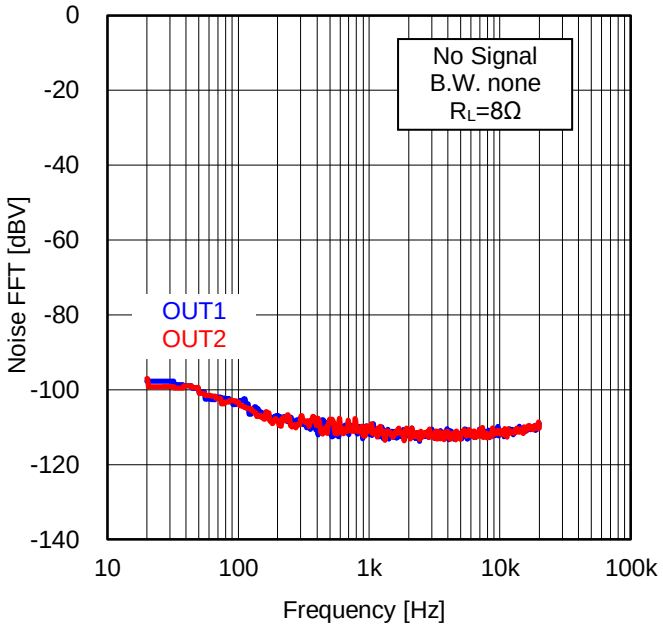


Figure 16. Noise FFT vs Frequency

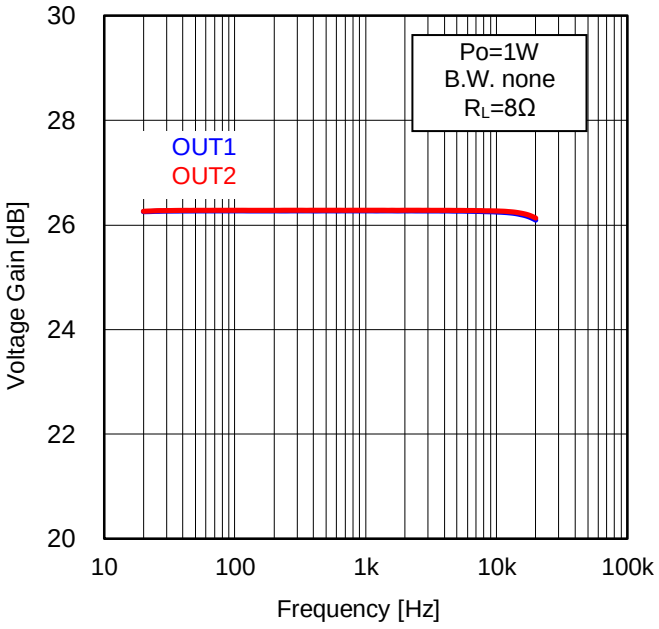


Figure 17. Voltage Gain vs Frequency

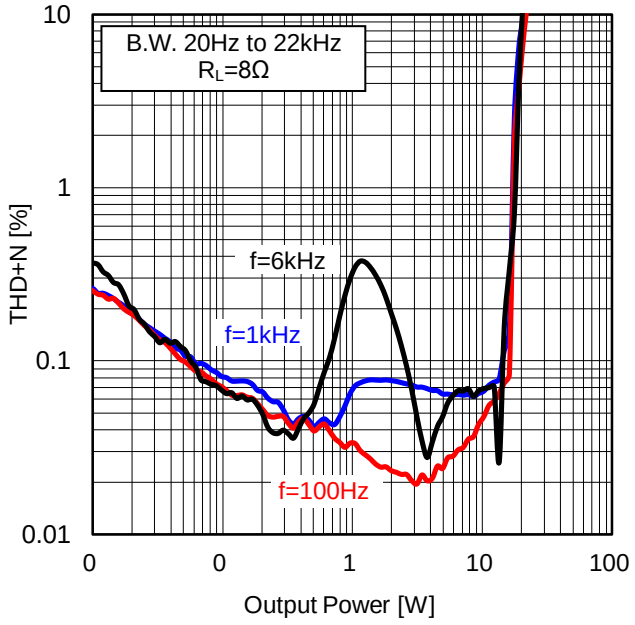


Figure 18. THD+N vs Output Power

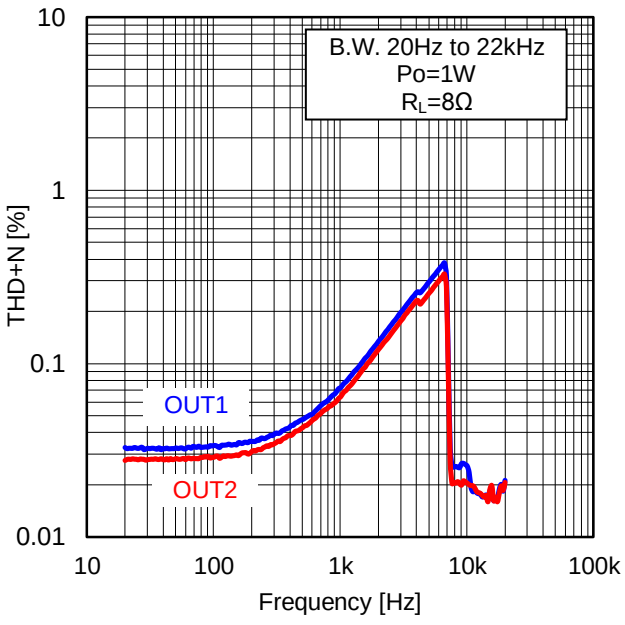


Figure 19. THD+N vs Frequency

(Note 12) 100mmx100mmx1.6mm FR4 4-layer glass epoxy board Cu Thickness 35µm/70µm/70µm/35µm For Application Evaluation Board

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Typical Performance Curves - continued

Unless otherwise specified Ta=25°C, V_{CCP1}, V_{CCP2}=18V, V_{DVDD}=3.3V, V_{RSTX}=3.3V, V_{MUTEX}=3.3V, f=1kHz, fs=48kHz, R_L=8Ω, DSP: Through, Driver Gain (G_{DRV}) =26dB
Measured by ROHM designed 4 layers board*(Note 12)*

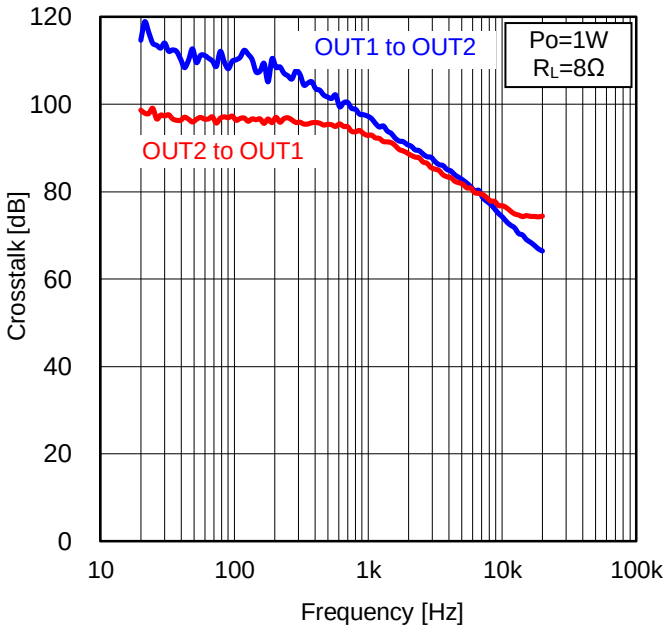


Figure 20. Crosstalk vs Frequency

(Note 12) 100mmx100mmx1.6mm FR4 4-layer glass epoxy board Cu Thickness 35µm/70µm/70µm/35µm For Application Evaluation Board

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Typical Performance Curves - continued

Unless otherwise specified Ta=25°C, V_{CCP1}, V_{CCP2}=18V, V_{DVDD}=3.3V, V_{RSTX}=3.3V, V_{MUTEX}=3.3V, f=1kHz, fs=48kHz, R_L=6Ω, DSP: Through, Driver Gain (G_{DRV}) =26dB
Measured by ROHM designed 4 layers board*(Note 12)*

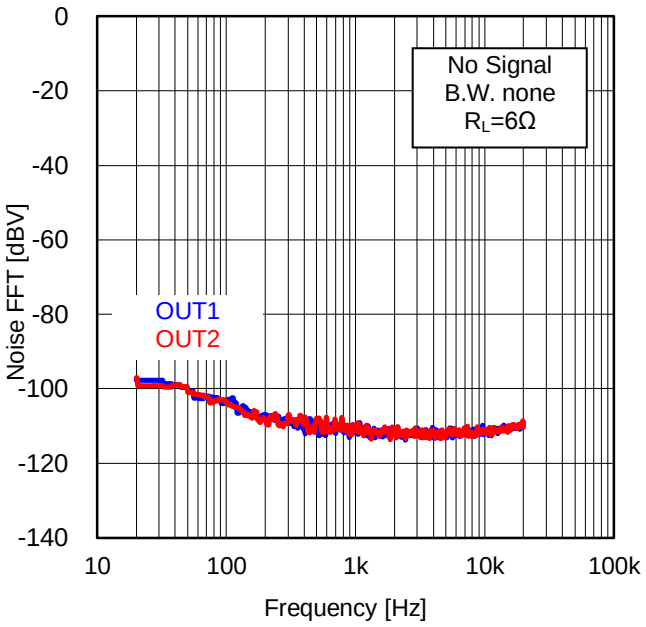


Figure 21. Noise FFT vs Frequency

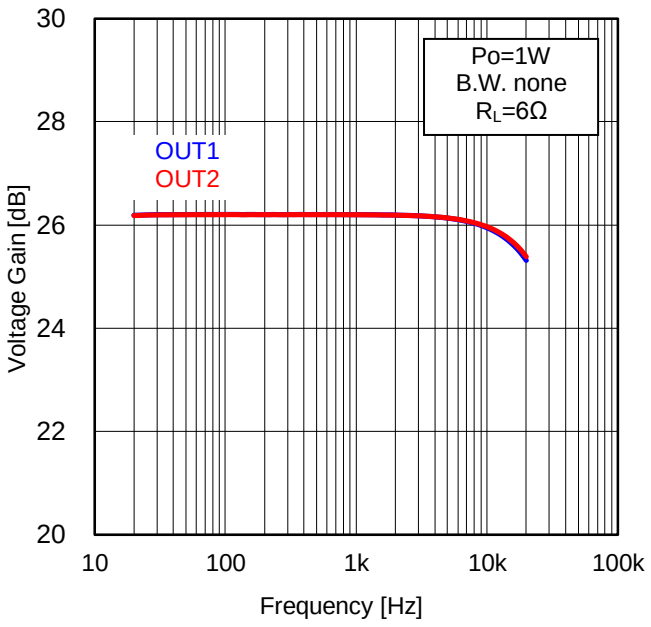


Figure 22. Voltage Gain vs Frequency

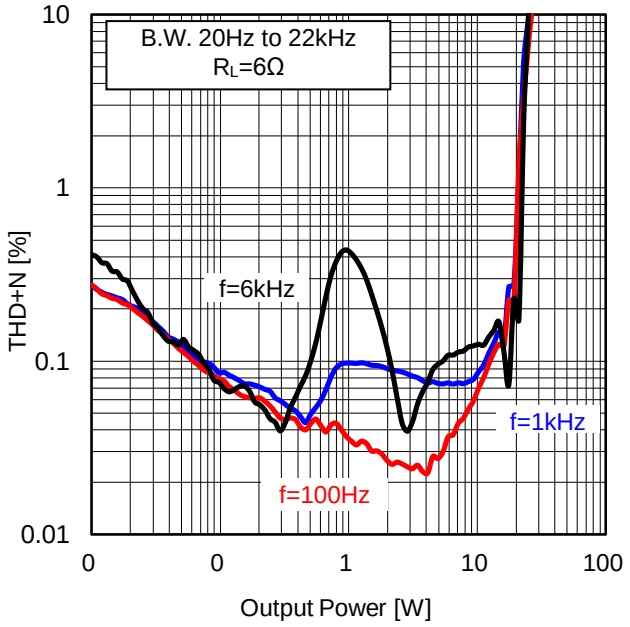


Figure 23. THD+N vs Output Power

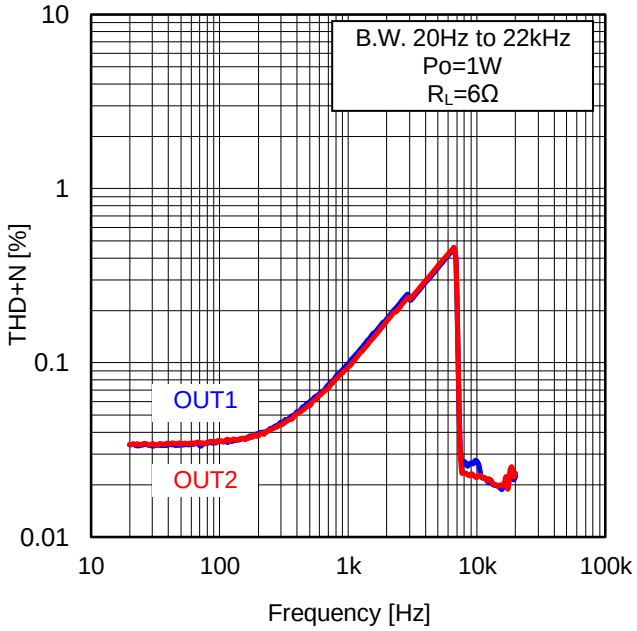


Figure 24. THD+N vs Frequency

(Note 12) 100mmx100mmx1.6mm FR4 4-layer glass epoxy board Cu Thickness 35µm/70µm/70µm/35µm For Application Evaluation Board

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Typical Performance Curves - continued

Unless otherwise specified Ta=25°C, V_{CCP1}, V_{CCP2}=18V, V_{DVDD}=3.3V, V_{RSTX}=3.3V, V_{MUTEX}=3.3V, f=1kHz, fs=48kHz, R_L=6Ω, DSP: Through, Driver Gain (G_{DRV}) =26dB
Measured by ROHM designed 4 layers board*(Note 12)*

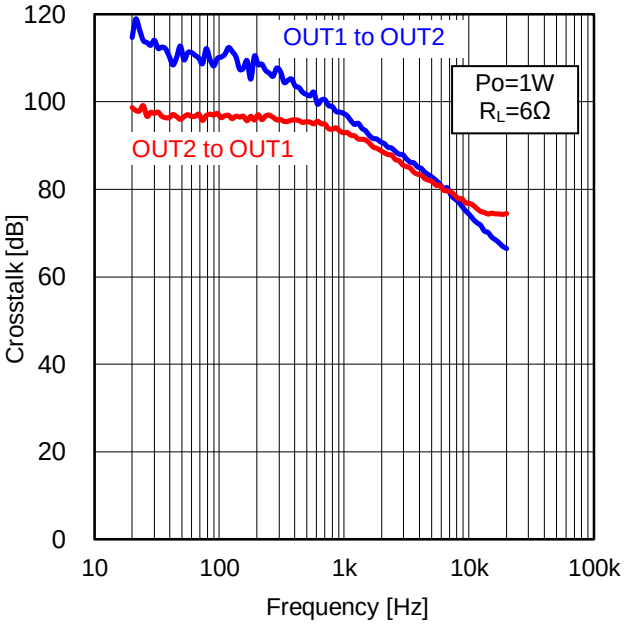


Figure 25. Crosstalk vs Frequency

(Note 12) 100mmx100mmx1.6mm FR4 4-layer glass epoxy board Cu Thickness 35µm/70µm/70µm/35µm For Application Evaluation Board

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Typical Performance Curves - continued

Unless otherwise specified Ta=25°C, V_{CCP1}, V_{CCP2}=18V, V_{DVDD}=3.3V, V_{RSTX}=3.3V, V_{MUTEX}=3.3V, f=1kHz, fs=48kHz, R_L=4Ω, DSP: Through, Driver Gain (G_{DRV}) =26dB
Measured by ROHM designed 4 layers board*(Note 12)*

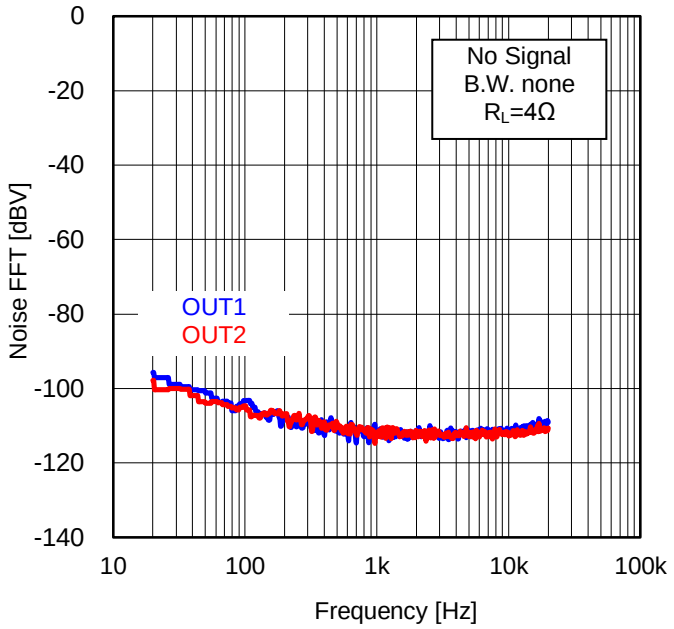


Figure 26. Noise FFT vs Frequency

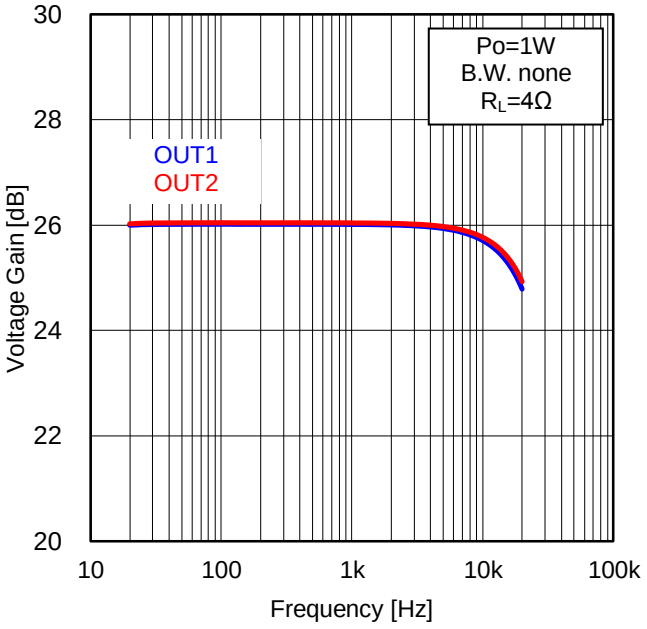


Figure 27. Voltage Gain vs Frequency

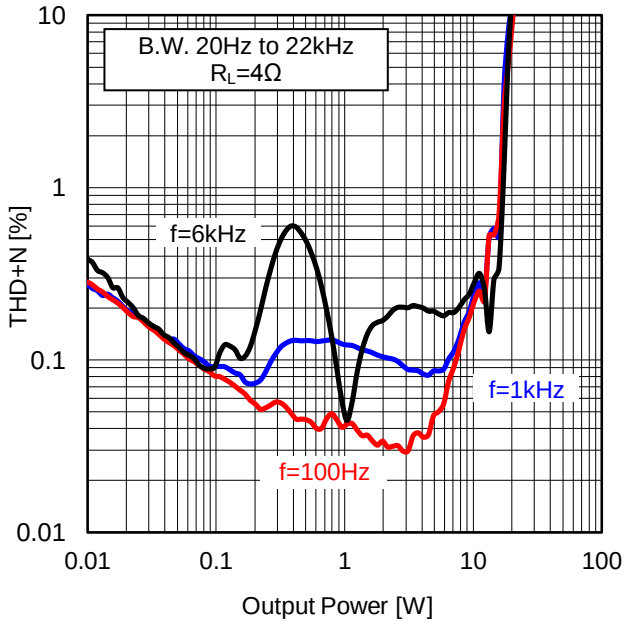


Figure 28. THD+N vs Output Power

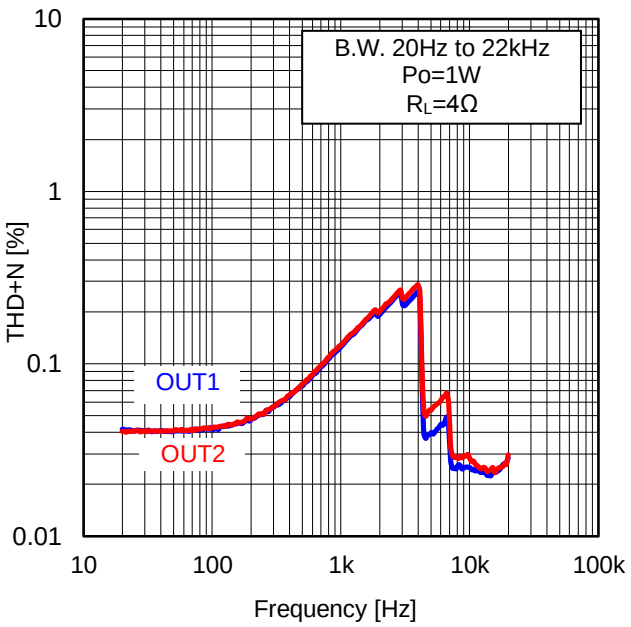


Figure 29. THD+N vs Frequency

(Note 12) 100mmx100mmx1.6mm FR4 4-layer glass epoxy board Cu Thickness 35µm/70µm/70µm/35µm For Application Evaluation Board

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Typical Performance Curves - continued

Unless otherwise specified Ta=25°C, V_{CCP1}, V_{CCP2}=18V, V_{DVDD}=3.3V, V_{RSTX}=3.3V, V_{MUTEX}=3.3V, f=1kHz, fs=48kHz, R_L=4Ω, DSP: Through, Driver Gain (G_{DRV}) =26dB
Measured by ROHM designed 4 layers board*(Note 12)*

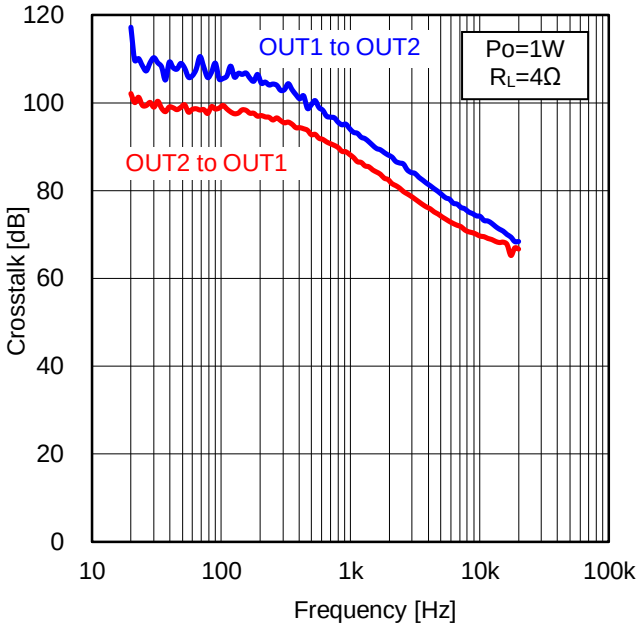


Figure 30. Crosstalk vs Frequency

(Note 12) 100mmx100mmx1.6mm FR4 4-layer glass epoxy board Cu Thickness 35µm/70µm/70µm/35µm For Application Evaluation Board

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Description of Function

1 DSP Block Functional Overview

No.	Function	Specification
1	Pre-Scaler	•Lch/Rch become same set point. •+48dB to -79dB (0.5dB step), -infinity dB
2	Channel Mixer	•It is able to set mixing of Left and Right channel which are inputted digital signal to Audio DSP •Selectable in L, (L+R) /2, L-R, R, MUTE
3	12 Band BQ	•12 Band Bi-quad (BQ) type filter. •Only 5 coefficients are required. (b0, b1, b2, a1, a2) •Lch/Rch dependent or independent. •The Filter types which can be attained are Peaking/Low-shelf/High-shelf/Low-pass/High-pass/All-pass/Notch. •There is soft transition function.
4	Fine Master Volume	•Lch/Rch become same set point or independent set. •+24dB to -103dB (0.125dB step), -infinity dB •There are soft transition and soft mute functions.
5	3 Band DRC	•There are 3 band DRC. •It is possible to set the slope of compression level.
6	Post-scaler	•Lch/Rch become same set point. •+48dB to -79dB (0.5dB step), -infinity dB
7	Fine Post-scaler	•Lch/Rch become independent set point. •+0.7dB to -0.8dB (0.1dB step)
8	DC cut HPF	•1st order HPF •Cut OFF frequency fc: 1Hz
9	Hard Clipper	•Lch/Rch become same set point. •Clip level: 0dB to -22.5dB (-0.1dB step)

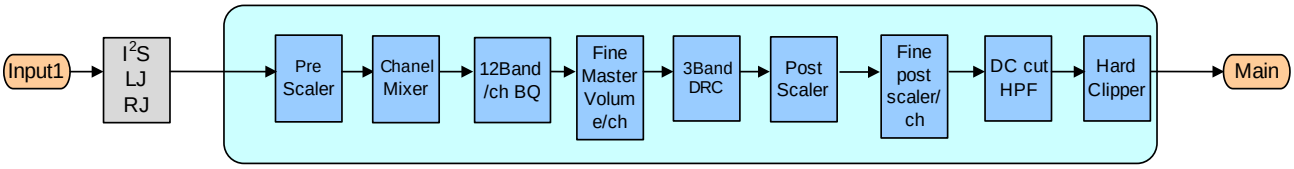


Figure 31. DSP Block Diagram

About description of the register setting the register value is written at hex.
Also, the value with blue background is initial value.

2 RSTX Pin*(Note 13) (Note 14)* , MUTEX Pin Function

RSTX (29pin)	MUTEX (30pin)	DSP Block	Speaker Output (OUT1P, OUT1N, OUT2P, OUT2N)
Low	Low	Reset ON	High-Z_low*(Note 15)* (Low power consumption)
High	Low	Normal operation (Mute ON)	High-Z_low*(Note 15)* (Mute ON) *(Note 16)*
High	High	Normal operation (Mute OFF)	Normal operation (Mute OFF)
Low	High	Don't use.	

(Note 13) When RSTX is set to low, internal registers are initialized.
(Note 14) If V_{DVDD} is under 3V, RSTX is set to low once for 10ms (Min), and set to high again. Then DSP is needed to set parameter again.
(Note 15) This means that all output transistors are OFF and output pins are pulled down by 10kΩ (Typ).
(Note 16) Speaker output becomes High-Z_low after elapse of PWM stop time after setting MUTEX Low.
Refer to PWM Sampling Frequency in next page for PWM stop time.

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Description of Function - continued

3 PWM Sampling Frequency

PWM sampling frequency of speaker output, Soft mute time, Soft start time and PWM stop time depend on sampling frequency (f_S) of the digital audio signal. These transition times are changed by sending the data to select address 0x15[1:0].

Default=0x3

Sampling frequency (f_S)	PWM Sampling Frequency	0x15[1:0] Value	Soft Mute Time	Soft Start Time	PWM Stop Time
48kHz	384kHz	0x0	10.7ms	10.7ms	86ms
		0x1	21.4ms	10.7ms	106ms
		0x2	42.7ms	10.7ms	125ms
		0x3	85.4ms	10.7ms	162ms
44.1kHz	352.8kHz	0x0	11.7ms	11.7ms	93ms
		0x1	23.3ms	11.7ms	113ms
		0x2	46.5ms	11.7ms	135ms
		0x3	92.9ms	11.7ms	177ms
32 kHz	256kHz	0x0	16.1ms	16.1ms	116ms
		0x1	32.1ms	16.1ms	148ms
		0x2	64.1ms	16.1ms	178ms
		0x3	128.1ms	16.1ms	241ms

4 Setting Driver Gain (G_{DRV})

It can change the driver gain of the output FET driver part.
Set it depending on speaker used because the maximum output level changes by speaker load impedance value.

When set the driver gain, change after setting MUTEX pin to Low (>PWM stop time).
Pop noise may be occurred if the driver gain is set while MUTEX=High.

Default=0x03

Select Address	Value	Driver Gain G_{DRV} (BTL)
0xF3[7:0]	0x03	26dB (Typ)
0xF3[7:0]	0x0B	32dB (Typ)

Regarding 0xF3 address,
Prohibit to set except data 0x03 and 0x0B to address 0xF3.
The setting value is fixed by transmitting 0xF8=0x01. If the setting value of address 0xF3 is changed, certainly set 0xF8=0x01 again. In addition, wait time more than 10ms is necessary after 0xF8=0x01 setting.

5 Setting of When Monaural output

When monaural output setting is applied as shown in Application Circuit Example3, set 0xF2 register during start-up (Refer to P.62 “20. The wake-up Procedure of power-up”).
Setting 0xF2=0x0A, DC voltage protection function at the speaker of OUT2 side can be disabled, therefore it is possible to use Application Circuit Example3.

Default=0x02

Select Address	Value	PWM Output
0xF2[7:0]	0x02	Stereo
0xF2[7:0]	0x0A	Monaural

Regarding 0xF2 address,
Prohibit to set except data 0x02 and 0x0A to address 0xF2.
The setting value is fixed by transmitting 0xF8=0x01. If the setting value of address 0xF2 is changed, certainly set 0xF8=0x01 again. In addition, wait time more than 10ms is necessary after 0xF8=0x01 setting.

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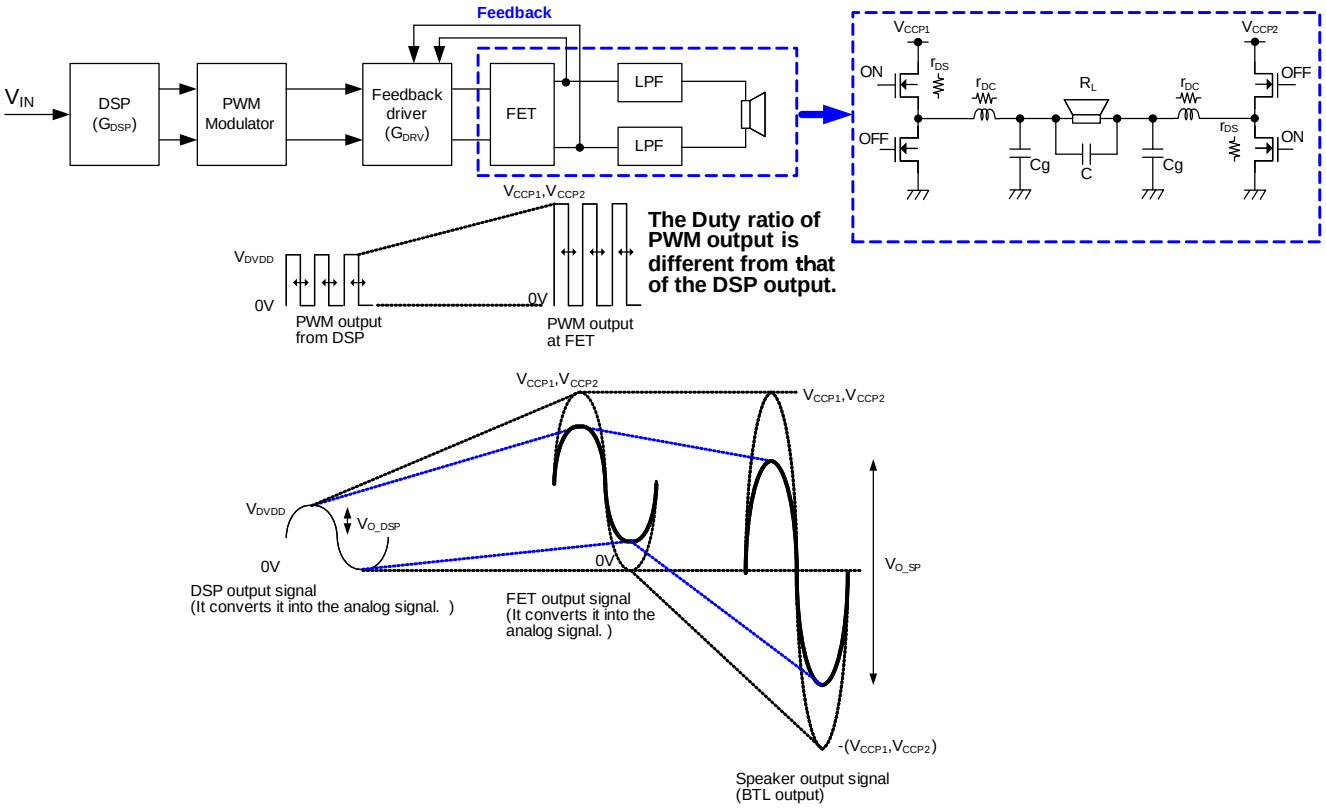
Description of Function - continued

6 Level Diagram

$$(1)\,DSP\,Gain = 10^{\left(\frac{V_{IN}+G_{DSP}}{20}\right)}$$

$$(2)\,Driver\,Gain(BTL) = 10^{\left(\frac{G_{DRV}}{20}\right)}$$

$$(3)\,Loss = \frac{R_L}{2(r_{DS}+r_{DC})+R_L}$$



$$V_{O_DSP} = 10^{\left(\frac{V_{IN}+G_{DSP}}{20}\right)} \text{ [Vrms]}$$

$$V_{O_SP} = V_{O_DSP} \times 10^{\left(\frac{G_{DRV}}{20}\right)} \times \frac{R_L}{2(r_{DS}+r_{DC})+R_L} \text{ [Vrms]}$$

$$P_{O(THD=1\%)} = \frac{\left[10^{\left(\frac{V_{IN}+G_{DSP}}{20}\right)} \times 10^{\left(\frac{G_{DRV}}{20}\right)} \times \frac{R_L}{2(r_{DS}+r_{DC})+R_L}\right]^2}{R_L} \text{ [W]}$$

$$P_{O(THD=10\%)} = P_{O(THD=1\%)} \times 1.25 \text{ [W]}$$

V_{IN}	: I²S input level [dBFS]
G_{DSP}	: DSP gain [dB]
G_{DRV}	: Feedback driver gain [dB]
V_{CCP1},V_{CCP2}	: Power supply voltage for power amp [V]
V_{DVDD}	: Power supply voltage for DSP [V]
R_L	: Speaker load resistance [Ω]
r_{DS}	: Output FET on resistance [Ω] (Typ=0.23Ω)
r_{DC}	: Direct current resistance of coil [Ω]

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Description of Function - continued

7 2 Wire Bus Control Signal Specification

7.1 Electrical Characteristics and Timing of Bus Line and I/O Stage

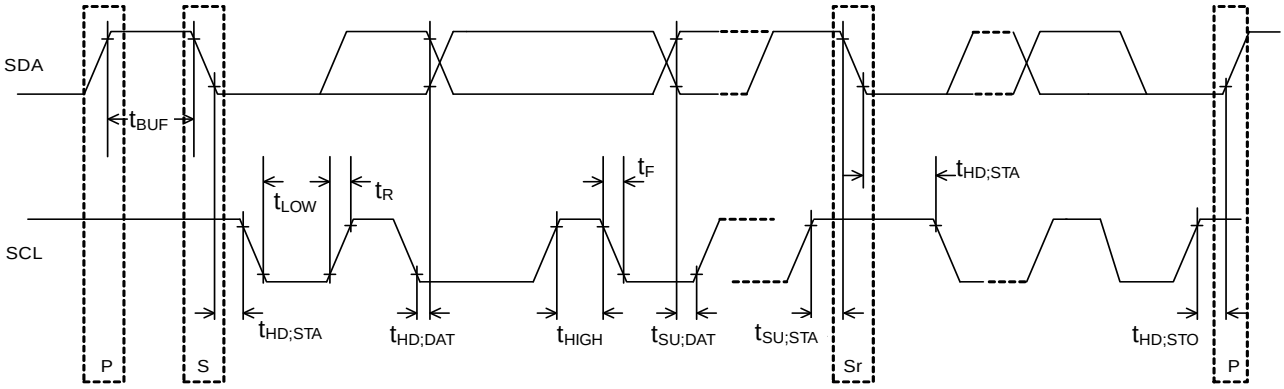


Figure 32

SDA and SCL bus line characteristics(Note 18) (Unless otherwise specified Ta=25°C, V_{DVDD}=3.3V)

	Parameter	Symbol	High Speed Mode		Unit
			Min	Max	
1	SCL Clock Frequency	f_{SCL}	0	400	kHz
2	Bus Free Time between a STOP and START Condition	t_{BUF}	1.3	-	µs
3	Hold Time (repeated) START Condition. After this period, the first clock pulse is generated.	$t_{HD;STA}$	0.6	-	µs
4	Low Period of the SCL Clock	t_{LOW}	1.3	-	µs
5	High Period of the SCL Clock	t_{HIGH}	0.6	-	µs
6	Set-up Time for a Repeated START Condition	$t_{SU;STA}$	0.6	-	µs
7	Data Hold Time	$t_{HD;DAT}$	0(Note 17)	-	µs
8	Data Set-up Time	$t_{SU;DAT}$	250	-	ns
9	Rise Time of both SDA and SCL Signals	t_R	20+0.1Cb	300	ns
10	Fall Time of both SDA and SCL Signals	t_F	20+0.1Cb	300	ns
11	Set-up Time for STOP Condition	$t_{SU;STO}$	0.6	-	µs
12	Capacitive Load for each Bus Line	Cb	-	400	pF

Caution: The above-mentioned numerical values are all the values corresponding to V_{IHmin} and the V_{ILmax} level.
(Note 17) To exceed an undefined area on the fall-edge of SCL (Refer to V_{IH} min of the SCL signal) , the transmitting set like SoC should internally offer the holding time of 300ns or more for the SDA signal.
(Note 18) SCL and SDA pin is not corresponding to threshold tolerance of 5V.
Use it within Input voltage 1 of the absolute maximum rating.

7.2 Command Interface

2 wire Bus Control is used for command interface between host CPU. It not only writes but also it is possible to read it excluding a part of register. In addition to Slave Address, set and write 1 byte of Select Address to read out the data. 2 wire bus Slave mode format is illustrated below.

	MSB LSB		MSB LSB		MSB LSB		
S	Slave Address	A	Select Address	A	Data	A	P

Figure 33

S:	Start Condition
Slave Address:	Data of 8bit in total is sent with a bit of Read mode (High) or Write mode (Low) after slave Address (7bit) set by ADDR pin. (MSB first)
A:	Acknowledge-bit will be added byte per byte in the data that acknowledge is sent and received. Low will be sent and received when the data is correctly sent and received. There was no acknowledgement for High.
Select Address:	Use 1byte of select address. (MSB first)
Data:	Sent and received data-byte data. (MSB first)
P:	Stop Condition

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Command Interface - continued

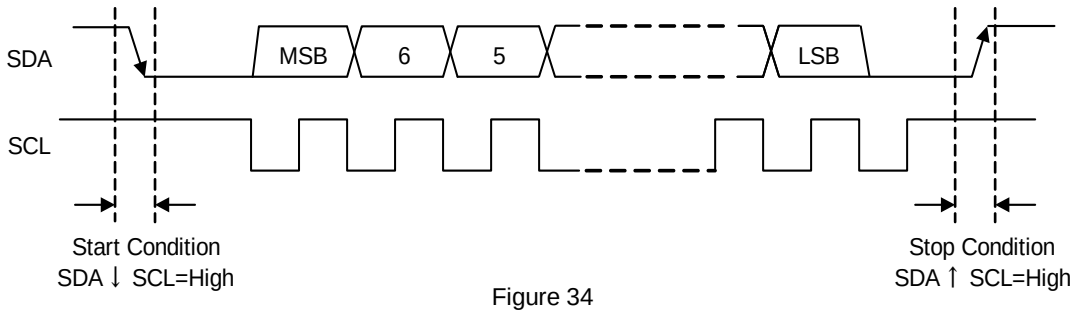


Figure 34

7.3 Slave Address

•While ADDR Pin is Low

MSB LSB

A6	A5	A4	A3	A2	A1	A0	R/W
1	0	0	0	0	0	0	1/0

•While ADDR Pin is High

MSB LSB

A6	A5	A4	A3	A2	A1	A0	R/W
1	0	0	0	0	0	1	1/0

Figure 35

7.4 Writing of Data

•Basic format

S	Slave Address	A	Select Address	A	Data	A	P

: Master to Slave, : Slave to Master

•Auto-increment format

S	Slave Address	A	Select Address	A	Data 1	A	Data 2	A	Data 3…N	A	P

: Master to Slave, : Slave to Master

Figure 36

7.5 Reading of Data

First of all, the address (0x20 in the example) for reading is written in the register of the 0xD0 address at the time of reading. In the following stream, data is read after the slave address. Do not return the acknowledge when ending the reception.

S	Slave Address	A	Req_Addr	A	Select Address	A	P
(ex.)	0x80		0xD0		0x20		

S	Slave Address	A	Data 1	A	Data 2	A		A	Data N	Ā	P
(ex.)	0x81		0x**		0x**				0x**		

: Master to Slave, : Slave to Master, A: With Acknowledge, Ā: Without Acknowledge

Figure 37

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Description of Function - continued

8 Format of Digital Audio Signal

•LRCLK: It is L/R Clock Input Signal
It is available of 32kHz/44.1kHz/48kHz with those clocks (f_S) that are same to the sampling frequency (f_S).
The data of the left channel and the right channel for one sample is input to this section.

•BCLK: It is Bit Clock Input Signal
It is used for the latch of data in everyone bit by sampling frequency's 32 times frequency ($32f_S$) or 48 times frequency ($48f_S$) or 64 times sampling frequency ($64f_S$). However, if the $32f_S$ is selected, the data length is held static of 16bit.

•SDATA: It is Data Input Signal
It is amplitude data. Word length is different according to the resolution of the input digital audio signal.
It is available of 16bit/20bit/24bit.
The digital input format is available of I²S, Left-justified and Right-justified formats.
The figure below shows the timing chart of each transmission mode.

•SDATAO: Audio Data Output After DSP Processing
This output syncs with inputted LRCLK and BCLK.
Output format is available of I²S format only.

BCLK Clock $64f_S$

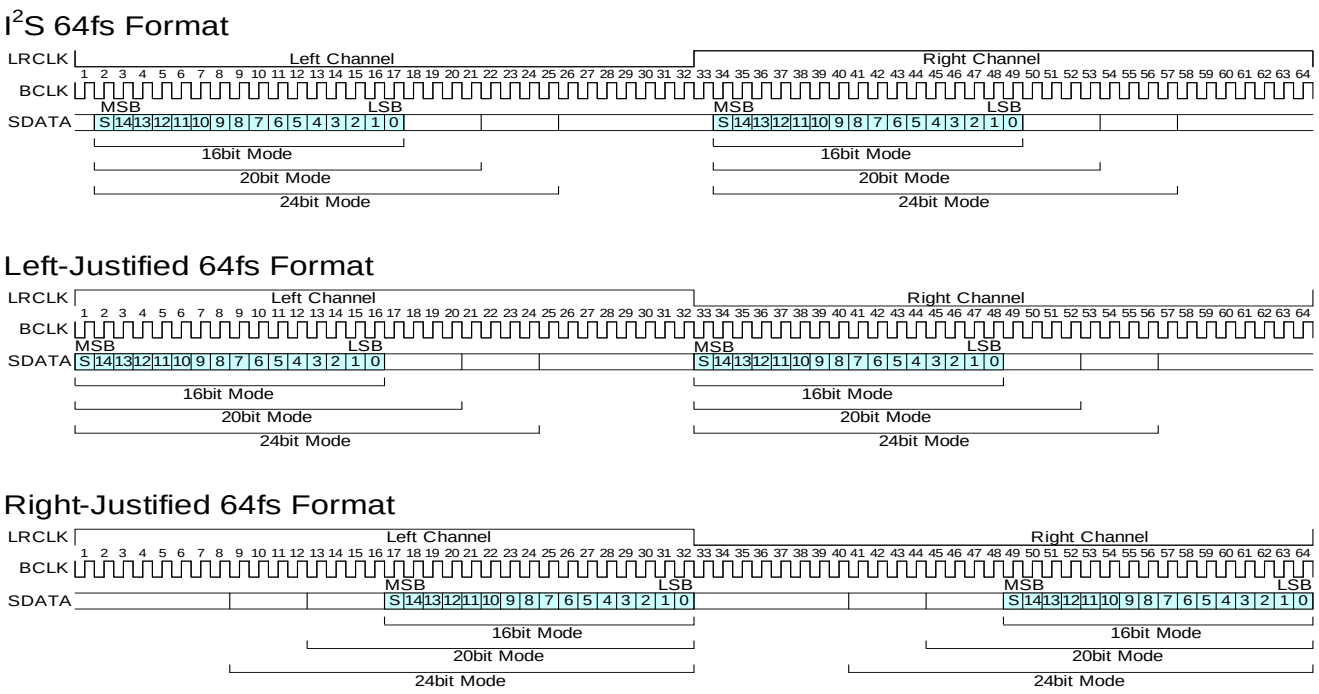


Figure 38

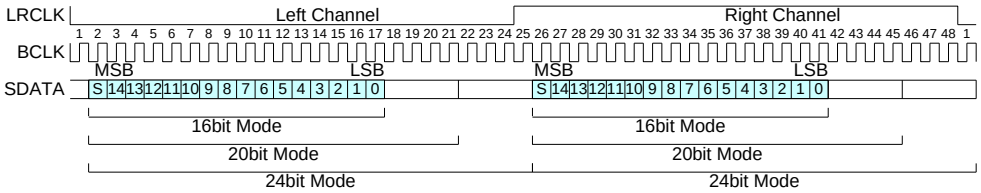
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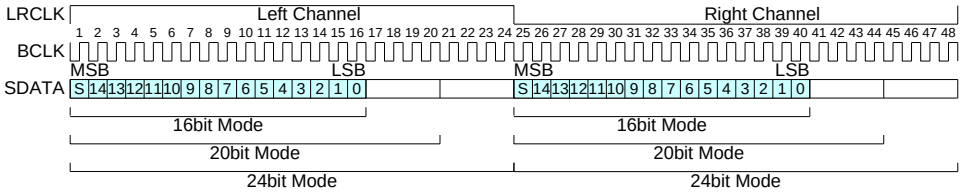
8 Format of Digital Audio Signal - continued

BCLK Clock 48f_S

I^2S 48fs Format



Left-Justified 48fs Format



Right-Justified 48fs Format

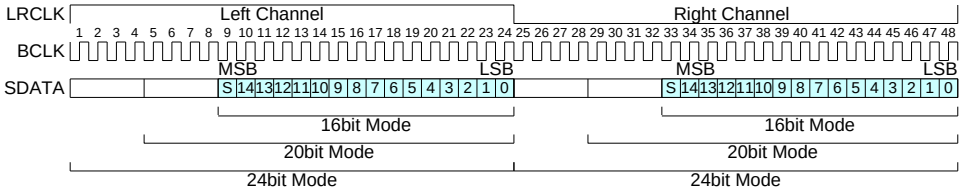
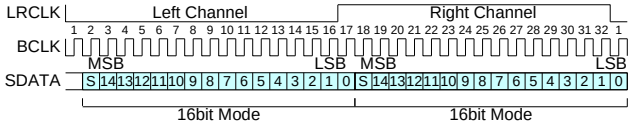


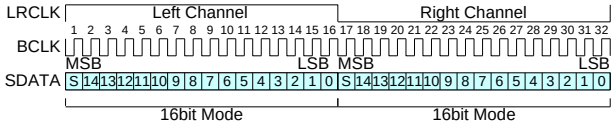
Figure 39

BCLK Clock 32f_S

I^2S 32fs Format



Left-Justified 32fs Format



Right-Justified 32fs Format

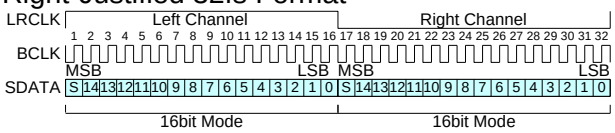


Figure 40

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Description of Function - continued

9 Format Setting for Digital Audio Signal

Set BCLK clock fs, word length and data format by transmitting command according to the inputted digital audio signal.
SDATAO output word length is able to be set independently of input word length.
It is available of I^2S format only.

BCLK Clock

Default=0x0

Select Address	Value	Explanation of Operation
0x03[5:4]	0x0	$64f_S$
	0x1	$48f_S$
	0x2	$32f_S$
	0x3	Don't use

Data Format

Default=0x0

Select Address	Value	Explanation of Operation
0x03[3:2]	0x0	I^2S format
	0x1	Left-justified format
	0x2	Right-justified format
	0x3	Don't use

Word Length

Default=0x2

Select Address	Value	Explanation of Operation
0x03[1:0]	0x0	16 bit
	0x1	20 bit
	0x2	24 bit
	0x3	Don't use

SDATAO Output Word Length

Default=0x2

Select Address	Value	Explanation of Operation
0x78[1:0]	0x0	16 bit
	0x1	20 bit
	0x2	24 bit
	0x3	Don't use

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Description of Function - continued

10 Audio Interface Format and Timing

Electrical characteristics and timing of BCLK, LRCLK and SDATA

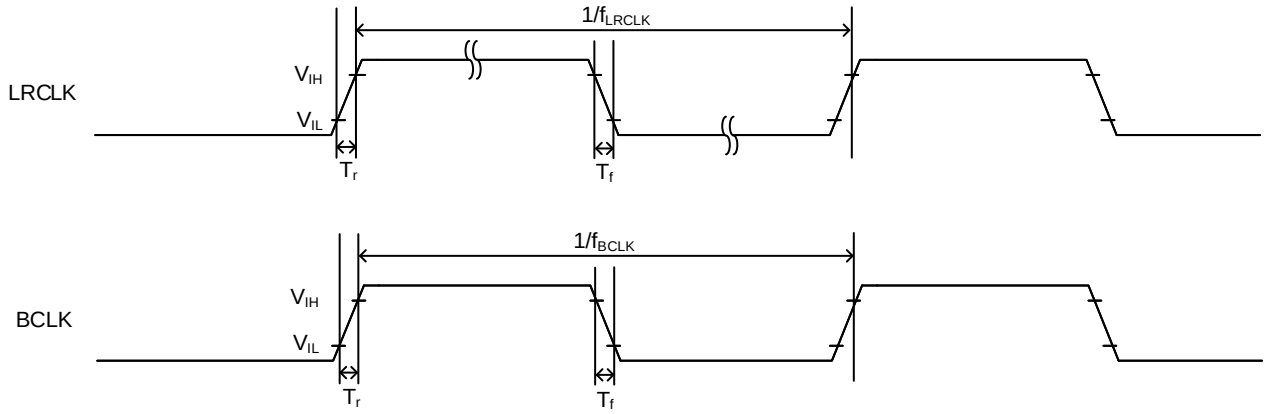
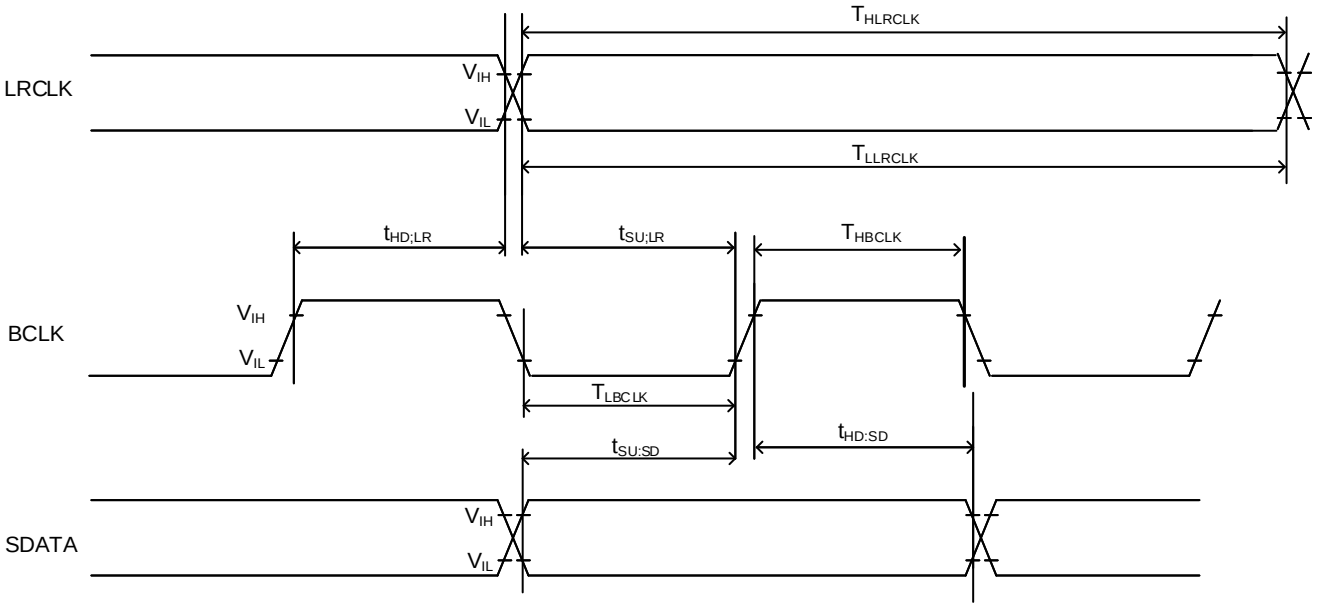


Figure 41. Clock Timing



LRCLK DUTY=f_{LRCLK} x (T_{HLRCLK} or T_{LLRCLK})
BCLK DUTY =f_{BCLK} x (T_{HBCLK} or T_{LBCLK})

Figure 42. Audio Interface Timing

No.	Parameter	Symbol	Limit		Unit
			Min	Max	
1	LRCLK Frequency	f_{LRCLK}	32 -10%	48 +10%	kHz
2	BCLK Frequency	f_{BCLK}	2.048 -10%	3.072 +10%	MHz
3	Setup Time, LRCLK*(Note 19)*	$t_{SU;LR}$	20	-	ns
4	Hold Time, LRCLK*(Note 19)*	$t_{HD;LR}$	20	-	ns
5	Setup Time, SDATA	$t_{SU;SD}$	20	-	ns
6	Hold Time, SDATA	$t_{HD;SD}$	20	-	ns
7	LRCLK, DUTY Ratio	d_{LRCLK}	40	60	%
8	BCLK, DUTY Ratio	d_{BCLK}	40	60	%
9	LRCLK, BCLK, Rise Time, Fall Time	T_r,T_f	-	12	ns

(Note 19) This regulation is to keep rising edge of LRCLK and rising edge of BCLK from overlapping.

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Description of Function - continued

11 Power Supply Start-up Sequence

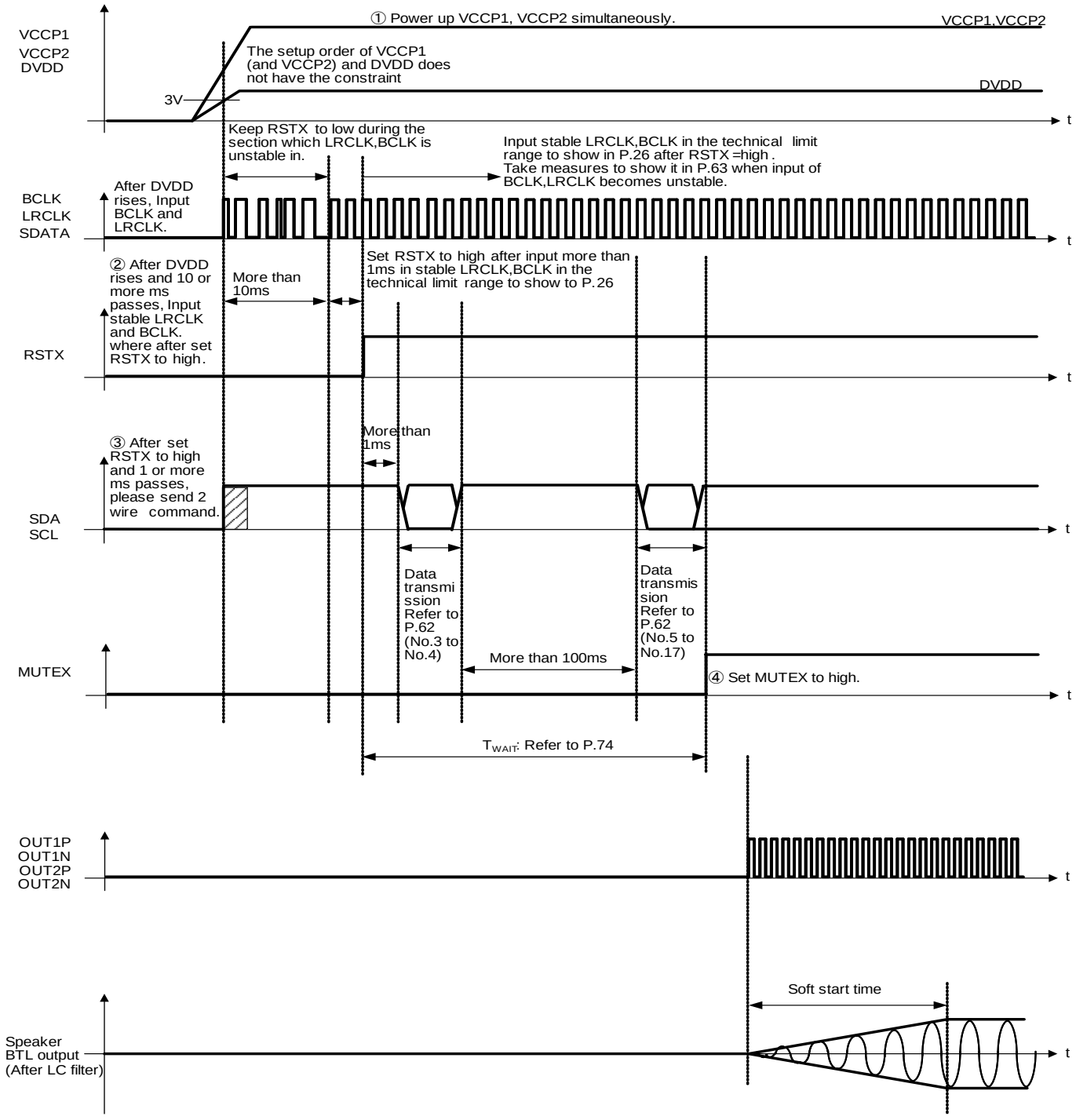


Figure 43. Power Supply Start-up Sequence

Caution 1: Refer to P.62 “20. The wake-up Procedure of power-up”.
Caution 2: Make sure to input Low to RSTX pin from external at the time power up DVDD.

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Description of Function - continued

12 Power Supply Shut-down Sequence

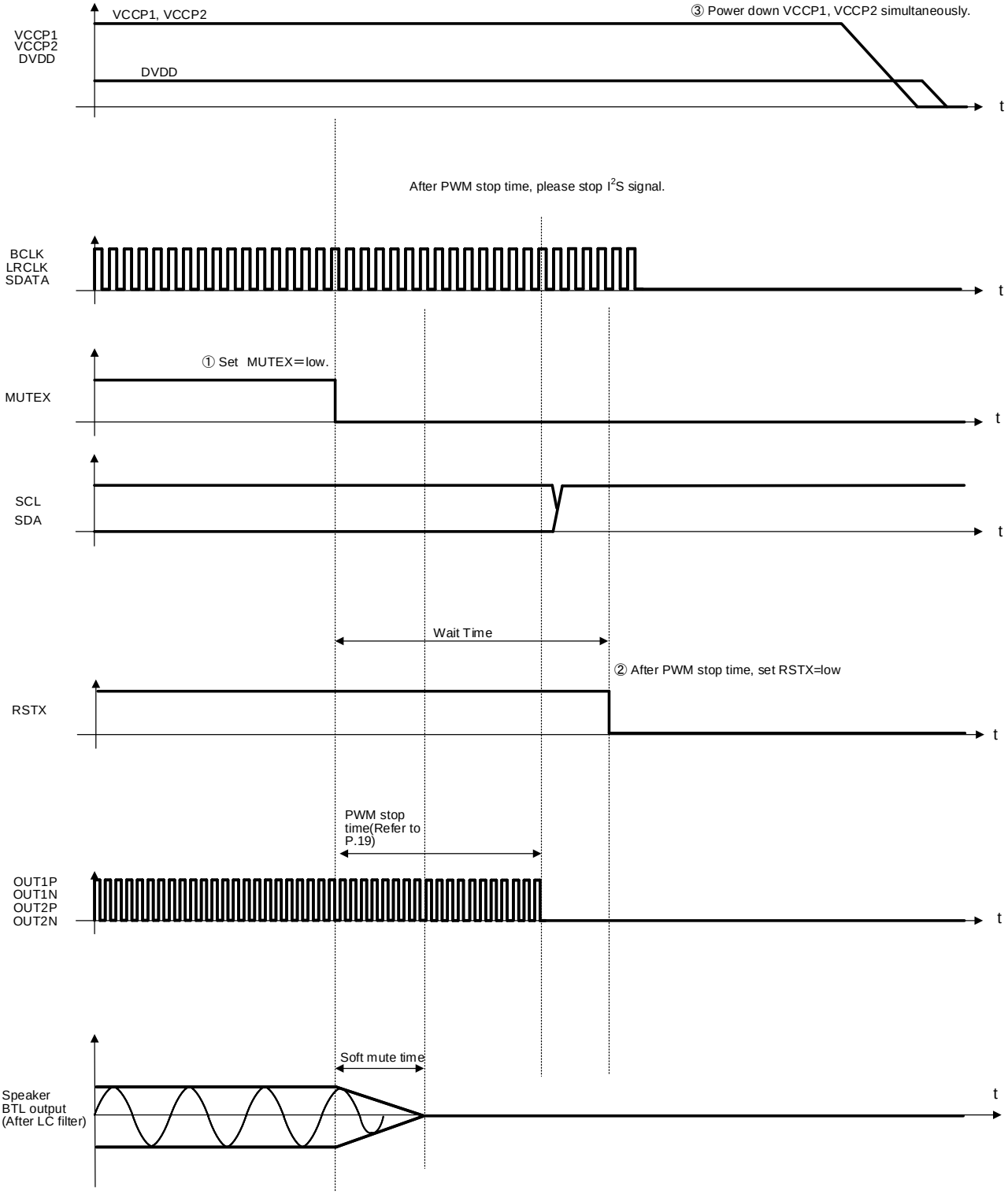


Figure 44. Power Supply Shut-down Sequence

Caution: When power supply shut-down sequence is executed, before doing RSTX Highy → Low, set MUTEX High → Low and hold Wait time > PWM stop time.

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Description of Function - continued

13 Protection Function

About ERRORX pin (Pin 13)
If LSI detects Output short protection or DC voltage protection or high temperature protection, LSI informs abnormality with ERRORX pin as Low level in the protection function operation. This is a function indicating the abnormal condition of this product.
ERRORX pin does not become Low in the case of detecting Under voltage protection or Clock stop protection.

Protection Function	Detecting & Releasing Condition		Speaker PWM Output	ERRORX Output(Note 20)
Output Short Protection	Detecting condition	Detecting current=10A (Typ)/5A (Min, Tj=85°C) /3.9A (Min, Tj=150°C)	High-Z_low (Latch) (Note 21)	Low (Latch)
DC Voltage Protection	Detecting condition	PWM output Duty ratio=0% or 100% for 42ms (Typ, f_S=48kHz) and over	High-Z_low (Latch) (Note 21)	Low (Latch)
High Temperature Protection	Detecting condition	Chip temperature to be more than 150°C (Min)	High-Z_low	Low
	Releasing condition	Chip temperature to be less than 120°C (Min)	Normal operation	
Under Voltage Protection	Detecting condition	Power supply voltage to be below 7.0V (Typ)/6.0V (Min)/8.0V (Max)	High-Z_low	High
	Releasing condition	Power supply voltage to be above 7.5V (Typ)/6.5V (Min)/8.5V (Max)	Normal operation	
Clock Stop Protection	Detecting condition	BCLK signal has stopped more than constant period of time. LRCLK signal has stopped more than constant period of time. BCLK frequency becomes lower than constant frequency speed. BCLK frequency becomes higher than constant frequency speed. Clock stop protection is detected if any of the condition described above happens. Refer to P.58 to P.61.	High-Z_low	High
	Releasing condition	LRCLK has not stopped more than constant period of time. And BCLK frequency keeps between the constant frequency speed more than maximum 60ms. Refer to P.58 to P.61.	Normal operation	

(Note 20) The ERRORX pin is Nch open-drain output. The ERRORX output pin should be pulled-up by external resistor.
(Note 21) Once LSI is latched, the circuit will not be released automatically even after the abnormal condition has been removed.
The following procedure is available for recovery.
To let LSI return from latch state, set MUTEX pin to Low once for more than PWM stop time and then return it back to high.

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13 Protection Function - continued

13.1 Output Short Protection (Short to the Power Supply)

This LSI has the output short protection circuit that mutes the PWM output when the PWM output is short-circuited to the power supply unintentionally.

Detecting condition - It will detect when MUTEX pin is set high and the current that flows in the PWM output pin becomes over 10A (Typ) more than 0.3µs (Typ). The PWM output immediately transition to the state of High-Z_low if detected, and LSI does the latch.

Releasing method - Set MUTEX pin to low once for more than PWM stop time (Refer to P.19) and then return it back to high.

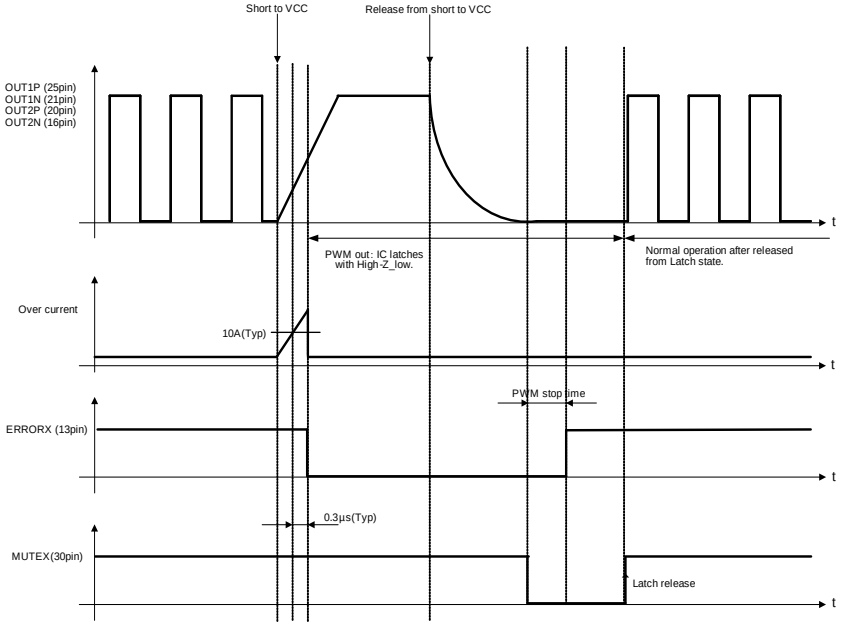


Figure 45. Output Short Protection (Short to the power supply) Sequence

13.2 Output Short Protection (Short to GND)

This LSI has the output short protection circuit that mutes the PWM output when the PWM output is short-circuited to GND unintentionally.

Detecting condition - It will detect when MUTEX pin is set high and the current that flows in the PWM output pin becomes over 10A (Typ) more than 0.4µs (Typ). If Output short protection is detected, the PWM output immediately transition to the state of High-Z_low, and LSI latches the stop state.

Releasing method - Set MUTEX pin to low once for more than PWM stop time (Refer to P.19) and then return it back to high.

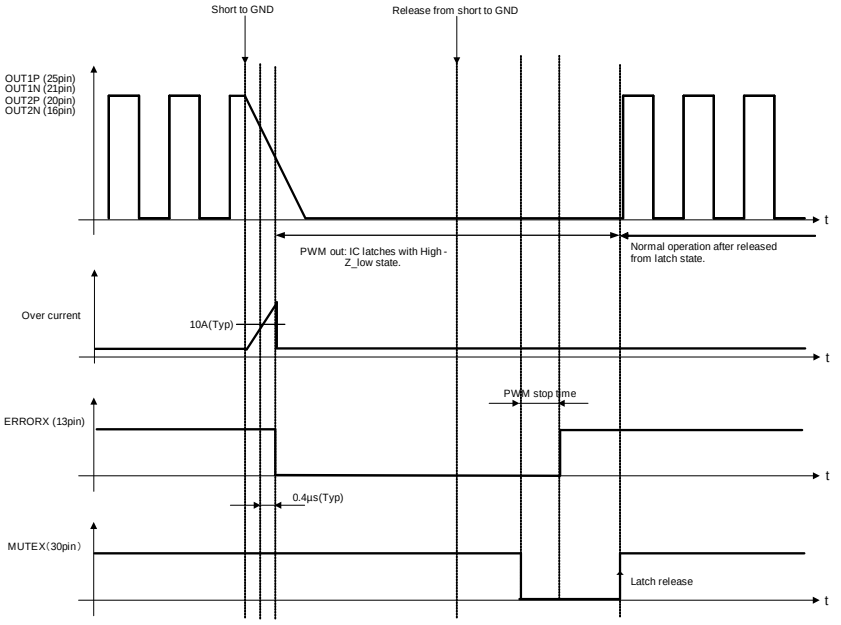


Figure 46. Output Short Protection (Short to GND) Sequence

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13 Protection Function – continued

13.3 DC Voltage Protection for Speaker

When the DC voltage is applied to the speaker unintentionally, the embedded DC Voltage Protection circuit mute the PWM output circuit for preventing the speaker from destruction.

Detecting condition - It will detect when MUTEX pin is set to high and PWM output Duty ratio=0% or 100% over 42ms (fs=48kHz). The PWM output immediately transition to the state of High-Z_low if detected, and LSI does the latch.

Releasing method - Set MUTEX pin to low once for more than PWM stop time (Refer to P.19) and then return it back to high.

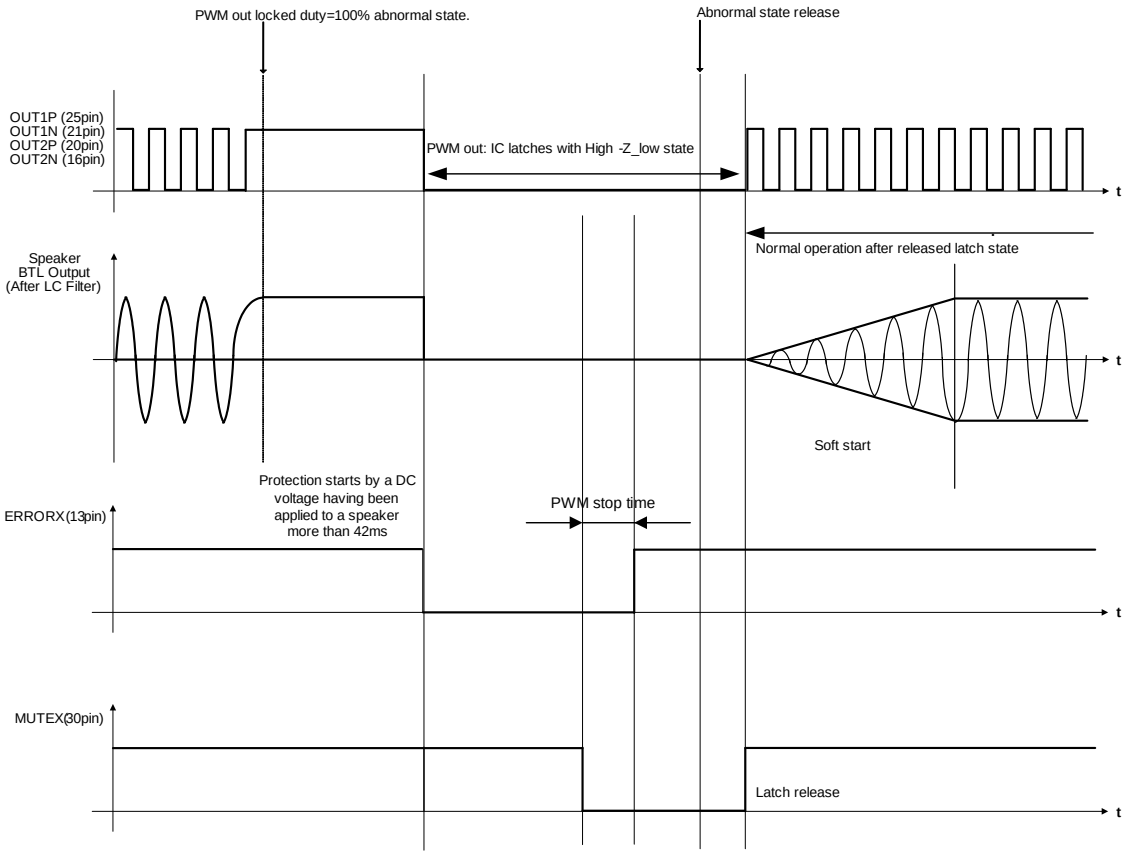


Figure 47. DC Voltage Protection in the Speaker Sequence

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13 Protection Function – continued

13.4 High Temperature Protection

This LSI has the high temperature protection circuit that prevents from thermal runaway under an abnormal state for the temperature of the chip to exceed Tj=150°C(Min).

Detecting condition - It will detect when MUTEX pin is set to high and the temperature of the chip becomes 150°C (Min) or more. The speaker output immediately transitions to the state of High-Z_low.

Releasing condition - It will release when MUTEX pin is set to high and the temperature of the chip becomes 120°C (Min) or less. If this protection is released, the PWM output pin return to output PWM signal state (Auto recovery).

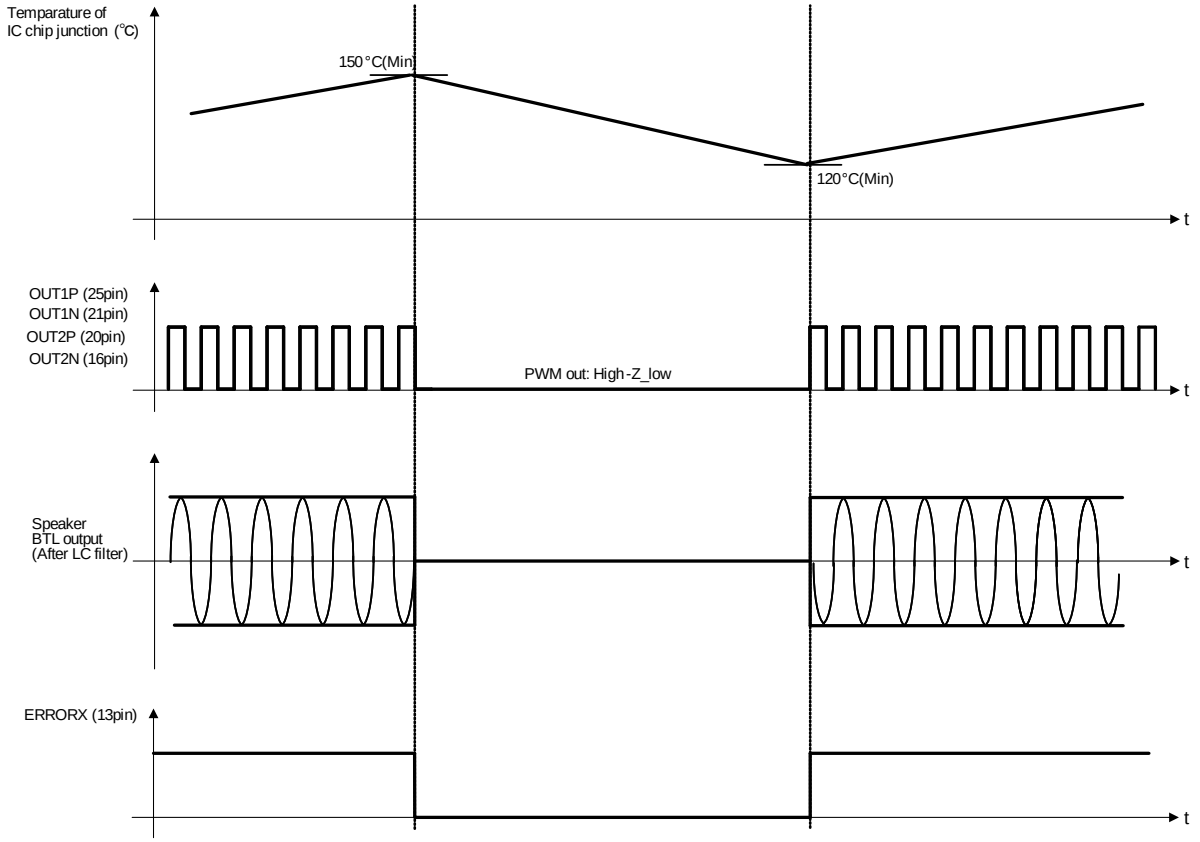


Figure 48. High Temperature Protection Sequence

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13 Protection Function – continued

13.5 Under Voltage Protection

This LSI has under voltage protection circuit that makes PWM output mutes when extreme drop of the power supply voltage is detected.

Detecting condition - It will detect when MUTEX pin is set to high and the power supply voltage becomes lower than 7.0V (Typ). The speaker output immediately transitions to the state of High-Z_low when detected.

Releasing condition - It will be released when MUTEX pin is set to high and the power supply voltage becomes more than 7.5V (Typ). If this protection is released, the PWM output pin return to output PWM signal state (Auto recovery).

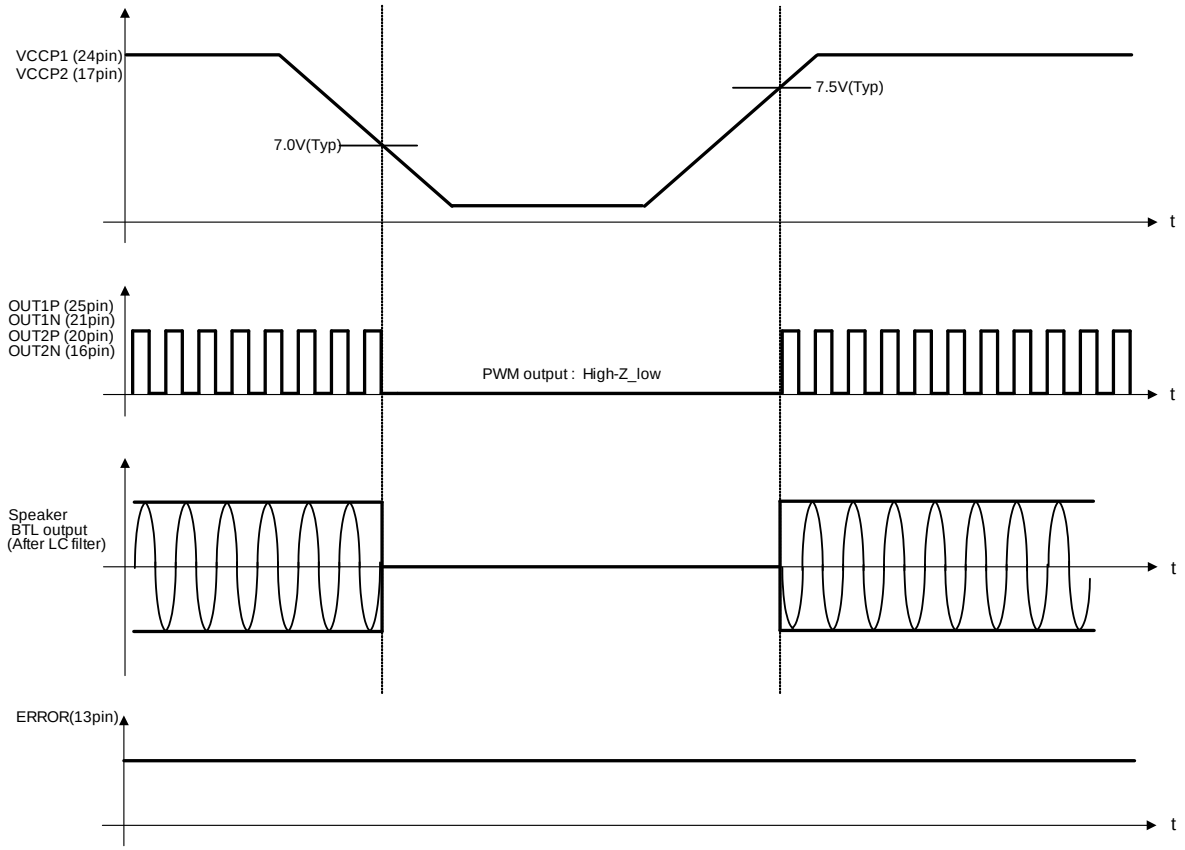


Figure 49. Under Voltage Protection Sequence

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13 Protection Function – continued

13.6 Clock Stop Protection

This LSI has the clock stop protection circuit that makes PWM output mutes when the BCLK and LRCLK frequency of the digital audio signal are stopped or become high frequency or become low frequency more than given period.

Detecting condition - If BCLK frequency is stop or high or low, LRCLK frequency is stop.
The speaker output immediately transitions to the state of High-Z_low when detected.
Releasing condition - If BCLK and LRCLK are normal input over 60ms (Max) and more.
After 60ms (Max) from releasing, the PWM output pin return to output PWM signal state after soft start (Auto recovery).

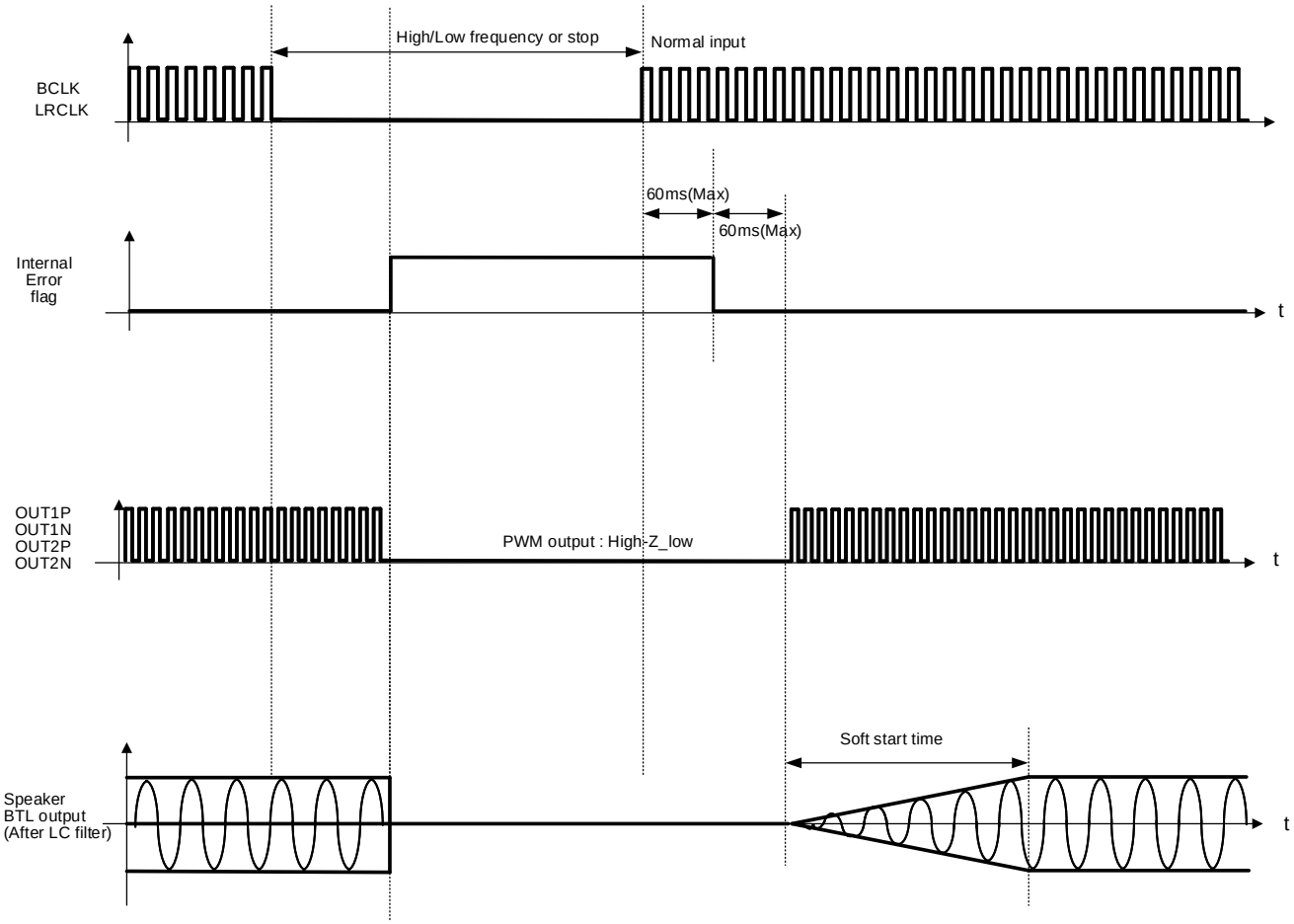


Figure 50. Clock Stop Protection Sequence

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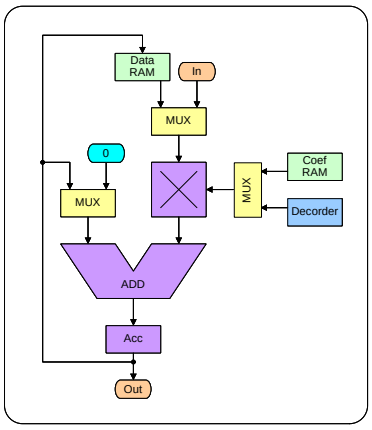
Description of Function - continued

14 Digital Sound Processing (DSP)

The digital sound processing (DSP) part of BM28723AMUV is composed of special hardware which is optimal for TV and Mini/Micro Component System. BM28723AMUV does the following processing using this special DSP.
Pre-Scaler, Channel mixer, 12 Band BQ, Fine Master Volume, 3 Band DRC, Fine Post-scaler,
DC Cut HPF, Hard Clipper

The outline and signal flow of the DSP part

Data width:	32 bit (DATA RAM)
Machine cycle:	20.3ns (1024f_S, fs=48kHz)
Multiplier:	32x24 → 56 bit
Adder:	56+56 → 56 bit
Data RAM:	512x32 bit
Coefficient RAM:	512x24 bit
Sampling frequency:	fs=32k, 44.1k, 48kHz



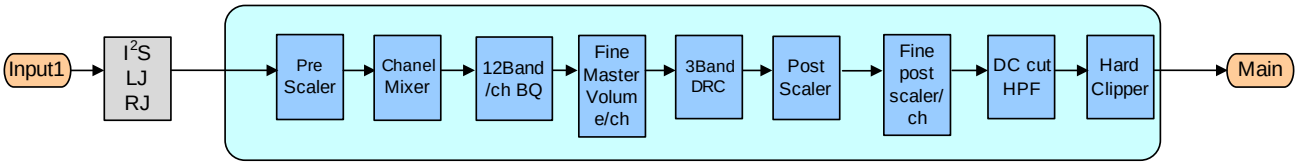


Figure 51

Digital signal from 16bit to 24bit is inputted to the DSP but extends 8bit (+48dB) as the overflow margin to the MSB side. When the processing is over this range, it will be clip processing inside DSP. Note that in case of commonly used second IIR-type (BQ) filter is the digital filter, output of the internal multiplier and adder will consume a lot of overflow margin.

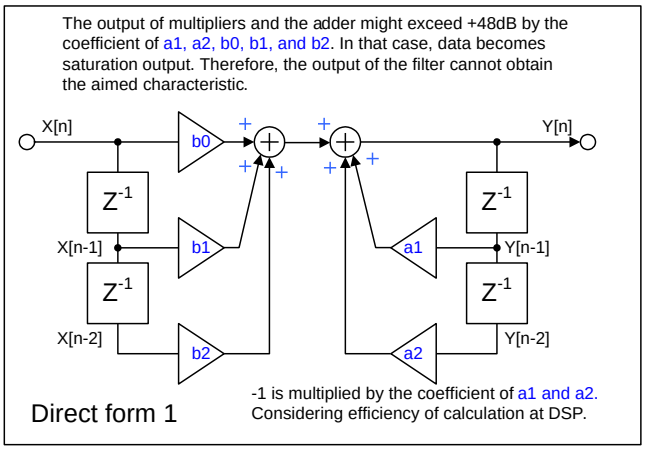


Figure 52

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14 Digital Sound Processing (DSP) - continued

The management of audio data and coefficient data is as follows by each block.

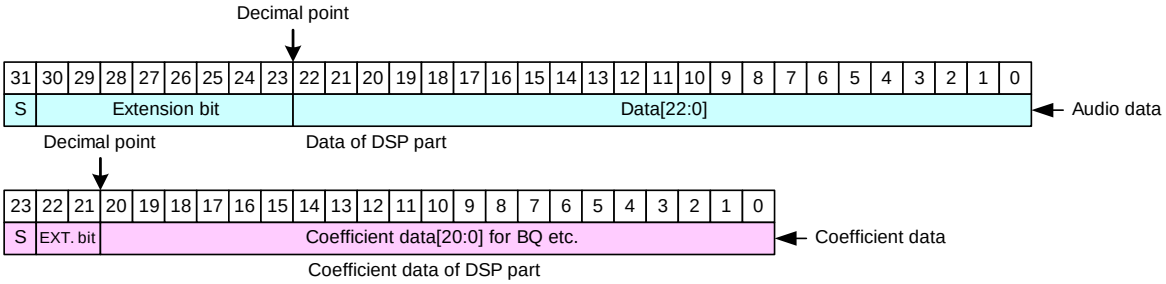


Figure 53

14.1 Bypass

There are commands to bypass selected DSP functions. This bypass can be set even the setting values are remained for each function; therefore, it is easy to check ON/OFF of the sound effect.
There are three bypass options, which are 12Band BQ, 3Band DRC or the whole DSP except Hard Clipper.

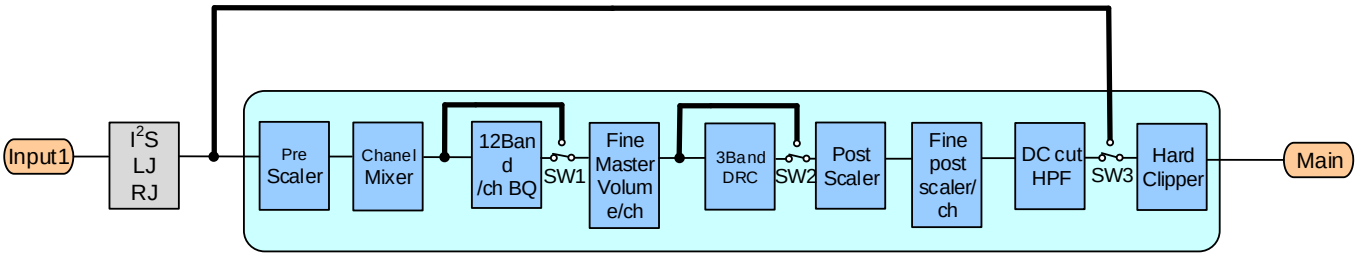


Figure 54

Default=0x0

Select Address	bit	Explanation of Operation
0x02[2:0]	2	Bypass of 12 Band BQ (SW1) 0: Normal 1: Bypass
	1	Bypass of 3 Band DRC (SW2) 0: Normal 1: Bypass
	0	Bypass of DSP (SW3) 0: Normal 1: Bypass (Except Hard Clipper)

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14 Digital Sound Processing (DSP) - continued

14.2 Pre-Scaler

To overflow when the level sometimes is full scale entry in case of the digital signal which is inputted to the sound DSP and does surround and equalizer processing, it adjusts an entry gain with Pre-Scaler. The adjustable-range can be set from +48dB to -79dB with the 0.5dB step. (Lch/Rch dependent control)
Pre-Scaler does not have the soft transition function.

Default=0x60

Select Address	Explanation of Operation
0x16[7:0]	See table below

Value	Gain
0x00	+48dB
0x01	+47.5dB
⋮	⋮
0x60	0dB
0x61	-0.5dB
0x62	-1dB
⋮	⋮
0xFE	-79dB
0xFF	-∞

14.3 Channel Setup with a Phase Inversion Function Channel Mixer 1

This function mixes the sound on the left channel and the right channel of the digital signal which was inputted to the DSP. Here, it changes stereo signal to monaural. In addition, the phase-inversion, the mute on each channel can be set.

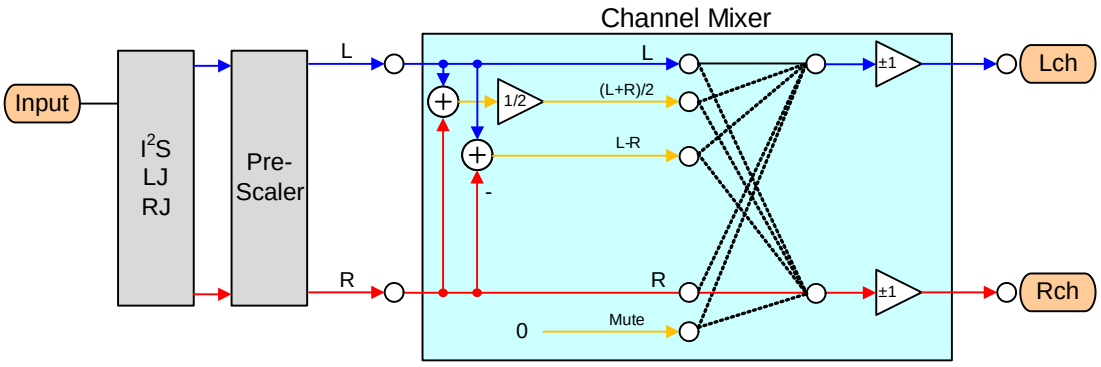


Figure 55

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14.3 Channel Setup with a Phase Inversion Function Channel Mixer 1- continued

DSP Input: The data inputted into Lch of DSP is inverted.

Default=0x0

Select Address	Value	Explanation of Operation
0x17[7]	0x0	Normal
	0x1	Invert

DSP Input: The data inputted into Lch of DSP is mixed.

Default=0x1

Select Address	Value	Explanation of Operation
0x17[6:4]	0x0	Mute
	0x1	Lch data input
	0x2	Rch data input
	0x3	(Lch+Rch)/2 data input
	0x4	Lch-Rch data input

DSP input: The data inputted into Rch of DSP is inverted.

Default=0x0

Select Address	Value	Explanation of Operation
0x17[3]	0x0	Normal
	0x1	Invert

DSP Input: The data inputted into Rch of DSP is mixed.

Default=0x2

Select Address	Value	Explanation of Operation
0x17[2:0]	0x0	Mute
	0x1	Lch data input
	0x2	Rch data input
	0x3	(Lch+Rch)/2 data input
	0x4	Lch-Rch data input

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14 Digital Sound Processing (DSP) - continued

14.4 Bi-quad Type Filter

This LSI has the following blocks that have a feature of the Bi-quad type filter:
12 Band BQ, Crossover filter of 3Band DRC block and BQ of the soft transition.
The shapes that can be used are peaking filter, low shelf filter, high shelf filter, low pass filter, high pass filter, all path filter and notch filter.
Setting the coefficient of the digital filter (b0, b1, b2, a1, a2) in the LSI by transmitting to the coefficient RAM via command.
12 Band BQ have the soft transition function. Note that the detailed order of the parameter setting refers to the following BQ setting method.

Select of BQ independent or dependent setting

Default=0x0

Select Address	Value	Explanation of Operation
0x60[4]	0x0	L/R dependent setting
	0x1	L/R independent setting

0x60[4] setting note.
Reset all the Bi-quad type filters when you change the setting of 0x60[4].
The Bi-quad type filters for which the re-setting is necessary are 18 BQs of BQ1-12, DRC1,DRC2 and DRC3 (Each DRC has 2 band).

Select the destination of BQ soft transition

Default=0x00

Select Address	Explanation of Operation
0x51[4:0]	

Value	Destination	Value	Destination
0x00	12BAND(1)	0x0A	12BAND(11)
0x01	12BAND(2)	0x0B	12BAND(12)
0x02	12BAND(3)		
0x03	12BAND(4)		
0x04	12BAND(5)		
0x05	12BAND(6)		
0x06	12BAND(7)		
0x07	12BAND(8)		
0x08	12BAND(9)		
0x09	12BAND(10)		

Select of soft transition

Default=0x0

Select Address	Value	Explanation of Operation
0x53[6]	0x0	Use soft transition
	0x1	Not use soft transition

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14.4 Bi-quad Type Filter – continued

Select the destination channel of soft transition

Default=0x0

Select Address	Value	Explanation of Operation
0x53[5:4]	0x0	Lch and Rch
	0x1	Lch
	0x2	Rch
	0x3	Don't use

Setting of soft transition time

Default=0x3

Select Address	Value	Explanation of Operation
0x53[3:2]	0x0	2.7ms
	0x1	5.3ms
	0x2	10.7ms
	0x3	21.3ms

Setting of transition filter wait time

Default=0x0

Select Address	Value	Explanation of Operation
0x53[1:0]	0x0	2.7ms
	0x1	5.3ms
	0x2	10.7ms
	0x3	21.3ms

Setting of soft transition start

Default=0x0

Select Address	Value	Explanation of Operation
0x58[0]	0x0	Stop the soft transition operation
	0x1	Start the soft transition operation (After the transition is completed, it becomes 0x0 by the automatic operation)

This register is write only.

Read-out soft transition status

Read only

Select Address	Explanation of Operation
0x59[0]	0x1 is read at the time of executing soft transition 0x0 is read at the time of except executing soft transition

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14 Digital Sound Processing (DSP) - continued

14.5 Volume Setting

Volume is from +24dB to -103dB, and can be selected by the step of 0.125dB. And it is also possible to be set to -infinity dB. L/R independent or L/R dependent can be selected by 0x10[7]. At the time of switching of Volume, soft transition is executed. Soft transition duration is optional with the command.
It becomes the following formula at the transition from AdB to BdB. C is soft transition duration selected by 0x15[7:6] command.

$$\text{Transition time} = \left| \left(10^{\left(\frac{A}{20}\right)} - 10^{\left(\frac{B}{20}\right)} \right) \times C \right| \quad [\text{ms}]$$

Setting of soft transition time

Default=0x0

Select Address	Value	Explanation of Operation
0x15[7:6]	0x0	21.3ms
	0x1	42.7ms
	0x2	85.3ms
	0x3	Don't use

Lch/dependent volume setting

Default=0xFF

Select Address	Explanation of Operation
0x11[7:0]	

Value	Gain
0x00	+24dB
0x01	+23.5dB
⋮	⋮
0x30	0dB
0x31	-0.5dB
0x32	-1dB
⋮	⋮
0xFE	-103dB
0xFF	-∞

Fine volume setting function becomes effective by sending the following command.
When using this command, it is possible to set a volume in 0.125dB step.
When L/R dependent volume setting, 0x11[7:0] is enable.
When L/R independent volume setting, 0x11[7:0] is the volume setting of Lch.

Lch/dependent fine volume setting
It is possible to use with the 0.5dB step in changing only 0x11[7:0] when 0x10[1:0]=0x0.

Default=0x0

Select Address	Value	Explanation of Operation
0x10[1:0]	0x0	0dB
	0x1	-0.125dB
	0x2	-0.25dB
	0x3	-0.375dB

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14.5 Volume Setting - continued

The Lch/Rch independent volume setting and the dependent volume setting can be selected by 0x10[7] command.
When Lch/Rch independent volume set, the volume setting of Lch is the setting of 0x10[1:0] and 0x11, and the volume setting of Rch is the settings of 0x10[5:4] and 0x12.

Setting of Lch/Rch independent volume

Default=0x0

Select Address	Value	Explanation of Operation
0x10[7]	0x0	Lch/Rch dependent volume setting
	0x1	Lch/Rch independent volume setting

Setting of volume (Setting of Rch volume, It is enable only to set an independent volume.)

Default=0xFF

Select Address	Explanation of Operation
0x12[7:0]	See table below

Value	Gain
0x00	+24dB
0x01	+23.5dB
⋮	⋮
0x30	0dB
0x31	-0.5dB
0x32	-1dB
⋮	⋮
0xFE	-103dB
0xFF	-∞

Fine volume setting function becomes effective by sending the following command.
When using this command, it is possible to set a volume in 0.125dB step.

Setting of fine volume (Setting of Rch fine volume, It is enable only to set an independent volume.)
It is possible to use with the 0.5dB step in changing only 0x12[7:0] when 0x10[5:4]=0.

Default=0x0

Select Address	Value	Explanation of Operation
0x10[5:4]	0x0	0dB
	0x1	-0.125dB
	0x2	-0.25dB
	0x3	-0.375dB

It is possible to use with the 0.125dB step in setting both 0x10[1:0] and 0x11[7:0].
In case of 0x10[1:0]=0x0, it becomes the set value of 0x11[7:0].
In case of 0x10[1:0]=0x1, it becomes the -0.125dB set value of 0x11[7:0].
In case of 0x10[1:0]=0x2, it becomes the -0.25dB set value of 0x11[7:0].
In case of 0x10[1:0]=0x3, it becomes the -0.375dB set value of 0x11[7:0].
Since the transfer of 0x11 fixes it in any case, the soft transition can be beforehand begun in the set value for the direct following of the purpose in setting 0x11 after setting in 0x10.
0x10[5:4] is the same function as 0x10[1:0], 0x12 is the same function as 0x11 when Lch/Rch independently set for Rch.



Figure 56

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14 Digital Sound Processing (DSP) - continued

14.6 3 Band DRC

This DRC is used in order to prevent speaker protection and the clip output of a large audio signal.
There are three kinds of DRC (DRC1, DRC2, and DRC3) , and no clip can be output to each three BAND.
DRC1, DRC2 and DRC3 can set up two threshold levels. Moreover, it is possible to also change one slope.

3 Band DRC block diagram

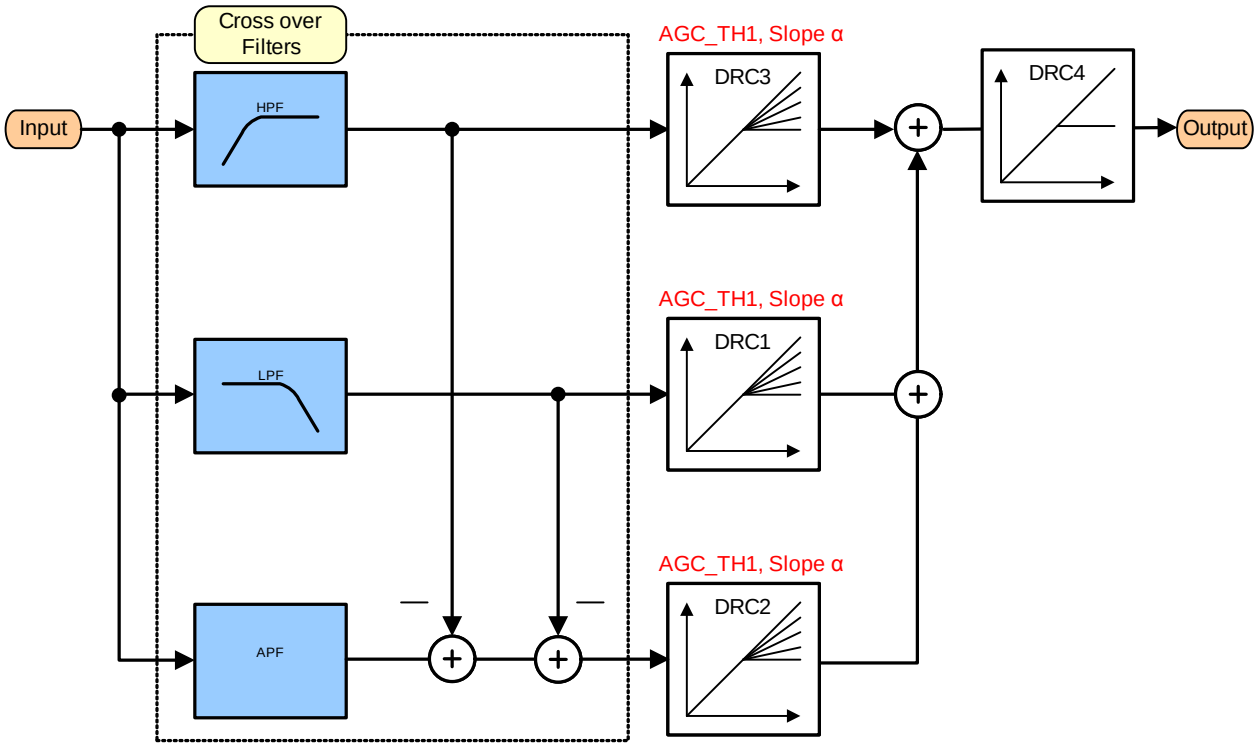


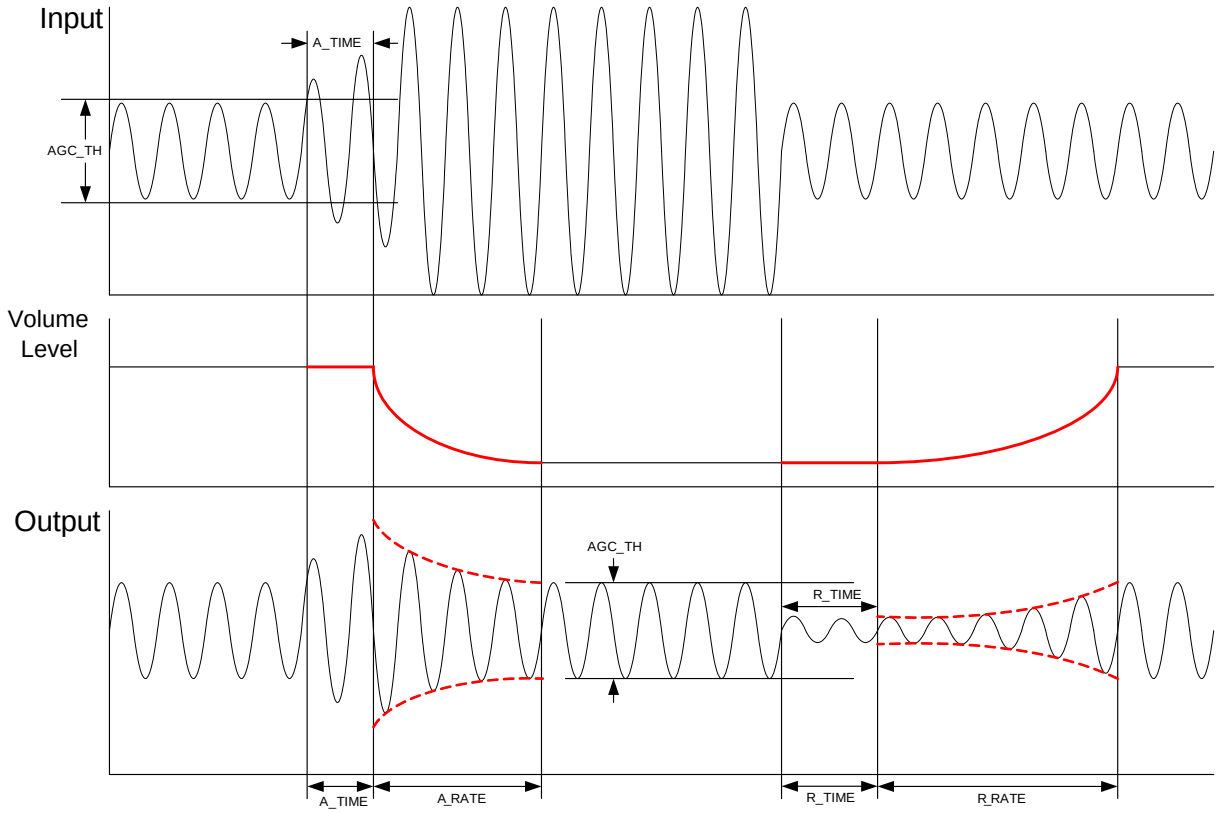
Figure 57

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14.6 3 Band DRC - continued

DRC transition figure



In here A_TIME is the time for detecting time before gain starts to decrease. And A_RATE decides the slope of gain compression.
On the other hand, R_TIME is the time for detecting before starting to release gain operation. And R_RATE decides slope of release gain.

Figure 58

DRC1, DRC2, DRC3 can be set 2 types of threshold (AGC_TH1 and AGC_TH2) as shown below. If output is in between AGC_TH1 and AGC_TH2, a slant for output gain can be made. If input become bigger and output over AGC_TH2, output gain doesn't have slant and become constant level. Slope setting (α) is calculated by AGC_TH1, AGC_TH2 and the value of input gain to DRC block for reaching AGC_TH2 (xdB).
The operation between AGC_TH1 and AGC_TH2 is named as $DRC1_{slope}$ and $DRC2_{slope}$ and $DRC3_{slope}$.
And the operation over AGC_TH2 is named as $DRC1_{comp}$ and $DRC2_{comp}$ and $DRC3_{comp}$.
Each operation can be set ON/OFF, A_TIME, A_RATE, R_TIME, R_RATE respectively.
For example, DRC1 do not have slope curve when setting $DRC1_{slope}$ OFF and $DRC1_{comp}$ ON.
DRC4 can be set only AGC_TH2 therefore DRC4 do not have slope function.

DRC input-and-output gain characteristics

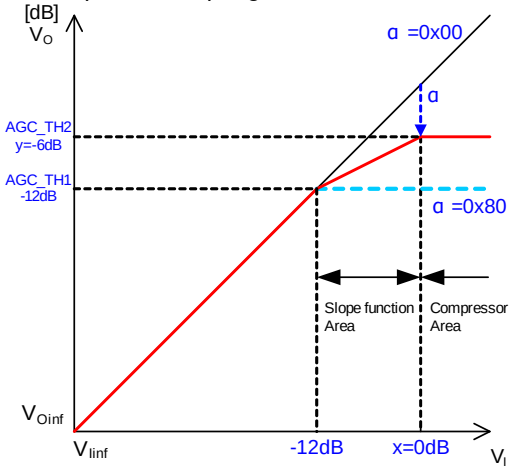


Figure 59

The formula which asks for Slope α is described below.
α changes into 8bit Hex data of the complement of 2 the value calculated by calculation.

$$\alpha = \frac{10^{\frac{y}{20}} - 10^{\frac{x}{20}}}{10^{\frac{TH}{20}} - 10^{\frac{x}{20}}} \times 128$$

TH is AGC_TH1. x is input level. y is output level.

Ex) It asks for α at the time of AGC_TH1 = -12dB, x = 0dB y = -6dB

$$\alpha = \frac{10^{\frac{-6}{20}} - 10^{\frac{0}{20}}}{10^{\frac{-12}{20}} - 10^{\frac{0}{20}}} \times 128$$

$\alpha = 85.266 \rightarrow 0x55$

0x55 calculated is setto command 0x29, 0x31 or 0x39.

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14.6 3 Band DRC - continued

Volume Curve

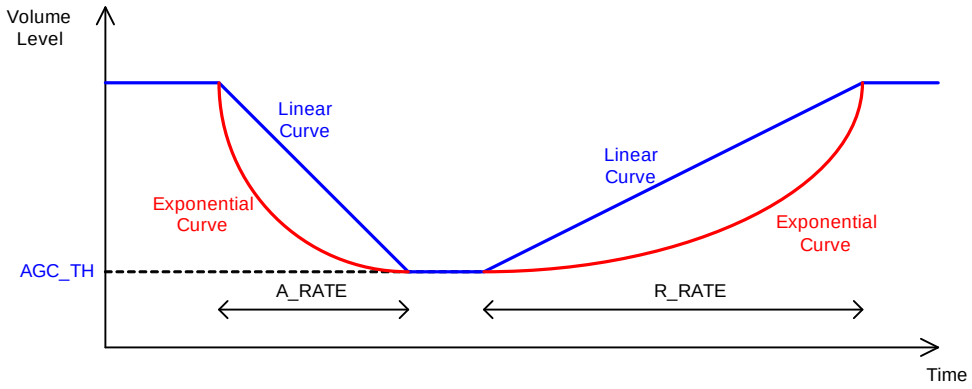


Figure 60

DRC1$_{slope}$ ON/OFF setting
OFF is through output.

Default=0x1

Select Address	Value	Explanation of Operation
0x20[7]	0x0	OFF
	0x1	ON

DRC1$_{comp}$ ON/OFF setting
OFF is through output.

Default=0x1

Select Address	Value	Explanation of Operation
0x20[6]	0x0	OFF
	0x1	ON

DRC2$_{slope}$ ON/OFF setting
OFF is through output.

Default=0x1

Select Address	Value	Explanation of Operation
0x20[5]	0x0	OFF
	0x1	ON

DRC2$_{comp}$ ON/OFF setting
OFF is through output.

Default=0x1

Select Address	Value	Explanation of Operation
0x20[4]	0x0	OFF
	0x1	ON

DRC3$_{slope}$ ON/OFF setting
OFF is through output.

Default=0x1

Select Address	Value	Explanation of Operation
0x20[3]	0x0	OFF
	0x1	ON

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14.6 3 Band DRC - continued

DRC3$_{comp}$ ON/OFF setting
OFF is through output.

Default=0x1

Select Address	Value	Explanation of Operation
0x20[2]	0x0	OFF
	0x1	ON

DRC4 ON/OFF setting
OFF is through output.

Default=0x0

Select Address	Value	Explanation of Operation
0x3F[4]	0x0	OFF
	0x1	ON

The volume curve at the time of an attack (A_RATE) is selected.

Default=0x1

Select Address	Value	Explanation of Operation
0x21[7]	0x0	Linear curve
	0x1	Exponential curve

The volume curve at the time of a release (R_RATE) is selected.

Default=0x1

Select Address	Value	Explanation of Operation
0x21[6]	0x0	Linear curve
	0x1	Exponential curve

Initial setting of DRC cross over filter is 1 Band.

To set the crossover filter (HPF, LPF and APF) which divides the frequency band of 3 Band DRC, therefore, it is referred to the 14.4 Bi-quad Type Filter.

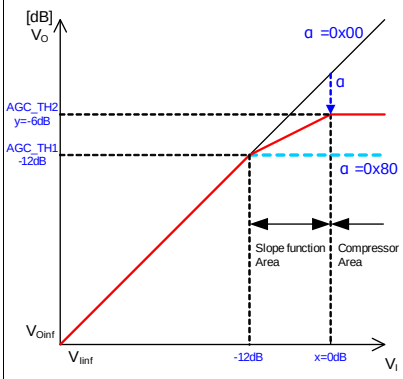
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14.6 3 Band DRC - continued

Slope (α) setting of $DRC1_{slope}$, $DRC2_{slope}$, and $DRC3_{slope}$
Each DRC can be set individually.

Default=0x80

Select Address	Explanation of Operation
$DRC1_{slope}$ 0x29[7:0] $DRC2_{slope}$ 0x31[7:0] $DRC3_{slope}$ 0x39[7:0]	 The formula which asks for Slope α is described below. α changes into 8bit Hex data of the complement of 2 the value calculated by calculation. $\alpha = \frac{10^{\frac{y}{20}} - 10^{\frac{x}{20}}}{10^{\frac{TH}{20}} - 10^{\frac{x}{20}}} \times 128$ TH is AGC_TH1. x is input level. y is output level. Ex) It asks for α at the time of AGC_TH1 = -12dB, x = 0dB y = -6dB $\alpha = \frac{10^{\frac{-6}{20}} - 10^{\frac{0}{20}}}{10^{\frac{-12}{20}} - 10^{\frac{0}{20}}} \times 128$ α = 85.266 → 0x55 0x55 calculated is setto command 0x29, 0x31 or 0x39.

AGC_TH1 setting of $DRC1_{slope}$, $DRC2_{slope}$, and $DRC3_{slope}$
Please set this value is smaller than the value of AGC_TH2.
Each DRC can be set individually.

Default=0x40

Select Address	Explanation of Operation
$DRC1_{slope}$ 0x28[6:0] $DRC2_{slope}$ 0x30[6:0] $DRC3_{slope}$ 0x38[6:0]	

Value	Threshold
0x00	-32dB
⋮	⋮
0x3F	-0.5dB
0x40	0dB
0x41	+0.5dB
⋮	⋮
0x58	+12dB

AGC_TH2 setting of $DRC1_{comp}$, $DRC2_{comp}$, $DRC3_{comp}$, and DRC4
Each DRC can be set individually.

Default=0x40

Select Address	Explanation of Operation
$DRC1_{comp}$ 0x2C[6:0] $DRC2_{comp}$ 0x34[6:0] $DRC3_{comp}$ 0x3C[6:0] DRC4 0x40[6:0]	

Value	Threshold
0x00	-32dB
⋮	⋮
0x3F	-0.5dB
0x40	0dB
0x41	+0.5dB
⋮	⋮
0x58	+12dB

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14.6 3 Band DRC - continued

A_RATE setting of $DRC1_{slope}$, $DRC2_{slope}$, $DRC3_{slope}$, $DRC1_{comp}$, $DRC2_{comp}$, $DRC3_{comp}$, DRC4
(Transition time setting for attack function)
Each DRC can be set individually.

Default=0x3

Select Address		Explanation of Operation
$DRC1_{slope}$	0x2A[6:4]	
$DRC2_{slope}$	0x32[6:4]	
$DRC3_{slope}$	0x3A[6:4]	
$DRC1_{comp}$	0x2E[6:4]	
$DRC2_{comp}$	0x36[6:4]	
$DRC3_{comp}$	0x3D[6:4]	
DRC4	0x41[6:4]	

Value	A_RATE	Value	A_RATE
0x0	1ms	0x4	5ms
0x1	2ms	0x5	10ms
0x2	3ms	0x6	20ms
0x3	4ms	0x7	40ms

R_RATE setting of $DRC1_{slope}$, $DRC2_{slope}$, $DRC3_{slope}$, $DRC1_{comp}$, $DRC2_{comp}$, $DRC3_{comp}$, DRC4
(Transition time setting for release function)
Each DRC can be set individually.

Default=0xB

Select Address		Explanation of Operation
$DRC1_{slope}$	0x2A[3:0]	
$DRC2_{slope}$	0x32[3:0]	
$DRC3_{slope}$	0x3A[3:0]	
$DRC1_{comp}$	0x2E[3:0]	
$DRC2_{comp}$	0x36[3:0]	
$DRC3_{comp}$	0x3D[3:0]	
DRC4	0x41[3:0]	

Value	R_RATE	Value	R_RATE
0x0	0.125s	0x8	2s
0x1	0.1825s	0x9	2.5s
0x2	0.25s	0xA	3s
0x3	0.5s	0xB	4s
0x4	0.75s	0xC	5s
0x5	1s	0xD	6s
0x6	1.25s	0xE	7s
0x7	1.5s	0xF	8s

A_TIME setting of $DRC1_{slope}$, $DRC2_{slope}$, $DRC3_{slope}$, $DRC1_{comp}$, $DRC2_{comp}$, $DRC3_{comp}$, DRC4
(Detection time setting for attack function)
Each DRC can be set individually.

Default=0x1

Select Address		Explanation of Operation
$DRC1_{slope}$	0x2B[7:4]	
$DRC2_{slope}$	0x33[7:4]	
$DRC3_{slope}$	0x3B[7:4]	
$DRC1_{comp}$	0x2F[7:4]	
$DRC2_{comp}$	0x37[7:4]	
$DRC3_{comp}$	0x3E[7:4]	
DRC4	0x42[7:4]	

Value	A_TIME	Value	A_TIME
0x0	0ms	0x8	6ms
0x1	0.5ms	0x9	7ms
0x2	1ms	0xA	8ms
0x3	1.5ms	0xB	9ms
0x4	2ms	0xC	10ms
0x5	3ms	0xD	20ms
0x6	4ms	0xE	30ms
0x7	5ms	0xF	40ms

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14.6 3 Band DRC - continued

R_TIME setting of $DRC1_{slope}$, $DRC2_{slope}$, $DRC3_{slope}$, $DRC1_{comp}$, $DRC2_{comp}$, $DRC3_{comp}$, DRC4
(Detection time setting for release function)
Each DRC can be set individually.

Default=0x3

Select Address	Explanation of Operation
$DRC1_{slope}$ 0x2B[2:0] $DRC2_{slope}$ 0x33[2:0] $DRC3_{slope}$ 0x3B[2:0] $DRC1_{comp}$ 0x2F[2:0] $DRC2_{comp}$ 0x37[2:0] $DRC3_{comp}$ 0x3E[2:0] DRC4 0x42[2:0]	

Value	R_TIME	Value	R_TIME
0x0	5ms	0x4	100ms
0x1	10ms	0x5	200ms
0x2	25ms	0x6	300ms
0x3	50ms	0x7	400ms

14.7 Post-scaler

Post-scaler is used to adjust the gain of post DSP processing data.
The adjustable-range can be set from +48dB to -79dB with the 0.5dB step. (Lch/Rch dependent control)
Pre-Scaler does not have a soft transition function.

Default=0x60

Select Address	Explanation of Operation
0x13[7:0]	

Value	Gain
0x00	+48dB
0x01	+47.5dB
⋮	⋮
0x60	0dB
0x61	-0.5dB
0x62	-1dB
⋮	⋮
0xFE	-79dB
0xFF	-∞

14.8 Fine Post-scaler

This function block is located after Post-scaler. An adjustable range can be set up from +0.7dB to –0.8dB at 0.1dB step.
Fine Post-scaler does not have a soft transition function.
(Independent control of Lch/Rch.)

Default=0x8

Select Address	Explanation of Operation
Lch 0x14[7:4] Rch 0x14[3:0]	

Value	Gain	Value	Gain
0x0	-0.8dB	0x8	0dB
0x1	-0.7dB	0x9	+0.1dB
0x2	-0.6dB	0xA	+0.2dB
0x3	-0.5dB	0xB	+0.3dB
0x4	-0.4dB	0xC	+0.4dB
0x5	-0.3dB	0xD	+0.5dB
0x6	-0.2dB	0xE	+0.6dB
0x7	-0.1dB	0xF	+0.7dB

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14 Digital Sound Processing (DSP) - continued

14.9 Hard Clipper

Measure the rated output power (practical maximum output power) of TV or any audio products at the 10% of Total Harmonic Distortion (THD+N). It can be made to clip with any output amplitude by using a clipper function. For example, the rated output of 10W or 5W can be gained using the amplifier of 15W output.

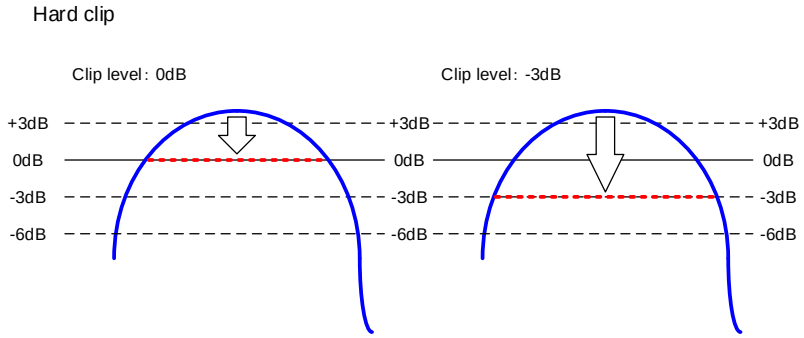


Figure 61

Clipper setting

Default=0x1

Select Address	Value	Explanation of Operation
0x1A[0]	0x0	Not use Clipper function
	0x1	Use Clipper function

Clip level selection

Default=0xE1

Select Address	Explanation of Operation
0x1B[7:0]	

Value	Gain
0x00	-22.5dB
0x01	-22.4dB
⋮	⋮
0xE0	-0.1dB
0xE1	0dB

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14 Digital Sound Processing (DSP) - continued

14.10 DC Cut 1st order HPF

DC offset element of the digital signal from audio DSP is cut by this HPF.
The cutoff frequency fc of HPF uses the 1Hz filter, and the degree uses the first-order filter.

Default=0x1

Select Address	Value	Explanation of Operation
0x18[0]	0x0	Not use DC Cut HPF
	0x1	Use DC Cut HPF

14.11 RAM Clear

The data RAM of DSP and coefficient RAM are cleared.
40µs or more is required until all the data is cleared.
After RAM Clear state keeps 40µs or more, change the mode RAM Clear to Normal.

Clear of the data RAM

Default=0x1

Select Address	Value	Explanation of Operation
0x01[7]	0x0	Normal
	0x1	Clear operation

Clear of coefficient RAM

Default=0x1

Select Address	Value	Explanation of Operation
0x01[6]	0x0	Normal
	0x1	Clear operation

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14 Digital Sound Processing (DSP) - continued

14.12 Audio Output Level Meter

It is possible to output the peak level of the PCM data inputted into a PWM processor.
A peak value can be read using the 2-wire command interface as 16 bit data of an absolute value.
The interval holding a peak value can be selected from six steps (50ms step) from 50ms to 300ms.
A peak hold result can be selected from L channel, R channel, and a monaural channel {(Lch+Rch)/2}.

Audio Output Level Meter block diagram

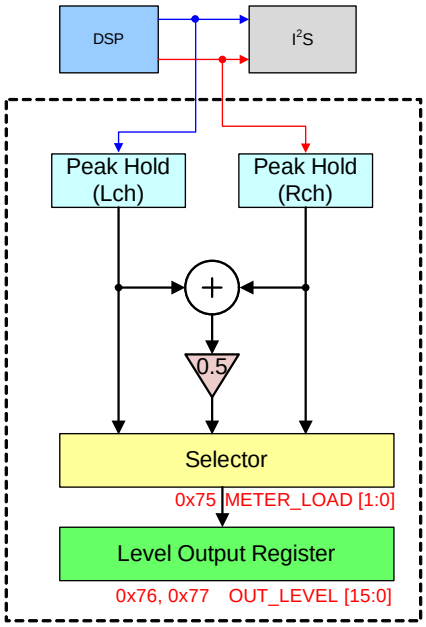


Figure 62

Setting of the peak level hold time interval of Audio Output Level Meter

Default=0x00

Select Address	Explanation of Operation
0x74[2:0]	Value / Hold time: 0x0 / 50ms; 0x1 / 100ms; 0x2 / 150ms; 0x3 / 200ms; 0x4 / 250ms; 0x5 / 300ms

Specify the read-target signal of Audio Level Meter.
A value will be taken into a read-only register if a setting value is written in.
In order to update this register value, it is necessary to write in a setting value again.

Write only

Select Address	Value	Explanation of Operation
0x75[1:0]	0x0	The peak level of L channel
	0x1	The peak level of R channel
	0x2	The peak level of monaural channel {(Lch+Rch)/2}

Read-back of Audio Output Level

0x76 (upper 8 bits) and a 0x77 (lower 8 bits) commands are read for the maximum within the period appointed by the command 0x74 using the 2-wire interface.

(Example)

When 0xFFFF is read, mean 1.0 (0dBFS).
When 0x8000 is read, mean 0.5 (-6dBFS).

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Description of Function - continued

15 Setting and Reading Method of BQ

It explains a detailed sequence of the setting method and the reading method of BQ separately for usage.

15.1 BQ coefficient setting

BQ consists of Bi-quad filter as follows. Each coefficient b0, b1, b2, a1, and a2 of BQ can be written directly.
It is S2.21 format, and setting range is -4≤x<+4.
Moreover, the coefficient address is shown in Table 1.

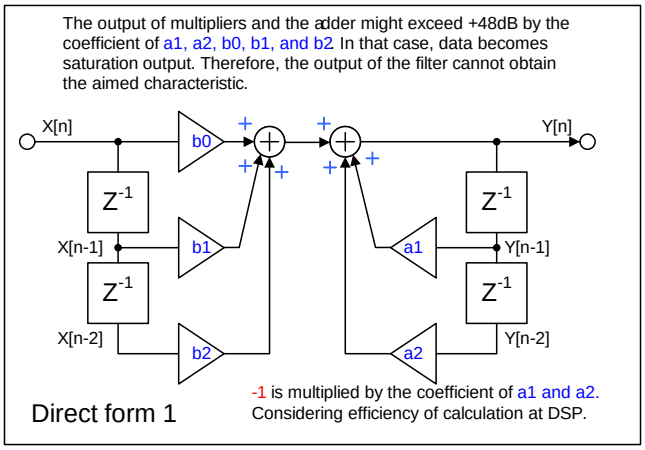


Figure 63

15.2 Writing sequence (Set in numerical order)

1. Address setting (0x61) Refer to Table 1.
2. 24bit coefficient upper [23:16] bit setting (0x62[7:0])
3. 24bit coefficient middle [15:8] bit setting (0x63[7:0])
4. 24bit coefficient lower [7:0] bit setting (0x64[7:0])
5. The writing of coefficients is performed. (0x65[0]=0x1)

Caution 1: After completion of writing coefficients this register is cleared automatically.
It is not necessary to write 0x65[0]=0x0. Coefficient writing takes about 100µs.
Caution 2: 100µs should not change an address setup and 24-bit coefficient setup after coefficient write-in execution.

(ex) When 0x3DEDE7 is written, same L/Rch, 12band BQ1 b0

1. 0x61=0x00 (12band BQ1 b0 is appointed)
2. 0x62=0x3D (Upper [23:16] is setting)
3. 0x63=0xED (Middle [15:8] is setting)
4. 0x64=0xE7 (Lower [7:0] is setting)
5. 0x65=0x01 (Coefficient transfer)
6. 100µs or more wait

15.3 Read-back sequence (Set in numerical order)

1. Address setting (0x61) Refer to Table 1.
2. Setting of a read-back register address (0xD0) Refer to P.22 “5 Reading of Data”
3. Read-back of the 24bit coefficient upper [23:16] bit (0x66[7:0])
4. Read-back of the 24bit coefficient middle [15:8] bit (0x67[7:0])
5. Read-back of the 24bit coefficient lower [7:0] bit (0x68[7:0])

15.4 When the coefficient of BQ is set up directly and a soft transition is performed

1. Set BQ coefficient to soft transition addresses. The addresses are 0x50 to 0x54. Please refer to Table1.
   Since in the case of 0x60[4]=0x1 (Enable L/R independent setting) and 0x53[5:4]=0x0 a soft transition is carried out and it is set to LR simultaneously, please write a coefficient in both LR address.
   In the case of 0x53[5:4]=0x1, coefficient is set to only Lch address.
   In the case of 0x53[5:4]=0x2, coefficient is set to only Rch address.
2. Select BQ Band that is performed soft transition by setting 0x51[4:0] address.
   (Refer to chapter 14.4 Bi-quad Type Filter)
3. 0x58[0]=0x1, Start soft transition (After the completion of soft transition this register is automatically cleared 0x0.)
4. Wait soft transition completion, or read command 0x59[0], and wait until it 0x59[0] cleared (0x0).

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15 Setting and Reading Method of BQ- continued

Table1. Specified Coefficient

0x61[6:0] Value	Select Coefficient	0x61[6:0] Value	Select Coefficient	0x61[6:0] Value	Select Coefficient
0x00	12BandBQ1 b0	0x23	12BandBQ8 b0	0x46	DRC2_1 b0
0x01	12BandBQ1 b1	0x24	12BandBQ8 b1	0x47	DRC2_1 b1
0x02	12BandBQ1 b2	0x25	12BandBQ8 b2	0x48	DRC2_1 b2
0x03	12BandBQ1 a1	0x26	12BandBQ8 a1	0x49	DRC2_1 a1
0x04	12BandBQ1 a2	0x27	12BandBQ8 a2	0x4A	DRC2_1 a2
0x05	12BandBQ2 b0	0x28	12BandBQ9 b0	0x4B	DRC2_2 b0
0x06	12BandBQ2 b1	0x29	12BandBQ9 b1	0x4C	DRC2_2 b1
0x07	12BandBQ2 b2	0x2A	12BandBQ9 b2	0x4D	DRC2_2 b2
0x08	12BandBQ2 a1	0x2B	12BandBQ9 a1	0x4E	DRC2_2 a1
0x09	12BandBQ2 a2	0x2C	12BandBQ9 a2	0x4F	DRC2_2 a2
0x0A	12BandBQ3 b0	0x2D	12BandBQ10 b0	0x50	Smooth BQ b0
0x0B	12BandBQ3 b1	0x2E	12BandBQ10 b1	0x51	Smooth BQ b1
0x0C	12BandBQ3 b2	0x2F	12BandBQ10 b2	0x52	Smooth BQ b2
0x0D	12BandBQ3 a1	0x30	12BandBQ10 a1	0x53	Smooth BQ a1
0x0E	12BandBQ3 a2	0x31	12BandBQ10 a2	0x54	Smooth BQ a2
0x0F	12BandBQ4 b0	0x32	12BandBQ11 b0	0x55	DRC3_1 b0
0x10	12BandBQ4 b1	0x33	12BandBQ11 b1	0x56	DRC3_1 b1
0x11	12BandBQ4 b2	0x34	12BandBQ11 b2	0x57	DRC3_1 b2
0x12	12BandBQ4 a1	0x35	12BandBQ11 a1	0x58	DRC3_1 a1
0x13	12BandBQ4 a2	0x36	12BandBQ11 a2	0x59	DRC3_1 a2
0x14	12BandBQ5 b0	0x37	12BandBQ12 b0	0x5A	DRC3_2 b0
0x15	12BandBQ5 b1	0x38	12BandBQ12 b1	0x5B	DRC3_2 b1
0x16	12BandBQ5 b2	0x39	12BandBQ12 b2	0x5C	DRC3_2 b2
0x17	12BandBQ5 a1	0x3A	12BandBQ12 a1	0x5D	DRC3_2 a1
0x18	12BandBQ5 a2	0x3B	12BandBQ12 a2	0x5E	DRC3_2 a2
0x19	12BandBQ6 b0	0x3C	DRC1_1 b0		
0x1A	12BandBQ6 b1	0x3D	DRC1_1 b1		
0x1B	12BandBQ6 b2	0x3E	DRC1_1 b2		
0x1C	12BandBQ6 a1	0x3F	DRC1_1 a1		
0x1D	12BandBQ6 a2	0x40	DRC1_1 a2		
0x1E	12BandBQ7 b0	0x41	DRC1_2 b0		
0x1F	12BandBQ7 b1	0x42	DRC1_2 b1		
0x20	12BandBQ7 b2	0x43	DRC1_2 b2		
0x21	12BandBQ7 a1	0x44	DRC1_2 a1		
0x22	12BandBQ7 a2	0x45	DRC1_2 a2		

Caution: When L/R independent, Lch: 0x61[7]=0x0, Rch: 0x61[7]=0x1.When L/R dependent, 0x61[7] is not reflected.

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Description of Function - continued

16 Mute Function by MUTEX Pin

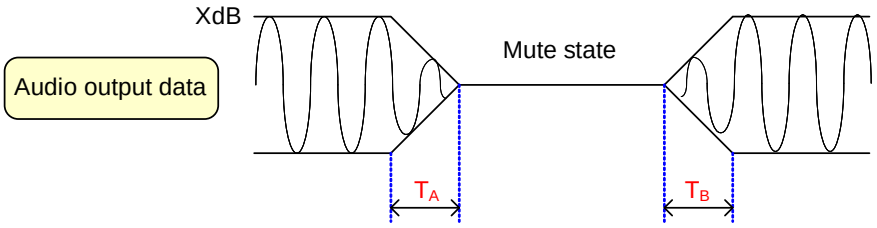
BM28723AMUV can mute output by setting the MUTEX pin to Low.

Transition time setting at the time of mute is as follows.
Soft transition mute time setting
The transition time when changing to a mute state is selected.
The soft transition time at the time of mute release is 10.7ms fixed.

Default=0x3

Select Address	Value	Explanation of Operation
0x15[1:0]	0x0	10.7ms (fs=48kHz)
	0x1	21.4ms (fs=48kHz)
	0x2	42.7ms (fs=48kHz)
	0x3	85.4ms (fs=48kHz)

0x15[1:0] Mute time setting
It is only operated to mute by MUTEX terminal.



0x15[1:0] setting

Value	T_A	T_B
0x0	10.7ms	10.7ms
0x1	21.4ms	10.7ms
0x2	42.7ms	10.7ms
0x3	85.4ms	10.7ms

Figure 64

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16 Mute Function by MUTEX Pin- continued

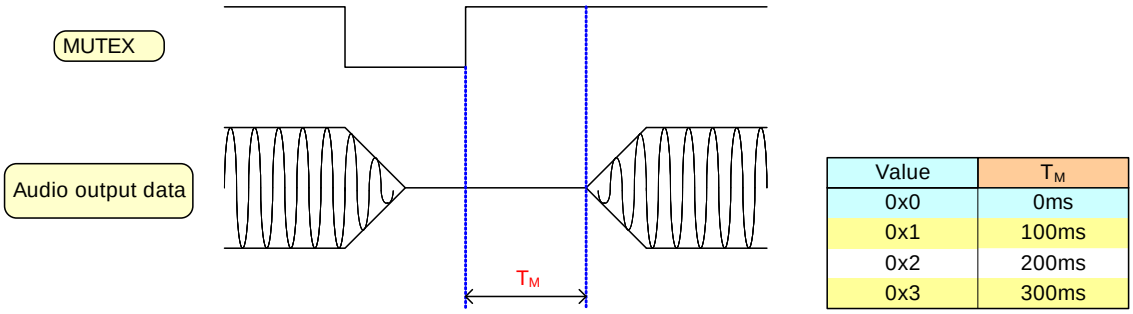
Soft start delay time setting

It is the delay time from detecting mute release to begin soft start actually.

Default=0x0

Select Address	Value	Explanation of Operation
0x15[5:4]	0x0	0ms
	0x1	100ms
	0x2	200ms
	0x3	300ms

Operation of Soft start delay 0x15[5:4]



Value	T_M
0x0	0ms
0x1	100ms
0x2	200ms
0x3	300ms

Figure 65

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Description of Function

17 Small Signal Input Detecting Function

There is a function which detects the audio data input of a non-signal or a small signal. This function is used in order to reduce the standby power consumption of an audio set.
If the signal below a setting detection level continues in both L channel and R channel, a small signal detection flag will become High. A detection result can be read from command 0x72[0].
The point which acts as a monitor of the small signal becomes input data of audio DSP block.

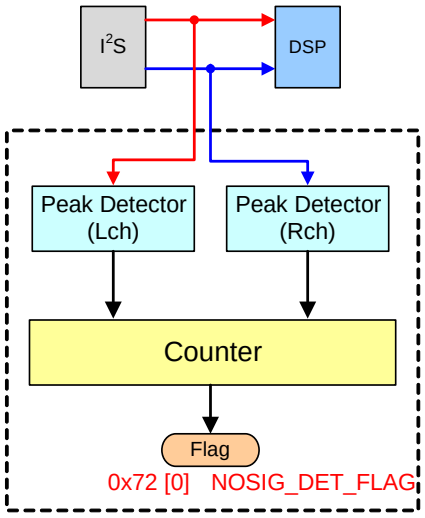


Figure 66. Block Diagram of Small Signal Input Detecting

Detection level setting

Default=0x00

Select Address	Explanation of Operation

Value	Level	Value	Level	Value	Level
0x00	-103dB	0x08	-77dB	0x10	-69dB
0x01	-93dB	0x09	-76dB	0x11	-68dB
0x02	-91dB	0x0A	-75dB	0x12	-67dB
0x03	-87dB	0x0B	-74dB	0x13	-66dB
0x04	-84dB	0x0C	-73dB	0x14	-65dB
0x05	-80dB	0x0D	-72dB	0x15	-64dB
0x06	-79dB	0x0E	-71dB	0x16	-62dB
0x07	-78dB	0x0F	-70dB	0x17	-60dB

Detection time setting

Default=0x0

Select Address	Value	Explanation of Operation
0x71[1:0]	0x0	42.7ms
	0x1	85.4ms
	0x2	170.7ms
	0x3	341.4ms

Caution: Sampling frequency is value of f_S=48kHz. In the case of f_S=44.1kHz, it will be about 1.09 times the setting value.

Detection flag read-back (Read Only)

Select Address	Value	Explanation of Operation
0x72[0]	0x0	Not detecting
	0x1	Detecting

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Description of Function - continued

18 Clock Stop Detection and detection of high speed and low speed or detection of out of sync

18.1 Clock Stop Detection

BM28723AMUV generates internal clock using for audio data processing from inputted several clocks.
By stopping these clock sources, the clocks that is used for audio data processing also stop (Or if that clock does not reach the frequency speed needed).
Therefore, the detection circuit is needed to avoid that situation.
State of BCLK and LRCLK are detected by using internal clock.
If valid flag is detected, output is muted (Immediate mute).

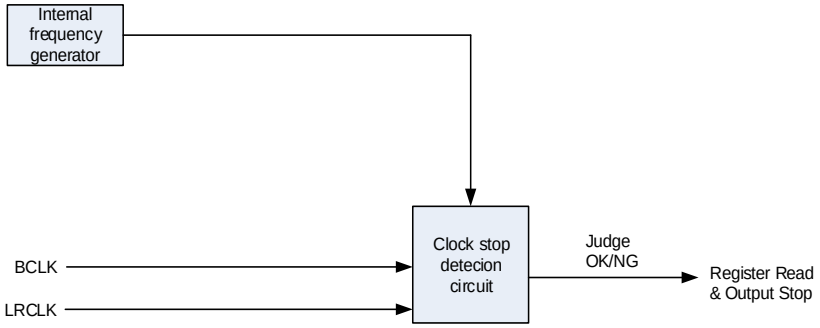


Figure 67

Each clock stop is detected when inputted clock stop during the time that is set by command. Detection result can be read back by command.
In addition, once stop flag is detected, these flags cannot be cleared until clear command is send even though the clock speed becomes normal.

LRCLK stop detection time

Default=0x2

Select Address	Value	Explanation of Operation
LRCLK 0x07[2:0]	0x0	10μs to 20μs
	0x1	20μs to 40μs
	0x2	50μs to 100μs
	0x3	100μs to 200μs
	0x4	200μs to 400μs
	0x5	300μs to 600μs
	0x6	400μs to 800μs
	0x7	500μs to 1000μs

Caution: Detection time has the above-mentioned variation within the limits

BCLK stop detection time

Default=0x0

Select Address	Value	Explanation of Operation
BCLK 0x08[6:4]	0x0	10μs to 20μs
	0x1	20μs to 40μs
	0x2	50μs to 100μs
	0x3	100μs to 200μs
	0x4	200μs to 400μs
	0x5	300μs to 600μs
	0x6	400μs to 800μs
	0x7	500μs to 1000μs

Caution: Detection time has the above-mentioned variation within the limits.

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18.1 Clock Stop Detection - continued

Stop detection flag read back register (Read Only)

Select Address	Value	Explanation of Operation
0x09[5]	0x0	Normal
	0x1	Detection of LRCLK stop flag
0x09[4]	0x0	Normal
	0x1	Detection of BCLK stop flag

Stop detection flag clear register (Write Only)

Select Address	Explanation of Operation
0x09[1]	LRCLK stop detection flag is cleared by writing 0x1.
0x09[0]	BCLK stop detection flag is cleared by writing 0x1.

Caution: When using Auto recovery from clock error function (P.62) , the above-mentioned flag is cleared automatically.

LRCLK stop flag valid or invalid selection

Default=0x1

Select Address	Value	Explanation of Operation
0x07[3]	0x0	Valid
	0x1	Invalid

BCLK stop flag valid or invalid selection

Default=0x0

Select Address	Value	Explanation of Operation
0x08[7]	0x0	Valid
	0x1	Invalid

18.2 Out of sync Detection

As for out of sync detecting function, it detects as out of sync error when it counts between the rising edges of LRCLK with internal clock (49.152MHz), and it shifts more than the definite value, and whether PLL is normally locked is judged.

Input Sampling Frequency	32kHz, 44.1kHz, 48kHz
Count value (Start of counting from 0)	1023

As for the detection result, reading from the register is possible. As a result of the judgment as out of sync once, it is not cleared until a clear command is transmitted even if the state of the clock returns normally. Moreover, out of sync count setting is also possible, and if the error is detected more than the number of times set by the command, the flag (0x06[1]) becomes 0x1.

Out of sync flag reading register (Read Only)

Select Address	Value	Explanation of Operation
0x06[1]	0x0	Normal
	0x1	Synchronous blank detects

Out of sync flag clear register (Write Only)

Select Address	Explanation of Operation
0x06[0]	When 0x1 is written, the out of sync flag is cleared.

Caution: When using Auto recovery from clock error function (P.62), the above-mentioned flag is cleared automatically.

Out of sync count setting

Default=0x2

Select Address	Explanation of Operation
0x06[6:4]	Set more than 0x1 (Set 0x1 to 0x7). When the actual detection count of out of sync exceeds the setting, Select Address 0x07[1] becomes 0x1.

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Description of Function - continued

18.3 BCLK High or Low Speed Detection function

BCLK high or low speed detection function counts the period of BCLK rising edge by using internal clock (12MHz to 25MHz) , and if the count value go beyond a constant value, it judge that abnormal speed of clock is occurred such as BCLK speed become high or low.
When using a BCLK speed detection, speed failure detection can be more correctly performed by making a command set reflect about an input sampling rate.
When you validate sampling rate setting, be sure to set up the sampling rate inputted with 0x0C [1:0] command. A high speed and the low speed detection flag can set up validity and the invalidity respectively. If valid flag is detected, output is muted (immediate mute).

Valid or invalid frequency value setting up by 0x0C[1:0] command.

Default=0x0

Select Address	Value	Explanation of Operation
0x0A[3]	0x0	Valid
	0x1	Invalid

Setting of input sampling rate

Default=0x0

Select Address	Value	Explanation of Operation
0x0C[1:0]	0x0	48kHz
	0x1	44.1kHz
	0x2	32kHz

The setting of constraints of a high speed or a low speed detection condition

Default=0x0

Select Address	Value	Explanation of Operation
0x0A[2]	0x0	±10%

It can check detection result by reading back.
The result judged that is once unusual is not cleared until it transmits a clear command, even if the condition of a clock returns to normal. It is possible to set the number of judging count of high speed flag detection and low speed flag detection by the command. If the error more than the predetermined number is detected, the flag (0x0A[1], 0x0B[1]) becomes 0x1.

BCLK high speed flag (Read Only)

Select Address	Value	Explanation of Operation
0x0A[1]	0x0	Normal
	0x1	High speed detection flag

BCLK low speed flag (Read Only)

Select Address	Value	Explanation of Operation
0x0B[1]	0x0	Normal
	0x1	Low speed detection flag

High speed detection clears register (Write Only)

Select Address	Explanation of Operation
0x0A[0]	If 0x1 writes in, a high speed detection flag will be cleared.

Caution: When using Auto recovery from clock error function (P.62) , the above-mentioned flag is cleared automatically.

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18.3 BCLK High or Low Speed Detection function - continued

Low speed detection clear register (Write Only)

Select Address	Explanation of Operation
0x0B[0]	If 0x1 is written, a low speed detection flag will be cleared.

Caution: When using Auto recovery from clock error function (P.62) , the above-mentioned flag is cleared automatically.

A constraint of the count of judging with high speed flag detection

Default=0x2

Select Address	Explanation of Operation
0x0A[6:4]	Set over 0x1. (0x1 to 0x7 are set up) it become 0x0A[1]=0x1 if the BCLK high speed condition more than the count of setting up is detected continuously.

A constraint of the count of judging with low speed flag detection

Default=0x2

Select Address	Explanation of Operation
0x0B[6:4]	Set over 0x1. (0x1 to 0x7 are set up) it become 0x0B[1]=0x1 if the BCLK low speed condition more than the count of setting up is detected continuously.

High speed detection flag valid or invalid

Default=0x0

Select Address	Value	Explanation of Operation
0x0A[7]	0x0	Valid
	0x1	Invalid

Low speed detection flag valid or invalid

Default=0x0

Select Address	Value	Explanation of Operation
0x0B[7]	0x0	Valid
	0x1	Invalid

The frequency range of BCLK by which high speed detection or low speed detection is carried out is as follows.

Setting1	Setting2	Low Speed Detection Lowest Frequency (MHz)	High Speed Detection Highest Frequency (MHz)
64fs BCLK (0x03[5:4]=0x0)	48kHz (0x0C[1:0]=0x0)	1.28	7.13
	44.1kHz (0x0C[1:0]=0x1)	1.21	6.55
	32kHz (0x0C[1:0]=0x2)	0.88	4.76
48fs BCLK (0x03[5:4]=0x1)	48kHz (0x0C[1:0]=0x0)	0.96	5.35
	44.1kHz (0x0C[1:0]=0x1)	0.91	4.92
	32kHz (0x0C[1:0]=0x2)	0.66	3.57
32fs BCLK (0x03[5:4]=0x2)	48kHz (0x0C[1:0]=0x0)	0.64	3.56
	44.1kHz (0x0C[1:0]=0x1)	0.60	3.28
	32kHz (0x0C[1:0]=0x2)	0.44	2.38

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Description of Function – continued

19 Auto Recovery of Clock Error Function

Establishment of Clock stop detection flag or BCLK high speed detection flag or BCLK low speed detection flag makes PWM output mute (Immediate mute).
In that case, if the Auto Recovery of Clock Error Function is enabled, when it returns to a normal input, a mute condition will be cancelled automatically.
When Auto Recovery of Clock Error Function is cancelled, it is necessary to control a series of operations called a mute-on and flag clear command transmission, an internal RAM data clear and mute release from an external microcomputer. Since it is invalid immediately after a wake-up, 0x0D[6]=0x1 is set up before mute release, and it is recommended to enable this function.

Valid or invalid auto recover from clock error

Default=0x0

Select Address	Value	Explanation of Operation
0x0D[6]	0x0	Invalid
	0x1	Valid

Each error flag can be read from the following addresses. When 0x1 is read from a read address, the error flag establishes. Moreover, a flag is not cleared until it writes 0x0 in the target address, even if error status will be canceled, once a flag leaves.

Error flag read register

Select Address	Explanation of Operation
0x0E[6]	Synchronous error flag
0x0E[4]	LRCLK stop flag
0x0E[3]	BCLK stop flag
0x0E[2]	BCLK high speed detection flag
0x0E[1]	BCLK low speed detection flag

20 The Wake-up Procedure of Power-up

It has to start power-up in the following procedures.
0x**=0x** means writing data to register. (For example) 0x10=0x00 It means writing data 0x00 to select address 0x10.

1. Power-up (VCCP1, VCCP2, DVDD)
   Input BCLK and LRCLK
   Wait over 10ms
   Input stable BCLK and LRCLK in the specification
   Wait over 1ms
2. Release reset (RSTX=High)
   Wait over 1ms
3. 0x0C=0x00 : Sampling rate setting
   (Set 48kHz: 0x00, 44.1kHz: 0x01, 32kHz: 0x02 to 0x0C address)
4. 0xE9=0x10 : Clock initialization
   Wait over 100ms
5. 0x01=0x00 : Set RAM clear OFF
6. 0x0D=0x40 : Valid auto recover from clock error
7. 0x0E=0x00 : Clear error flag
8. 0x92=0x1D : PWM setting1
9. 0x93=0x1B : PWM setting2
10. 0x94=0x0F : PWM setting3
11. 0x95=0x11 : PWM setting4
12. 0x90=0x40 : PWM setting5
13. 0xF4=0x14 : Protect function initialization
14. 0xF3=0x03 : Driver Gain setting (0x03: 26dB, 0x0B: 32dB)
15. 0xF2=0x02 : Stereo application setting (0x02: Stereo, 0x0A: Monaural)
16. 0xF8=0x01 : 0xF4, 0xF3, 0xF2 setting value is fixed
    Wait over 10ms
17. Set up DSP function such as volume, BQ, DRC, and Pre-Scaler etc.
18. MUTEX=High : Release mute

(Order from 8 to 12 and 17 can be interchanged.)

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Description of Function - continued

21 The Operating Procedure in a Status with an Unstable Clock

In the period there is the possibility that inputted I²S, BCLK, LRCLK and SDATA, may become unstable, set MUTEX=Low to mute output.

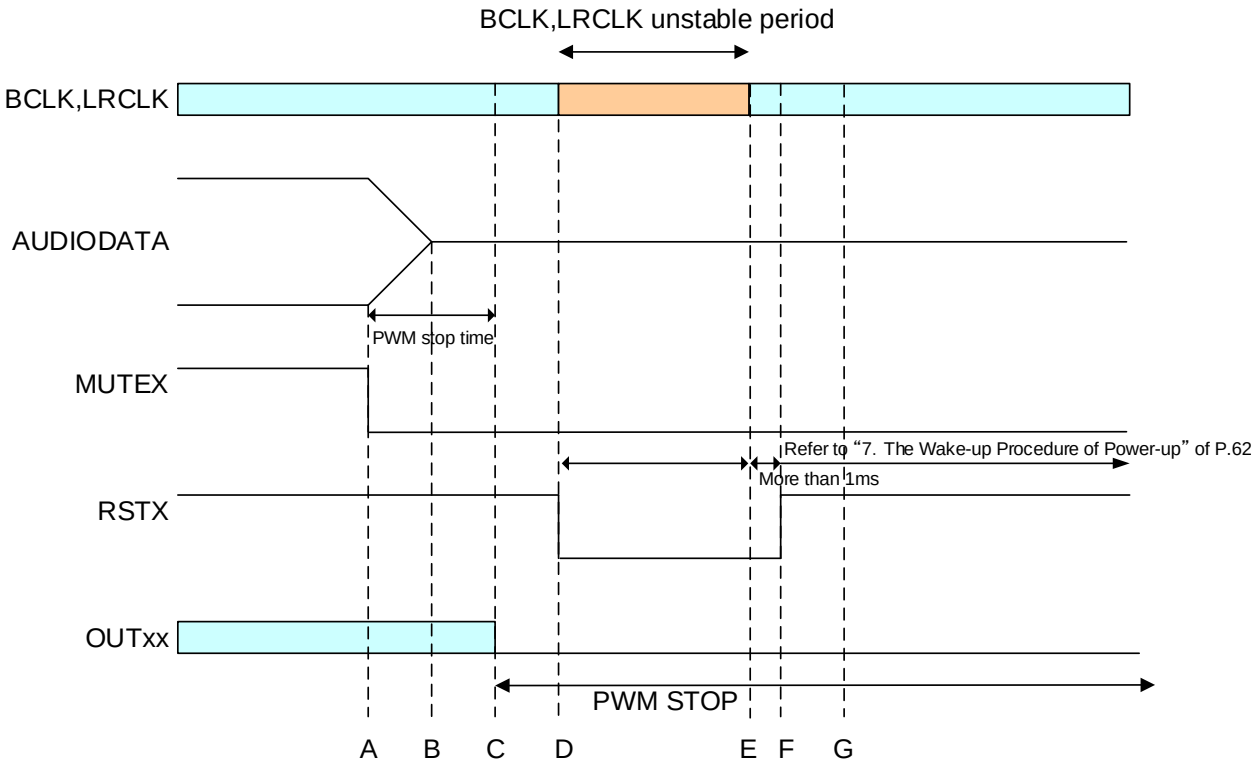


Figure 68. The Operating Procedure in a Status with an Unstable Clock

Caution: When clock stop was detected, mute release procedure will follow the clock stop error release sequence.

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Description of Function – continued

22 I²S Data Output Select

Capable of output I²S format digital audio data from SDATAO (pin12).
That signal synchronizes to inputted LRCK and BCK signal.
And enable to select output SDATA signal as shown below.
The Point of selected data is shown below diagram.
Whatever output is selected, hard clip is processed.

SDATAO output select

Default=0x0

Select Address	Value	Explanation of Operation
0x78[6:4]	0x0	DSP output (Point1)
	0x1	DSP input (Point2)
	0x2	Pre-Scaler output (Point3)
	0x3	Mixer output (Point4)
	0x4	12Band BQ output (Point5)
	0x5	Fine master volume output (Point6)
	0x6	Don't use
	0x7	Fine Post-Scaler output (Point7)

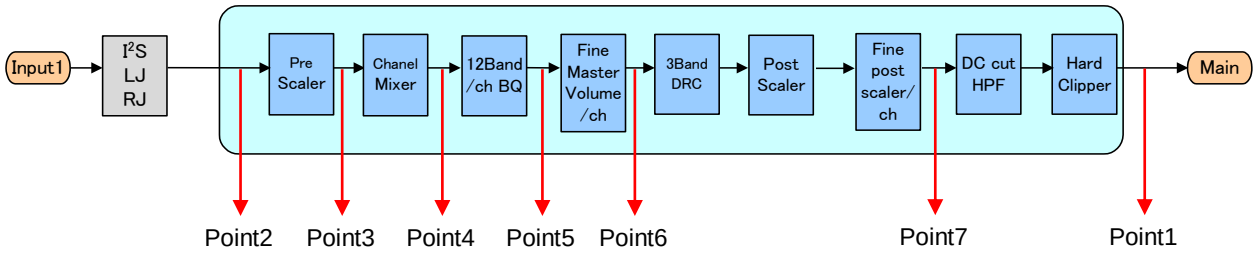


Figure 69

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Register Map

Address	Initial Value	Recommended value	Description	Function
0x01	0xE0	0x00*(Note 22)*	RAM clear	RAM clear setting
0x02	0x00	0x00	Bypass	Select bypass blocks
0x03	0x02	0x02	Digital audio input 1	I^2S input format setting
0x06	0x20	0x20	Synchronous error 2	Synchronous error setting
0x07	0x8A	0x8A	LRCLK,BCLK stop detection 1	LRCLK stop detection setting
0x08	0x00	0x00	LRCLK,BCLK stop detection 2	BCLK stop detection setting
0x09	Read/Write Only	-	LRCLK,BCLK stop detection 3	Read/Clear stop detection
0x0A	0x20	0x20	BCLK Measurement of velocity 1	BCLK fast detection setting
0x0B	0x20	0x20	BCLK Measurement of velocity 2	BCLK slow detection setting
0x0C	0x00	0x00 (48kHz sampling) *(Note 22)*	Sampling frequency setting	Sampling frequency setting
0x0D	0x00	0x40*(Note 22)*	Auto return 1	Auto return setting
0x0E	Read Only	0x00*(Note 22)*	Auto return 2	Auto return monitor
0x10	0x00	0x00	Volume, Balance, Post-scaler 1	Fine volume setting/ Independent volume setting
0x11	0xFF	0xFF	Volume, Balance, Post-scaler 2	Lch/dependent Volume setting (0dB: 0x30)
0x12	0xFF	0xFF	Volume, Balance, Post-scaler 3	Rch volume setting (0dB: 0x30)
0x13	0x60	0x60	Volume, Balance, Post-scaler 4	Post-scaler setting (0dB: 0x60)
0x14	0x88	0x88	Volume, Balance, Post-scaler 5	L/R fine postscaler setting
0x15	0x03	0x00	Mute function	Mute transition time setting
0x16	0x60	0x60	Pre-Scaler	Pre-Scaler setting (0dB: 0x60)
0x17	0x12	0x12	Channel mixer	Channel mixer setting
0x18	0x01	0x01	DC Cut HPF	DC cut HPF setting
0x1A	0x01	0x01	Hard Clipper 1	Hard Clipper setting
0x1B	0xE1	0xE1	Hard Clipper 2	Hard Clip level setting
0x20	0xFC	0xFC	DRC common 1	DRC select setting
0x21	0xC0	0xC0	DRC common 2	Transition form setting
0x28	0x40	0x40	AGC_TH1 setting of DRC1	Threshold setting
0x29	0x80	0x80	Slope (α) setting of DRC1	Slope setting
0x2A	0x3B	0x3B	RATE setting of DRC1	A_RATE and R_RATE setting
0x2B	0x13	0x13	TIME setting of DRC1	A_TIME and R_TIME setting
0x2C	0x40	0x40	AGC_TH2 setting of DRC1	Threshold setting
0x2E	0x3B	0x3B	RATE setting of DRC1	A_RATE and R_RATE setting
0x2F	0x13	0x13	TIME setting of DRC1	A_TIME and R_TIME setting

(Note 22) It must be set at the time of start-up. Refer to P.62 “20. The wake-up Procedure of power-up”.

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Register Map - continued

Address	Initial Value	Recommended value	Description	Function
0x30	0x40	0x40	AGC_TH1 setting of DRC2	Threshold setting
0x31	0x80	0x80	Slope (α) setting of DRC2	Slope setting
0x32	0x3B	0x3B	RATE setting of DRC2	A_RATE and R_RATE setting
0x33	0x13	0x13	TIME setting of DRC2	A_TIME and R_TIME setting
0x34	0x40	0x40	AGC_TH2 setting of DRC2	Threshold setting
0x36	0x3B	0x3B	RATE setting of DRC2	A_RATE and R_RATE setting
0x37	0x13	0x13	TIME setting of DRC2	A_TIME and R_TIME setting
0x38	0x40	0x40	AGC_TH1 setting of DRC3	Threshold setting
0x39	0x80	0x80	Slope (α) setting of DRC3	Slope setting
0x3A	0x3B	0x3B	RATE setting of DRC3	A_RATE and R_RATE setting
0x3B	0x13	0x13	TIME setting of DRC3	A_TIME and R_TIME setting
0x3C	0x40	0x40	AGC_TH2 setting of DRC3	Threshold setting
0x3D	0x3B	0x3B	RATE setting of DRC3	A_RATE and R_RATE setting
0x3E	0x13	0x13	TIME setting of DRC3	A_TIME and R_TIME setting
0x3F	0x00	0x00	DRC4 ON	ON/OFF setting
0x40	0x40	0x40	AGC_TH2 setting of DRC4	Threshold setting
0x41	0x3B	0x3B	RATE setting of DRC4	A_RATE and R_RATE setting
0x42	0x13	0x13	TIME setting of DRC4	A_TIME and R_TIME setting
0x51	0x00	0x00	Bi-quad type filter1	Select of BQ soft transition Band
0x53	0x0C	0x0C	Bi-quad type filter2	Setting of transition time and wait time
0x58	Write Only	-	Bi-quad type filter3	Soft transition start, 0x0: Stop 0x1: Start
0x59	Read Only	-	Bi-quad type filter4	Soft transition flag
0x60	0x00	0x00	The coefficient is written directly. 1	Select of BQ independence or synchronous setting
0x61	0x00	0x00	The coefficient is written directly. 2	Coefficient address bit7 to bit0
0x62	0x00	0x00	The coefficient is written directly. 3	Coefficient data bit23 to bit16
0x63	0x00	0x00	The coefficient is written directly. 4	Coefficient data bit15 to bit8
0x64	0x00	0x00	The coefficient is written directly. 5	Coefficient data bit7 to bit0
0x65	Write Only	-	The coefficient is written directly. 6	The writing of coefficients is performed
0x66	Read Only	-	The coefficient is written directly. 7	Coefficient reading bit23 to bit16
0x67	Read Only	-	The coefficient is written directly. 8	Coefficient reading bit15 to bit8
0x68	Read Only	-	The coefficient is written directly. 9	Coefficient reading bit7 to bit0
0x70	0x00	0x00	Small signal detection1	Small signal detection level setting
0x71	0x00	0x00	Small signal detection2	Small signal detection time setting
0x72	Read Only	-	Small signal detection3	Small signal detection flag read-back
0x74	0x00	0x00	Level meter1	Setting of the peak level hold time interval
0x75	Write Only	-	Level meter2	0x0: Lch 0x1: Rch 0x2: (Lch+Rch) /2
0x76	Read Only	-	Level meter3	Level reading (16bit high position 8bit)
0x77	Read Only	-	Level meter4	Level reading (16bit subordinate position 8bit)
0x78	0x02	0x02	SDATAO	SDATAO select

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Register Map - continued

Address	Initial Value	Recommended value	Description	Function
0x90	0x00	0x40*(Note 22)*	PWM setting 5	PWM initialization
0x92	0x00	0x1D*(Note 22)*	PWM setting 1	PWM delay
0x93	0x01	0x1B*(Note 22)*	PWM setting 2	PWM delay
0x94	0x04	0x0F*(Note 22)*	PWM setting 3	PWM delay
0x95	0x05	0x11*(Note 22)*	PWM setting 4	PWM delay
0xE9	0x01	0x10 (normal) *(Note 22)*	DSP clock setting	DSP clock initialization
0xF2	0x02	0x02 (Stereo) *(Note 22)*	Stereo/Mono	DC voltage protection setting for Stereo / Mono
0xF3	0x03	0x03 (26dB) *(Note 22)*	Driver Gain	Driver Gain setting (26dB or 32dB)
0xF4	0x04	0x14 *(Note 22)*	Protection initialization	Protection initialization
0xF8	0x00	0x01*(Note 22)*	The decision of 0xF2, 0xF3 and 0xF4	Decided by sending 0x01

(Note 22) It must be set at the time of start-up. Refer to P.62 “20. The wake-up Procedure of power-up”.

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Application Circuit Example1 (Stereo BTL output, R_L=8Ω, V_{CCP1}, V_{CCP2}≤22V)

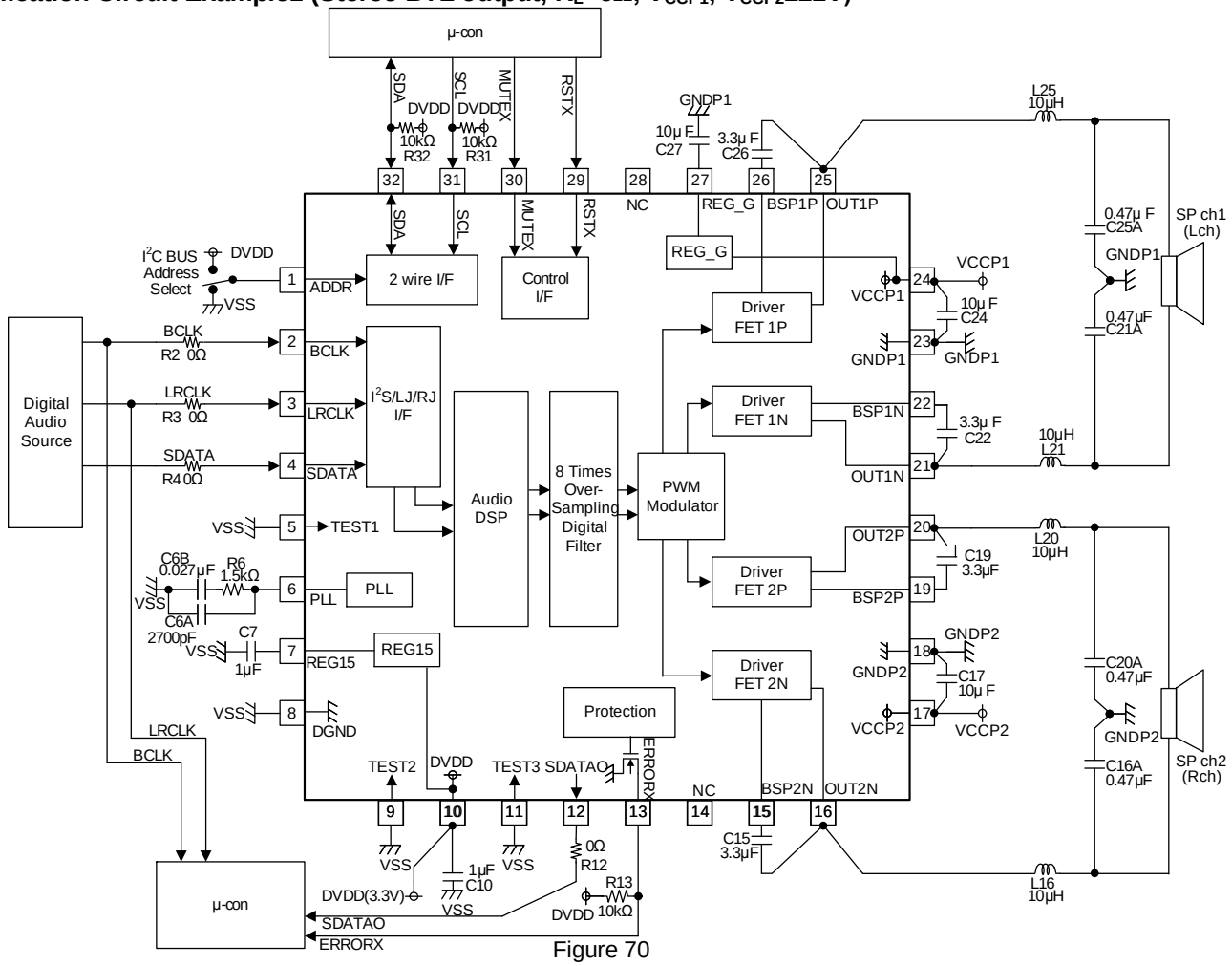


Figure 70

Parts	Qty	Parts No.	Description
Inductor	4	L16, L20, L21, L25	10µH / 3.8A / (±20%)
Resistor	1	R6	1.5kΩ / 1/16W / F(±1%)
	2	R31, R32	10kΩ / 1/16W / J(±5%)
	4	R2, R3, R4, R12	0Ω / 1/10W / J(±5%)
	1	R13	10kΩ / 1/16W / J(±5%)
Capacitor	1	C6A	2700pF / 6.3V / B(±10%)
	1	C6B	0.027µF / 6.3V / B(±10%)
	4	C16A, C20A, C21A, C25A	0.47µF / 50V / B(±10%)
	2	C17, C24	10µF / 35V / B(±10%)
	4	C15, C19, C22, C26	3.3µF / 16V / B(±10%)
	2	C7, C10	1.0µF / 10V / B(±10%)
	1	C27	10µF / 16V / B(±10%)

Caution 1: If the impedance characteristics of the speakers at high-frequency range increase rapidly, the LSI might not have stable operation in the resonance frequency range of the LC filter. Therefore, consider adding damping-circuit, etc., depending on the impedance of the speaker.

Caution 2: Though this LSI has a short protection function, when short to VCC or GND after the LC filter, over-current occurs during short protection function operation. Be careful about over/undershoot which exceeds the maximum standard ratings because back electromotive force of the inductor will occur which sometimes leads to LSI destruction.
The Inductor must be used to the coil with large margin of rated DC current (saturation current). When the short-circuit of the speaker output (after the LC filter) to VCC or GND occurs when the coil with small rated DC current is used, LSI destruction might be caused. Because the coil causes the magnetic saturation behavior, it instantaneously passes the heavy-current to LSI.

Caution 3: Overshoot of output PWM differs according to the board or coupling capacitor of V_{CC}, and etc. Check to ensure that it is lower than absolute maximum ratings.
If it exceeds the absolute maximum ratings, snubber circuit must need to be added.

Caution 4: When it is used at V_{CCP1}, V_{CCP2}>22V, snubber circuit must need to be added, and must change LC filter value to suppress the influence of the LCR resonance.

Caution 5: This circuit constant is value with ROHM evaluation board, and adjustment of the constant may be necessary for the application board. Must carry out enough evaluations.

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Application Circuit Example2 (Stereo BTL output, R_L=8Ω, 22V<V_{CCP1}, V_{CCP2}≤24V)

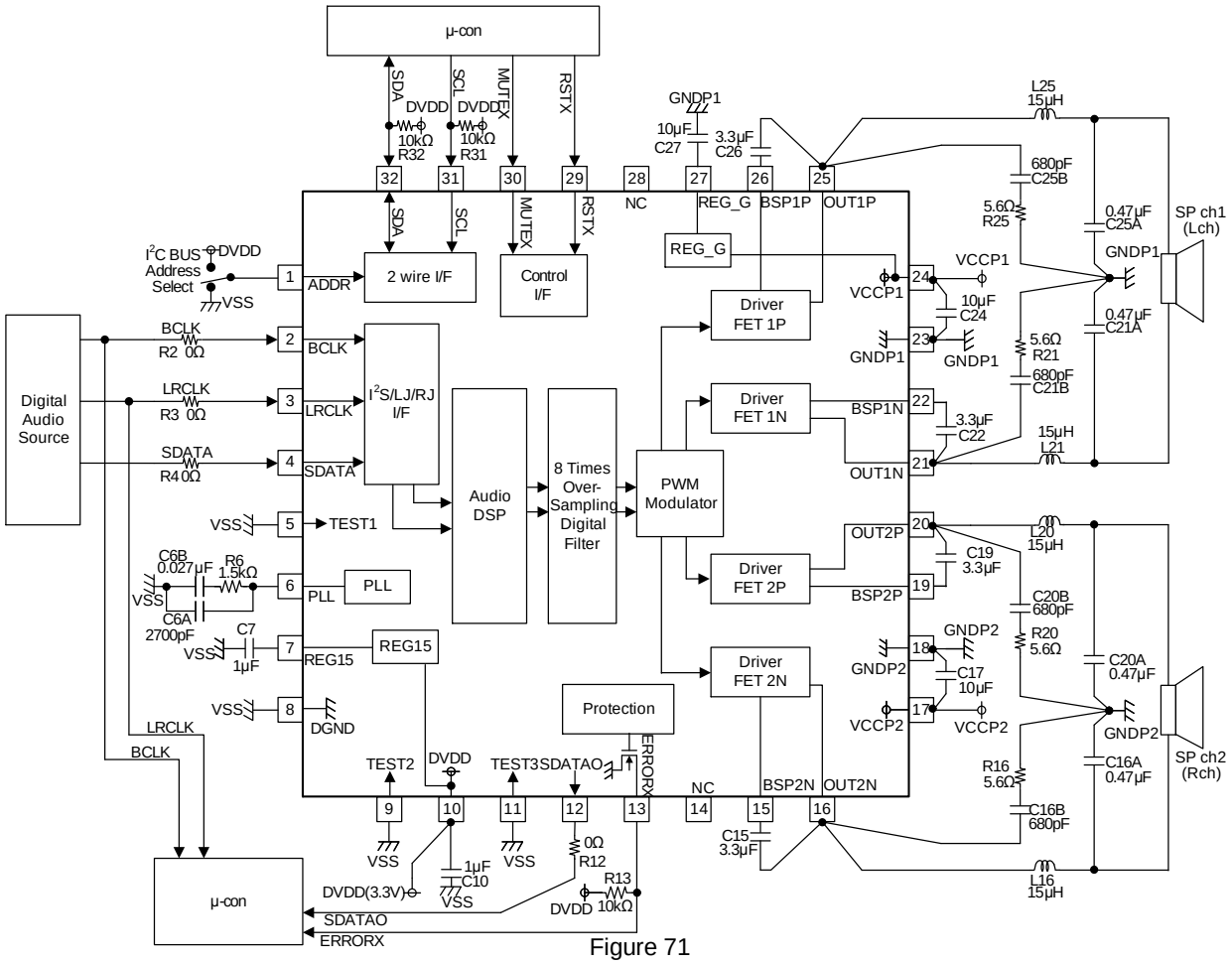


Figure 71

Parts	Qty	Parts No.	Description
Inductor	4	L16, L20, L21, L25	15µH / 2.9A / (±20%)
Resistor	1	R6	1.5kΩ / 1/16W / F(±1%)
	2	R31, R32	10kΩ / 1/16W / J(±5%)
	4	R2, R3, R4, R12	0Ω / 1/10W / J(±5%)
	4	R16, R20, R21, R25	5.6Ω / 1/4W / J(±5%)
	1	R13	10kΩ / 1/16W / J(±5%)
Capacitor	1	C6A	2700pF / 6.3V / B(±10%)
	1	C6B	0.027µF / 6.3V / B(±10%)
	4	C16B, C20B, C21B, C25B	680pF / 50V / CH(±5%)
	4	C16A, C20A, C21A, C25A	0.47µF / 50V / B(±10%)
	2	C17, C24	10µF / 35V / B(±10%)
	4	C15, C19, C22, C26	3.3µF / 16V / B(±10%)
	2	C7, C10	1.0µF / 10V / B(±10%)
	1	C27	10µF / 16V / B(±10%)

Caution 1: If the impedance characteristics of the speakers at high-frequency range increase rapidly, the LSI might not have stable operation in the resonance frequency range of the LC filter. Therefore, consider adding damping-circuit, etc., depending on the impedance of the speaker.

Caution 2: Though this LSI has a short protection function, when short to VCC or GND after the LC filter, over-current occurs during short protection function operation. Be careful about over/undershoot which exceeds the maximum standard ratings because back electromotive force of the inductor will occur which sometimes leads to LSI destruction.
The Inductor must be used to the coil with large margin of rated DC current (saturation current). When the short-circuit of the speaker output (after the LC filter) to VCC or GND occurs when the coil with small rated DC current is used, LSI destruction might be caused. Because the coil causes the magnetic saturation behavior, it instantaneously passes the heavy-current to LSI.

Caution 3: Overshoot of output PWM differs according to the board or coupling capacitor of VCC, and etc. Check to ensure that it is lower than absolute maximum ratings.
If it exceeds the absolute maximum ratings, snubber circuit must need to be added.

Caution 4: When it is used at V_{CCP1}, V_{CCP2}>22V, snubber circuit must need to be added, and must change LC filter value to suppress the influence of the LCR resonance.

Caution 5: This circuit constant is value with ROHM evaluation board, and adjustment of the constant may be necessary for the application board. Must carry out enough evaluations.

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Application Circuit Example3 (Monaural BTL output(Note 23), R_L=4Ω, V_{CCP1}, V_{CCP2}≤14V)

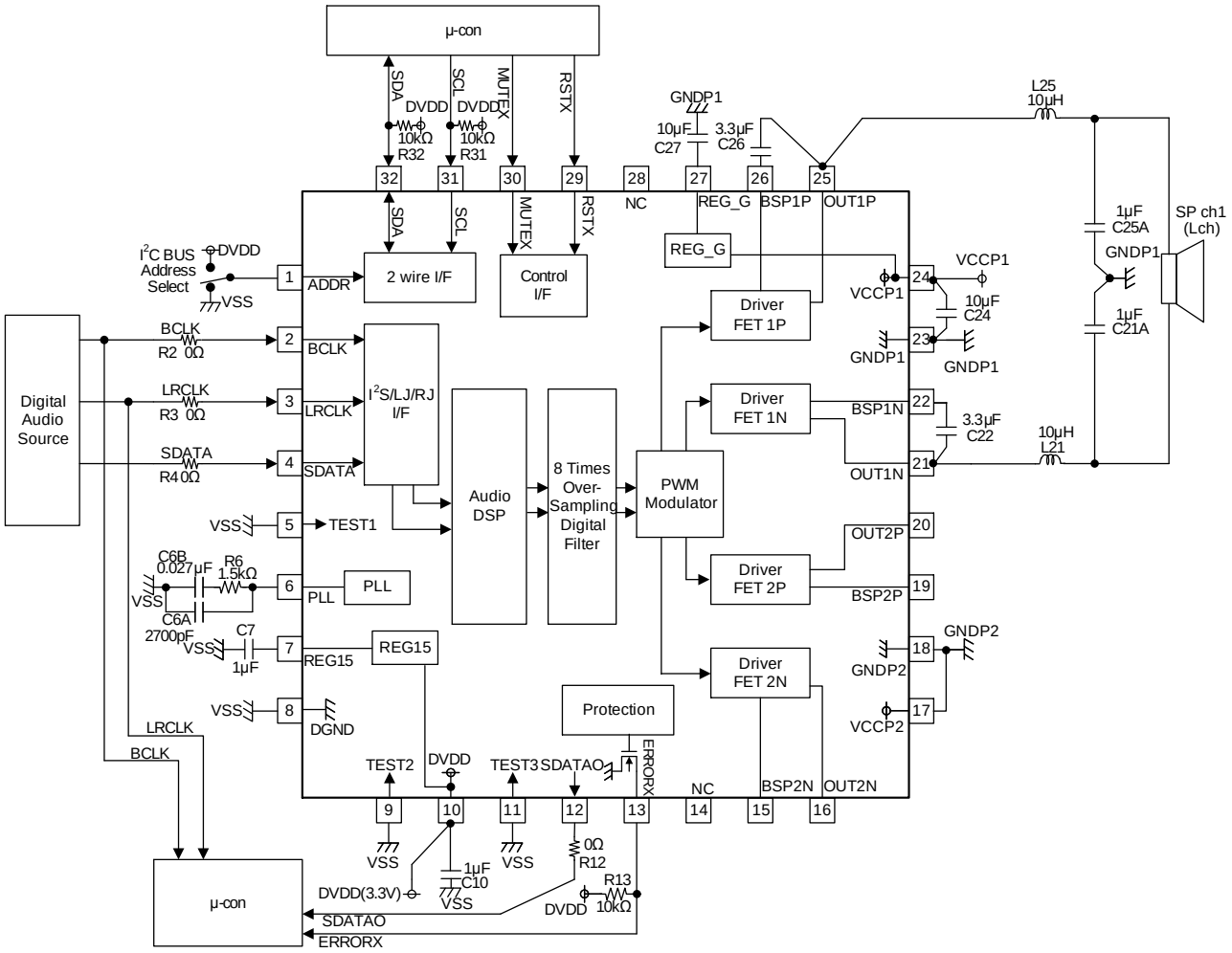


Figure 72

Parts	Qty	Parts No.	Description
Inductor	2	L21, L25	10µH / 3.8A / (±20%)
Resistor	1	R6	1.5kΩ / 1/16W / F(±1%)
	2	R31, R32	10kΩ / 1/16W / J(±5%)
	4	R2, R3, R4, R12	0Ω / 1/10W / J(±5%)
	1	R13	10kΩ / 1/16W / J(±5%)
Capacitor	1	C6A	2700pF / 6.3V / B(±10%)
	1	C6B	0.027µF / 6.3V / B(±10%)
	2	C21A, C25A	1.0µF / 50V / B(±10%)
	1	C24	10µF / 35V / B(±10%)
	2	C22, C26	3.3µF / 16V / B(±10%)
	2	C7, C10	1.0µF / 10V / B(±10%)
	1	C27	10µF / 16V / B(±10%)

Caution 1: If the impedance characteristics of the speakers at high-frequency range increase rapidly, the LSI might not have stable operation in the resonance frequency range of the LC filter. Therefore, consider adding damping-circuit, etc., depending on the impedance of the speaker.

Caution 2: Though this LSI has a short protection function, when short to VCC or GND after the LC filter, over-current occurs during short protection function operation. Be careful about over/undershoot which exceeds the maximum standard ratings because back electromotive force of the inductor will occur which sometimes leads to LSI destruction.
The Inductor must be used to the coil with large margin of rated DC current (saturation current). When the short-circuit of the speaker output (after the LC filter) to VCC or GND occurs when the coil with small rated DC current is used, LSI destruction might be caused. Because the coil causes the magnetic saturation behavior, it instantaneously passes the heavy-current to LSI.

Caution 3: Overshoot of output PWM differs according to the board or coupling capacitor of VCC, and etc. Check to ensure that it is lower than absolute maximum ratings. If it exceeds the absolute maximum ratings, snubber circuit must need to be added.

Caution 4: This circuit constant is value with ROHM evaluation board, and adjustment of the constant may be necessary for the application board. Must carry out enough evaluations.

(Note 23) Register setting of 0xF2=0x0A and 0xF8=0x01 is necessary at the time of start-up (in state of MUTEX=Low).
(Refer to “Monaural output setting”.)

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Selection of Components Externally Connected

1 Output LC Filter Circuit

An output filter is required to eliminate radio-frequency components exceeding the audio-frequency region supplied to a load (speaker). Because this LSI uses sampling frequency 384kHz (f_S=48kHz) in the output PWM signals, the high-frequency components must be appropriately removed.
This section takes an example of an LC type LPF shown below, in which coil L and capacitor C_g compose a differential filter with an attenuation property of -12dB/oct.

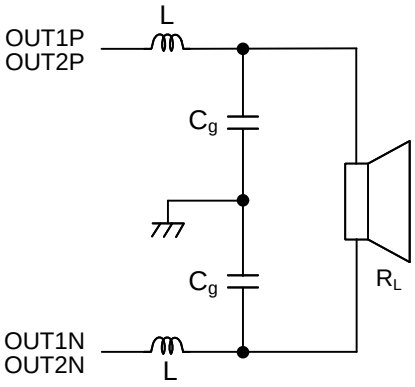


Figure 73. Output LC Filter

Following presents output LC filter constants with typical load impedances.

R_L	L	C_g	Note
4Ω	10μH	1μF	V_{CCP1}, V_{CCP2}≤14V
6Ω	10μH	0.68μF	V_{CCP1}, V_{CCP2}≤22V
	15μH	0.47μF	V_{CCP1}, V_{CCP2}>22V
8Ω	10μH	0.47μF	V_{CCP1}, V_{CCP2}≤22V
	15μH	0.47μF	V_{CCP1}, V_{CCP2}>22V

Use coils with a low direct-current resistance and a sufficient margin of allowable currents. In addition, select a closed magnetic circuit type product in normal cases to prevent unwanted emission. A high direct-current resistance causes power losses.
When the short-circuit of the speaker output (After the LC filter) to VCC or GND occurs when the coil with small rated DC current is used, LSI destruction might be caused. Because the coil causes the magnetic saturation behavior, it instantaneously passes the heavy-current to LSI.
When using at V_{CCP1}, V_{CCP2}>22V, the coil of the rated DC current: 7.2A or more will be recommended.
And, f_{CL} (LC resonance frequency) of the LC filter should be lowered and decrease the influence of LC resonance.

Use capacitors with low equivalent series resistance and good impedance characteristics at high frequency ranges.
Also, select the parts with the margin of the ratings enough.

2 The Value of the LC Filter Circuit Computed Equation

The output LC filter circuit of BM28723AMUV is as it is shown in Figure 74. The LC filter circuit of Figure 74 is thought to substitute it like Figure 75 on the occasion of the computation of the value of the LC filter circuit.

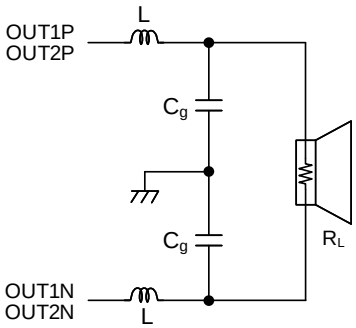


Figure 74. Output LC Filter 1

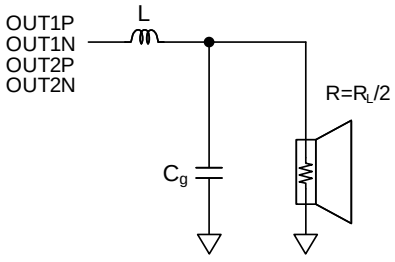


Figure 75. Output LC Filter 2

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2 The Value of the LC Filter Circuit Computed Equation - continued

The transfer function H(s) of the LC filter circuit of Figure 75. becomes the following.

$$H(s)=\frac{\frac{1}{LC_g}}{s^2+\frac{1}{C_gR}s+\frac{1}{LC_g}}=\frac{\omega^2}{s^2+\frac{\omega}{Q}s+\omega^2}$$

The ω and Q become the followings here.

$$\omega^2=\frac{1}{LC_g} \qquad \omega=2\pi f_{CL} \qquad f_{CL}=\frac{1}{2\pi\sqrt{LC_g}}$$

$$Q=R\sqrt{\frac{C_g}{L}}=\frac{1}{2}R_L\sqrt{\frac{C_g}{L}}$$

Therefore, L and C_g become the followings.

$$L=\frac{1}{\omega^2C_g}=\frac{R_L}{4\pi f_{CL}Q} \qquad C_g=\frac{Q}{\omega R}=\frac{Q}{\pi f_{CL}R_L}$$

The R_L and L should be made known, and f_{CL} is set up, and C_g is decided.

3 The Settlement of the Inductance Value of the Coil

A standard for selection of the L value of a coil to use is to take the following consideration except for the factor such as a low cost, miniaturization and thin.

1.When the inductance value was made small

- •Circuit electric currents increase without a signal. Efficiency in the low output power gets bad.
- •Direct current resistance value of the coil becomes small.
  Therefore, maximum output power becomes bigger.
  Rated DC current and Temperature rise current of the coil become high.

2.When the inductance value was made large

- •Circuit electric current is decrease without a signal. Efficiency in the low output power improves.
- •Direct current resistance value of the coil becomes big.
  Therefore, maximum output power becomes smaller.
  Rated DC current and Temperature rise current of the coil becomes low.

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Selection of Components Externally Connected - continued

4 Snubber Circuit Constant

When overshoot of PWM Output exceeds absolute maximum rating, and when V_{CCP1}, V_{CCP2}>22V, or when overshoot of PWM output negatively affects EMI, or when ringing deteriorates the audio characteristic of the PWM output, snubber circuit is used as shown below.

1. Measure the ringing resonance frequency f_1 of PWM output waveform (when rising) by using low capacitance Probe (e.g. FET probe) at the OUT pin. (Figure 76)
   Shorten GND lead of FET probe and monitor as near as possible to output pin.
2. Measure the resonance frequency f_2 of the ringing as the snubber-circuit Rsnb=0Ω (capacitor is connected to GND)
   Adjust the value of the capacitor C until it becomes half of f_1 ($2f_2=f_1$).
   The value of C that becomes ($2f_2=f_1$) is 3 times of the parasitic capacity C_p that a ringing is formed. ($C=3C_p$)
3. Parasitic inductance L_p is calculated using the next formula.

$$L_p = \frac{1}{(2\pi f_1)^2 C_p}$$

4. The characteristics impedance Z of resonance is calculated from the parasitic capacity C_p and the parasitic inductance L_p using the next formula.

$$Z = \sqrt{\frac{L_p}{C_p}}$$

5. Set snubber circuit R_{snb} same as the character impedance Z.
   Set snubber circuit C_{snb} 4 to 10 times of the parasitic capacity C_p ($C_{snb}=4C_p$ to $10C_p$).
   If C_{snb} value is set large, switching current will possibly increase.
   Therefore, please decide it by the trade-off with the characteristic.

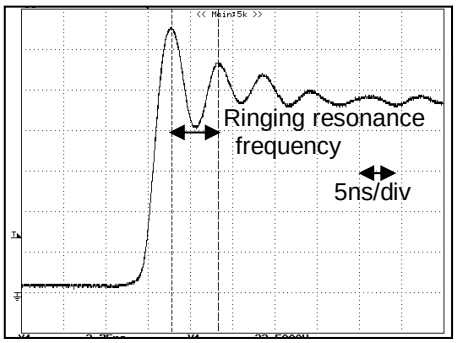


Figure 76. PWM Output Waveform
(Measure of spike resonance frequency)

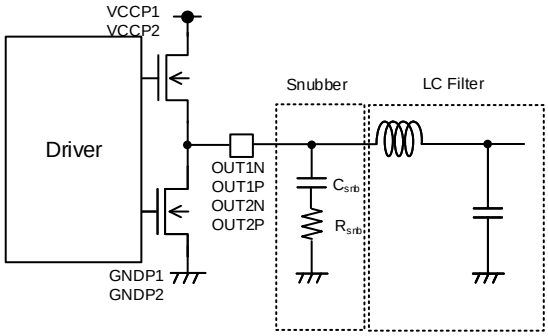


Figure 77. Snubber Schematic

Following presents Snubber filter constants with the recommendation value at 22V<V_{CCP1}, V_{CCP2}≤24V, R_L=8Ω, Po=10W+10W, ROHM 4 layer board*(Note 12).*

C_{snb}	R_{snb}
680pF 50V CH (±5%)	5.6Ω 1/4W J (±5%)

Following presents Snubber filter constants with the recommendation value at V_{CCP1}, V_{CCP2}≤22V, R_L=8Ω, Po=10W+10W, ROHM 4 layer board*(Note 12).*

C_{snb}	R_{snb}
470pF 50V CH (±5%)	0Ω or 5.6Ω 1/8W J (±5%)

(Note 12) 100mmx100mmx1.6mm FR4 4-layer glass epoxy board Cu Thickness 35µm/70µm/70µm/35µm For Application Evaluation Board

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Selection of Components Externally Connected - continued

5 Operating Condition with the Application Component

Parameter	Parts No.	Limit			Unit	Conditions
		Min	Typ	Max		
Coupling Capacitor for Power Supply	C17, C24	1*(Note 24)*	10	-	µF	B characteristics Ceramic type capacitor recommended
Capacitor for REG_G	C27	1*(Note 24)*	10	13.5*(Note 26)*	µF	B characteristics, 16V Ceramic type capacitor recommended
Capacitor for REG15	C7	0.4*(Note 24)*	1.0	1.35*(Note 26)*	µF	B characteristics, 10V Ceramic type capacitor recommended
Capacitor for BSP	C15, C19, C22, C26	2.0*(Note 24)* *(Note 25)*	3.3	4.5*(Note 26)*	µF	B characteristics, 16V Ceramic type capacitor recommended
		2.0*(Note 24)* *(Note 25)*	4.7	6.3*(Note 26)* *(Note 27)*	µF	B characteristics, 16V Ceramic type capacitor recommended

(Note 24) Should use the capacity of the capacitor not to be less than a minimum in consideration of temperature characteristics and dc-bias characteristics.
(Note 25) Minimum value to guarantee Speaker output operating range (20Hz to 20kHz, sin wave, THD+N ≤ 10%)
(Note 26) Use it within this rating. (Capacitance±10%, Capacitance change ratio±22%)
(Note 27) Influence it at the RSTX → MUTEX Wait time (T_{WAIT}: Refer to P.27) at the time of the Power Supply Start-up. Use it within this rating.

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Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the LSI. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the LSI's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition. However, pins that drive inductive loads (e.g. motor driver outputs, DC-DC converter outputs) may inevitably go below ground due to back EMF or electromotive force. In such cases, the user should make sure that such voltages going below ground will not cause the LSI and the system to malfunction by examining carefully all relevant factors and conditions such as motor characteristics, supply voltage, operating frequency and PCB wiring to name a few.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Recommended Operating Conditions**
   These conditions represent a range within which the expected characteristics of the LSI can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

6. **Inrush Current**
   When power is first supplied to the LSI, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the LSI has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. **Testing on Application Boards**
   When testing the LSI on an application board, connecting a capacitor directly to a low-impedance output pin may subject the LSI to stress. Always discharge capacitors completely after each process or step. The LSI's power supply should always be turned OFF completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the LSI during assembly and use similar precautions during transport and storage.

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Operational Notes – continued

8. Inter-pin Short and Mounting Errors

Ensure that the direction and position are correct when mounting the LSI on the PCB. Incorrect mounting may result in damaging the LSI. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

9. Unused Input Pins

Input pins of an LSI are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the LSI. So, unless otherwise specified, unused input pins should be connected to the power supply or ground line.

10. Regarding the Input Pin of the LSI

This LSI contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When ground > Pin A and ground > Pin B, the P-N junction operates as a parasitic diode.

When ground > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the LSI. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the ground voltage to an input pin (and thus to the P substrate) should be avoided.

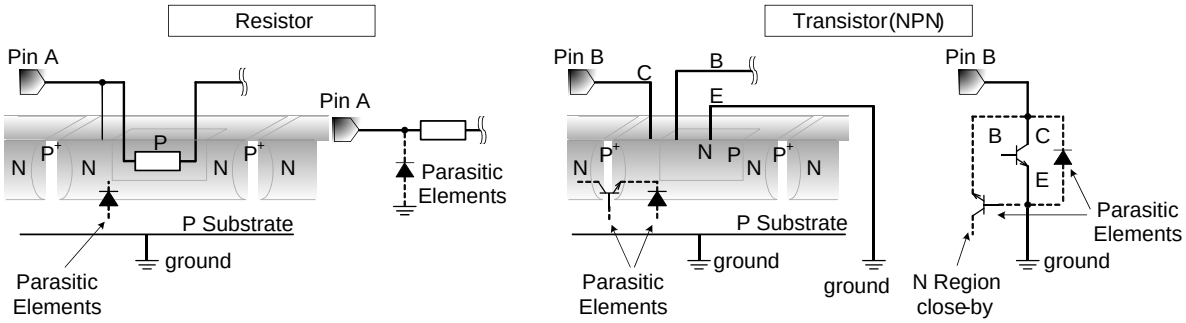


Figure 78. Example of LSI structure

11. Ceramic Capacitor

When using a ceramic capacitor, determine the dielectric constant considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

12. Thermal Shutdown Circuit (TSD)

This LSI has a built-in thermal shutdown circuit that prevents heat damage to the LSI. Normal operation should always be within the LSI's maximum junction temperature rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF all output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.

Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the LSI from heat damage.

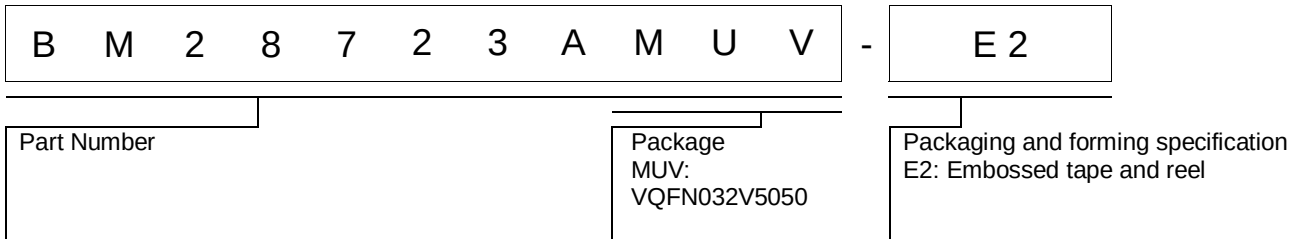
13. Over Current Protection Circuit (OCP)

This LSI incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the LSI should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

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Ordering Information



The tape of BM28723AMUV-E2 is a dry pack.

Marking Diagram

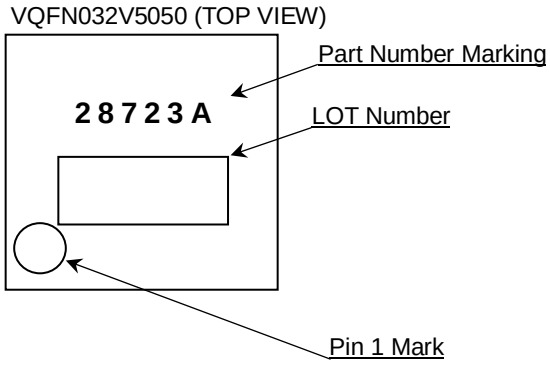


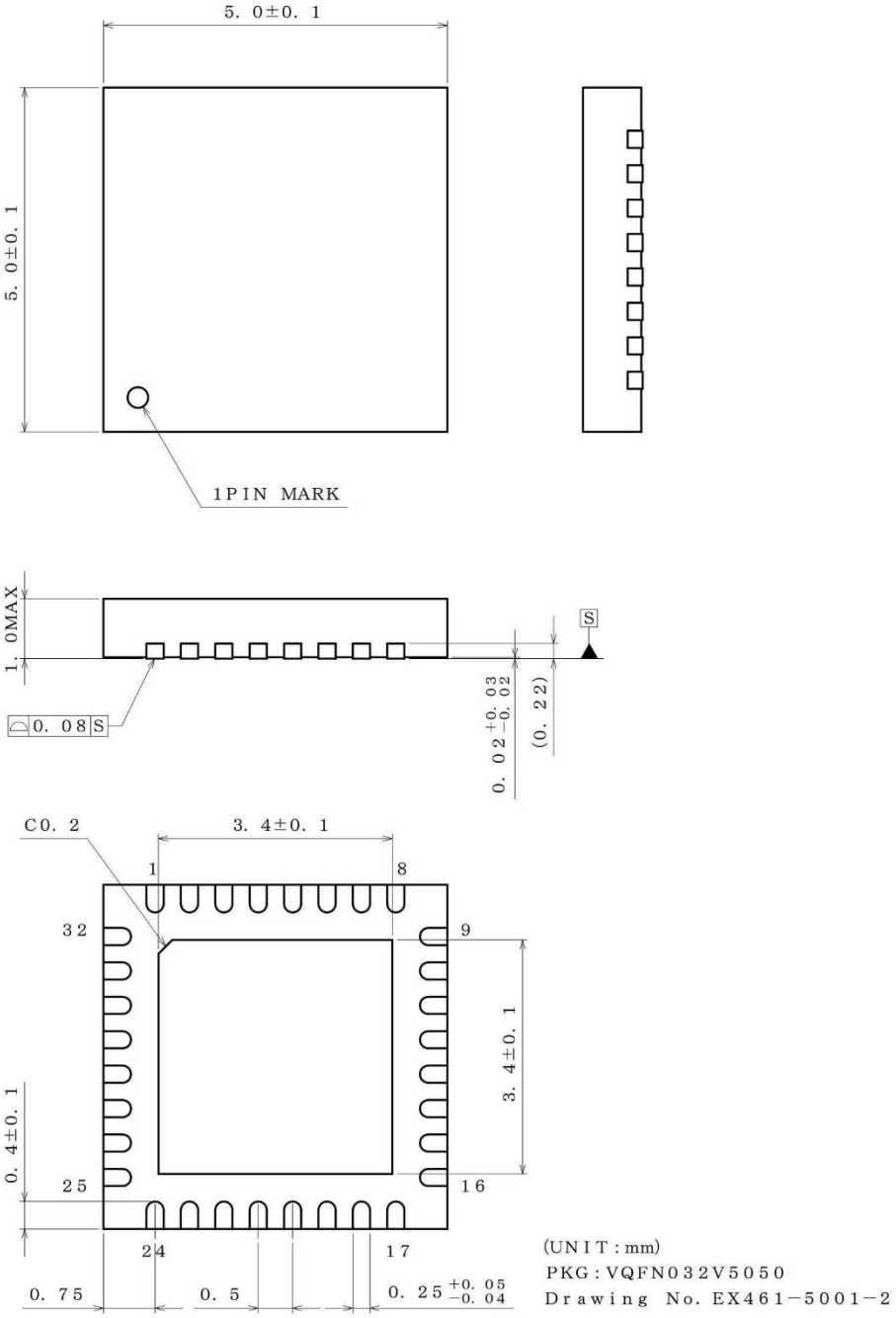
Figure 79

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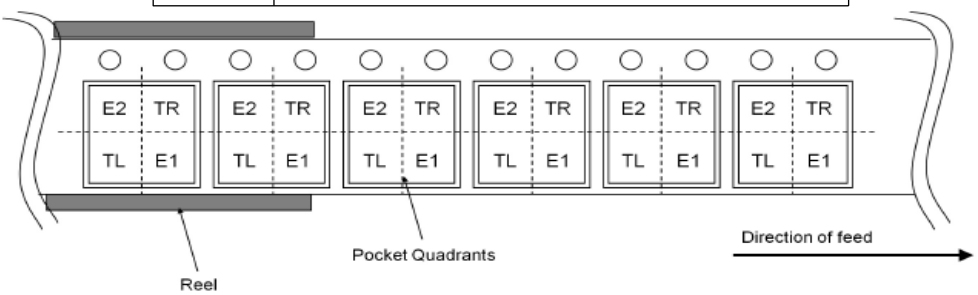
Physical Dimension and Packing Information

Package Name	VQFN032V5050



<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



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Revision History

Date	Revision	Changes
31.Aug.2018	001	New release

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JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

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   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

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2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

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   - [b] the temperature or humidity exceeds those recommended by ROHM
   - [c] the Products are exposed to direct sunshine or condensation
   - [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

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4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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