Fixed/Adjustable Current-Limiting Power-Distribution Switches

NCP380, NCV380

The NCP380 is a high side power-distribution switch designed for applications where heavy capacitive loads and short-circuits are likely to be encountered. The device includes an integrated 55 mΩ (DFN package), P-channel MOSFET. The device limits the output current to a desired level by switching into a constant-current regulation mode when the output load exceeds the current-limit threshold or a short is present. The current-limit threshold is either user adjustable between 500 mA and 2.1 A via an external resistor or internally fixed. The power-switch rise and fall times are controlled to minimize current ringing during switching.

An internal reverse-voltage detection comparator disables the power-switch if the output voltage is higher than the input voltage to protect devices on the input side of the switch.

The $\overline{\text{FLAG}}$ logic output asserts low during over current, reverse-voltage or over temperature conditions. The switch is controlled by a logic enable input active high or low.

Features

- 2.5 V – 5.5 V Operating Range
- 70 mΩ High-side MOSFET
- Current Limit:
  - User adjustable from 500 mA to 2.1 A
  - Fixed 500 mA, 1 A, 1.5 A, 2 A and 2.1 A
- Under Voltage Lock-out (UVLO)
- Built-in Soft-start
- Thermal Protection
- Soft Turn-off
- Reverse Voltage Protection
- Junction Temperature Range: −40°C to 125°C
- Enable Active High or Low (EN or $\overline{\text{EN}}$)
- Compliance to IEC61000−4−2 (Level 4)
  - 8.0 kV (Contact)
  - 15 kV (Air)
- UL Listed − File No. E343275 (NCP Versions Only)
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- These are Pb-Free Devices

Typical Applications

- Laptops
- USB Ports/Hubs
- TVs



UDFN6
CASE 517AB

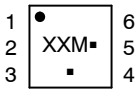


TSOP−5
CASE 483

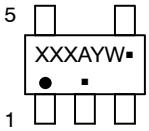


TSOP−6
CASE 318G

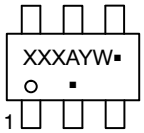
MARKING DIAGRAMS



UDFN6



TSOP−5



TSOP−6

XXX = Specific Device Code
A =Assembly Location
M = Date Code
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 20 of this data sheet.

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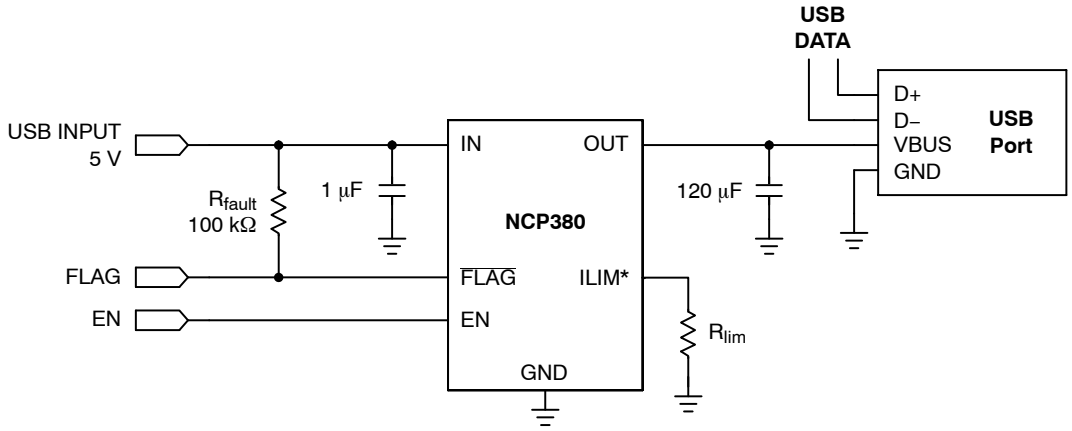
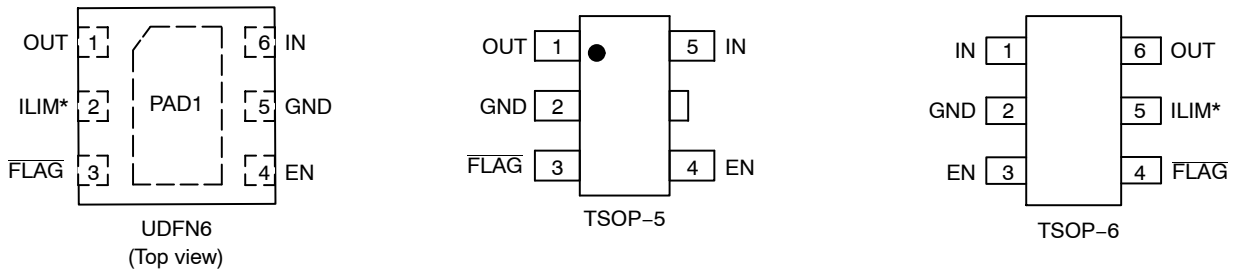


*For Adjustable Version Only.

Figure 1. Typical Application Circuit



*For adjustable version only, otherwise not connected.

Figure 2. Pin Connections

Table 1. PIN FUNCTION DESCRIPTION

Pin Name	Type	Description
EN	INPUT	Enable input, logic low/high (i.e. $\overline{EN}$ or EN) turns on power switch
GND	POWER	Ground connection;
IN	POWER	Power-switch input voltage; connect a 1 μF or greater ceramic capacitor from IN to GND as close as possible to the IC.
$\overline{FLAG}$	OUTPUT	Active-low open-drain output, asserted during overcurrent, overtemperature or reverse-voltage conditions. Connect a 10 kΩ or greater resistor pull-up, otherwise leave unconnected.
OUT	OUTPUT	Power-switch output; connect a 1 μF ceramic capacitor from OUT to GND as close as possible to the IC is recommended. A 1 μF or greater ceramic capacitor from OUT to GND must be connected if the USB requirement (i.e.120 μF capacitor minimum) is not met.
ILIM*	INPUT	External resistor used to set current-limit threshold; recommended 5 kΩ < R_{ILIM} < 250 kΩ.
PAD1**	THERMAL	Exposed Thermal Pad: Must be soldered to PCB Ground plane

*(For adjustable version only, otherwise not connected.
**For DFN version only.

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Table 2. MAXIMUM RATINGS

Rating	Symbol	Value	Unit
From IN to OUT Pins: Input/Output (Note 1)	V_{IN} , V_{OUT}	−7.0 to +7.0	V
IN, OUT, EN, ILIM, $\overline{FLAG}$, Pins: Input/Output (Note 1)	V_{EN}, V_{ILIM}, V_{FLAG}, V_{IN}, V_{OUT}	−0.3 to +7.0	V
$\overline{FLAG}$ Sink Current	I_{SINK}	1	mA
I_{LIM} Source Current	I_{LIM}	1	mA
ESD Withstand Voltage (IEC 61000−4−2) (Output Only, when Bypassed with 1.0 μF Capacitor Minimum)	ESD IEC	15 Air, 8 Contact	kV
Human Body Model (HBM) ESD Rating (Note 2)	ESD HBM	2,000	V
Machine Model (MM) ESD Rating (Notes 2 and 3)	ESD MM	200	V
Latch-up Protection (Note 4) Pins IN, OUT, EN, ILIM, $\overline{FLAG}$	LU	100	mA
Maximum Junction Temperature Range (Note 6)	T_J	−40 to +TSD	°C
Storage Temperature Range	T_{STG}	−40 to +150	°C
Moisture Sensitivity (Note 5)	MSL	Level 1	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. According to JEDEC standard JESD22−A108.
2. This device series contains ESD protection and passes the following tests:
   Human Body Model (HBM) ±2.0 kV per JEDEC standard: JESD22−A114 for all pins.
   Machine Model (MM) ±200 V per JEDEC standard: JESD22−A115 for all pins.
3. Except EN pin, 150 V.
4. Latch up Current Maximum Rating: ±100 mA per JEDEC standard: JESD78 class II.
5. Moisture Sensitivity Level (MSL): 1 per IPC/JEDEC standard: J−STD−020.
6. A thermal shutdown protection avoids irreversible damage on the device due to power dissipation.

Table 3. OPERATING CONDITIONS

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IN}	Operational Power Supply			2.5	–	5.5	V
V_{EN}	Enable Voltage			0	–	5.5	
T_A	Ambient Temperature Range			−40	25	+85	°C
T_J	Junction Temperature Range			−40	25	+125	°C
R_{ILIM}	Resistor from ILIM to GND Pin			5.0	–	250	kΩ
I_{SINK}	$\overline{FLAG}$ Sink Current			–	–	1.0	mA
C_{IN}	Decoupling Input Capacitor			1.0	–	–	μF
C_{OUT}	Decoupling Output Capacitor	USB Port per Hub		120	–	–	μF
$R_{\theta JA}$	Thermal Resistance Junction-to-Air	UDFN−6 Package (Notes 7 and 8)		–	120	–	°C/W
		TSOP−5 Package (Notes 7 and 8)		–	305	–	°C/W
		TSOP−6 Package (Notes 7 and 8)		–	280	–	°C/W
I_{OUT}	Maximum DC Current	UDFN−6 Package		–	–	2.1	A
		TSOP−5, TSOP−6 Package		–	–	1.0	A
P_D	Power Dissipation Rating (Note 9)	$T_A \le 25°C$	UDFN−6 Package	–	830	–	mW
			TSOP−5 Package	–	325	–	mW
			TSOP−6 Package	–	350	–	mW
		$T_A = 85°C$	UDFN−6 Package	–	325	–	mW
			TSOP−5 Package	–	130	–	mW
			TSOP−6 Package	–	145	–	mW

7. A thermal shutdown protection avoids irreversible damage on the device due to power dissipation.
8. The $R_{\theta JA}$ is dependent of the PCB heat dissipation. Board used to drive this data was a 2” × 2” NCP380EVB board. It is a 2 layers board with 2-once copper traces on top and bottom of the board. Exposed pad is connected to ground plane for UDFN−6 version only.
9. The maximum power dissipation (P_D) is given by the following formula:

$$P_D = \frac{T_{JMAX} - T_A}{R_{\theta JA}}$$

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Table 4. ELECTRICAL CHARACTERISTICS

(Min & Max Limits apply for T_A between −40°C to +85°C and T_J up to +125°C for V_{IN} between 2.5 V to 5.5 V (Unless otherwise noted). Typical values are referenced to T_A = +25°C and V_{IN} = 5 V.)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
POWER SWITCH							
$R_{DS(on)}$	Static Drain-source On-state Resistance DFN Package	V_{IN} = 5 V	−40°C < T_J < 125°C	–	55	75	mΩ
		2.5 V < V_{IN} < 5.5 V	−40°C < T_J < 125°C	–	–	110	
	TSOP Package	V_{IN} = 5 V	−40°C < T_J < 125°C	–	70	95	mΩ
		2.5 V < V_{IN} < 5.5 V	−40°C < T_J < 125°C	–	–	135	
T_R	Output Rise Time	V_{IN} = 5 V	C_{LOAD} = 1 μF, R_{LOAD} = 100 Ω (Note 10)	0.3	1.0	1.5	ms
		V_{IN} = 2.5 V		0.2	0.65	1.0	
T_F	Output Fall Time	V_{IN} = 5 V		0.1	–	0.5	
		V_{IN} = 2.5 V		0.1	–	0.5	
ENABLE INPUT EN OR $\overline{EN}$							
V_{IH}	High-level Input Voltage			1.2	–	–	V
V_{IL}	Low-level Input Voltage			–	–	0.4	V
I_{EN}	Input Current	V_{EN} = 0 V, $V_{\overline{EN}}$ = 5 V		−0.5	–	0.5	μA
T_{ON}	Turn On Time	C_{LOAD} = 1 μF, R_{LOAD} = 100 Ω (Note 11)		2.0	3.0	4.0	ms
T_{OFF}	Turn Off Time			1.0	–	3.0	ms
CURRENT LIMIT							
I_{OCP}	Current-limit Threshold (Maximum DC Output Current I_{OUT} Delivered to Load)	V_{IN} = 5 V	R_{ILIM} = 20 kΩ (Note 11)	1.02	1.20	1.38	A
			R_{ILIM} = 40 kΩ (Notes 11 and 13)	0.595	0.700	0.805	
			Fixed 0.5 A (Note 12)	0.5	0.58	0.65	A
			Fixed 1.0 A (Note 12)	1.0	1.15	1.3	
			Fixed 1.5 A (Note 12)	1.5	1.75	1.9	
			Fixed 2.0 A (Note 12)	2.0	2.25	2.5	
			Fixed 2.1 A (Note 12)	2.1	2.25	2.5	
T_{DET}	Response Time to Short Circuit	V_{IN} = 5 V		–	2.0	–	μs
T_{REG}	Regulation Time			1.8	3.0	4.0	ms
T_{OCP}	Overcurrent Protection Time			14	20	26	ms
REVERSE-VOLTAGE PROTECTION							
V_{REV}	Reverse-voltage Comparator Trip Point ($V_{OUT} - V_{IN}$)			–	100	–	mV
T_{REV}	Time from Reverse-voltage Condition to MOSFET Switch Off & $\overline{FLAG}$ Low	V_{IN} = 5 V		4.0	6.0	9.0	ms
T_{RREV}	Re-arming Time			7.0	10	15	ms
UNDERVOLTAGE LOCKOUT							
V_{UVLO}	IN Pin Low-level Input Voltage	V_{IN} Rising		2.0	2.3	2.4	V
V_{HYST}	IN Pin Hysteresis	T_J = 25°C		25	–	60	mV
T_{RUVLO}	Re-arming Time			7.0	10	15	ms
SUPPLY CURRENT							
I_{INOFF}	Low-level Output Supply Current	V_{IN} = 5 V, No Load on OUT, Device OFF V_{EN} = 0 V or $V_{\overline{EN}}$ = 5 V		–	1.0	2.1	μA
I_{INON}	High-level Output Supply Current	V_{IN} = 5 V, Device Enable 2 A and 2.1 A Versions 1 A and 1.5 A Current Versions 0.5 A Current Version		 – – –	 – – –	 90 80 70	μA
I_{REV}	Reverse Leakage Current	V_{OUT} = 5 V, V_{IN} = 0 V	T_J = 25°C	–	–	1.0	μA

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Table 4. ELECTRICAL CHARACTERISTICS (continued)
(Min & Max Limits apply for T_A between −40°C to +85°C and T_J up to +125°C for V_{IN} between 2.5 V to 5.5 V (Unless otherwise noted). Typical values are referenced to T_A = +25°C and V_{IN} = 5 V.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$\overline{\text{FLAG}}$ PIN						
V_{OL}	$\overline{\text{FLAG}}$ Output Low Voltage	$I_{\overline{\text{FLAG}}}$ = 1 mA			400	mV
I_{LEAK}	Off-state Leakage	$V_{\overline{\text{FLAG}}}$ = 5 V			1.0	μA
T_{FLG}	$\overline{\text{FLAG}}$ Deglitch	$\overline{\text{FLAG}}$ De-assertion Time due to Overcurrent or Reverse Voltage Condition	4.0	6.0	9.0	ms
T_{FOCP}	$\overline{\text{FLAG}}$ Deglitch	$\overline{\text{FLAG}}$ Assertion due to Overcurrent	6.0	8.0	12	ms
THERMAL SHUTDOWN						
T_{SD}	Thermal Shutdown Threshold			140		°C
T_{SDOCP}	Thermal Regulation Threshold			125		°C
T_{RSD}	Thermal Shutdown Rearming Threshold			115		°C

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
10. Parameters are guaranteed for C_{LOAD} and R_{LOAD} connected to the OUT pin with respect to the ground, See Figure 3.
11. Adjustable current version, R_{ILIM} tolerance ±1%.
12. Fixed current version.
13. Not production test, guaranteed by characterization.

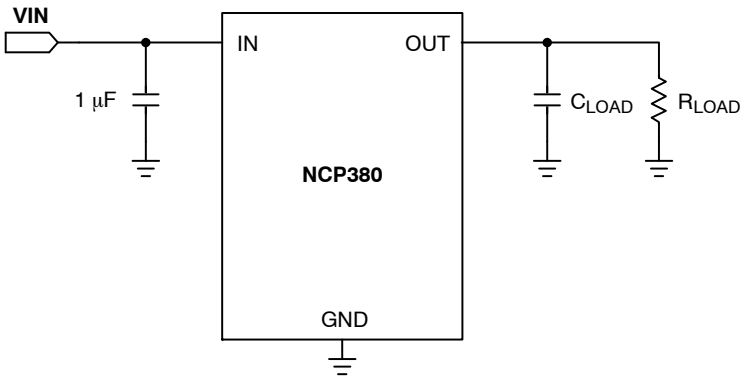

Figure 3. Test Configuration

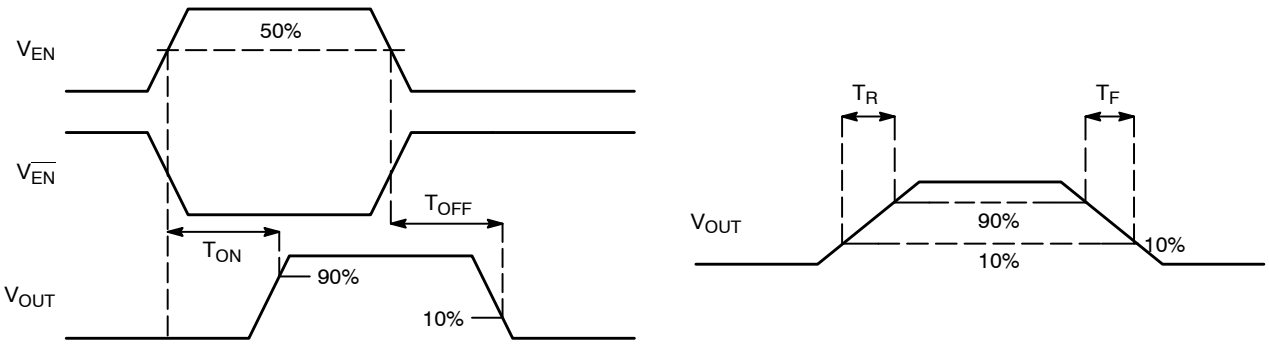

Figure 4. Voltage Waveform

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BLOCK DIAGRAM

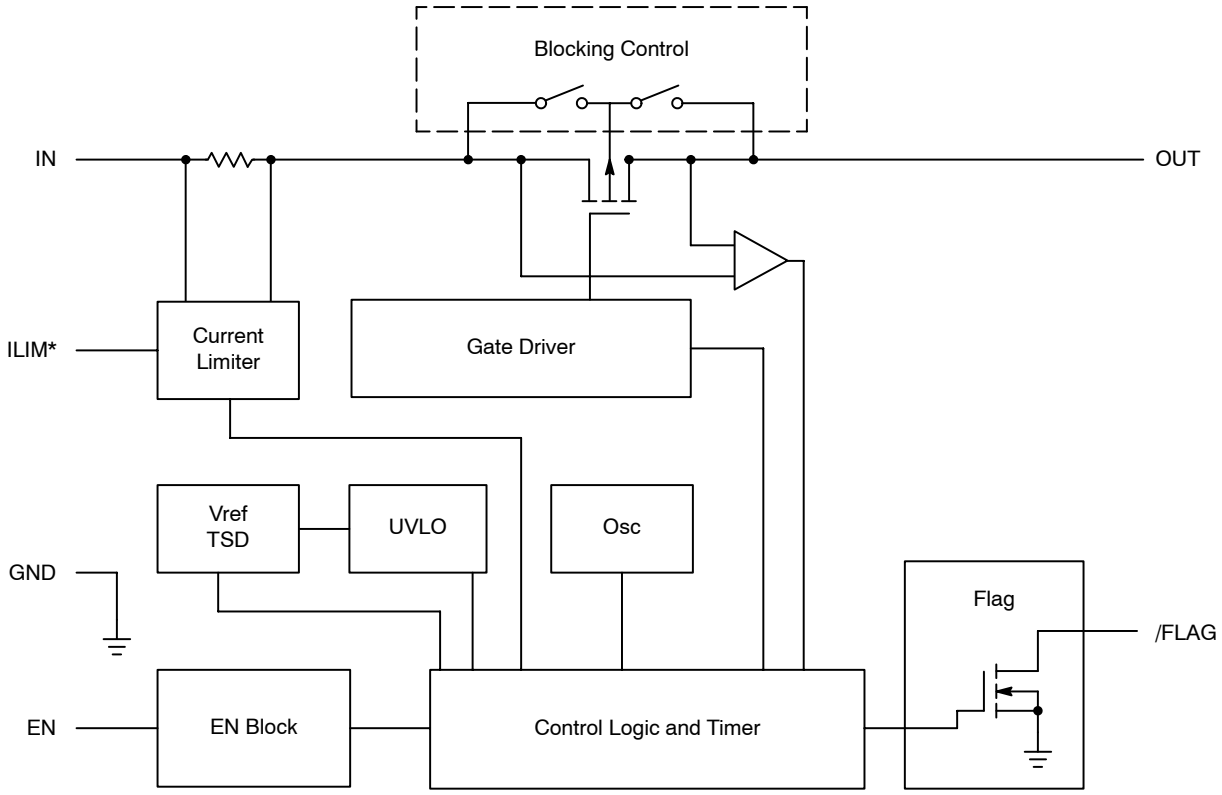

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Figure 5. Block Diagram

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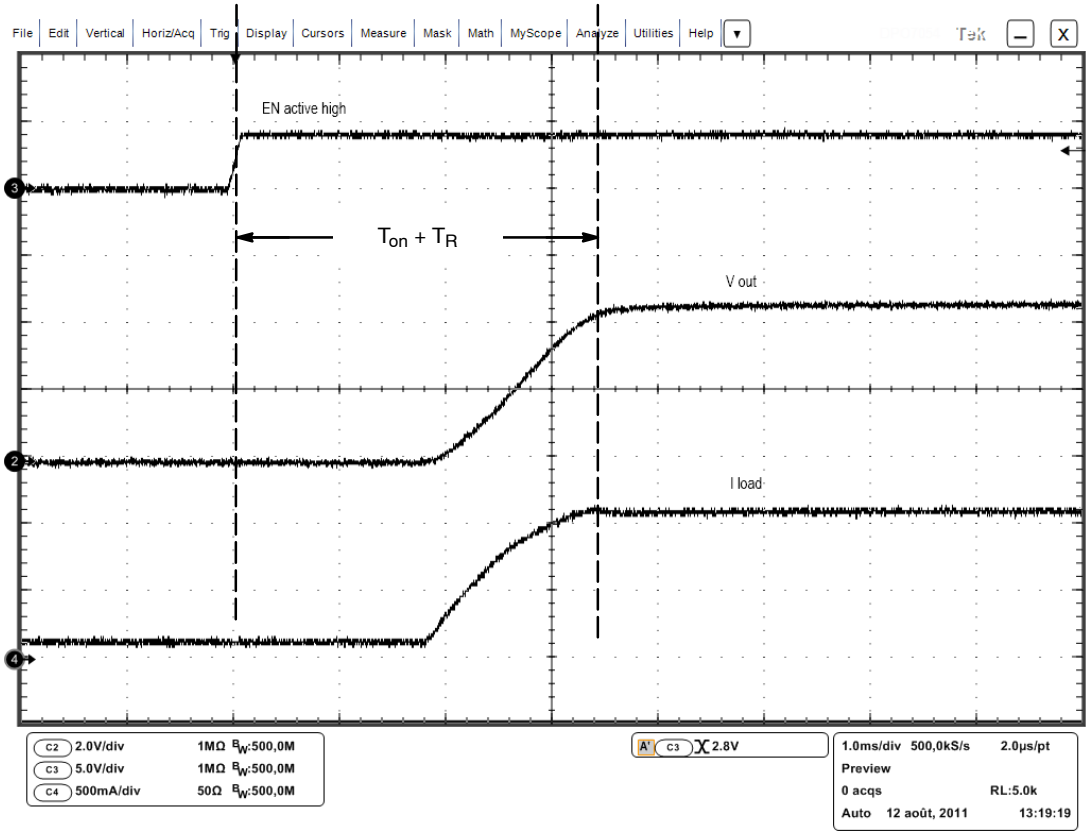

Figure 6. T_{on} Delay and T_{rise} Time

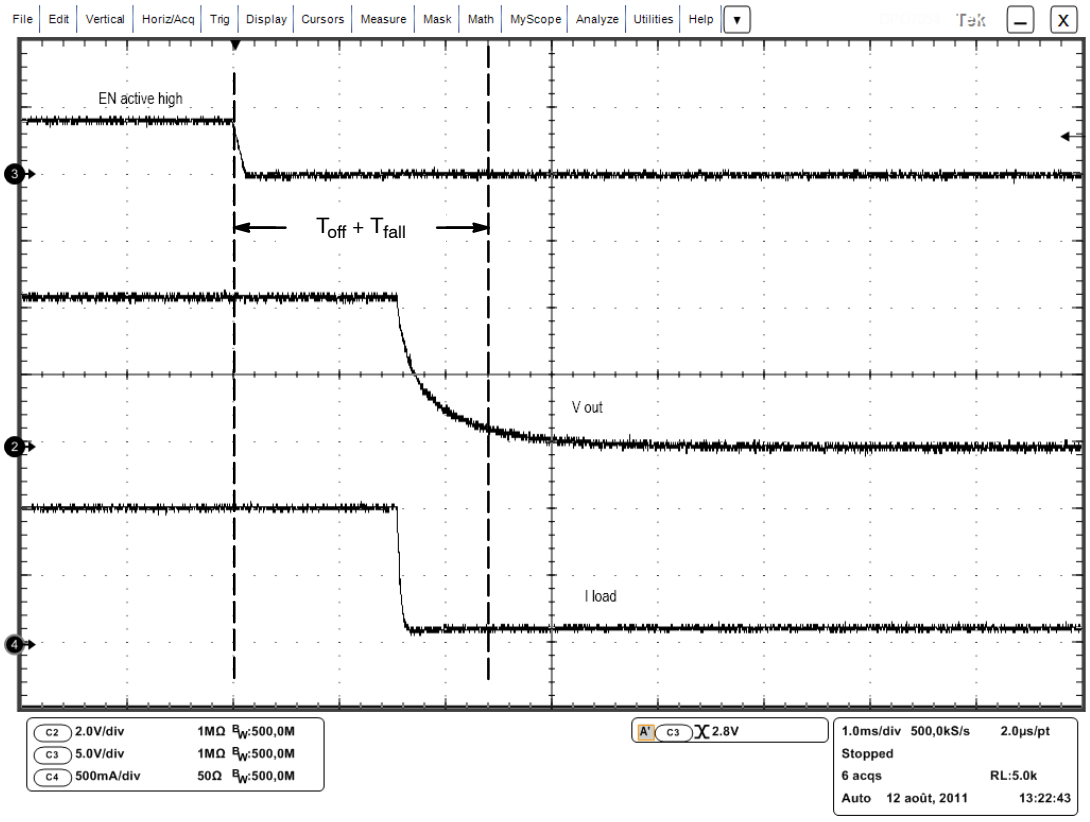

Figure 7. T_{off} Delay and T_{fall}

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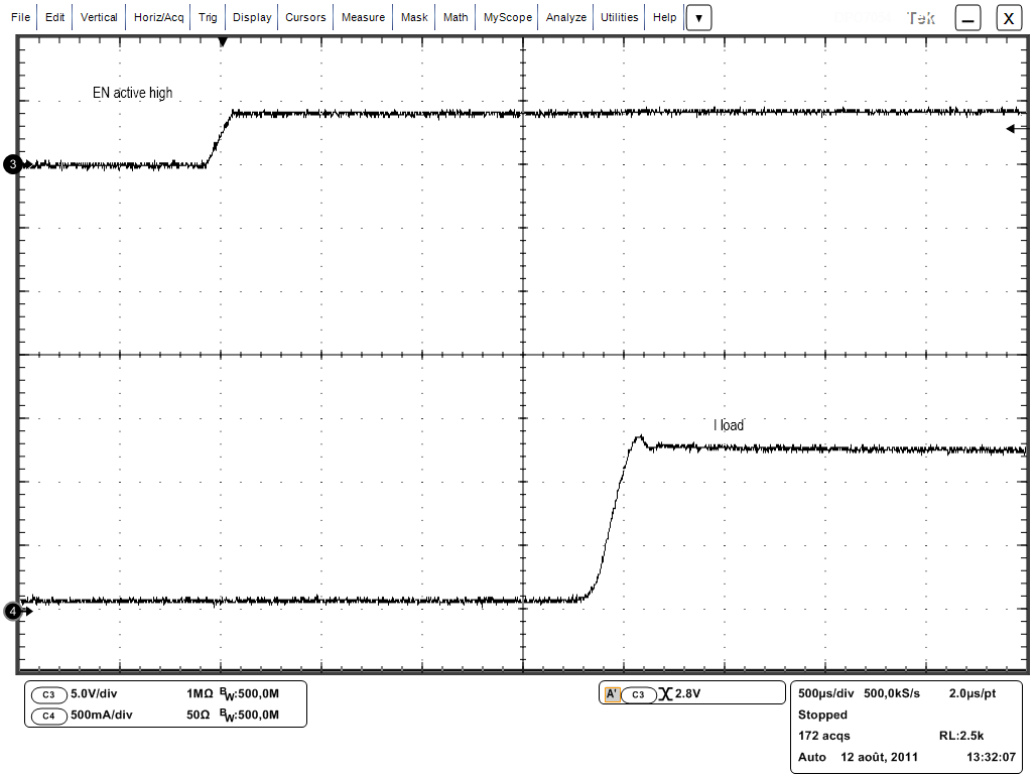

Figure 8. Turn On a Short

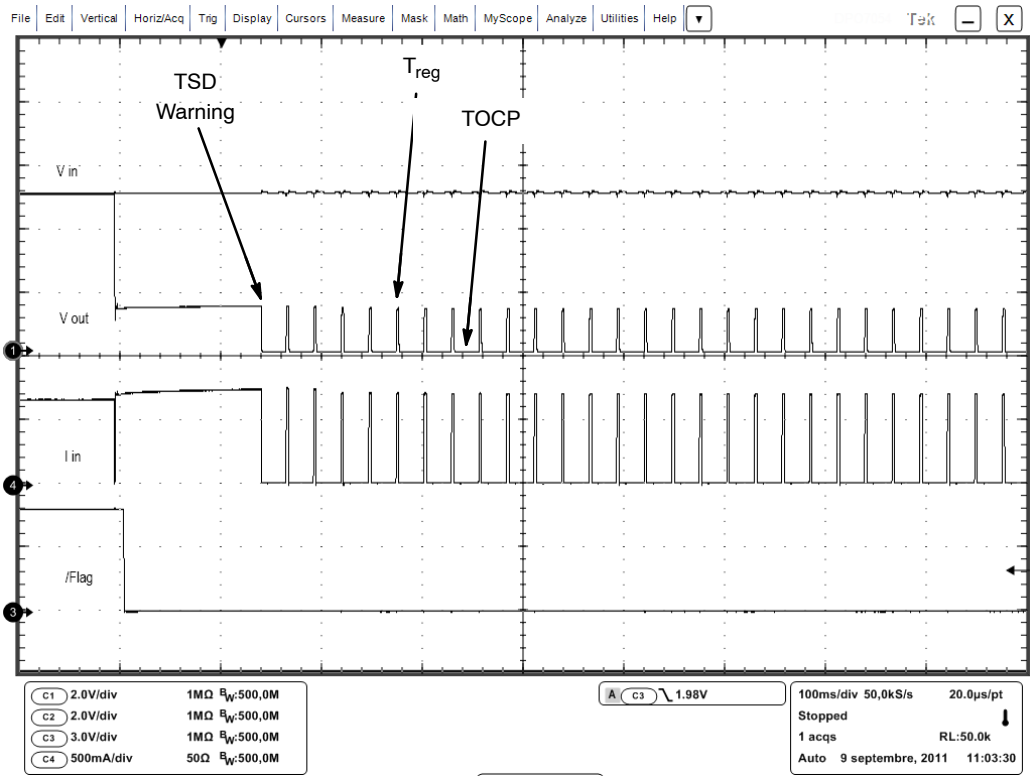

Figure 9. 2 Ω Short on Output. Complete Regulation Sequence

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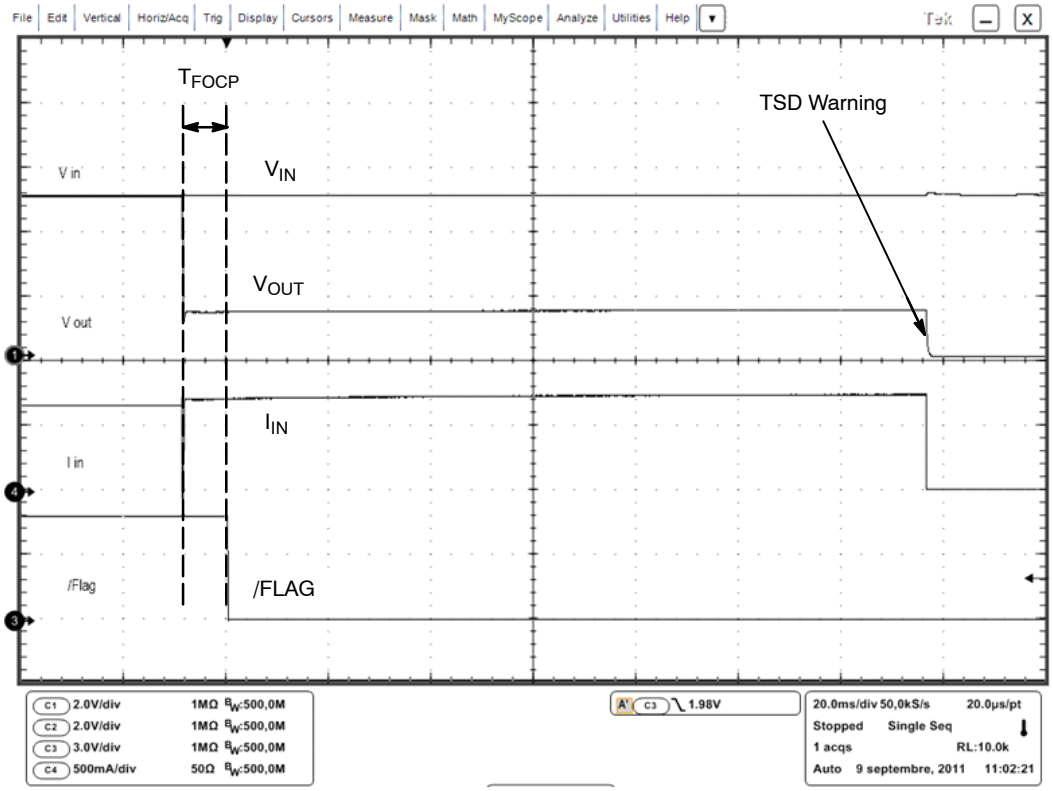

Figure 10. OCP Regulation and TSD Warning Event

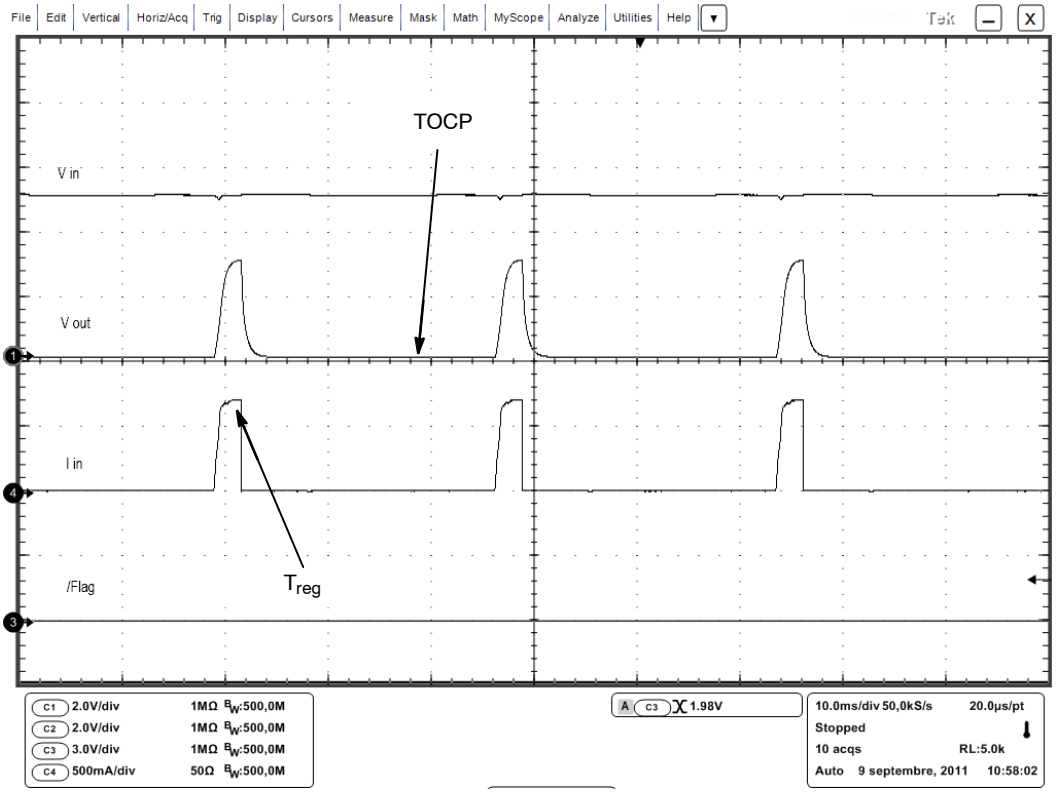

Figure 11. Timer Regulation Sequence During 2 Ω Overload

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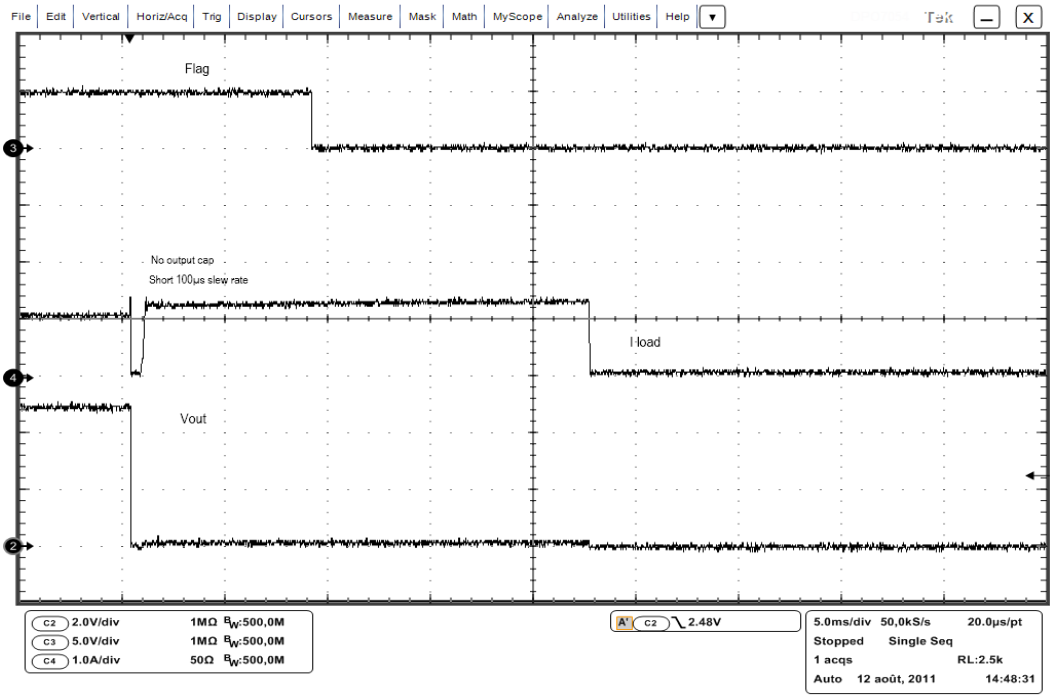

Figure 12. Direct Short on OUT Pin

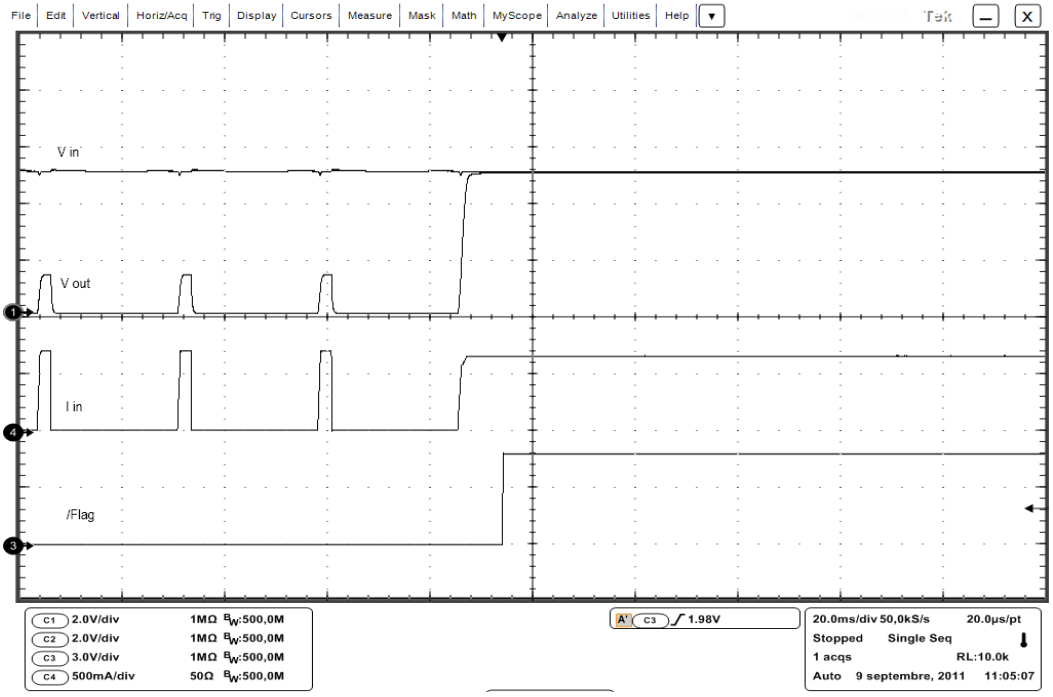

Figure 13. From Timer Regulation to Load Removal Sequence

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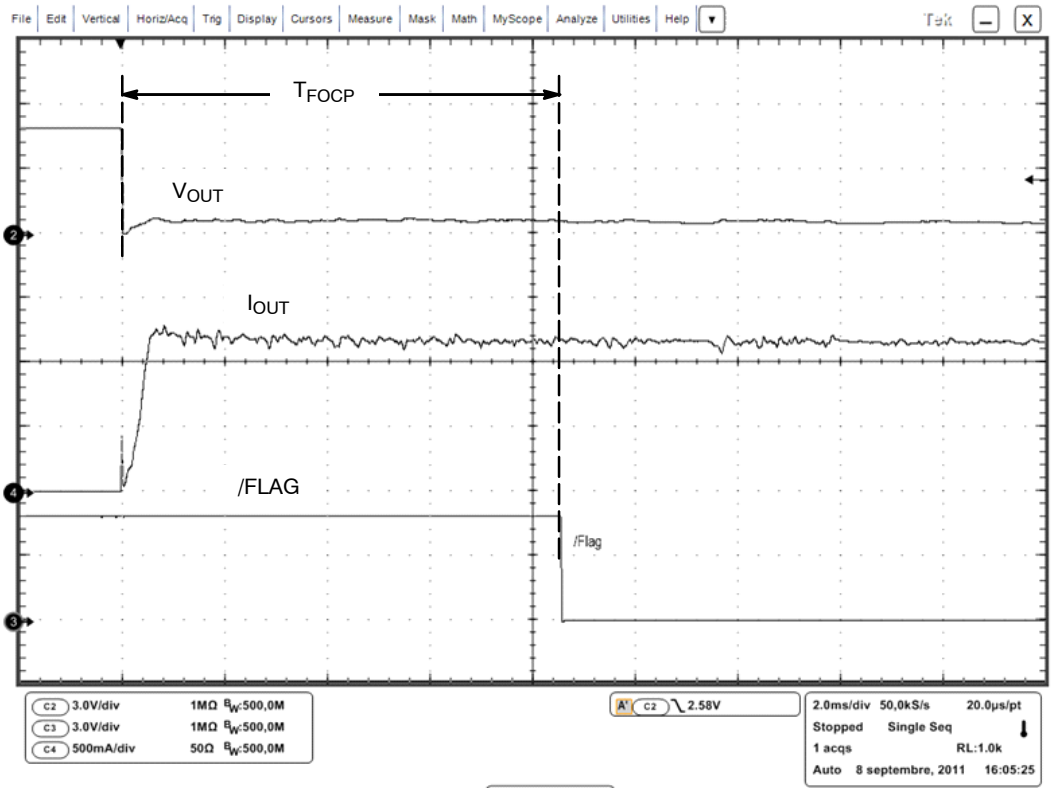

Figure 14. From No Load to Direct Short Circuit

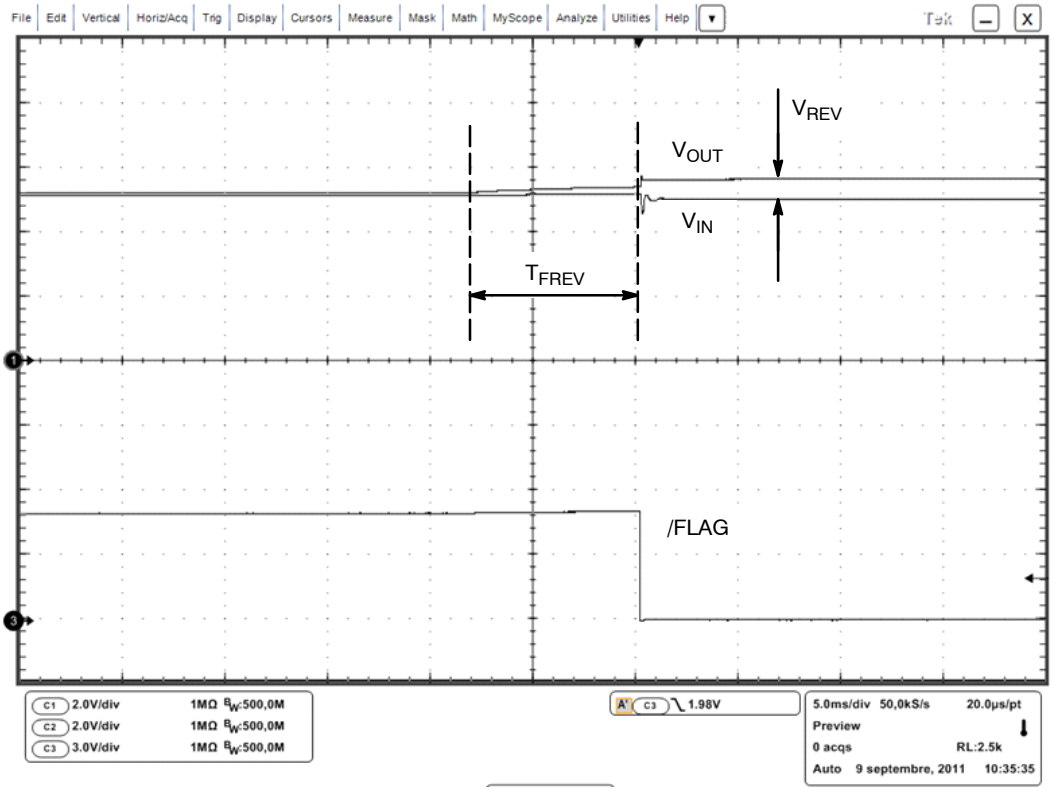

Figure 15. Reverse Voltage Detection

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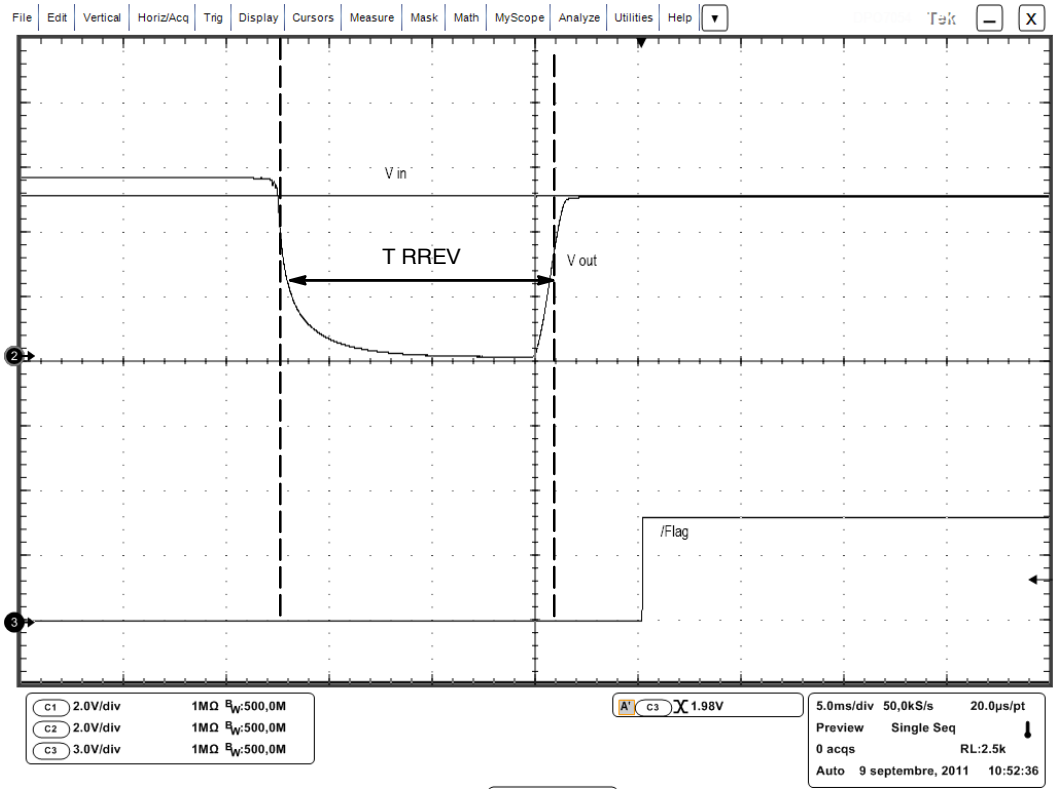

Figure 16. Reverse Voltage Removal

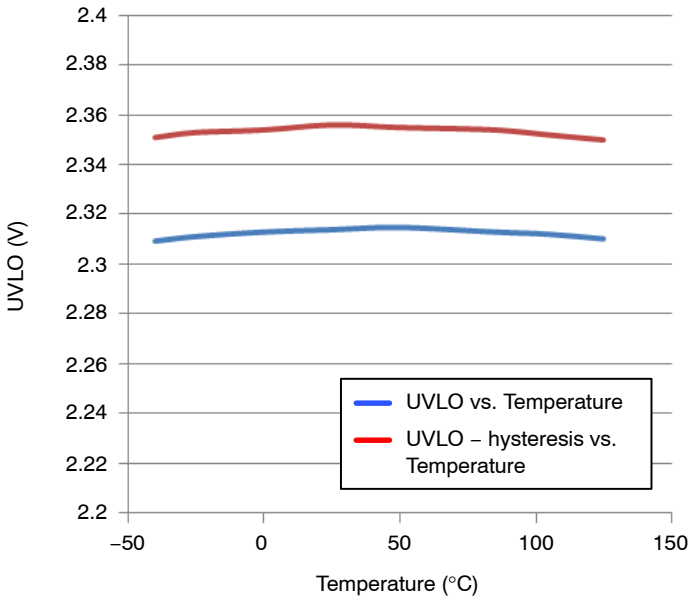

Figure 17. Undervoltage Threshold (Falling) and Hysteresis

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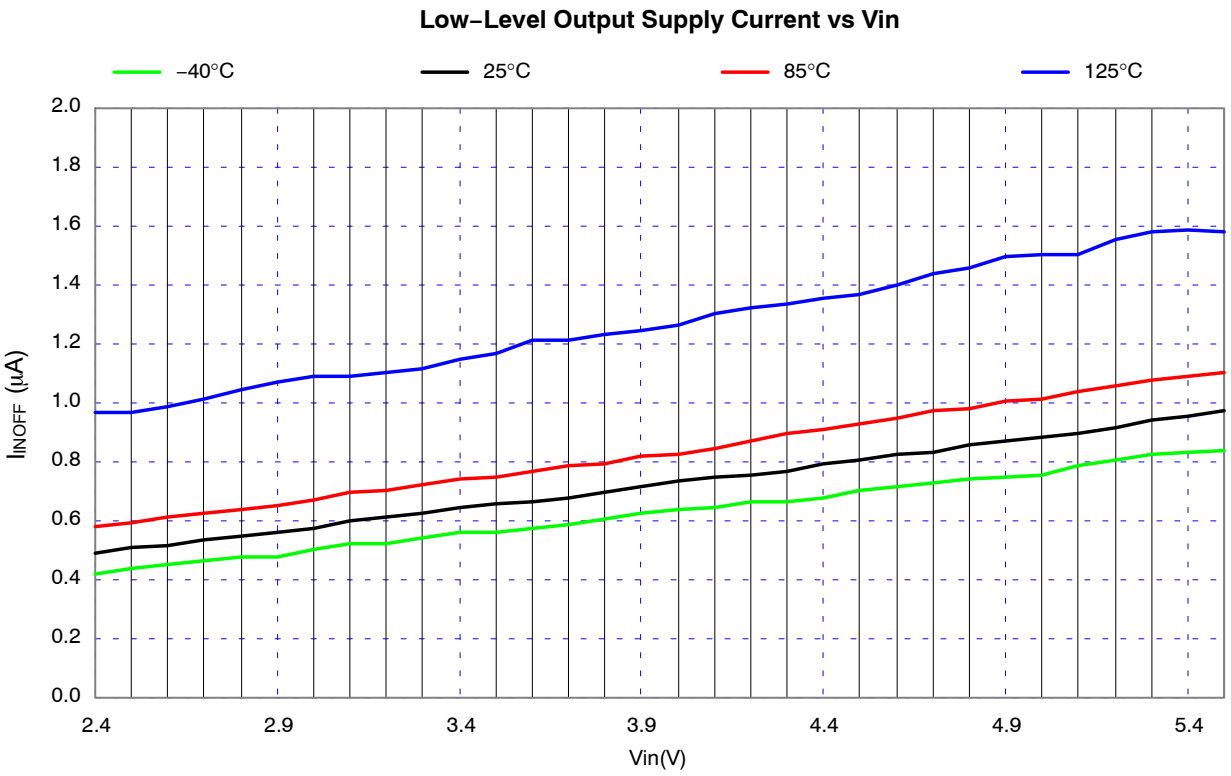

Figure 18. Standby Current vs Vin

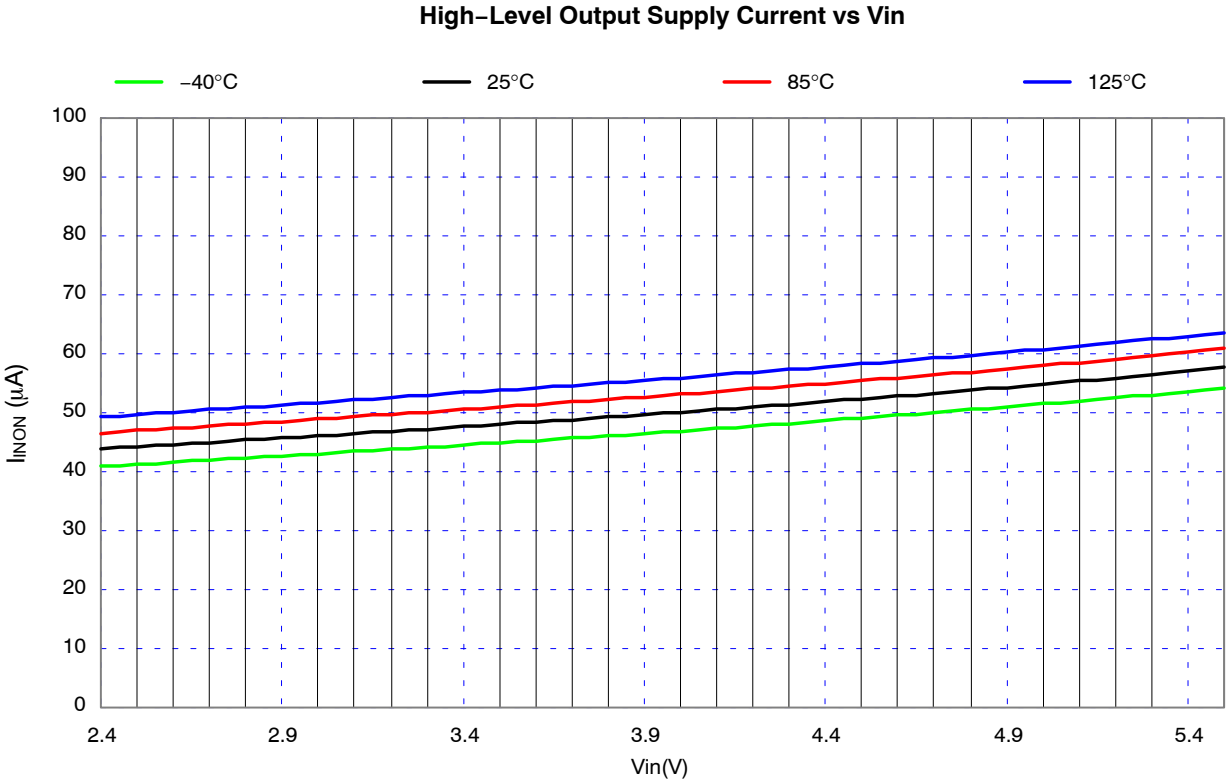

Figure 19. Quiescent Current vs Vin

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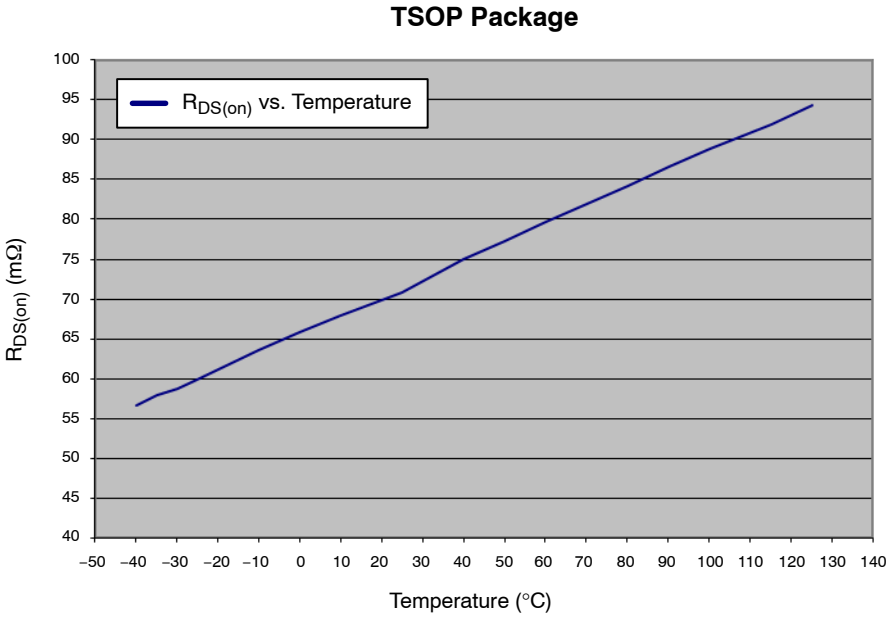

Figure 20. $R_{DS(on)}$ vs Temperature, TSOP Package

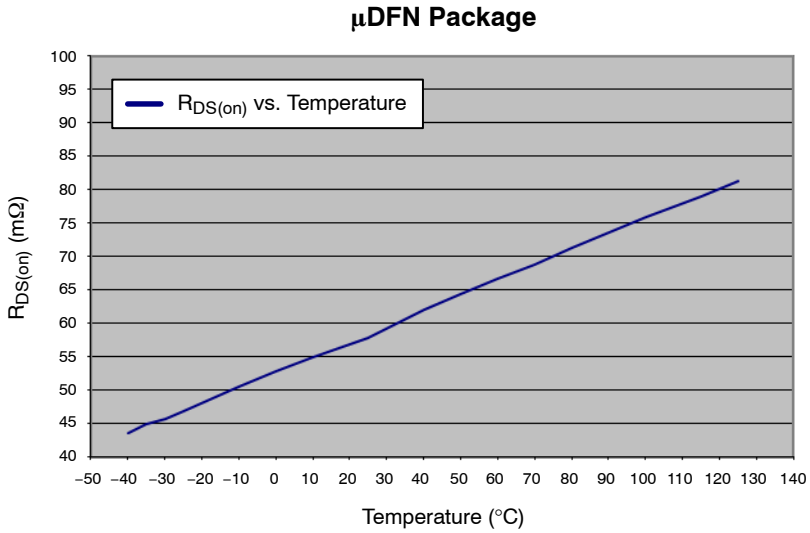

Figure 21. $R_{DS(on)}$ vs Temperature, µDFN Package

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FUNCTIONAL DESCRIPTION

Overview

The NCP380 is a high side P channel MOSFET power distribution switch designed to protect the input supply voltage in case of heavy capacitive loads, short circuit or over current. In addition, the high side MOSFET is turned off during under voltage, thermal shutdown or reverse voltage condition. Adjustable version allows the user to program the current limit threshold using an external resistor. Thanks to the soft start circuitry, NCP380 is able to limit large current and voltage surges.

Overcurrent Protection

NCP380 switches into a constant current regulation mode when the output current is above the I_{OCP} threshold. Depending on the load, the output voltage is decreased accordingly.

- In case of hot plug with heavy capacitive load, the output voltage is brought down to the capacitor voltage. The NCP380 will limit the current to the I_{OCP} threshold value until the charge of the capacitor is completed.

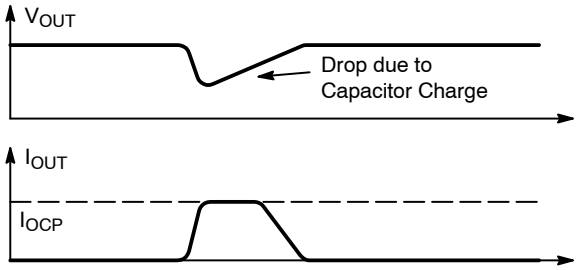

Figure 22. Heavy capacitive load

- In case of overload, the current is limited to the I_{OCP} value and the voltage value is reduced according to the load by the following relation:

$$V_{OUT} = R_{LOAD} \times I_{OCP} \quad \text{(eq. 1)}$$

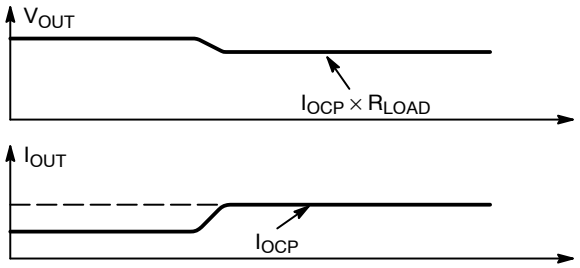

Figure 23. Overload

- In case of short circuit or huge load, the current is limited to the I_{OCP} value within T_{DET} time until the short condition is removed. If the output remains shorted or tied to a very low voltage, the junction temperature of the chip exceeds T_{SDOCP} value and the device enters in thermal shutdown (MOSFET is turned-off).

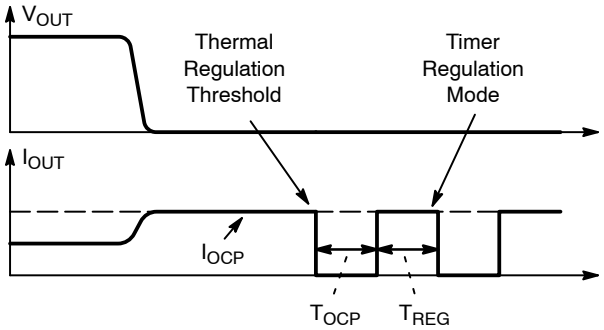

Figure 24. Short circuit

Then, the device enters in timer regulation mode, described in 2 phases:

- Off-phase: Power MOSFET is off during T_{OCP} to allow the die temperature to drop.
- On-phase: regulation current mode during T_{REG}. The current is regulated to the I_{OCP} level.

The timer regulation mode allows the device to handle high thermal dissipation (in case of short circuit for example) within temperature operating condition.

NCP380 stays in on-phase/off-phase loop until the over current condition is removed or enable pin is toggled.

Remark: Other regulation modes can be available for different applications. Please contact our **onsemi** representative for availability.

$\overline{\text{FLAG}}$ Indicator

The $\overline{\text{FLAG}}$ pin is an open-drain MOSFET asserted low during over current, reverse-voltage or over temperature conditions. When an over current or a reverse voltage fault is detected on the power path, $\overline{\text{FLAG}}$ pin is asserted low at the end of the associate deglitch time (see electrical characteristics). Thanks to this feature, the $\overline{\text{FLAG}}$ pin is not tied low during the charge of a heavy capacitive load or a voltage transient on output. Deglitch time is T_{FOCP} for over current fault and T_{REV} for reverse voltage. The $\overline{\text{FLAG}}$ pin remains low until the fault is removed. Then, the $\overline{\text{FLAG}}$ pin goes high at the end of T_{FGL}.

Undervoltage Lock-out

Thanks to a built-in under voltage lockout (UVLO) circuitry, the output remains disconnected from input until V_{IN} voltage is below V_{UVLO}. When V_{IN} voltage is above V_{UVLO}, the system try to reconnect the output after a rearming time. T_{RUVLO}. This circuit has a V_{HYST} hysteresis witch provides noise immunity to transient.

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Thermal Sense

Thermal shutdown turns off the power MOSFET if the die temperature exceeds T_{SD}. A Hysteresis prevents the part from turning on until the die temperature cools at T_{RSD}.

Reverse Voltage Protection

When the output voltage exceeds the input voltage by V_{REV} voltage during T_{REV}, the reverse voltage circuitry disconnects the output in order to protect the power supply. The same time T_{REV} is needed to turn on again the power MOS plus a rearming time T_{RREV}.

Enable Input

Enable pin must be driven by a logic signal (CMOS or TTL compatible) or connected to the GND. V_{IN} and EN should not be connected together directly. V_{IN} should be well established and stablized prior to enabling the IC. If no separate EN signal is available, a 10 kΩ/100 nF RC network can be added between V_{IN} and EN to delay the EN signal. A logic low on $\overline{EN}$ or high on EN turns-on the device. A logic high on $\overline{EN}$ or low on EN turns off device and reduces the current consumption down to I_{INOFF}.

Blocking Control

The blocking control circuitry switches the bulk of the power MOS. When the part is off, the body diode limits the leakage current I_{REV} from OUT to IN. In this mode, anode of the body diode is connected to IN pin and cathode is connected to OUT pin. In operating condition, anode of the body diode is connected to OUT pin and cathode is connected to IN pin preventing the discharge of the power supply.

APPLICATION INFORMATION

Power Dissipation

The junction temperature of the device depends on different contributing factors such as board layout, ambient temperature, device environment, etc... Yet, the main contributor in terms of junction temperature is the power dissipation of the power MOSFET. Assuming this, the power dissipation and the junction temperature in normal mode can be calculated with the following equations:

$$R_D = R_{DS(on)} \times \left(I_{OUT}\right)^2 \quad \text{(eq. 2)}$$

Where:

P_D = Power dissipation (W)
$R_{DS(on)}$ = Power MOSFET on resistance (Ω)
I_{OUT} = Output current (A)

$$T_J = P_D \times R_{\theta JA} + T_A \quad \text{(eq. 3)}$$

Where:

T_J = Junction temperature (°C)
$R_{\theta JA}$ = Package thermal resistance (°C/W)
T_A = Ambient temperature (°C)

Power dissipation in regulation mode can be calculated by taking into account the drop $V_{IN}-V_{OUT}$ link to the load by the following relation:

$$P_D = \left(V_{IN} - R_{LOAD} \times I_{OCP}\right) \times I_{OCP} \quad \text{(eq. 4)}$$

Where:

P_D = Power dissipation (W)
V_{IN} = Input Voltage (V)
R_{LOAD} = Load Resistance (Ω)
I_{OCP} = Output regulated current (A)

Adjustable Current-Limit Programming (for adjustable version only)

The NCP380xMUAJAA and NCP380xSNAJAA, respectively µDFN and TSOP6 packages, are proposed to have current limit flexibility for end Customer. Indeed, Ilim pin is available to connect pull down resistor to ground, which participate to the current threshold adjustment. It's strongly recommended to use 0.1 or 1% resistor tolerance to keep the over current accuracy.

For this resistance selection, Customer should define first of all, the USB current to sustain, without the device enters in the protection sequence. Main rule is to select this pull down resistor in order to make sure min current limit is above the USB current to provide continuously to the upstream accessory.

Following, the main table selection contains the USB current port for the accessory, the standard resistor selection and typical/max over current threshold.

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Table 5. RESISTOR SELECTION FOR ADJUSTABLE CURRENT LIMIT VERSION

Min Current Limit Value (A)	Theoric Resistor Value (kΩ)	Selected Resistor Value (kΩ) 1% or 0.1%	Typical OCP Target Value (A)	Maximum Current Value (A)
0.5	44.2	44.2	0.59	0.67
0.6	37.5	37.4	0.71	0.81
0.7	32.2	31.6	0.825	0.95
0.8	27.7	27.4	0.94	1.08
0.9	24.0	23.7	1.06	1.22
1.0	21.0	21	1.18	1.35
1.1	18.5	18.2	1.3	1.49
1.2	16.6	16.5	1.41	1.62
1.3	14.6	14.3	1.53	1.76
1.4	13.0	13	1.65	1.9
1.5	11.4	11.3	1.78	2.05
1.6	10.4	10.2	1.88	2.17
1.7	9.2	9.09	2.01	2.31
1.8	8.3	8.25	2.12	2.438
1.9	7.4	7.32	2.23	2.56
2.0	6.5	6.49	2.36	2.7
2.1	5.6	5.49	2.48	2.85

The “Min current limit Value” column, represents the DC current to provide to the accessory without over current activation.

Second column is the theoretical resistor value obtained with following formula to achieve typical current target:

$$Rlim = -5.2959 \times ILIM^5 + 45.256 \times ILIM^4 - 155.25 \times ILIM^3 + 274.39 \times ILIM^2 - 267.6 \times ILIM + 134.21 \quad \text{(eq. 5)}$$

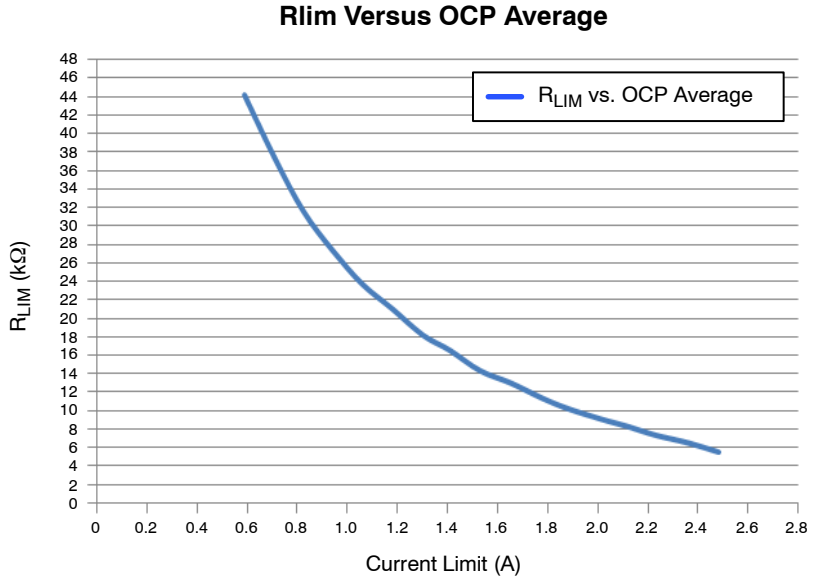

Figure 25. R_{LIM} Curve vs. Current Limit

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When the resistor is choosing to fit with the Customer application, the limits of the over current threshold can be calculated with the following formula:

$$IOCP\,min = 1.6915129 - 0.0330328 \times Rlim + 0.0011207(Rlim - 22.375)^2 - 0.0000451 \times (Rlim - 22.375)^3 + + 0.0000009 \times (Rlim - 22.375)^4 \quad \text{(eq. 6)}$$

$$IOCP\,max = 2.2885175 - 0.0446914 \times Rlim + 0.0015163(Rlim - 22.375)^2 - 0.000061 \times (Rlim - 22.375)^3 + + 0.0000012 \times (Rlim - 22.375)^4 \quad \text{(eq. 7)}$$

$$IOCPtyp = 1.9900152 - 0.0388621 \times Rlim + 0.0013185(Rlim - 22.375)^2 - 0.0000531 \times (Rlim - 22.375)^3 + + 0.0000011 \times (Rlim - 22.375)^4 \quad \text{(eq. 8)}$$

The minimum, typical and maximum current curves are described in the following graph:

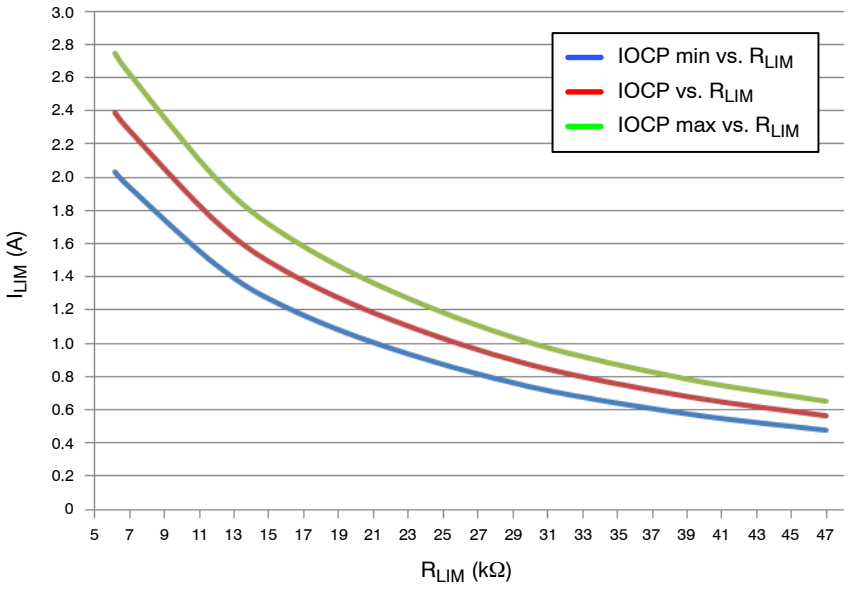

Figure 26. Current Threshold vs. Rlim Resistor

That is recommended to respect 6 kΩ−47 kΩ resistor range for two reasons.

For the low resistor values, the current limit is pushed up to high current level. Due to internal power dissipation capability, a maximum of 2.4 A typical can be set for the μDFN package if thermal consideration are respected. For the TSOP6 version 1.2 A is the maximum recommended value because the part could enter in thermal shutdown mode before constant current regulation mode.

In the other side, if we want to keep 15% of accuracy, high resistor values can be used up to 50 kΩ. With higher value, the current threshold is lower than 500 mA, so in this case degraded accuracy can be observed.

PCB Recommendations

The NCP380 integrates a PMOS FET rated up to 2 A, and the PCB design rules must be respected to properly evacuate the heat out of the silicon. The UDFN6 PAD1 must be connected to ground plane to increase the heat transfer if necessary. This pad must be connected to ground plane. By increasing PCB area, the $R_{\theta JA}$ of the package can be decreased, allowing higher power dissipation.

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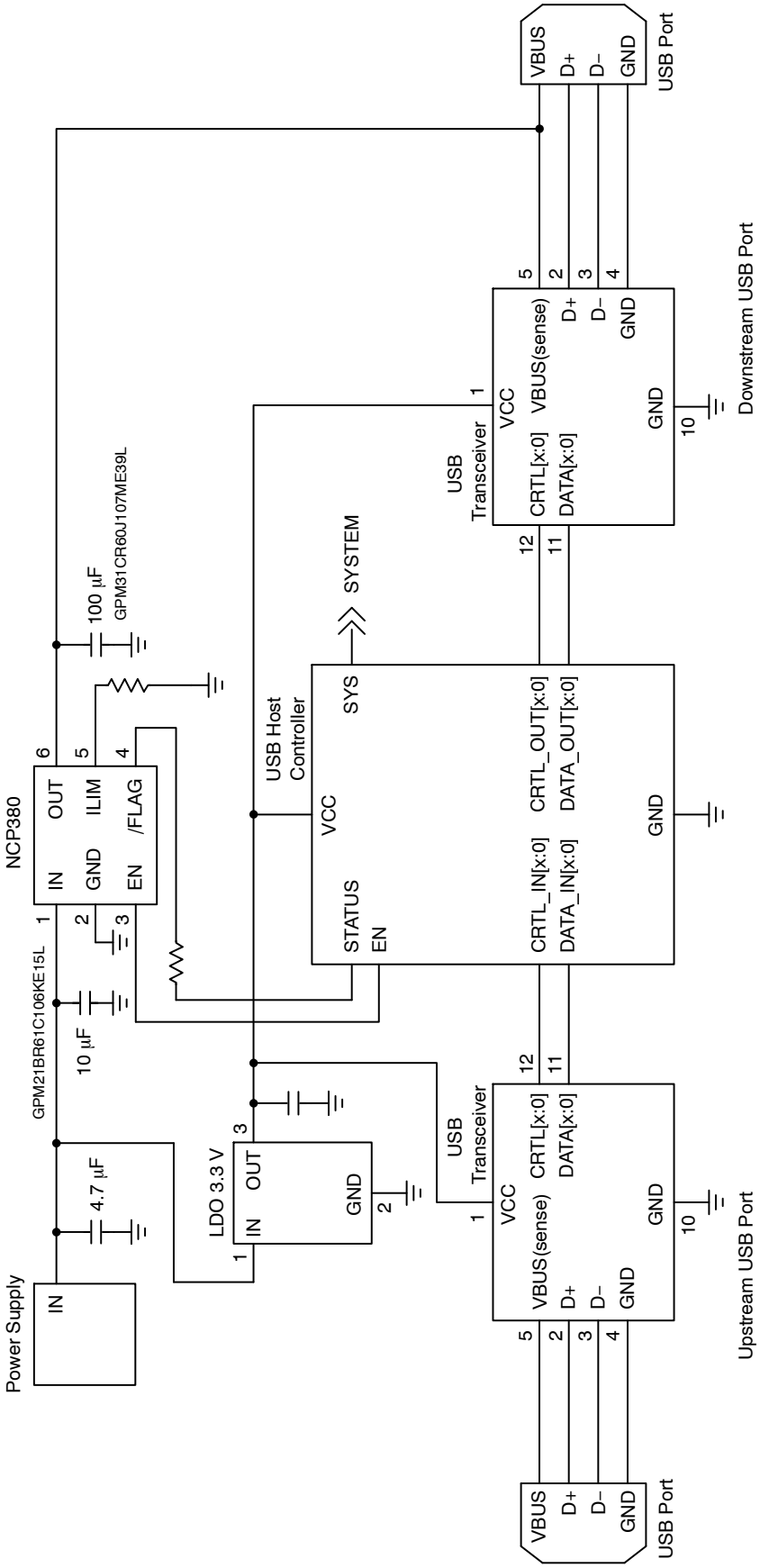

Figure 27. USB Host Typical Application

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Table 6. ORDERING INFORMATION

Device	Marking	Active Enable Level	Over Current Limit	Evaluation Board	UL Listed	CB Scheme	Package	Shipping†
NCP380LSNAJAAT1G	AAC	Low	Adj.	NCP380LSNAJAGEVB	Y	Y	TSOP−6 (Pb−Free)	3,000 Tape / Reel
NCP380LSN05AAT1G	AC5		0.5 A	NCP380LSN05AGEVB	Y	Y	TSOP−5 (Pb−Free)	
NCP380LSN10AAT1G	AC6		1.0 A	NCP380LSN10AGEVB	Y	Y		
NCP380LMUAJAATBG	AA		Adj.	NCP380LMUAJAGEVB	Y	Y	UDFN6 (Pb−Free)	
NCV380LMUAJAATBG*	AN		Adj.	NCP380LMUAJAGEVB	N	N		
NCP380LMU05AATBG	AE		0.5 A	NCP380LMU05AGEVB	Y	Y		
NCP380HSNAJAAT1G	AAD	High	Adj.	NCP380HSNAJAGEVB	Y	Y	TSOP−6 (Pb−Free)	
NCP380HSN05AAT1G	AC7		0.5 A	NCP380HSN05AGEVB	Y	Y	TSOP−5 (Pb−Free)	
NCP380HSN10AAT1G	ADA		1.0 A	NCP380HSN10AGEVB	Y	Y		
NCP380HMUAJAATBG	AC		Adj.	NCP380HMUAJAGEVB	Y	Y	UDFN6 (Pb−Free)	
NCV380HMUAJAATBG*	AP		Adj.	NCP380HMUAJAGEVB	N	N		
NCP380HMU05AATBG	AH		0.5 A	NCP380HMU05AGEVB	Y	Y		
NCP380HMU10AATBG	AJ		1.0 A	NCP380HMU10AGEVB	Y	Y		
NCP380HMU15AATBG	AK		1.5 A	NCP380HMU15AGEVB	Y	Y		
NCP380HMU20AATBG	AM		2.0 A	NCP380HMU20AGEVB	Y	Y		
NCP380HMU21AATBG	AU		2.1 A	NCP380HMU21AGEVB	Y	Y		

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable

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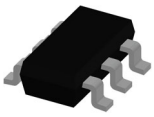
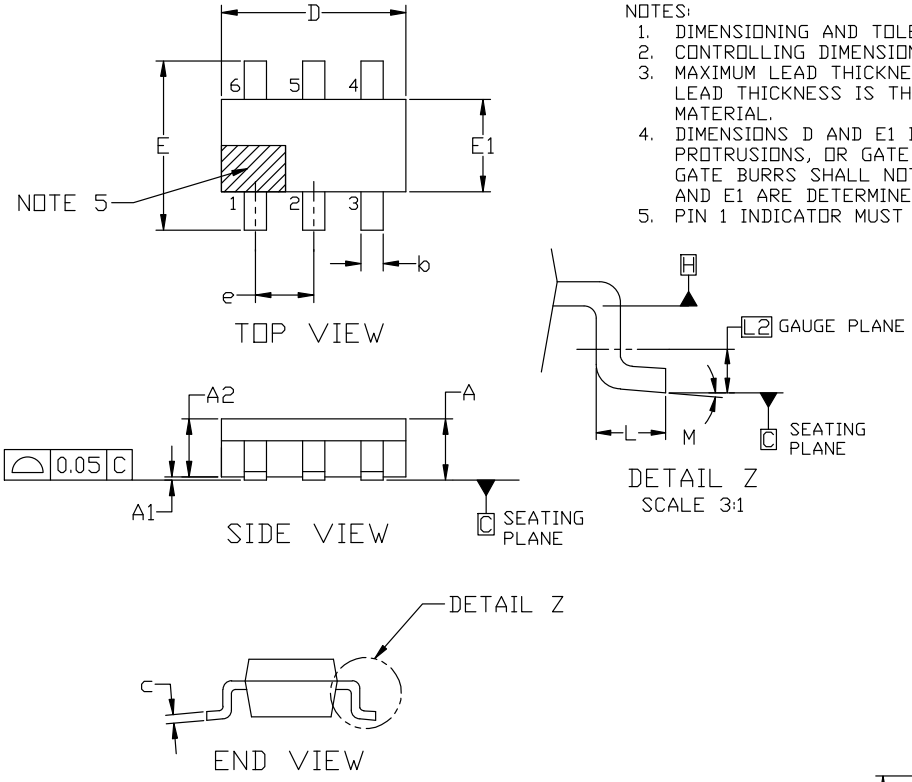


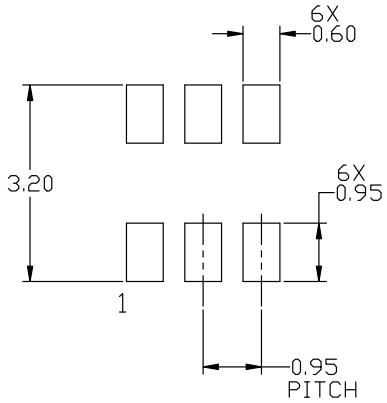
TSOP−6 3.00x1.50x0.90, 0.95P
CASE 318G
ISSUE W

DATE 26 FEB 2024



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSIONS D AND E1 ARE DETERMINED AT DATUM H.
5. PIN 1 INDICATOR MUST BE LOCATED IN THE INDICATED ZONE

MILLIMETERS			
DIM	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.01	0.06	0.10
A2	0.80	0.90	1.00
b	0.25	0.38	0.50
c	0.10	0.18	0.26
D	2.90	3.00	3.10
E	2.50	2.75	3.00
E1	1.30	1.50	1.70
e	0.85	0.95	1.05
L	0.20	0.40	0.60
L2	0.25 BSC		
M	0°	---	10°



RECOMMENDED MOUNTING FOOTPRINT

*For additional information on our Pb-Free strategy and soldering details, please download th e ON Semiconductor Soldering and Mounting Techniques Reference manual, SOLDERRM/D.

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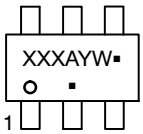
CASE 318G
ISSUE W

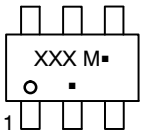
DATE 26 FEB 2024

GENERIC MARKING DIAGRAM*



IC

XXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package



STANDARD

XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLE 1:
PIN 1. DRAIN
2. DRAIN
3. GATE
4. SOURCE
5. DRAIN
6. DRAIN

STYLE 2:
PIN 1. EMITTER 2
2. BASE 1
3. COLLECTOR 1
4. EMITTER 1
5. BASE 2
6. COLLECTOR 2

STYLE 3:
PIN 1. ENABLE
2. N/C
3. R BOOST
4. Vz
5. V in
6. V out

STYLE 4:
PIN 1. N/C
2. V in
3. NOT USED
4. GROUND
5. ENABLE
6. LOAD

STYLE 5:
PIN 1. EMITTER 2
2. BASE 2
3. COLLECTOR 1
4. EMITTER 1
5. BASE 1
6. COLLECTOR 2

STYLE 6:
PIN 1. COLLECTOR
2. COLLECTOR
3. BASE
4. EMITTER
5. COLLECTOR
6. COLLECTOR

STYLE 7:
PIN 1. COLLECTOR
2. COLLECTOR
3. BASE
4. N/C
5. COLLECTOR
6. EMITTER

STYLE 8:
PIN 1. Vbus
2. D(in)
3. D(in)+
4. D(out)+
5. D(out)
6. GND

STYLE 9:
PIN 1. LOW VOLTAGE GATE
2. DRAIN
3. SOURCE
4. DRAIN
5. DRAIN
6. HIGH VOLTAGE GATE

STYLE 10:
PIN 1. D(OUT)+
2. GND
3. D(OUT)−
4. D(IN)−
5. VBUS
6. D(IN)+

STYLE 11:
PIN 1. SOURCE 1
2. DRAIN 2
3. DRAIN 2
4. SOURCE 2
5. GATE 1
6. DRAIN 1/GATE 2

STYLE 12:
PIN 1. I/O
2. GROUND
3. I/O
4. I/O
5. VCC
6. I/O

STYLE 13:
PIN 1. GATE 1
2. SOURCE 2
3. GATE 2
4. DRAIN 2
5. SOURCE 1
6. DRAIN 1

STYLE 14:
PIN 1. ANODE
2. SOURCE
3. GATE
4. CATHODE/DRAIN
5. CATHODE/DRAIN
6. CATHODE/DRAIN

STYLE 15:
PIN 1. ANODE
2. SOURCE
3. GATE
4. DRAIN
5. N/C
6. CATHODE

STYLE 16:
PIN 1. ANODE/CATHODE
2. BASE
3. EMITTER
4. COLLECTOR
5. ANODE
6. CATHODE

STYLE 17:
PIN 1. EMITTER
2. BASE
3. ANODE/CATHODE
4. ANODE
5. CATHODE
6. COLLECTOR

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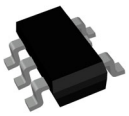

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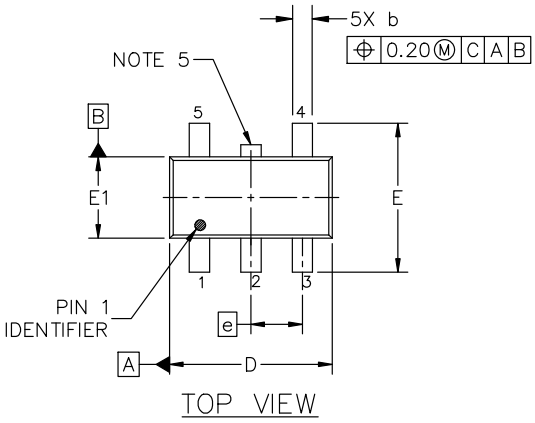
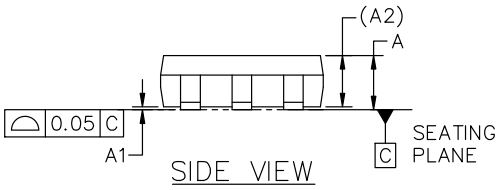
CASE 483
ISSUE P

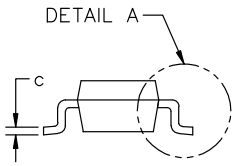
DATE 01 APR 2024



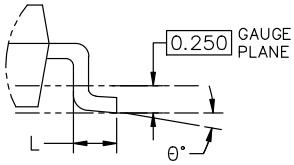
TOP VIEW



SIDE VIEW



END VIEW



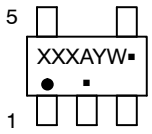
DETAIL "A"
SCALE 2:1

NOTES:

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5−2018.
2. ALL DIMENSION ARE IN MILLIMETERS (ANGLES IN DEGREES).
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OF GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSION D.
5. OPTIONAL CONSTRUCTION: AN ADDITIONAL TRIMMED LEAD IS ALLOWED IN THIS LOCATION. TRIMMED LEAD NOT TO EXTEND MORE THAN 0.2 FROM BODY.

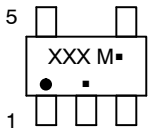
DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.900	1.000	1.100
A1	0.010	0.055	0.100
A2		0.950 REF.	
b	0.250	0.375	0.500
c	0.100	0.180	0.260
D	2.850	3.000	3.150
E	2.500	2.750	3.000
E1	1.350	1.500	1.650
e		0.950 BSC	
L	0.200	0.400	0.600
θ	0°	5°	10°

GENERIC
MARKING DIAGRAM*



Analog

XXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package

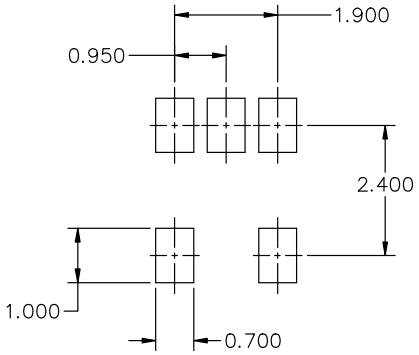


Discrete/Logic

XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.



RECOMMENDED MOUNTING FOOTPRINT*

* FOR ADDITIONAL INFORMATION ON OUR Pb−FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

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DESCRIPTION:	**TSOP−5 3.00x1.50x0.95, 0.95P**	**PAGE 1 OF 1**

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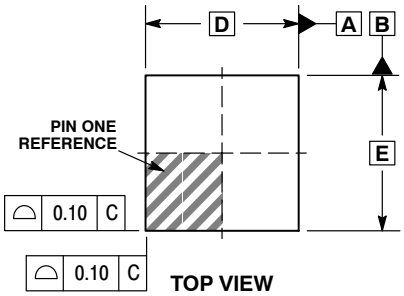
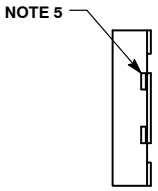
SCALE 4:1

UDFN6 2x2, 0.65P
CASE 517AB
ISSUE C

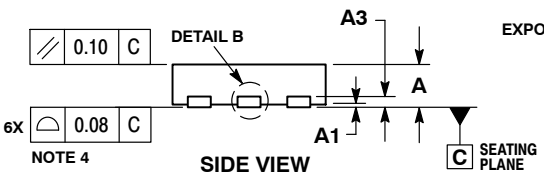
DATE 10 APR 2013

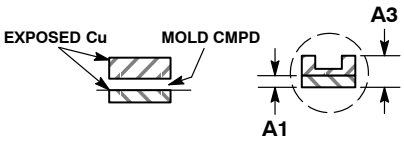




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.25MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. TIE BARS MAY BE VISIBLE IN THIS VIEW AND ARE CONNECTED TO THE THERMAL PAD.

DIM	MILLIMETERS MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A3	0.127 REF	
b	0.25	0.35
D	2.00 BSC	
D2	1.50	1.70
E	2.00 BSC	
E2	0.80	1.00
e	0.65 BSC	
L	0.25	0.35
L1	---	0.15





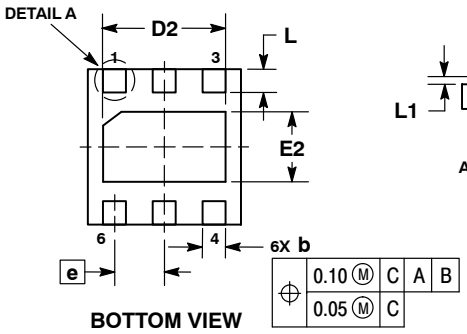
GENERIC MARKING DIAGRAM*

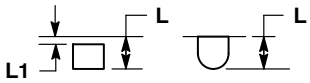


XX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

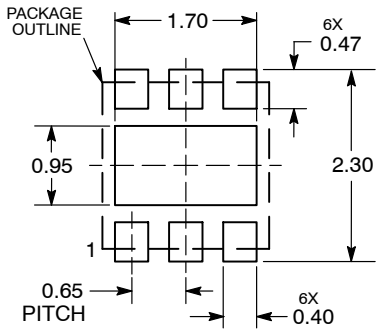
(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.





RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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