STA8089G

GPS/Galileo/GLONASS/BeiDou/QZSS receiver

Datasheet - production data

VFQFPN56
(7x7x1.0mm)

Features

- STMicroelectronics® positioning receiver with 48 tracking channels and 2 fast acquisition channels supporting GPS, Galileo, GLONASS, BeiDou and QZSS systems
- ST DRAW (Dead Reckoning Automotive Way) supported (STA8089GBD Only)
- Pin to pin compatible with STA8088G
- Single die standalone receiver embedding RF Front-End and low noise amplifier
- -162 dBm indoor sensitivity (tracking mode)
- Fast TTFF < 1 s in Hot start and 30 s in Cold Start
- High performance ARM946 MCU (up to 196 MHz)
- External SQI Flash interface
- 256 Kbyte embedded SRAM
- Real Time Clock (RTC) circuit
- 32-bit Watch-dog timer
- 2 UARTs
- 1 I^2C master/slave interface
- USB2.0 full speed (12 MHz) with integrated physical layer transceiver
- 2 Controller Area Network (CAN)
- 2 channels ADC (10 bits)
- Operating condition:
  - Main voltage regulator (V_{INL}): 1.8 V ± 5%
  - Backup voltage (V_{INB}): 1.6 V to 4.3 V
  - Digital voltage (V_{DD}): 1.1 V to 1.32 V
  - RF core voltage (V_{CC}): 1.2 V ± 10%
  - IO Ring Voltage (V_{ddIO}): 1.8 V ± 5% or 3.3 V ± 10%
- Package:
  - VFQFPN56 (7 x 7 x 1.0 mm) 0.4 mm pitch
- Ambient temperature range: -40/+85°C

Description

STA8089G belongs to Teseo III family products.

STA8089G is a single die standalone positioning receiver IC working on multiple constellations (GPS/Galileo/GLONASS/BeiDou/QZSS).

The device is offered with a complete GNSS firmware which performs all GNSS operations including tracking, acquisition, navigation and data output.

STA8089GBD can run also TESEO-DRAW the STMicroelectronics dead reckoning firmware.

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1 Overview

STA8089G is one of the part number of Teseo III STA8089x series.

STA8089G is a highly integrated single-chip standalone GNSS receiver designed for positioning system applications.

STA8089G embeds the new ST GNSS positioning engine capable of receiving signals from multiple satellite navigation systems, including the US GPS, European Galileo, Russia's GLONASS, Chinese BeiDou and Japan's QZSS.

The STA8089G ability of tracking simultaneously the signals from multiple satellites regardless of their constellation, make this chip capable of delivering exceptional accuracy in urban canyons and in the environments where buildings and other obstructions make satellite visibility challenging.

The STA8089G combines a high performance ARM946 microprocessor with I/O capabilities and enhanced peripherals. It supports USB2.0 standard at full speed (12 Mbps) with on-chip PHY.

The chip embeds backup logic with real time clock.

The device is offered with a complete firmware performing all positioning operations including acquisition, tracking, navigation and data output.

STA8089GBD can be offered also bundled with STMicroelectronis dead reckoning firmware called TESEO-DRAW; TESEO-DRAW firmware is a multi-sensors data fusion hub for Teseo family IC's.

The device powered with 1.8 V enables the on-chip voltage regulators to internally supply the RF front-end, core logic and the backup logic. The device can be directly powered with 1.2 V bypassing the embedded voltage regulators which will be put in power down mode.

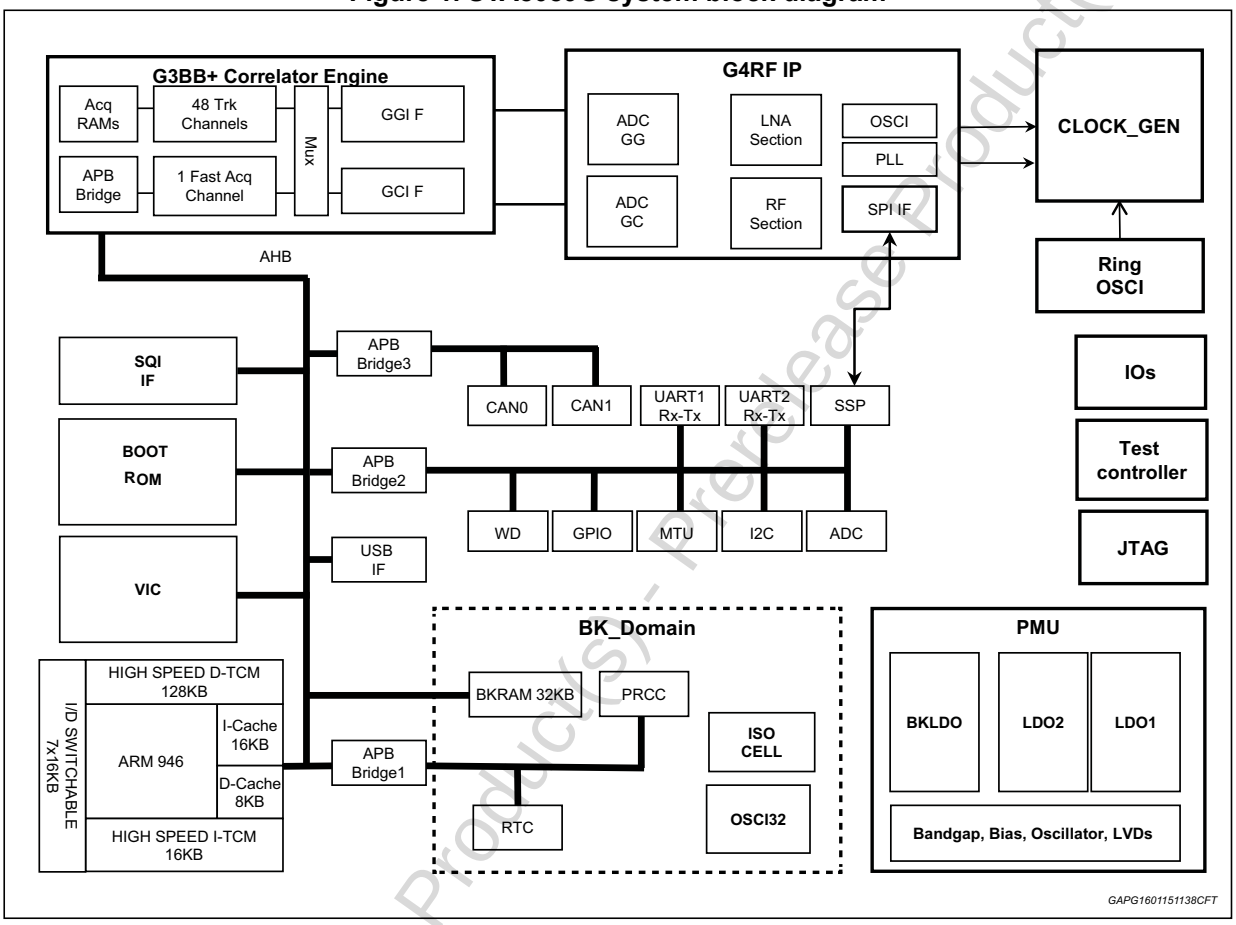
I/O lines are compatible with 1.8 V and 3.3 V.

The STA8089G, using STMicroelectronics CMOSRF Technology, is housed in a VFQFPN56 (7 x 7 x 1.0 mm) package.

2 Pin description

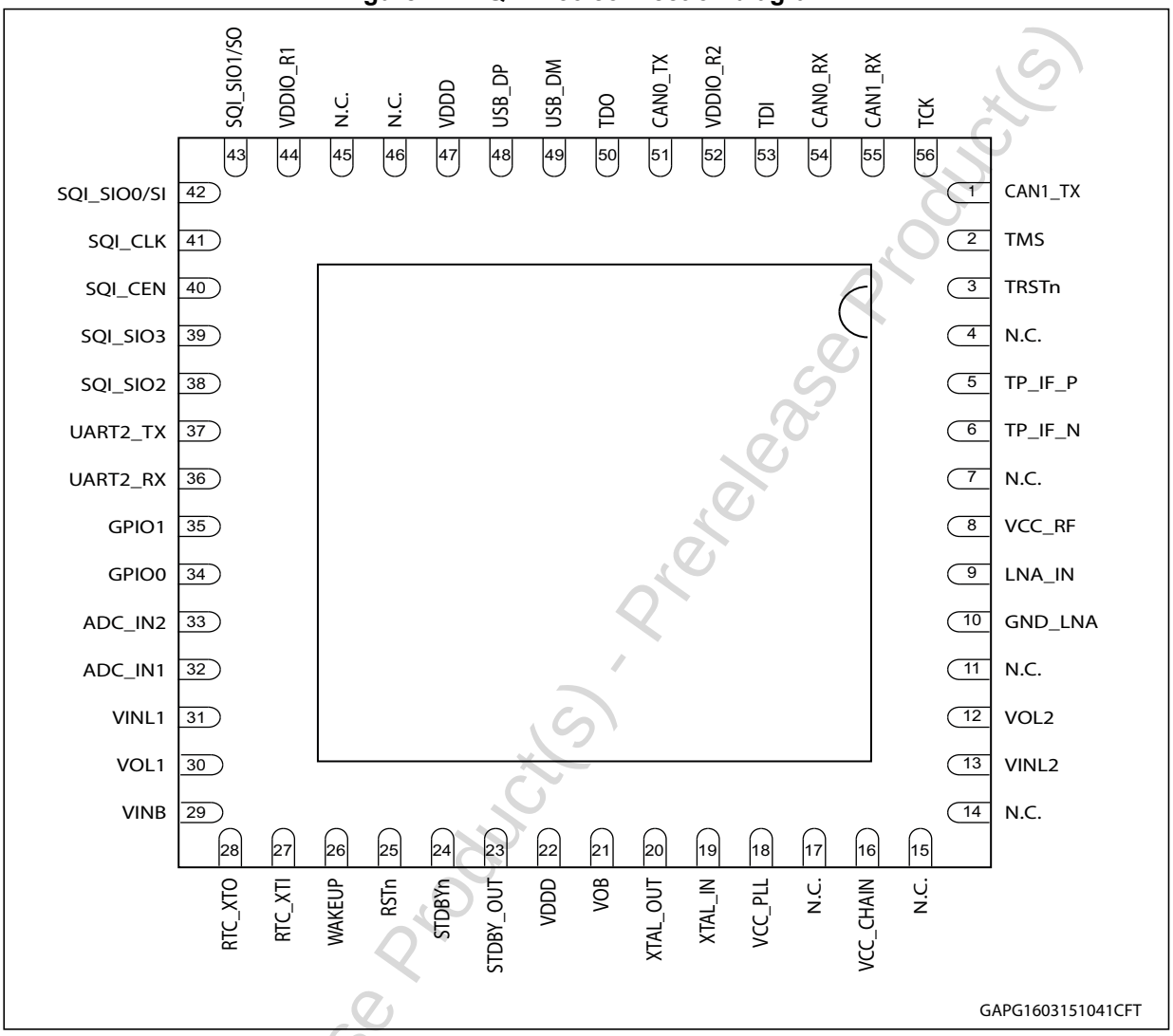
2.1 Block diagram

Figure 1. STA8089G system block diagram



2.2 VFQFPN56 pin configuration

Figure 2. VFQFPN56 connection diagram



2.3 Power supply pins

Table 1. Power supply pins

Symbol	I/O voltage	I/O	Description	STA8089G
VCC_CHAIN	1.2 V	PWR	Analog supply voltage for RF chain (1.2 V)	16
VCC_PLL	1.2 V	PWR	Analog supply voltage for PLL RF (1.2 V)	18
VCC_RF	1.2 V	PWR	Analog supply voltage for RF (1.2 V)	8
VDDD	1.1 V	PWR	Digital supply voltage	22, 47
VDDIO_R1	1.8 V or 3.3 V	PWR	Digital supply voltage for I/O ring 1 (1.8 V or 3.3V)	44
VDDIO_R2	3.3 V	PWR	Digital supply voltage for I/O ring 2 (3.3 V)	52

Table 1. Power supply pins (continued)

Symbol	I/O voltage	I/O	Description	STA8089G
VINB	1.6 V - 4.3 V	PWR	Backup LDO input supply voltage (1.6 V to 4.3 V)	29
VINL1	1.8 V	PWR	LDO1 and ADC input supply voltage	31
VINL2	1.6 V - 4.3 V	PWR	LDO2 input supply voltage (1.6 V to 4.3 V)	13
VOB	1.0 V	PWR	LDO backup output voltage (1.0 V)	21
VOL1	1.1 V	PWR	LDO1 output voltage (1.1 V)	30
VOL2	1.2 V	PWR	LDO2 output voltage (1.2 V)	12
GND	GND	GND	Ground	EP
GND_LNA	GND	GND	Ground	10

2.4 Main function pins

Table 2. Main function pins

Symbol	I/O voltage	I/O	Description	STA8089G
ADC_IN1	1.4 V – 0 V typ range	I	ADC Analog input [1]	32
ADC_IN2	1.4 V – 0 V typ range	I	ADC Analog input [2]	33
RSTn	1.0 V	I	Reset Input with Schmitt-Trigger characteristics and noise filter.	25
RTC_XTI	1.0 V (max)	I	Input of the 32 KHz oscillator amplifier circuit and input of the internal real time clock circuit.	27
RTC_XTO	1.0 V (max)	O	Output of the oscillator amplifier circuit.	28
STDBY_OUT	1.0 V	O	When low, indicates the chip is in Standby mode	23
STDBYn	1.0 V	I	When low, the chip is forced in Standby Mode - All pins in high impedance except the ones powered by Backup supply	24
WAKEUP	1.0 V	I	WAKEUP from STANDBY mode	26

2.5 Test/emulated dedicated pins

Table 3. Test/emulated dedicated pins

Symbol	I/O voltage	I/O	Description	STA8089G
TCK	VDDIO_R2	I	JTAG Test Clock	56
TDI	VDDIO_R2	I	JTAG Test Data In	53
TDO	VDDIO_R2	O	JTAG Test Data Out	50
TMS	VDDIO_R2	I	JTAG Test Mode Select	2
TRSTn	VDDIO_R2	I	JTAG Test Circuit Reset	3

Table 3. Test/emulated dedicated pins (continued)

Symbol	I/O voltage	I/O	Description	STA8089G
TP_IF_N	1.2 V	O	Diff.Test Point for IF – Neg.	6
TP_IF_P	1.2 V	O	Diff.Test Point for IF – Pos.	5

2.6 Communication interface pins

Table 4. Communication interface pins

Symbol	I/O voltage	I/O	Alternative function	Function	Description	STA8089G
SQI_CLK	VDDIO_R1	O	AF2 (default)	SQI_CLK	SQI Flash clock	41
		—	AF0, AF1, AF3	Reserved	Reserved	
SQI_CEN	VDDIO_R1	O	AF2 (default)	SQI_CEN	SQI Flash chip enable	40
		—	AF0, AF1, AF3	Reserved	Reserved	
SQI_SIO0/SI	VDDIO_R1	I/O	AF2 (default)	SQI_SIO0/SI	SQI Flash data IO 0 / ser. I/ BOOT2	42
		—	AF0, AF1, AF3	Reserved	Reserved	
SQI_SIO1/SO	VDDIO_R1	I/O	AF2 (default)	SQI_SIO1/SO	SQI Flash data IO 1 / ser. O	43
		—	AF0, AF1, AF3	Reserved	Reserved	
SQI_SIO2	VDDIO_R1	I/O	AF2 (default)	SQI_SIO2	SQI Flash data IO 2	38
		—	AF0, AF1, AF3	Reserved	Reserved	
SQI_SIO3	VDDIO_R1	I/O	AF2 (default)	SQI_SIO3	SQI Flash data IO 3 / BOOT1	39
		—	AF0, AF1, AF3	Reserved	Reserved	
CAN1_TX (1)	VDDIO_R2	O	AF0	I2C_CLK	I2C clock	1
		I/O	AF1	GPIO8	General purpose I/O #8	
		O	AF2 (default)	CAN1_TX	CAN1 transmit data output	
		—	AF3	Reserved	Reserved	
CAN1_RX (1)	VDDIO_R2	I/O	AF0	I2C_SD	I2C serial data	55
		I/O	AF1	GPIO9	General purpose I/O #9	
		I/O	AF2 (default)	CAN1_RX	CAN1 receive data input	
		—	AF3	Reserved	Reserved	
CAN0_TX (1)	VDDIO_R2	O	AF0 (default)	CAN0_TX	CAN0 transmit data output	51
		O	AF1	UART0_TX	UART0 Tx data	
		I/O	AF2	GPIO7	General purpose I/O #7	
		O	AF3	I2C_CLK	I2C clock	

Table 4. Communication interface pins (continued)

Symbol	I/O voltage	I/O	Alternative function	Function	Description	STA8089G
CAN0_RX (1)	VDDIO_R2	I	AF0 (default)	CAN0_RX	CAN0 receive data input	54
		I	AF1	UART0_RX	UART0 receive data input	
		I/O	AF2	T_{SENSE}	External temperature capture port	
		I/O	AF3	I2C_SD	I2C serial data	
UART2_RX	VDDIO_R1	I	AF0 (default)	UART2_RX	UART2 Rx data	36
		I/O	AF1	GPIO28	General purpose I/O #28	
		I/O	AF2	I2C_SD	I2C serial data	
		—	AF3	Reserved	Reserved	
UART2_TX	VDDIO_R1	O	AF0 (default)	UART2_TX	UART2 Tx data / BOOT0	37
		I/O	AF1	GPIO29	General purpose I/O #29	
		O	AF2	I2C_CLK	I2C clock	
		—	AF3	Reserved	Reserved	
GPIO0	VDDIO_R1	I/O	AF0 (default)	GPIO0	General purpose I/O #0	34
		I	AF1	PPS_IN	Pulse per second input	
		O	AF2	Timer_OCMPB	Extended Function Timer - Output Compare B	
		O	AF3	Mag_0 GC	GLONASS and BeiDou 3-bit coding Output (MAG0)	
GPIO1	VDDIO_R1	I/O	AF0 (default)	GPIO1	General purpose I/O #1 / BOOT3	35
		—	AF1	Reserved	Reserved	
		O	AF2	PPS_OUT	Pulse per second output	
		I/O	AF3	Tsense	External temperature capture port	
USB_DM	VDDIO_R2	USB	AF0	USB_DM	USB D- signal	49
		I	AF1 (default)	UART1_RX	UART1 Rx data	
		I	AF2	CAN1_RX	CAN1 receive data input	
		I/O	AF3	I2C_SD	I2C serial data	
USB_DP	VDDIO_R2	USB	AF0	USB_DP	USB D+ signal	48
		O	AF1 (default)	UART1_TX	UART1 Tx data	
		O	AF2	CAN1_TX	CAN1 transmit data output	
		O	AF3	I2C_CLK	I2C clock	

1. Only for STA8089GB and STA8089GBD.

2.7 RF front-end pins

Table 5. RF front-end pins

Symbol	I/O voltage	I/O	Description	STA8089G
LNA_IN	1.2V	I	Low Noise Amplifier Input	9
XTAL_IN	1.2V	I	Input Side of Crystal Oscillator or TCXO Input	19
XTAL_OUT	1.2V	O	Output Side of Crystal Oscillator	20

3 General description

3.1 RF front end

The RF front-end is able to down-convert both the GPS-Galileo signal from 1575.42 MHz to 4.092 MHz (4 Fo, being F0 = 1.023 MHz), the GLONASS signal from 1601.718 MHz to 8.57 MHz and the BeiDou signal from 1561.098 MHz to 10.23 MHz.

It embeds high performance LNA minimizing external component count and a LDO to supply the internal core facilitating requirements for external power supply. A three bits ADC converts the IF signals to sign (SIGN) and magnitude (MAG0 and MAG1). They can be sampled or not by SPI. The magnitude bits are internally integrated in order to control the variable gain amplifiers. The VGA gain can be also set by the SPI interface.

The RF tuner accepts a wide range of reference clocks (10 to 52 MHz) and can generate 64 Fo sampling clock for the baseband and 192 Fo clock for MCU subsystem.

3.2 GPS/Galileo/GLONASS/BeiDou Base Band (G3BB+) processor

STA8089G integrates G3BB+ proprietary IP, which is the ST last generation high-sensitivity Baseband processor fully compliant with GPS, Galileo, GLONASS and BeiDou systems.

The baseband receives, from the embedded RF Front-End, two separate IF signals coded in sign-magnitude digital format on 3 bits and the related clocks. The Galileo/GPS (GALGPS) and GLONASS/BeiDou (GNSCOM) signals at the base band inputs are centered on 4.092 MHz, 8.57 MHz and 10.23 MHz.

The baseband processes the two IF signals performing data codification, sample rate conversion and final frequency conversion to zero IF before acquisition and tracking correlations.

The baseband processor has the capability of acquire and track the Galileo, GPS, GLONASS and BeiDou signals in a simultaneous or single way, or a combination of three, being GLONASS and BeiDou mutually exclusive. The number of tracking channels to be used is programmable; the not used tracking channels can be powered down.

A complete multi-OS software library is provided by ST to handle GPS processing, managing satellite acquisition, tracking, pseudo-range calculation and positioning, generating the output in the standard NMEA message format or in a ST binary format. The library includes support of ST self-trained assisted GPS (ST-AGPS), a complete and scalable solution for assisting GPS start-up with autonomous and server-based ephemeris prediction and extension.

3.3 MCU Subsystem

The implemented sub-system includes an AHB Lite bus matrix.

An ARM946 core is embedded in the sub-system and masters the AHB bus. The totally available TCM SRAM is 256 KB. The amount of memory on ITCM and DTCM can be configured by the ARM946 (see *Table 6: TCM Configuration*). ITCM can be configured as Ni x 16 KB; DTCM can be configured as 128 + Nd x 16 KB, where Ni + Nd = 8, Ni ≥ 1.

Table 6. TCM Configuration

TCMcfg [2]	TCMcfg [1]	TCMcfg [0]	ITCM	DTCM
0	0	0	16 KB	240 KB
0	0	1	32 KB	224 KB
0	1	0	48 KB	208 KB
0	1	1	64 KB	192 KB
1	0	0	80 KB	176 KB
1	0	1	96 KB	160 KB
1	1	0	112 KB	144 KB
1	1	1	128 KB	128 KB

3.3.1 AHB slaves

- G3 APB port that allows to interface with the G3BB acquisition memory and control registers.
- 512 Kbytes ROM
- Vectored Interrupt Controller (VIC).
- SQI flash memory controller
- 3 x ARM946 APB peripheral bus (APB1, APB2, APB3).

Vectored Interrupt Controller (VIC)

This Vectored Interrupt Controller (VIC) allows the operative system interrupt handler to quickly dispatch interrupt service routines in response to peripheral interrupts. It provides a software interface to the interrupt system. There are up to 64 interrupt lines. The VIC uses a bit position for each different interrupt source.

The software can control each request line to generate software interrupts. Each interrupt line can be independently enabled and configured to trigger a non-vectored Normal Interrupt Request (IRQ) or Fast Interrupt Request (FIQ) to the ARM946 CPU. Sixteen interrupt lines can also be selected to trigger a vectored IRQ.

The VIC has two operation modes: the user mode and the privilege mode, in order to have the possibility to set (or not) one level of protection during execution.

FS USB device controller

Full speed USB device with transceiver. It is an AHB slave. When active requires a 48 MHz clock XTAL_IN.

SQI Flash interface

STA8089G includes a high-performance interface to Serial Quad Interface (SQI) NOR Flash chips, to support a low-cost simple implementation.

3.4 APB peripherals

3.4.1 CAN (only STA8089GB and STA8089GBD)

The 2 CAN cores perform communication according to the CAN protocol version 2.0 part A and B. The bit rate can be programmed to values up to 1 MBit/s. For the connection to the physical layer, additional transceiver hardware is required.

CAN consists of the CAN core, message RAM, message handler, control registers and module. For communication on a CAN network, individual message objects are configured. The message objects and identifier masks for acceptance filtering of received messages are stored in the message RAM. All functions concerning the handling of messages are implemented in the message handler. These functions include acceptance filtering, the transfer of messages between the CAN core and the message RAM, and the handling of transmission requests as well as the generation of the module interrupt.

The register set of the CAN can be accessed directly by the CPU through the module interface. These registers are used to control/configure the CAN core and the message handler and to access the message RAM.

CAN features

- Supports CAN protocol version 2.0 part A and B
- 32 messages objects
- Each message object has its own identifier mask
- Maskable interrupt
- Disabled automatic re-transmission mode for time triggered CAN applications
- Programmable loop-back mode for self-test operation
- Two 16-bit module interfaces to the AMBA APB bus from ARM

3.4.2 UART

The UARTx (x = 1|2) performs serial-to-parallel conversion on data asynchronously received from a peripheral device on UARTx_RX pin, and parallel-to-serial conversion on data written by CPU for transmission on UARTx_TX pin. The transmit and receive paths are buffered with internal FIFO memories allowing up to 64 data byte for transmission, and 64 data byte with 4-bit status (break, frame, parity, and overrun) for receive.

UART features

The UARTx (x = 1|2) are Universal Asynchronous Receiver/Transmitter that support much of the functionality of the industry-standard 16C650 UART. The main features are:

- Programmable baud rates up to UARTCLK / 16 (1.5 Mbps with UARTCLK at 24 MHz), or up to UARTCLK / 8 (3.0 Mbps with UARTCLK at 24 MHz), with fractional baud-rate generator
- 5, 6, 7 or 8 bits of data
- Even, odd, stick or no-parity bit generation and detection
- 1 or 2 stop bit generation
- Support of software flow control using programmable Xon/Xoff characters
- False start bit detection
- Line break generation and detection
- Separate 8-bit wide, 64-deep transmit FIFO and 12-bit wide, 64-deep receive FIFO
- Programmable FIFO disabling for 1-byte depth data path

These UARTs vary from industry-standard 16C650 on some minor points which are:

- Receive FIFO trigger levels
- The internal register map address space, and the bit function of each register differ
- The deltas of the modem status signals are not available
- 1.5 stop bits is not supported
- Independent receive clock feature is not supported

3.4.3 I2C

STA8089G includes an I2C interface configurable as master or slave.

3.4.4 MTU

The 2 Multi Timer Units provide access to eight interrupt generating programmable 32-bit Free-Running decrementing Counters (FRCs). The FRCs have their own clock input, allowing the counters to run from a much slower clock than the system clock.

The FRC is the part of the timer that performs the counting. There are four instantiations of the FRC block in each MTU, allowing eight counts to be performed in parallel. The 32-bit counter in the FRC is split up into two 16-bit counters.

3.4.5 WDT

Watchdog Timer (WDT) provides a way of recovering from software crashes. The watchdog clock is used to generate a regular interrupt (WDOGINT), depending on a programmed value.

The watchdog monitors the interrupt and asserts a reset signal (WDOGRES) if the interrupt remains unserviced for the entire programmed period. You can enable or disable the watchdog unit as required.

Note: Watchdog is stalled when the ARM processor is in Debug mode.

3.4.6 GPIO

The GPIO block provides seven (7) programmable inputs or outputs. Each input or output can be controlled in two modes:

- software mode through an APB bus interface
- alternate mode, where GPIO becomes a peripheral input or output line

Any GPIO input can be independently enabled or disabled (masked) for interrupt generation. User can select for each GPIO which edge (rising, falling, both) will trigger an interrupt.

3.4.7 ADC

10 bit SAR ADC operating at 1.8 V analog supply. It can convert up to 2 single ended channels with analog input multiplexer at 500KSPS

3.4.8 RTC

This is an always-on power domain dedicated to RTC logic (backup system) with 32 Kbyte SRAM and supplied with a dedicated voltage regulator.

The RTC provides a high resolution clock which can be used for GPS. It keeps the time when the system is inactive and can be used to wake the system up when a programmed alarm time is reached. It has a clock trimming feature to compensate for the accuracy of the 32.768 kHz crystal and a secured time update.

RTC features

- 47-bit counter clocked by 32.768 kHz clock
- 32-bit for the integer part (seconds) and 15-bit for the fractional part
- The integer part and the fractional part are readable independently
- The counter, once enabled, can be stopped
- Integer part load register (32-bit)
- Fractional part load register (15-bit)
- Load bit to transfer the content of the entire load register (integer+fractional part) to the 47-bit counter. Once set by the MCU this bits is cleared by the hardware to signal to the MCU that the RTC has been updated.

4 Electrical characteristics

4.1 Parameter conditions

Unless otherwise specified, all voltages are referred to GND.

4.2 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A = 25 °C.

4.3 Typical values

Unless otherwise specified, typical data are based on T_A = 25°C, V_{ddio} = 1.8 V, V_{dd} = 1.20 V. They are given only as design guidelines and are not tested.

4.4 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

4.5 Absolute maximum ratings

This product contains devices to protect the inputs against damage due to high static voltages, however it is advisable to take normal precautions to avoid application of any voltage higher than the specified maximum rated voltages.

Table 7 lists the absolute maximum rating.

Table 7. Voltage characteristics

Symbol	Parameter	Min.	Max.	Unit
V_{CC_CHAIN}	Analog supply voltage for RF chain (1.2 V)	-0.3	1.32	V
V_{CC_PLL}	Analog supply voltage for PLL RF (1.2 V)	-0.3	1.32	V
V_{CC_RF}	Analog supply voltage for RF (1.2 V)	-0.3	1.32	V
V_{DDD}	Power supply pins for the core logic.	-0.3	1.32	V
V_{DDIO_R1}	Digital supply voltage for I/O ring 1 (1.8 V or 3.3 V)	-0.3	3.63	V
V_{DDIO_R2}	Digital supply voltage for I/O ring 2 (3.3 V)	-0.3	3.63	V
V_{INB}	Backup LDO input supply voltage (1.6 V to 4.3 V)	-0.3	4.8	V
V_{INL1}	LDO1 input supply voltage (1.8 V)	-0.3	1.98	V
V_{INL2}	LDO2 input supply voltage (1.6 V to 4.3 V)	-0.3	4.8	V

Table 7. Voltage characteristics (continued)

Symbol	Parameter	Min.	Max.	Unit
$V_{ESD-HBM}$	Electrostatic discharge, human body model(1).	-2	2	kV
$V_{ESD-CDM}$	Electrostatic discharge, charge device model(2).	-250	250	V

1. Pins sustaining only ±500 V are: 12, 13, 21, 27, 28, 29, 30 and 31,
2. Pin 9 (LNA_IN) sustains only ±100 V.

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 8. Thermal characteristics

Symbol	Parameter	Min.	Max.	Unit
T_{oper}	Operative ambient temperature	-40	85	°C
T_j	Operative junction temperature	-40	125	°C
T_{st}	Storage temperature	-55	150	°C
R_{j-amb}	Thermal resistance junction to ambient(1)	—	24.4	°C/W

1. According to JEDEC specification on a 2 layers board.

Table 9. Frequency limits

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
F_{CLK}	Operating ARM9 CPU frequency	V_{DDD} = 1.2 V; T_C = 85 °C(1)	—	—	196	MHz
F_{AHB}	AHB frequency		—	—	49	MHz

1. Not tested in production.

Table 10. Power consumption

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
P_{RF}	RFIP power (total V_{INL2})	G2 = GPS/Galileo; T_{amb} = 25 °C; V_{INL2} = 1.8 V	—	25	—	mW
		G2 + GLONASS; T_{amb} = 25 °C; V_{INL2} = 1.8 V	—	35	—	mW
		G2 + BeiDou; T_{amb} = 25 °C; V_{INL2} = 1.8 V	—	35	—	mW

Table 10. Power consumption (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
P_{MVR}(1)	Switchable area power; (total V_{INL1})	f_{ARM} = 196 MHz; f_{AHB} = 49 MHz; T_{amb} = 25 °C; V_{INL1} = 1.8 V; UART active; other peripherals inactive	—	90	—	mW
P_{LPVR}(1)	Always ON area power (total V_{INB})	f_{ARM} = 196 MHz; f_{AHB} = 49 MHz; T_{amb} = 25 °C; V_{INB} = 3.3 V	—	1	—	mW
P_{IO}(1)	IO rings power (total V_{DDIO_R1} + V_{DDIO_R2})	f_{ARM} = 196 MHz; f_{AHB} = 49 MHz; T_{amb} = 25 °C; V_{INL1} = 1.8 V; UART active; other peripherals inactive	—	4	—	mW
$I_{DStandby}$	Standby mode supply current	RTC running = 32.768 KHz; T_{amb} = 25 °C; V_{INB} = 1.8 V	—	29	—	µA
$I_{DDeepStandby}$	Deep standby mode supply current(2)		—	7	—	µA

1. Not tested in production.
2. STDBY_OUT pin not supported in deep standby.

4.6 Recommended DC operating conditions

Table 11 lists the functional recommended operating DC parameters for STA8089G.

Table 11. Recommended DC operating conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC_CHAIN}	Analog supply voltage for RF chain (1.2 V)	1.08	1.20	1.32	V
V_{CC_PLL}	Analog supply voltage for PLL RF (1.2 V)	1.08	1.20	1.32	V
V_{CC_RF}	Analog supply voltage for RF (1.2 V)	1.08	1.20	1.32	V
V_{DDD}	Power supply pins for the core logic.	1.0	1.1	1.32	V
V_{DDIO_R1}	Digital supply voltage for I/O ring 1 (1.8 V)	1.71	1.80	1.89	V
	Digital supply voltage for I/O ring 1 (3.3 V)	3.00	3.30	3.60	V
V_{DDIO_R2}	Digital supply voltage for I/O ring 2 (3.3 V)	3.00	3.30	3.60	V
V_{INB}	Backup LDO input supply voltage (1.6 V to 4.3 V)	1.60		4.30	V
V_{INL1}	LDO1 input supply voltage	1.71		1.89	V
V_{INL2}	LDO2 input supply voltage to generate 1.2 V	1.60		4.30	V
T_C	Operating case temperature	-40		85	°C

4.7 DC characteristics

Table 12 specifies the LDO1 voltage regulator characteristics.

Table 12. LDO1 DC characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{OL1}	Output voltage (1.2 V)	1.71 V ≤ V_{INL1} ≤ 1.89 V; I_{OL1} ≤ 70 mA	1.1	1.20	1.32	V
I_{OL1}	Output current		0	—	70	mA

Table 13 specifies the LDO2 voltage regulator characteristics.

Table 13. LDO2 DC characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{OL2}	Output voltage	1.6 V ≤ V_{INL2} ≤ 4.3 V; I_{OL2} ≤ 30 mA	1.08	1.20	1.32	V
I_{OL2}	Output current		0	—	30	mA

Table 14 specifies the low voltage detection thresholds

Table 14. Low voltage detection thresholds

Parameter		Min.	Typ.	Max.	Unit
Input LVD always on and main VRs(1)	Upper voltage threshold	—	1.680	—	V
	Lower voltage threshold	—	1.650	—	V
Output LVD always on VR(1)	Upper voltage threshold	—	0.995	—	V
	Lower voltage threshold	—	0.935	—	V
Output LVD main VR (1)	Upper voltage threshold @ V_{OLM} = 1.2 V	—	1.142	—	V
	Lower voltage threshold @ V_{OLM} = 1.2 V	—	1.076	—	V

1. Non tested in production.

Table 15 lists the DC characteristics for all the IO digital buffers except for the following input buffers: STBYn (24), STDBY_OUT (23), WAKEUP (26), TRSTn (3) and RSTn (25).

Table 15. I/O buffers DC characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IL}(1)	Logical input low level voltage	V_{DDIO} = 1.8 V	-0.3	—	0.3 * V_{DDIO}	V
		V_{DDIO} = 3.3V	-0.3	—	0.8	V
V_{IH}(1)	Logical input high level voltage	V_{DDIO} = 1.8 V	0.7 * V_{DDIO}	—	V_{DDIO} + 0.3	V
		V_{DDIO} = 3.3V	2.0	—	V_{DDIO} + 0.3	V
V_{HYST}(2)	Schmitt-trigger hysteresis	–	50	—		mV

Table 15. I/O buffers DC characteristics (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{OL}	Low level output voltage	V_{DDIO} = 1.8 V		—	0.4	V
		V_{DDIO} = 3.3V		—	0.4	V
V_{OH}	High level output voltage	V_{DDIO} = 1.8 V	V_{DDIO} - 0.4	—		V
		V_{DDIO} = 3.3V	V_{DDIO} - 0.4	—		V

1. Excludes oscillator inputs RTC_XTI and XTAL_IN. Refer to oscillator electrical specifications.
2. Apply to all digital inputs unless specified otherwise.

Table 16 lists the DC characteristics for the 1.0 V IO digital buffers input buffers: STBYn (24), STDBY_OUT (23), WAKEUP (26), TRSTn (3) and RSTn (25).

Table 16. 1.0 V I/O buffers DC characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IL}	Logical input low level voltage	V_{OB} = 1.0 V	-0.3	—	0.35 * V_{OB}	V
V_{IH}	Logical input high level voltage	V_{OB} = 1.0 V	0.65 * V_{OB}	—	V_{OB} + 0.3	V
V_{OL}	Low level output voltage	V_{OB} = 1.0 V		—	0.2	V
V_{OH}	High level output voltage	V_{OB} = 1.0 V	V_{OB} - 0.2	—		V

4.8 AC characteristics

4.8.1 RF electrical specifications

Table 17. RFCHAIN – GALGPS filter and VGA

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
S11(1)	Input return loss	GPS band	—	-8		dB
f_{IF}	IF frequency	PLL in default condition with 26Mhz as reference	—	4.045		MHz
NF	Noise figure	NF overall chain with AGC set at 0 dB	—	2(1)		dB
C_G	Conversion gain from RF input to ADC input	VGA at max gain	—	119		dB
		VGA at min gain	—	69		dB
IP_{1dB}	RF-IF-VGA input compression point	VGA min	—	-80		dBm
IRR	Image rejection ratio		—	20		dB
BW_{GPS}	-3dB IF bandwidth	GPS mode	—	2.4		MHz
BW_{GAL}		Galileo mode	—	4.8		MHz

Table 17. RFCHAIN – GALGPS filter and VGA (continued)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
ATT	Alias frequency rejection	F = 60 MHz (fs = 65.474 MHz)	—	30		dB
T_{gGPS}	IF filter group delay variation	GPS mode	—		200(1)	ns
T_{gGAL}		Galileo mode	—		30(1)	ns

1. Not tested in production.

Table 18. RFCHAIN – GLONASS/BeiDou filter and VGA

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
S11(1)	Input return loss	GLONASS band		-10		dB
		BeiDou band		-7		
$f_{IFGNS/BDU}$	IF frequency for GLONASS	PLL in default condition with 26 Mhz as reference	—	8.519		MHz
	IF frequency for BeiDou		—	10.277		
NF	Noise figure	NF overall chain with AGC set at 0 dB	—	2(1)		dB
C_G	Conversion gain from RF input to ADC input	VGA at max gain	—	118		dB
		VGA at min gain	—	68		dB
IP_{1dB}	RF-IF-VGA input compression point	VGA min	—	-80		dBm
IRR	Image rejection ratio		—	25		dB
$BW_{GNS/BDU}$	-3dB IF bandwidth		—	10		MHz
ATT	Alias frequency rejection	F = 53 MHz (fs = 65.474 MHz)	—	30		dB
$T_{gGNS/BDU}$	IF filter group delay variation		—		20(1)	ns

1. Not tested in production.

Table 19. Synthesizer

Symbol	Parameter	Min.	Typ.	Max.	Unit
F_{TCXO_XTAL}	Input frequency for xtal amplifier (1)	10		52	MHz
R_{DIV}	Reference divider range	1		63	
N_{DIV}	Loop divider range	56		2047	
F_{LO}	LO operating frequency		3142.656		MHz

1. That amplifier can be used also like TCXO input buffer

4.8.2 Oscillator electrical specifications

This device contains two oscillators:

- a 32.768 kHz oscillator/buffer for RTC circuit.
- an OSCI oscillator/buffer in the RF Front-End

When used in oscillator mode, each oscillator requires a specific crystal, with parameters that must be as close as possible to the following recommended values. When used in input buffer mode, an external clock source must be applied.

32.768 kHz OSCI32 oscillator specifications

The 32.768 kHz OSCI32 oscillator is connected between RTC_XTI (oscillator amplifier input) and RTC_XTO (oscillator amplifier output). It also requires two external capacitors of 18 pF[(a)], as shown on *Figure 3*.

OSCI32 is disabled by default and must be enabled by setting bit28-OSCI_EN of PRCC_BACKUP_REG0 to have 32.768KHz oscillation when an XTAL pi-network is connected to RTC_XTI/RTC_XTO pins.

The recommended oscillator specifications are shown in *Table 20*:

Table 20. Crystal recommended specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
F_{SXTAL}	Crystal frequency(1)	—	32.768	—	kHz
LM_{SXTAL}	Motion inductance(1)	—	5	—	kH
CM_{SXTAL}	Motional capacitance(1)	—	5.0	—	fF
CO_{SXTAL}	Shunt capacitance(1)	—	1.3	—	pF
ESR	Resonance resistance(1)	—	—	80	kΩ
CL	External load capacitance(1)	—	18	—	pF

1. Not tested in production.

The oscillator amplifier specifications are shown in following table:

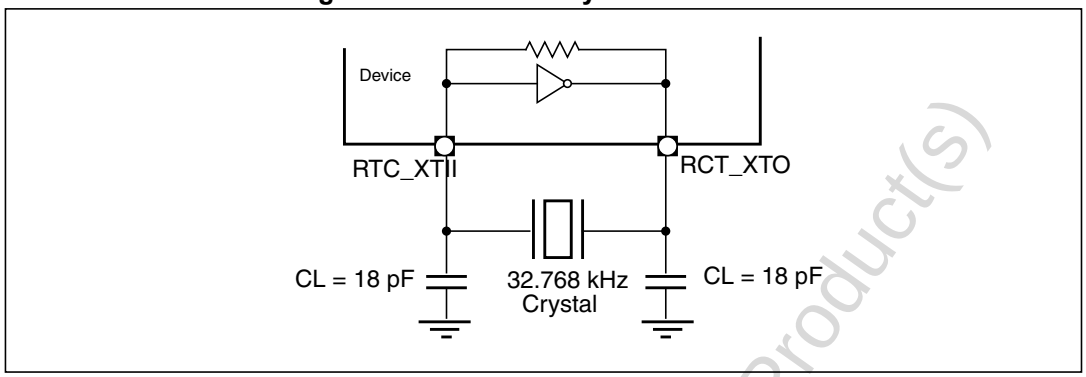
Table 21. Oscillator amplifier specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_S	Startup time(1)	—	0.3	0.6	s
DL	Drive level(1)	—	—	<0.1	µW
RLC	Required load capacitance(1)	—	12.5	—	pF
GM	Startup transconductance	22.5	33.6	—	µA/V

1. Not tested in production.

a. Using crystal with recommended characteristics as per *Table 20*.

Figure 3. 32.768 kHz crystal connection



To drive the 32.768 kHz crystal pins from an external clock source:

- Disable the oscillator (bit28-OSCI_EN = 0b in PRCC_BACKUP_REG0 register). This disables the internal inverter, thus reducing the power consumption to minimum.
- Drive the RTC_XTI pin with a square signal or a sine wave.

Table 22. Characteristics of external slow clock input

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_{JIT} (cc)	Cycle-to-cycle jitter	-70	—	70	ps
T_{JIT} (per)	Period jitter	-70	—	70	ps
	Variation	-500	—	500	ppm
T_{DUTY}	Duty cycle	45	—	55	%

4.8.3 OSCI oscillator specifications

Default supported values are 16.368 MHz, 24 MHz, 26 MHz and 48 MHz.

To enable USB peripheral the 48 MHz is mandatory

4.8.4 ADC specifications

This section gives the AC specification of the 10 bit Successive Approximation Register ADC embedded in STA8089G device. It is controlled by the ARM9 MCU through a wrapper and an APB bridge as depicted in *Figure 4* and it has a maximum conversion rate of 1MSPS with 8 muxed analog input channels capability. An internal voltage reference is used and analog/digital power supplies connections are implemented inside the device without any needs of dedicated external pins.

Figure 4. SARADC connections

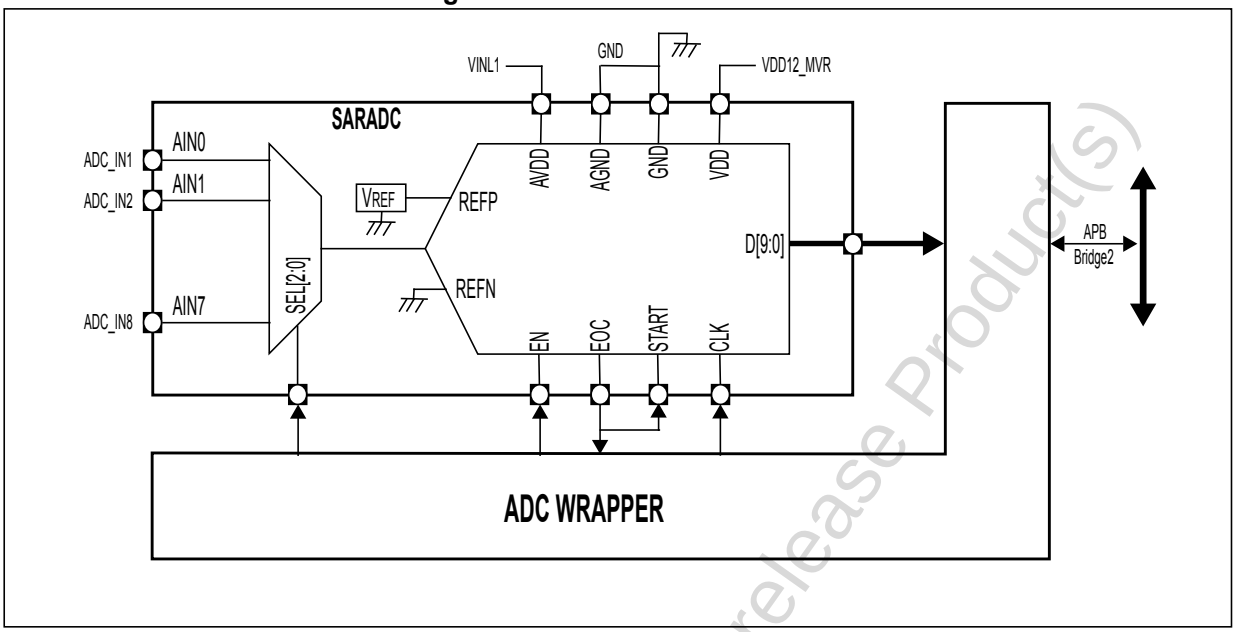


Table 23. SARADC specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{ADCIN}	ADC_IN input range	V_{GND}-0.3	—	V_{DD_ADC}+0.3	V
V_{ADCCR}	Conversion range	V_{GND}	—	V_{REF}	V
V_{REF}	Voltage reference	1.35	1.4	1.45	V
C_{IN}	Input capacitance(1)	5.5	7.0	8.5	pF
R_{IN}	Input mux resistance (total equivalent sampling resistance)(2)	1.5	2.0	2.5	kΩ
F_{CLK}	Clock frequency	2.5		15	MHz
δ_{CLK}	Clock duty cycle	45	50	55	%
T_{SUP}	Start up time(1)(3)	—	—	20	µs
T_C	Conversion time	—	14	—	cycles
T_S	Sampling time	—	3		cycles
INL	Performance	—	—	< ±2	LSB
DNL		—	—	< ±2	LSB

1. Not tested in production.
2. Pad input capacitance included.
3. From EN = 1.

5 Package and packing information

5.1 ECOPACK® packages

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com.

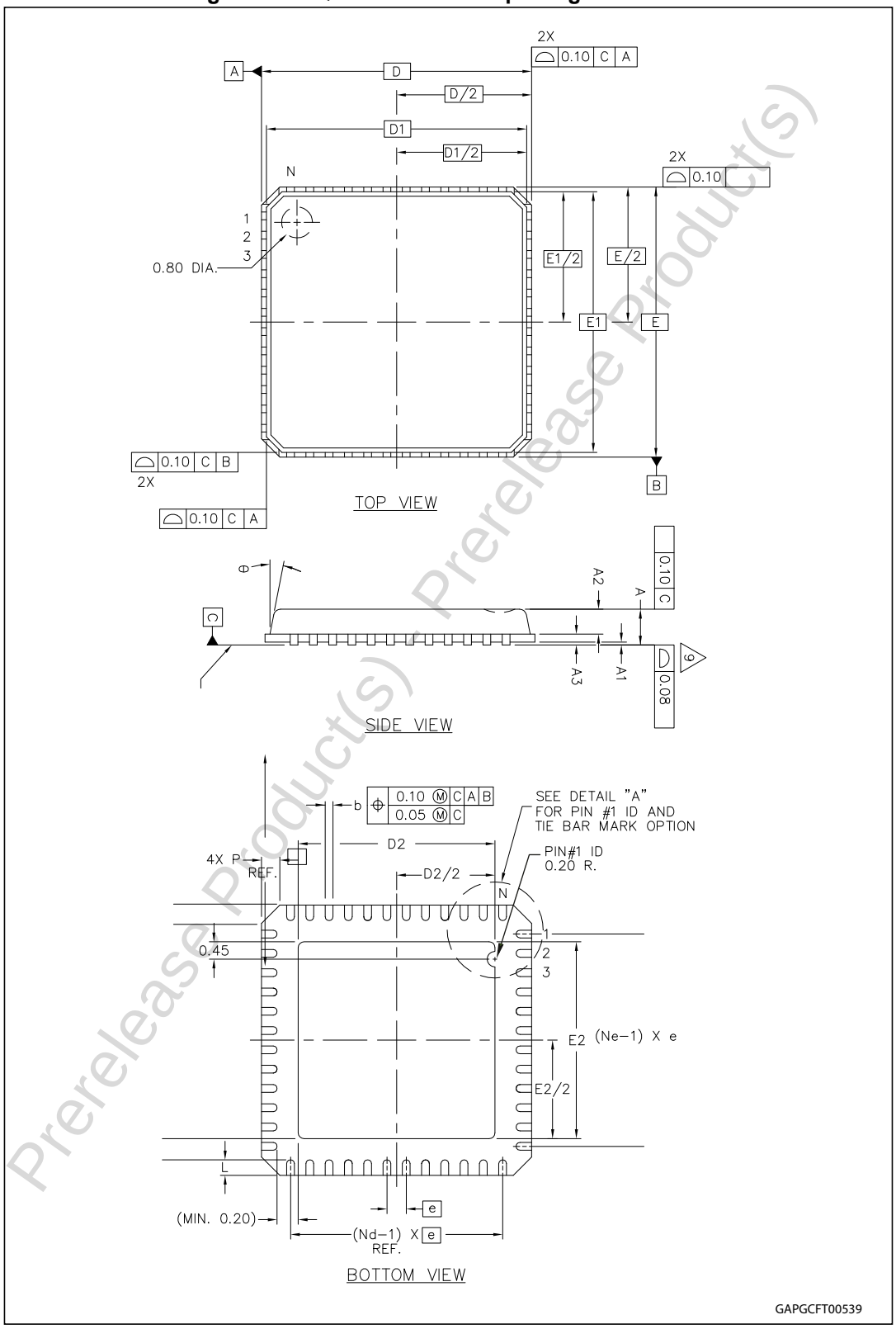
ECOPACK® is an ST trademark.

5.2 VFQFPN56 7 x 7 mm package information

Table 24. VFQFPN56 7 x 7 mm package dimensions

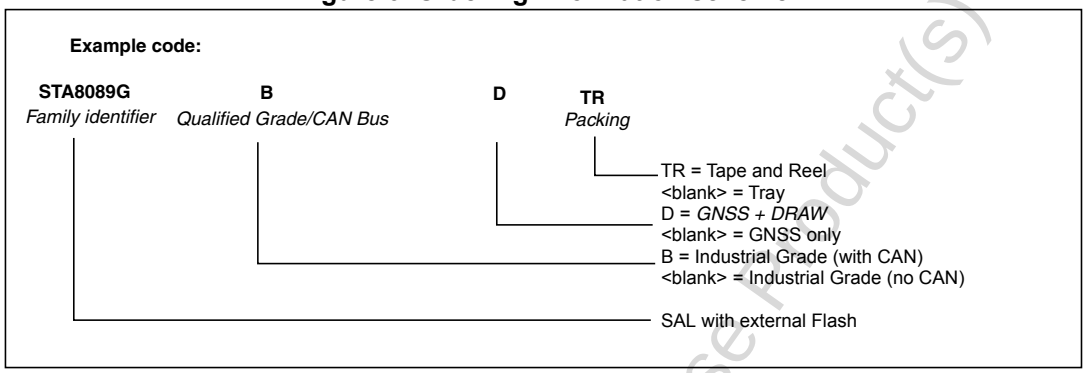
Symbol	Min.	Typ.	Max
Common dimensions			
A	0.80	0.85	0.90
A1	0	0.01	0.05
A2	0.60	0.65	0.70
A3		0.20 REF	
b	0.15	0.20	0.25
D		7.00 BSC	
D1		6.75 BSC	
D2	5.0	5.1	5.2
E		7.00 BSC	
E1		6.75 BSC	
E2	5.0	5.1	5.2
e		0.40 BSC	
θ	0°		12°
L	0.30	0.40	0.50
N		56	
Nd		14	
Ne		14	
P	0.24	0.42	0.60

Figure 5. VFQFPN56 7 x 7 mm package dimension



6 Ordering information

Figure 6. Ordering information scheme



7 Revision history

Table 25. Document revision history

Date	Revision	Changes
08-Jun-2017	1	Initial release.

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