











TRF370417

SLWS213A – JANUARY 2010 – REVISED NOVEMBER 2015

TRF370417 50-MHz to 6-GHz Quadrature Modulator

1 Features

- 76-dBc Single-Carrier WCDMA ACPR at –8 dBm Channel Power
- Low Noise Floor: -162.3 dBm/Hz at 2140 MHz
- OIP3 of 26.5 dBm at 2140 MHz
- P1dB of 12 dBm at 2140 MHz
- Carrier Feedthrough of -38 dBm at 2140 MHz
- Side-Band Suppression of -50 dBc at 2140 MHz
- Single Supply: 4.5-V-5.5-V Operation
- Silicon Germanium Technology
- 1.7-V CM at I, Q Baseband Inputs

2 Applications

- · Cellular Base Station Transceiver
- CDMA: IS95, UMTS, CDMA2000, TD-SCDMA
- TDMA: GSM, IS-136, EDGE/UWC-136
- Multicarrier GSM
- WiMAX: 802.16d/e
- 3GPP: LTE
- · Point-to-Point (P2P) Microwave
- Wideband Software-Defined Radio
- Public Safety: TETRA/APC025
- Communication-System Testers
- Cable Modem Termination System (CMTS)

3 Description

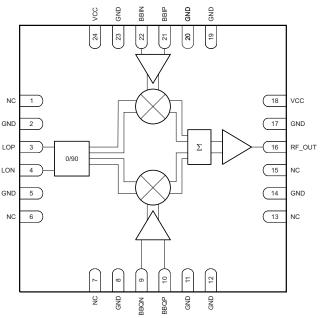
The TRF370417 is a low-noise direct quadrature modulator, capable of converting complex modulated signals from baseband or IF directly up to RF. The TRF370417 is a high-performance, superior-linearity device that operates at RF frequencies of 50 MHz through 6 GHz. The modulator is implemented as a double-balanced mixer. The RF output block consists of a differential to single-ended converter and an RF amplifier capable of driving a single-ended 50- Ω load without any need of external components. The TRF370417 requires a 1.7-V common-mode voltage for optimum linearity performance.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TRF370417	VQFN(24)	4.00 mm × 4.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Block Diagram



B0175-

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.



Table of Contents

1	Features 1		7.4 Device Functional Modes	16
2	Applications 1	8	Application and Implementation	18
3	Description 1		8.1 Application Information	18
4	Revision History2		8.2 Typical Application	20
5	Pin Configuration and Functions	9	Power Supply Recommendations	23
6	Specifications4	10	Layout	23
•	6.1 Absolute Maximum Ratings 4		10.1 Layout Guidelines	23
	6.2 ESD Ratings		10.2 Layout Example	23
	6.3 Recommended Operating Conditions	11	Device and Documentation Support	25
	6.4 Thermal Information		11.1 Device Support	25
	6.5 Electrical Characteristics 5		11.2 Documentation Support	26
	6.6 RF Output Parameters5		11.3 Community Resources	26
	6.7 Typical Characteristics 8		11.4 Trademarks	26
7	Detailed Description		11.5 Electrostatic Discharge Caution	26
	7.1 Overview		11.6 Glossary	26
	7.2 Functional Block Diagram	12	3,	0.0
	7.3 Feature Description		Information	26

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (January 2010) to Revision A

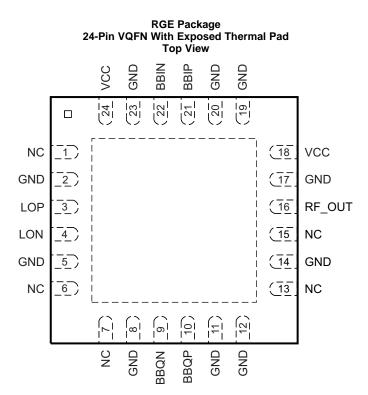
Page

Added ESD Ratings table, Feature Description section, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and

Product Folder Links: TRF370417



5 Pin Configuration and Functions



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.	1/0	DESCRIPTION
BBIN	22	I	In-phase negative input
BBIP	21	I	In-phase positive input
BBQN	9	1	Quadrature-phase negative input
BBQP	10	I	Quadrature-phase positive input
GND	2, 5, 8, 11, 12, 14, 17, 19, 20, 23	_	Ground
LON	4	I	Local oscillator (LO) negative input
LOP	3	I	Local oscillator (LO) positive input
NC	1, 6, 7, 13, 15	_	No connect
RF_OUT	16	0	RF output
VCC	18, 24	_	Power supply



6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
	Supply voltage range	-0.3	6	V
T_{J}	Operating virtual junction temperature range	-40	150	°C
T_A	Operating ambient temperature range	-40	85	°C
T _{stg}	Storage temperature range	-65	150	°C

⁽¹⁾ Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
		Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±75	
V _(ESD)	Electrostatic discharge	Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±75	V

⁽¹⁾ JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CC}	Power-supply voltage	4.5	5	5.5	V

6.4 Thermal Information

		TRF370417	
	THERMAL METRIC ⁽¹⁾	RGE (VQFN)	UNIT
		24 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance (High-K board, still air)	29.4	°C/W
R _{0JC(top)}	Junction-to-case (top) thermal resistance	18.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	14	°C/W
ΨЈТ	Junction-to-top characterization parameter	_	°C/W
ΨЈВ	Junction-to-board characterization parameter	_	°C/W
R ₀ JC(bot)	Junction-to-case (bottom) thermal resistance	_	°C/W

For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report, SPRA953.

Product Folder Links: TRF370417

Submit Documentation Feedback

Copyright © 2010–2015, Texas Instruments Incorporated

⁽²⁾ JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.



6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DC Para	ameters					
I _{CC}	Total supply current (1.7 V CM)	T _A = 25°C		205	245	mA
LO Inpu	ıt (50-Ω, Single-Ended)				<u>.</u>	
	LO frequency range		0.05		6	GHz
f_{LO}	LO input power		-5	0	12	dBm
	LO port return loss			15		dB
Baseba	nd Inputs		•		•	
V_{CM}	I and Q input dc common voltage			1.7		
BW	1-dB input frequency bandwidth			1		GHz
Z _{I(single} ended)	Input impedance, resistance			5		kΩ
	Input impedance, parallel capacitance			3		pF

6.6 RF Output Parameters

over recommended operating conditions, power supply = 5 V, $T_A = 25$ °C, $V_{CM} = 1.7$ V, $V_{inBB} = 98$ mVrms single-ended in quadrature, $f_{BB} = 50$ kHz (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN TYP I	MAX UNIT
f _{LO} = 7	0 MHz at 8 dBm			
G	Voltage gain	Output rms voltage over input I (or Q) rms voltage	-8	dB
P1dB	Output compression point		7.3	dBm
IP3	Output IP3	f _{BB} = 4.5, 5.5 MHz; P _{out} = -8 dBm per tone	22	dBm
IP2	Output IP2	f _{BB} = 4.5, 5.5 MHz; P _{out} = -8 dBm per tone	69	dBm
	Carrier feedthrough	Unadjusted	-46	dBm
	Sideband suppression	Unadjusted; f _{BB} = 4.5, 5.5 MHz	-27.5	dBc
f _{LO} = 4	00 MHz at 8 dBm			
G	Voltage gain	Output rms voltage over input I (or Q) rms voltage	-1.9	dB
P1dB	Output compression point		11	dBm
IP3	Output IP3	$f_{BB} = 4.5, 5.5 \text{ MHz}; P_{out} = -8 \text{ dBm per tone}$	24.5	dBm
IP2	Output IP2	f _{BB} = 4.5, 5.5 MHz; P _{out} = -8 dBm per tone	68	dBm
	Carrier feedthrough	Unadjusted	-38	dBm
	Sideband suppression	Unadjusted; f _{BB} = 4.5, 5.5 MHz	-40	dBc
f _{LO} = 9	45.6 MHz at 8 dBm			
G	Voltage gain	Output rms voltage over input I (or Q) rms voltage	-2.5	dB
P1dB	Output compression point		11	dBm
IP3	Output IP3	$f_{BB} = 4.5, 5.5 \text{ MHz}; P_{out} = -8 \text{ dBm per tone}$	25	dBm
IP2	Output IP2	$f_{BB} = 4.5, 5.5 \text{ MHz}; P_{out} = -8 \text{ dBm per tone}$	65	dBm
	Carrier feedthrough	Unadjusted	-40	dBm
	Sideband suppression	Unadjusted; f _{BB} = 4.5, 5.5 MHz	-42	dBc
	Output return loss		9	dB
	Output noise floor	≥13 MHz offset from f _{LO} ; P _{out} = −5 dBm	-161.2	dBm/Hz
f _{LO} = 1	800 MHz at 8 dBm			
G	Voltage gain	Output rms voltage over input I (or Q) rms voltage	-2.5	dB
P1dB	Output compression point		12	dBm
IP3	Output IP3	f _{BB} = 4.5, 5.5 MHz; P _{out} = -8 dBm per tone	26	dBm
IP2	Output IP2	$f_{BB} = 4.5$, 5.5 MHz; $P_{out} = -8$ dBm per tone	60	dBm
	Carrier feedthrough	Unadjusted	-40	dBm
	Sideband suppression	Unadjusted; f _{BB} = 4.5, 5.5 MHz	-50	dBc

Product Folder Links: TRF370417

Copyright © 2010–2015, Texas Instruments Incorporated



RF Output Parameters (continued)

over recommended operating conditions, power supply = 5 V, $T_A = 25$ °C, $V_{CM} = 1.7$ V, $V_{inBB} = 98$ mVrms single-ended in quadrature, $f_{BB} = 50$ kHz (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN TYP	MAX	UNIT
	Output return loss		8	·	dB
	Output noise floor	≥13 MHz offset from f _{LO} ; P _{out} = −5 dBm	-161.5		dBm/Hz
f _{LO} = 19	960 MHz at 8 dBm				
G	Voltage gain	Output rms voltage over input I (or Q) rms voltage	-2.5		dB
P1dB	Output compression point		12		dBm
IP3	Output IP3	$f_{BB} = 4.5$, 5.5 MHz; $P_{out} = -8$ dBm per tone	26.5		dBm
IP2	Output IP2	$f_{BB} = 4.5$, 5.5 MHz; $P_{out} = -8$ dBm per tone	60		dBm
	Carrier feedthrough	Unadjusted	-38		dBm
	Sideband suppression	Unadjusted; f _{BB} = 4.5, 5.5 MHz	– 50		dBc
	Output return loss		8		dB
	Output noise floor	≥13 MHz offset from f _{LO} ; P _{out} = −5 dBm	-162		dBm/Hz
EVM	Error vector magnitude (rms)	1 EDGE signal, P _{out} = -5 dBm ⁽¹⁾	0.43%		
		1 WCDMA signal; P _{out} = -8 dBm ⁽²⁾	-76		
ACPR	Adjacent-channel power ratio	1 WCDMA signal; P _{out} = -8 dBm ⁽³⁾	-74		40.4
		2 WCDMA signals; P _{out} = -11 dBm per carrier ⁽³⁾	-68		dBc
		4 WCDMA signals; P _{out} = -14 dBm per carrier ⁽³⁾	-67		
ACPR	Alternate-channel power ratio	1 WCDMA signal; P _{out} = -8 dBm ⁽²⁾	-80		dBc
		1 WCDMA signal; P _{out} = -8 dBm ⁽³⁾	-78		
		2 WCDMA signals; P _{out} = -11 dBm per carrier ⁽³⁾	-72		
		4 WCDMA signals; P _{out} = -14 dBm per carrier ⁽³⁾	-69		
f _{LO} = 2	140 MHz at 8 dBm				
G	Voltage gain	Output rms voltage over input I (or Q) rms voltage	-2.4		dB
P1dB	Output compression point		12		dBm
IP3	Output IP3	$f_{BB} = 4.5$, 5.5 MHz; $P_{out} = -8$ dBm per tone	26.5		dBm
IP2	Output IP2	$f_{BB} = 4.5, 5.5 \text{ MHz}; P_{out} = -8 \text{ dBm per tone}$	66		dBm
	Carrier feedthrough	Unadjusted	-38		dBm
	Sideband suppression	Unadjusted; f _{BB} = 4.5, 5.5 MHz	-50		dBc
	Output return loss		8.5		dB
	Output noise floor	≥13 MHz offset from f _{LO} ; P _{out} = −5 dBm	-162.3		dBm/Hz
		1 WCDMA signal; P _{out} = -8 dBm ⁽²⁾	-76		
	Adiacont channel newer ratio	1 WCDMA signal; P _{out} = -8 dBm ⁽³⁾	-72		dD.o
	Adjacent-channel power ratio	2 WCDMA signal; P _{out} = -11 dBm per carrier ⁽³⁾	-67		dBc
٨٥٥٥		4 WCDMA signals; P _{out} = -14 dBm per carrier ⁽³⁾	-66		
ACPR		1 WCDMA signal; P _{out} = -8 dBm ⁽²⁾	-80		
	Allowed to the second second	1 WCDMA signal; P _{out} = -8 dBm ⁽³⁾	-78		ID -
	Alternate-channel power ratio	2 WCDMA signal; P _{out} = -11 dBm ⁽³⁾	-74		dBc
		4 WCDMA signals; P _{out} = -14 dBm per carrier ⁽³⁾	-68		

⁽¹⁾ The contribution from the source of about 0.28% is not de-embedded from the measurement.

Submit Documentation Feedback

Copyright © 2010–2015, Texas Instruments Incorporated

⁽²⁾ Measured with DAC5687 as source generator; with 2.5 MHz LPF.

⁽³⁾ Measured with DAC5687 as source generator; no external BB filters are used.



RF Output Parameters (continued)

over recommended operating conditions, power supply = 5 V, $T_A = 25$ °C, $V_{CM} = 1.7$ V, $V_{inBB} = 98$ mVrms single-ended in quadrature, $f_{BB} = 50$ kHz (unless otherwise noted)

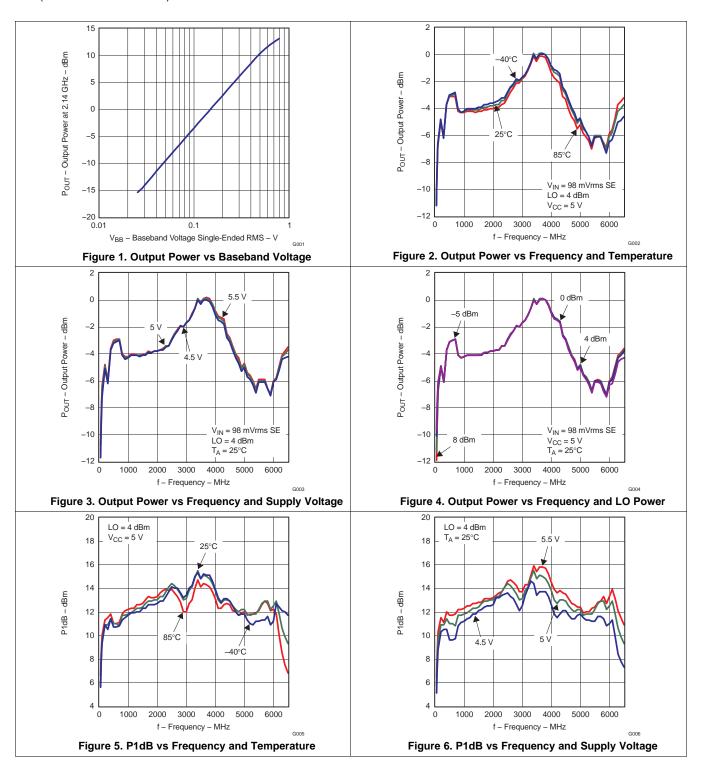
	PARAMETER	TEST CONDITIONS	MIN TYP MAX	UNIT
f _{LO} = 2	500 MHz at 8 dBm			
G	Voltage gain	Output rms voltage over input I (or Q) rms voltage	-1.6	dB
P1dB	Output compression point		13	dBm
IP3	Output IP3	$f_{BB} = 4.5$, 5.5 MHz; $P_{out} = -8$ dBm per tone	29	dBm
IP2	Output IP2	$f_{BB} = 4.5$, 5.5 MHz; $P_{out} = -8$ dBm per tone	65	dBm
	Carrier feedthrough	Unadjusted	-37	dBm
	Sideband suppression	Unadjusted; f _{BB} = 4.5, 5.5 MHz	-47	dBc
E) /A 4	F	WiMAX 5-MHz carrier, P _{out} = -8 dBm ⁽⁴⁾	-47	dB
EVM	Error vector magnitude (rms)	WiMAX 5-MHz carrier, P _{out} = 0 dBm ⁽⁴⁾	–45	dB
f _{LO} = 3	500 MHz at 8 dBm			
G	Voltage gain	Output rms voltage over input I (or Q) rms voltage	0.6	dB
P1dB	Output compression point		13.5	dBm
IP3	Output IP3	f _{BB} = 4.5, 5.5 MHz	25	dBm
IP2	Output IP2	f _{BB} = 4.5, 5.5 MHz	65	dBm
	Carrier feedthrough	Unadjusted	- 35	dBm
	Sideband suppression	Unadjusted; f _{BB} = 4.5, 5.5 MHz	-36	dBc
E\ / \ A		WiMAX 5-MHz carrier, P _{out} = -8 dBm ⁽⁴⁾	–47	dB
EVM	Error vector magnitude (rms)	WiMAX 5-MHz carrier, P _{out} = 0 dBm ⁽⁴⁾	-43	dB
f _{LO} = 4	000 MHz at 8 dBm			
G	Voltage gain	Output rms voltage over input I (or Q) rms voltage	0.2	dB
P1dB	Output compression point		12	dBm
IP3	Output IP3	f _{BB} = 4.5, 5.5 MHz	22.5	dBm
IP2	Output IP2	f _{BB} = 4.5, 5.5 MHz	60	dBm
	Carrier feedthrough	Unadjusted	-36	dBm
	Sideband suppression	Unadjusted; f _{BB} = 4.5, 5.5 MHz	-36	dBc
f _{LO} = 5	800 MHz at 4 dBm			
G	Voltage gain	Output rms voltage over input I (or Q) rms voltage	-5.5	dB
P1dB	Output compression point		12.9	dBm
IP3	Output IP3	f _{BB} = 4.5, 5.5 MHz	25	dBm
IP2	Output IP2	f _{BB} = 4.5, 5.5 MHz	55	dBm
	Carrier feedthrough	Unadjusted	-31	dBm
	Sideband suppression	Unadjusted; f _{BB} = 4.5, 5.5 MHz	-36	dBc
EVM	Error-vector magnitude	WiMAX 5-MHz carrier, P _{out} = -12 dBm ⁽⁴⁾	-40	dB

⁽⁴⁾ Sideband suppression optimized with LO drive level; EVM contribution from instrument is not accounted for.



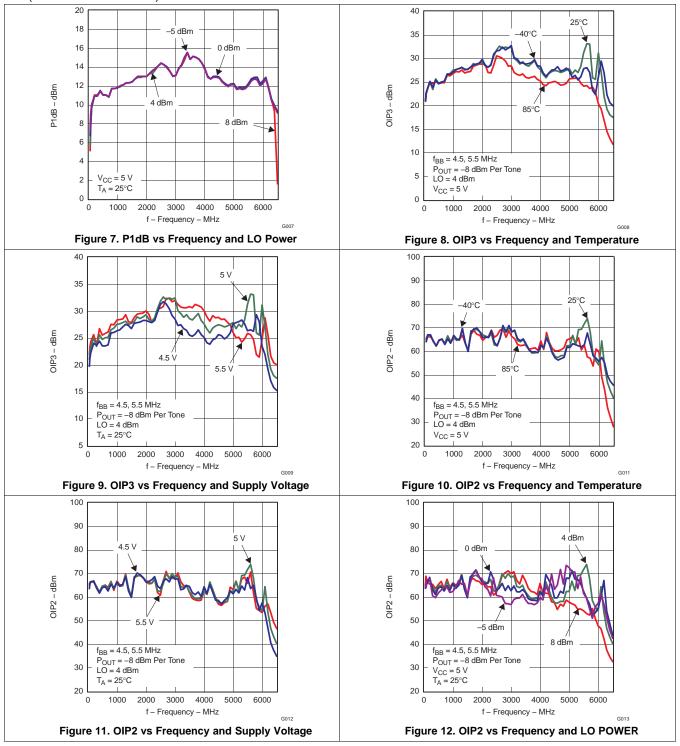
6.7 Typical Characteristics

 $V_{CM} = 1.7 \text{ V}$, $V_{inBB} = 98 \text{ mVrms}$ single-ended sine wave in quadrature, $V_{CC} = 5 \text{ V}$, LO power = 4 dBm (single-ended), $f_{BB} = 50 \text{ kHz}$ (unless otherwise noted).





 $V_{CM} = 1.7 \text{ V}$, $V_{inBB} = 98 \text{ mVrms}$ single-ended sine wave in quadrature, $V_{CC} = 5 \text{ V}$, LO power = 4 dBm (single-ended), $f_{BB} = 50 \text{ kHz}$ (unless otherwise noted).



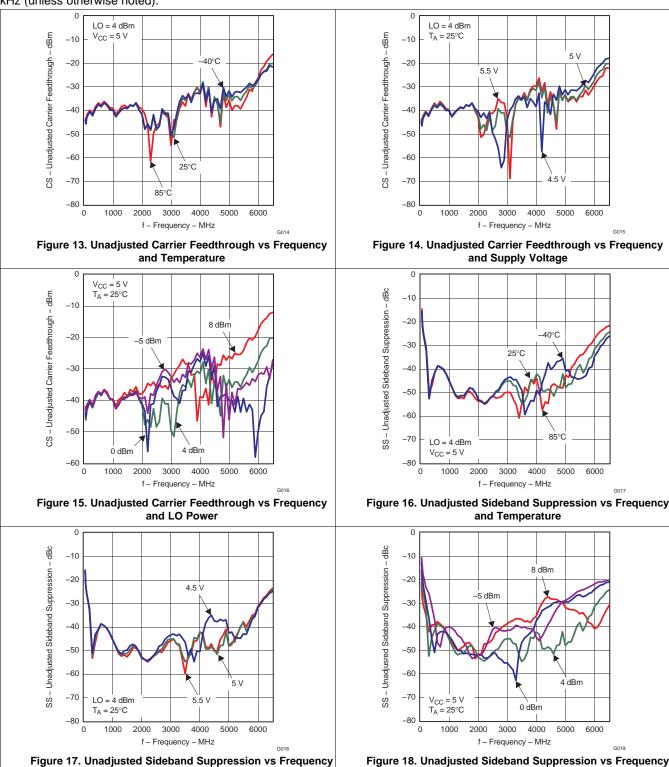
Product Folder Links: TRF370417

Copyright © 2010–2015, Texas Instruments Incorporated

TEXAS INSTRUMENTS

Typical Characteristics (continued)

 $V_{CM} = 1.7 \text{ V}$, $V_{inBB} = 98 \text{ mVrms}$ single-ended sine wave in quadrature, $V_{CC} = 5 \text{ V}$, LO power = 4 dBm (single-ended), $f_{BB} = 50 \text{ kHz}$ (unless otherwise noted).



Product Folder Links: TRF370417

Submit Documentation Feedback

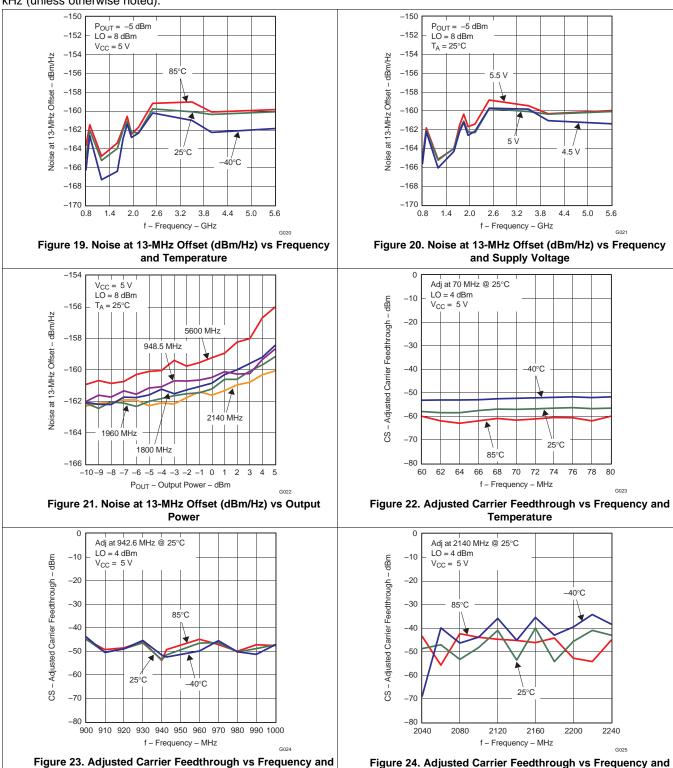
and Supply Voltage

Copyright © 2010–2015, Texas Instruments Incorporated

and LO Power



 $V_{CM} = 1.7 \text{ V}$, $V_{inBB} = 98 \text{ mVrms}$ single-ended sine wave in quadrature, $V_{CC} = 5 \text{ V}$, LO power = 4 dBm (single-ended), $f_{BB} = 50 \text{ kHz}$ (unless otherwise noted).



Product Folder Links: TRF370417

Copyright © 2010–2015, Texas Instruments Incorporated

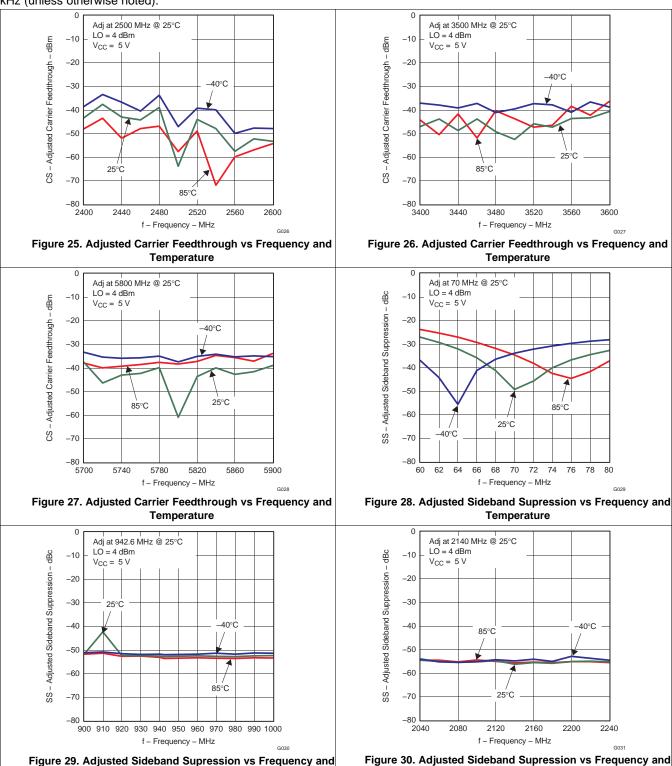
Temperature

Submit Documentation Feedback

Temperature



 $V_{CM} = 1.7 \text{ V}$, $V_{inBB} = 98 \text{ mVrms}$ single-ended sine wave in quadrature, $V_{CC} = 5 \text{ V}$, LO power = 4 dBm (single-ended), $f_{BB} = 50 \text{ kHz}$ (unless otherwise noted).



Product Folder Links: TRF370417

Submit Documentation Feedback

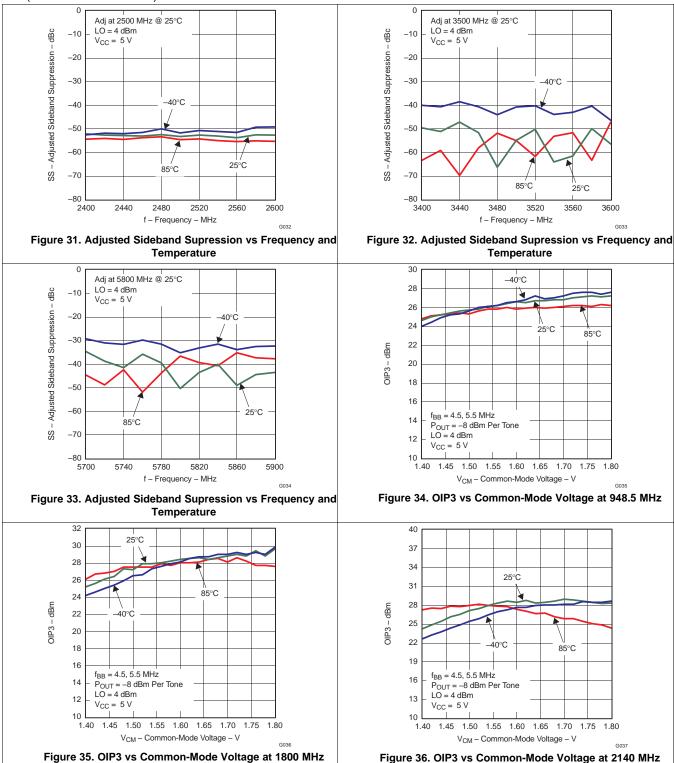
Copyright © 2010–2015, Texas Instruments Incorporated

Temperature

Temperature



 $V_{CM} = 1.7 \text{ V}$, $V_{inBB} = 98 \text{ mVrms}$ single-ended sine wave in quadrature, $V_{CC} = 5 \text{ V}$, LO power = 4 dBm (single-ended), $f_{BB} = 50 \text{ kHz}$ (unless otherwise noted).

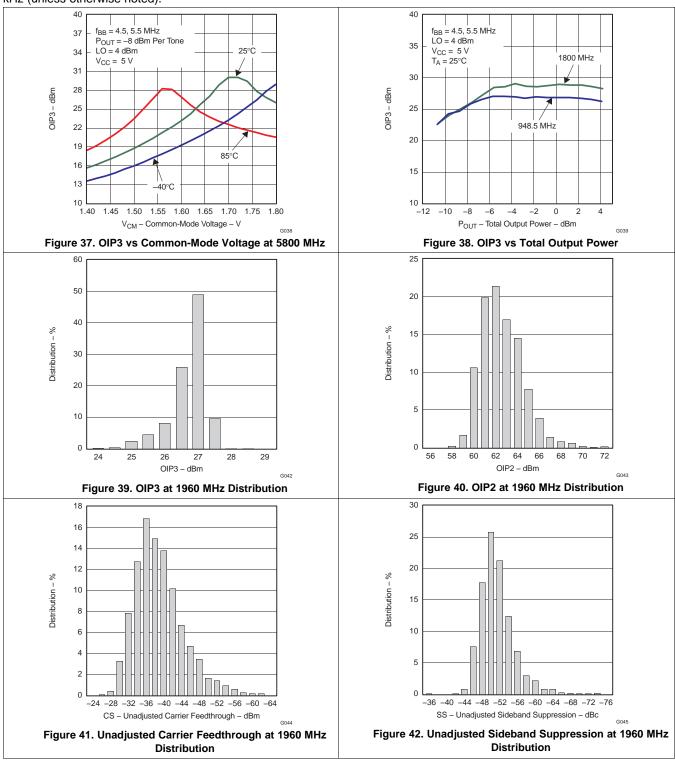


Product Folder Links: TRF370417

TEXAS INSTRUMENTS

Typical Characteristics (continued)

 V_{CM} = 1.7 V, V_{inBB} = 98 mVrms single-ended sine wave in quadrature, V_{CC} = 5 V, LO power = 4 dBm (single-ended), f_{BB} = 50 kHz (unless otherwise noted).



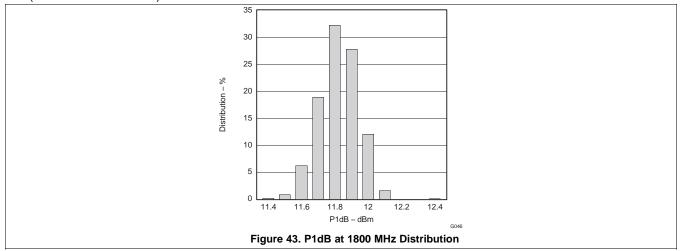
Submit Documentation Feedback

Copyright © 2010–2015, Texas Instruments Incorporated

Downloaded from Arrow.com.



 V_{CM} = 1.7 V, V_{inBB} = 98 mVrms single-ended sine wave in quadrature, V_{CC} = 5 V, LO power = 4 dBm (single-ended), f_{BB} = 50 kHz (unless otherwise noted).



Product Folder Links: TRF370417

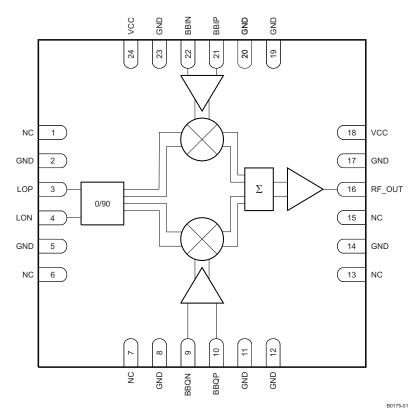


7 Detailed Description

7.1 Overview

TRF370417 is a low-noise direct quadrature modulator with high linearity, capable of converting complex modulated signals from baseband or IF directly to RF. With high-performance and superior-linearity, the TRF370417 is an ideal device to up-convert to RF frequencies from 50-MHz through 6-GHz. The baseband inputs can support an input bandwidth up to 1-GHz. The modulator is implemented as a double-balanced mixer. The RF output block contains a differential to single-ended converter to drive a 50-ohm load without the need for external matching components. The baseband input common-mode voltage is set at 1.7-V for optimum linearity performance.

7.2 Functional Block Diagram



NOTE: NC = No connection

7.3 Feature Description

TRF370417 supports an I/Q baseband input bandwidth of 1-GHz. With this bandwidth capability the input signal can be centered at a high IF frequency to provide frequency separation from unwanted carrier feed-through or sideband image. Utilizing the full baseband bandwidth yields an RF output bandwidth up to 2-GHz.

7.4 Device Functional Modes

7.4.1 Baseband Common-Mode Voltage

TRF370417 input baseband pins operate around a common-mode voltage of 1.7-V. Variation around this common-mode is possible but best linearity performance is generally achieved when kept at nominal voltage.

Submit Documentation Feedback

Product Folder Links: TRF370417

Copyright © 2010–2015, Texas Instruments Incorporated



Device Functional Modes (continued)

7.4.2 LO Drive Level

The LO drive level is nominally specified at 4-dBm. The device can accept a large range of LO drive level. A higher drive level generally provides better output noise performance and some linearity improvement. There is some trade-off between carrier feed-through and sideband suppression performance that is dependent on frequency and drive level. The LO drive level of 4-dB is deemed a good balance between those two parameters across frequency.



8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Basic Connections

- See Figure 44 for proper connection of the TRF3704 modulator.
- Connect a single power supply (4.5 V–5.5 V) to pins 18 and 24. These pins should be decoupled as shown on pins 4, 5, 6, and 7.
- Connect pins 2, 5, 8, 11, 12, 14, 17, 19, 20, and 23 to GND.
- Connect a single-ended LO source of desired frequency to LOP (amplitude between -5 dBm and 12 dBm).
 This should be ac-coupled through a 100-pF capacitor.
- Terminate the ac-coupled LON with 50 Ω to GND.
- Connect a baseband signal to pins 21 = I, $22 = \overline{I}$, 10 = Q, and $9 = \overline{Q}$.
- The differential baseband inputs should be set to the proper common-mode voltage of 1.7 V.
- RF_OUT, pin 16, can be fed to a spectrum analyzer set to the desired frequency, LO ± baseband signal. This pin should also be ac-coupled through a 100-pF capacitor.
- · All NC pins can be left floating.

8.1.1.1 ESD Sensitivity

RF devices may be extremely sensitive to electrostatic discharge (ESD). To prevent damage from ESD, devices should be stored and handled in a way that prevents the build-up of electrostatic voltages that exceed the rated level. Rated ESD levels should also not be exceeded while the device is installed on a printed circuit board (PCB). Follow these guidelines for optimal ESD protection:

- Low ESD performance is not uncommon in RF ICs; see the *Absolute Maximum Ratings* table. Therefore, customers' ESD precautions should be consistent with these ratings.
- The device should be robust once assembled onto the PCB *unless* external inputs (connectors, etc.) directly connect the device pins to off-board circuits.

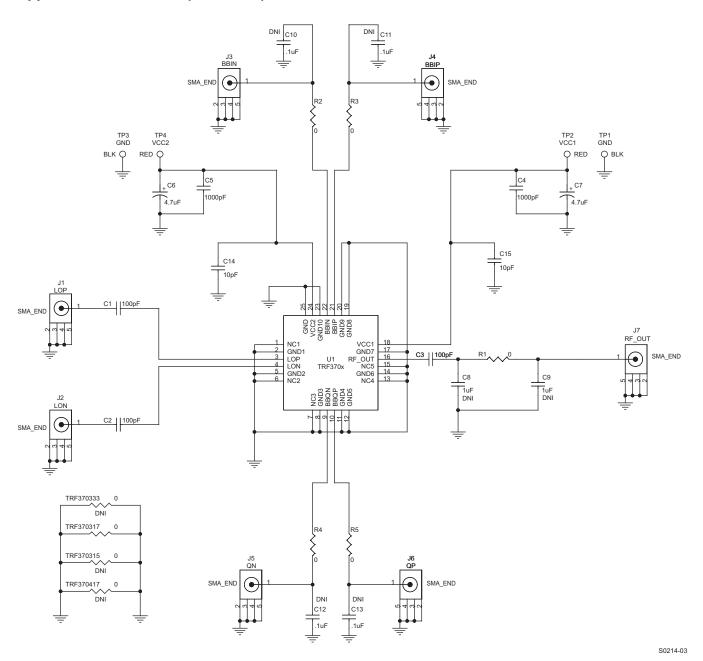
Product Folder Links: TRF370417

Submit Documentation Feedback

Copyright © 2010–2015, Texas Instruments Incorporated



Application Information (continued)



NOTE: DNI = Do not install.

Figure 44. TRF3704 EVM Schematic

8.1.2 GSM Applications

Downloaded from Arrow.com.

The TRF370417 is suited for GSM and multicarrier GSM applications because of its high linearity and low noise level over the entire recommended operating range. It also has excellent EVM performance, which makes it ideal for the stringent GSM/EDGE applications.



Application Information (continued)

8.1.3 WCDMA Applications

The TRF370417 is also optimized for WCDMA applications where both adjacent-channel power ratio (ACPR) and noise density are critically important. Using Texas instruments' DAC568X series of high-performance digital-to-analog converters as depicted in Figure 44, excellent ACPR levels were measured with one-, two-, and four-WCDMA carriers. See *Electrical Characteristics*, $f_{LO} = 1960$ MHz and $f_{LO} = 2140$ MHz for exact ACPR values.

8.2 Typical Application

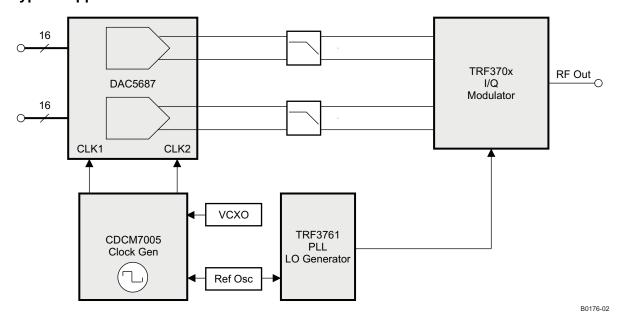


Figure 45. Typical Transmit Setup Block Diagram

8.2.1 Design Requirements

Table 1 lists the requirements and limitations for pin termination.

Table 1. Pin Termination Requirements and Limitations

NAME	PIN NO.	DESCRIPTION
BBQM	9	Baseband in-quadrature input: negative terminal. Optimal linearity is obtained if VCM is 1.7-V. Normally terminated in 50 Ω
BBQP	10	Baseband in-quadrature input: positive terminal. Optimal linearity is obtained if VCM is 1.7-V. Normally terminated in 50 Ω
BBIP	21	Baseband in-phase input: positive terminal. Optimal linearity is obtained if VCM is 1.7-V. Normally terminated in 50 Ω
BBIM	22	Baseband in-phase input: negative terminal. Optimal linearity is obtained if VCM is 1.7-V. Normally terminated in 50 Ω
LOP	3	Local oscillator input: positive terminal. This is preferred port when driving single ended. Normally AC coupled and terminated in 50 Ω
LOM	4	Local oscillator input: negative terminal. When driving LO single-ended, normally AC coupled and terminated in 50 Ω .
RFOUT	16	RF output. Normally AC coupled. Recommend to terminate with broadband 50- Ω load.
VCC	18, 24	5.0-V power supply. Can be tied together and sourced from a single clean supply. Each pin should be properly RF bypassed.

Product Folder Links: TRF370417

Submit Documentation Feedback

Copyright © 2010–2015, Texas Instruments Incorporated



8.2.2 Detailed Design Procedure

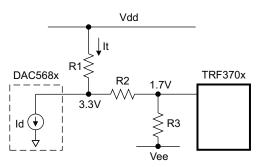
Table 2. Bill of Materials for TRF370x EVM

ITEM NUMBER	QUANTITY	REFERENCE DESIGNATOR	VALUE	PCB FOOTPRINT	MFR. NAME	MFT. PART NUMBER	NOTE				
1	3	C1, C2, C3	100 pF	0402	PANASONIC	ECJ-0EC1H101J					
2	2	C4, C5	1000 pF	0402	PANASONIC	ECJ-0VC1H102J					
3	2	C6, C7	4.7 μF	TANT_A	ANT_A KERMET						
4	0	C8, C9	1 μF	0402	PANASONIC	ECJ- 0EC1H010C_DNI	DNI				
5	0	C10, C11, C12, C13	0.1 μF	0402	PANASONIC	ECJ- 0EB1A104K_DNI	DNI				
6	2	C14, C15	10 pF	0402	MURATA	GRM1555C1H100JZ0 1D					
7	7	J1, J2, J3, J4, J5, J6, J7	LOP	SMA_SMEL_250x215	JOHNSON COMPONENTS	142-0711-821					
8	2	R1	0	0402	PANASONIC	ERJ-2GE0R00	OR EQUIVALENT				
9	4	R2, R3, R4, R5	0	0402	PANASONIC	ERJ-2GE0R00	OR EQUIVALENT				
			TRF370333	QFN_24_163x163_ 0p50mm	TI	TRF370333	For TRF370333 EVM, TI supplied				
10	4	U1	TRF370317	QFN_24_163x163_ 0p50mm		TRF370317	For TRF370317 EVM, TI supplied				
10	1	'	ı	1	ı	01	TRF370315	QFN_24_163x163_ 0p50mm	TI	TRF370315	For TRF370315 EVM, TI supplied
			TRF370417	QFN_24_163x163_ 0p50mm	ТІ	TRF370417	For TRF370417 EVM, TI supplied				
11	2	TP1, TP3	BLK	TP_THVT_100_RND	KEYSTONE	5001K					
12	2	TP2, TP4	RED	TP_THVT_100_RND	KEYSTONE	5000K					

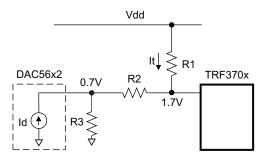
8.2.2.1 DAC-to-Modulator Interface Network

For optimum linearity and dynamic range, the digital-to-analog converter (DAC) can interface directly with the modulator; however, the common-mode voltage of each device must be maintained. A passive interface circuit is used to transform the common-mode voltage of the DAC to the desired set-point of the modulator. The passive circuit invariably introduces some insertion loss between the two devices. In general, it is desirable to keep the insertion loss as low as possible to achieve the best dynamic range. Figure 46 shows the passive interconnect circuit for two different topologies. One topology is used when the DAC (such as the DAC568x) common-mode is larger than the modulator. The voltage $V_{\rm ee}$ is nominally set to ground, but can be set to a negative voltage to reduce the insertion loss of the network. The second topology is used when the DAC (such as the DAC56x2) common-mode is smaller than the modulator. Note that this passive interconnect circuit is duplicated for each of the differential I/Q branches.





Topology 1: DAC Vcm > TRF370x Vcm



Topology 2: DAC Vcm < TRF370x Vcm

S0338-01

Figure 46. Passive DAC-to-Modulator Interface Network

Table 3. DAC-to-Modulator Interface Network Values

	ТОРО	LOGY 1	TODOL OOV 2		
	WITH VEE = 0 V	WITH VEE = 5 V	TOPOLOGY 2		
DAC Vcm [V]	3.3	3.3	0.7		
TRF370x Vcm [V]	1.7	1.7	1.7		
Vdd [V]	5	5	5		
Vee [V]	Gnd	-5	N/A		
R1 [Ω]	66	56	960		
R2 [Ω]	100	80	290		
R3 [Ω]	108	336	52		
Insertion loss [dB]	5.8	1.9	2.3		

Product Folder Links: TRF370417

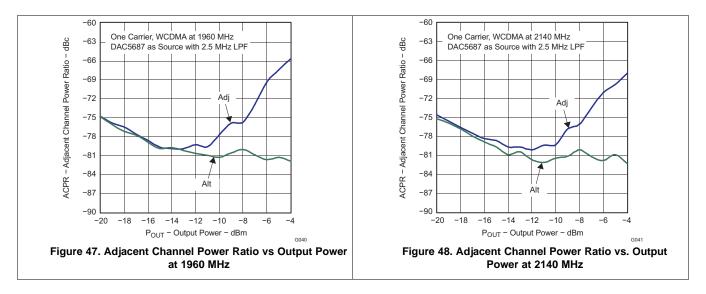
Submit Documentation Feedback

Copyright © 2010–2015, Texas Instruments Incorporated

Downloaded from Arrow.com.



8.2.3 Application Curves



9 Power Supply Recommendations

The TRF370417 is powered by supplying a nominal 5 V to pins 18 and 24. These supplies can be tied together and sourced from a single clean supply. Proper RF bypassing should be placed close to each power supply pin. Ground pin connections should have at least one ground via close to each ground pin to minimize ground inductance. The thermal pad must be tied to ground, preferably with the recommended ground via pattern to provide a good thermal conduction path to the alternate side of the board and to provide a good RF ground for the device. (Refer to *Layout Guidelines* for additional information.)

10 Layout

10.1 Layout Guidelines

The TRF370417 device is fitted with a ground slug on the back of the package that must be soldered to the printed circuit board (PCB) ground with adequate ground vias to ensure a good thermal and electrical connection. The recommended via pattern and ground pad dimensions are shown in Figure 76. The recommended via diameter is 10 mils (0.10 in or 0.25 mm). The ground pins of the device can be directly tied to the ground slug pad for a low-inductance path to ground. Additional ground vias may be added if space allows. Decoupling capacitors at each of the supply pins are strongly recommended. The value of these capacitors should be chosen to provide a low-impedance RF path to ground at the frequency of operation. Typically, the value of these capacitors is approximately 10 pF or lower. The device exhibits symmetry with respect to the quadrature input paths. TI recommends that the PCB layout maintain this symmetry to ensure that the quadrature balance of the device is not impaired. The I/Q input traces should be routed as differential pairs and the respective lengths all kept equal to each other. On the RF traces, maintain proper trace widths to keep the characteristic impedance of the RF traces at a nominal $50~\Omega$.

10.2 Layout Example

Figure 49 shows the top view of the TRF3704 EVM board.



Layout Example (continued)

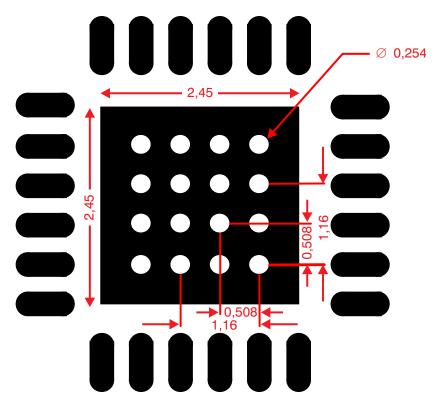


Figure 49. PCB Via Ground Layout Guide



11 Device and Documentation Support

11.1 Device Support

11.1.1 Device Nomenclature

Adjusted (Optimized) Carrier Feedthrough This differs from the unadjusted suppression number in that the baseband input dc offsets are iteratively adjusted around their theoretical value of VCM to yield the maximum suppression of the LO component in the output spectrum. This is measured in dBm.

Adjusted (Optimized) Sideband Suppression This differs from the unadjusted sideband suppression in that the gain and phase of the baseband inputs are iteratively adjusted around their theoretical values to maximize the amount of sideband suppression. This is measured in dBc.

Suppressions Over Temperature This specification assumes that the user has gone though the optimization process for the suppression in question, and set the optimal settings for the I, Q inputs. This specification then measures the suppression when temperature conditions change after the initial calibration is done.

Figure 50 shows a simulated output and illustrates the respective definitions of various terms used in this data sheet.

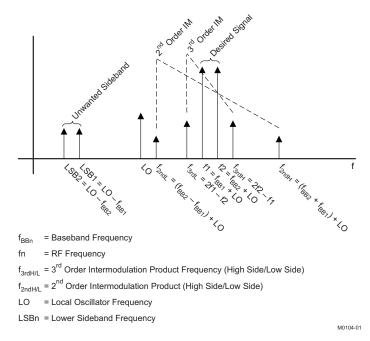


Figure 50. Graphical Illustration of Common Terms

Unadjusted Carrier Feedthrough This specification measures the amount by which the local oscillator component is suppressed in the output spectrum of the modulator. If the common-mode voltage at each of the baseband inputs is exactly the same and there was no dc imbalance introduced by the modulator, the LO component would be naturally suppressed. DC offset imbalances in the device allow some of the LO component to feed through to the output. Because this phenomenon is independent of the RF output power and the injected LO input power, the parameter is expressed in absolute power, dBm.

Unadjusted Sideband Suppression This specification measures the amount by which the unwanted sideband of the input signal is suppressed in the output of the modulator, relative to the wanted sideband. If the amplitude and phase within the I and Q branch of the modulator were perfectly matched, the unwanted sideband (or image) would be naturally suppressed. Amplitude and phase imbalance in the I and Q branches results in the increase of the unwanted sideband. This parameter is measured in dBc relative to the desired sideband.

Product Folder Links: TRF370417

Copyright © 2010–2015, Texas Instruments Incorporated



11.2 Documentation Support

11.2.1 Related Documentation

For related documentation, see the documents that follow:

- TRF370x User's Guide
- TRF370417: Optimizing OIP3 Performance at Local Oscillator (LO) Frequencies Beyond 4.5 GHz
- High Bandwidth, High Frequency Transmitter Reference Design

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community TI's Engineer-to-Engineer (E2E) Community. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

E2E is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — TI Glossary.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

Submit Documentation Feedback

Copyright © 2010–2015, Texas Instruments Incorporated

www.ti.com 7-May-2025

PACKAGING INFORMATION

Orderable part number	Status	Material type	Package Pins	Package qty Carrier	RoHS	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
						(4)	(5)		
TRF370417IRGER	Active	Production	VQFN (RGE) 24	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TRF37 0417
TRF370417IRGET	Active	Production	VQFN (RGE) 24	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TRF37 0417

⁽¹⁾ Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

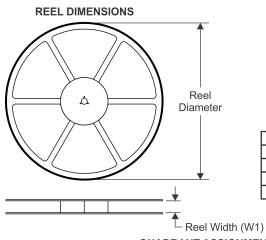
⁽⁵⁾ MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

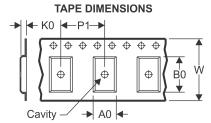
⁽⁶⁾ Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

PACKAGE MATERIALS INFORMATION

www.ti.com 1-Aug-2018

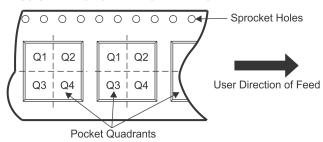
TAPE AND REEL INFORMATION





	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



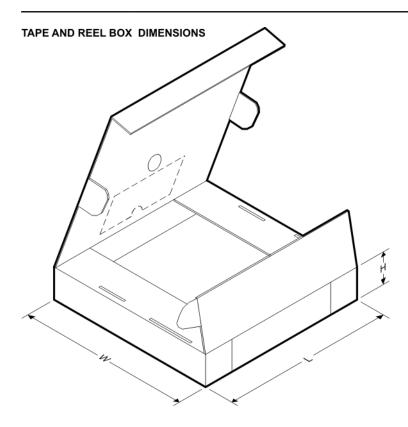
*All dimensions are nominal

	ill diffoliorio di o fiorittidi												
	Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ı	TRF370417IRGER	VQFN	RGE	24	3000	330.0	12.4	4.3	4.3	1.5	8.0	12.0	Q1
ı	TRF370417IRGET	VQFN	RGE	24	250	330.0	12.4	4.3	4.3	1.5	8.0	12.0	Q1



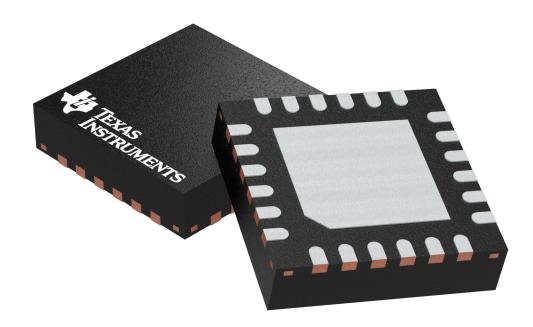
PACKAGE MATERIALS INFORMATION

www.ti.com 1-Aug-2018



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TRF370417IRGER	VQFN	RGE	24	3000	367.0	367.0	38.0
TRF370417IRGET	VQFN	RGE	24	250	367.0	367.0	38.0

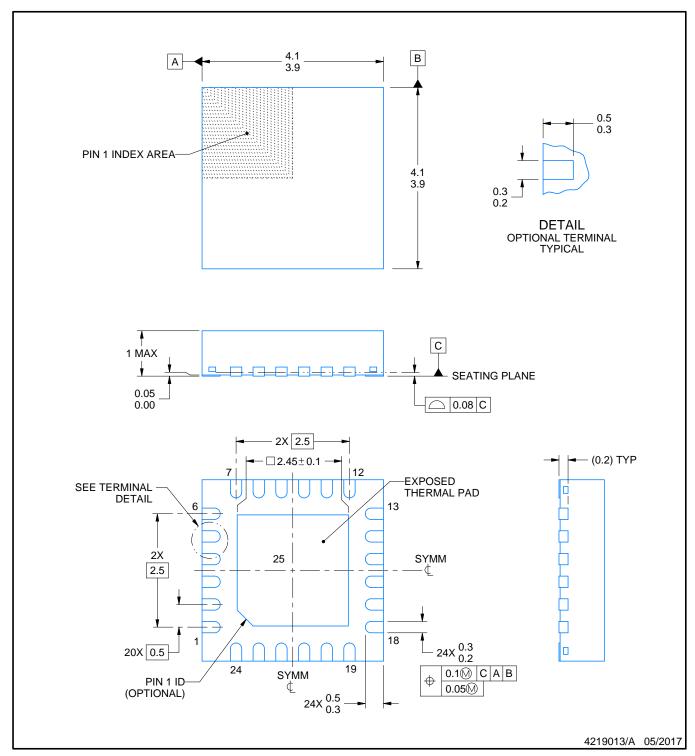


Images above are just a representation of the package family, actual package may vary. Refer to the product data sheet for package details.

4204104/H



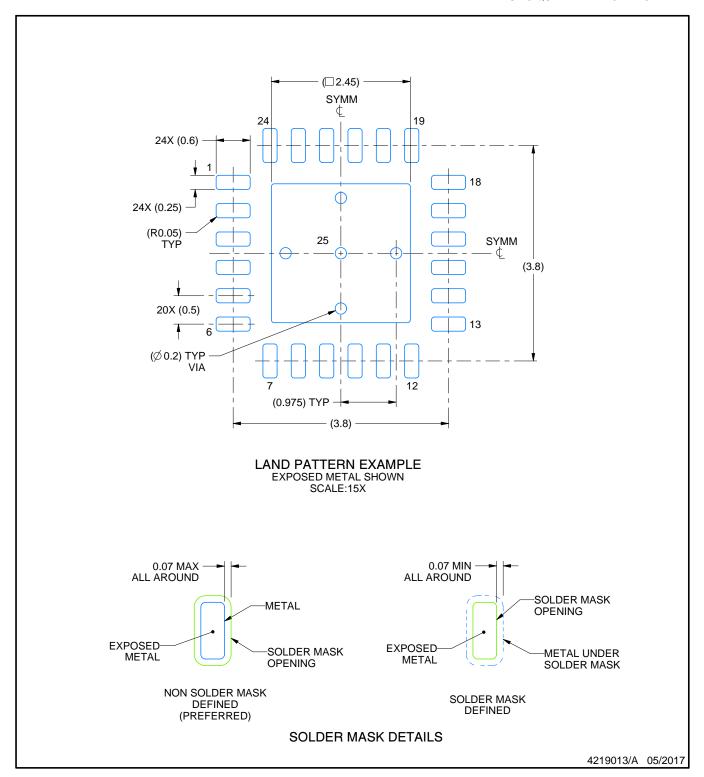




NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
 2. This drawing is subject to change without notice.
- 3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

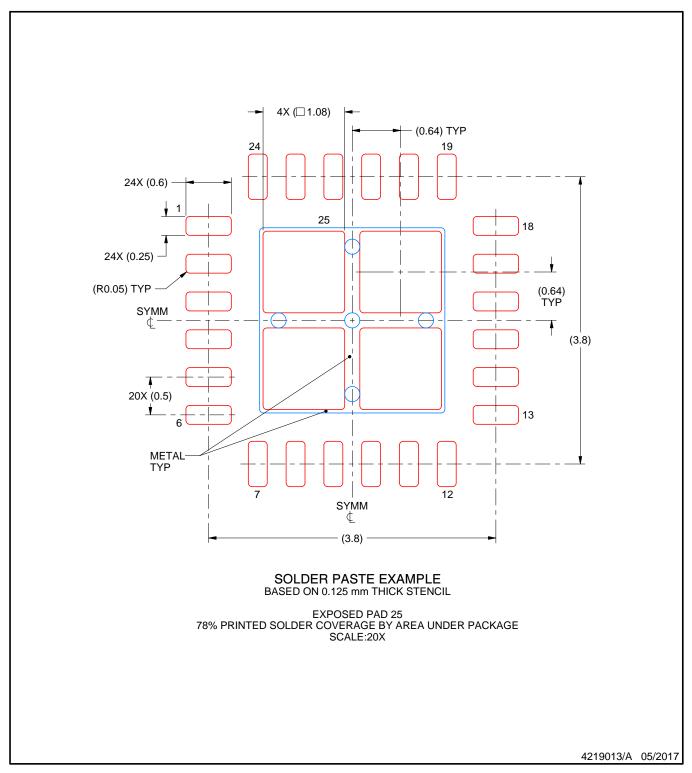




NOTES: (continued)

- 4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
- 5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.





NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265 Copyright © 2025. Texas Instruments Incorporated