



## High-Voltage Switchmode Controller

### FEATURES

- 9- to 80-V Input Range
- Current-Mode Control
- High-Speed, Source-Sink Output Drive
- High Efficiency Operation (> 80%)
- Internal Start-Up Circuit
- Internal Oscillator (1 MHz)
- $\overline{\text{SHUTDOWN}}$  and RESET

### DESCRIPTION

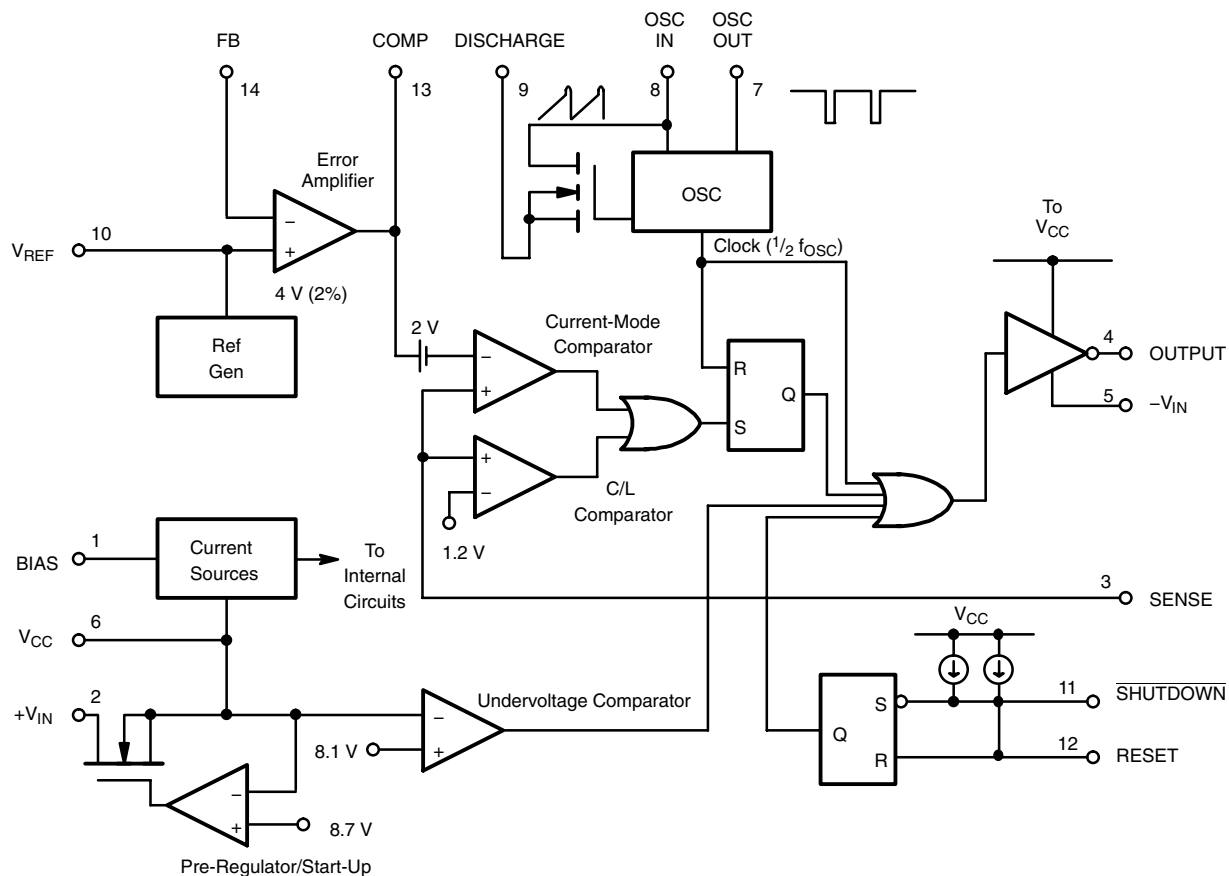
The Si9112 is a BiC/DMOS integrated circuit designed for use in high-efficiency switchmode power converters. A high-voltage DMOS input allows this controller to work over a wide range of input voltages (9- to 80-VDC). Current-mode PWM control circuitry is implemented in CMOS to reduce internal power consumption to less than 10 mW.

A CMOS output driver provides high-speed switching of MOSPOWER devices large enough to supply 50 W of output

power. When combined with an output MOSFET and transformer, the Si9112 can be used to implement single-ended power converter topologies (i.e., flyback, forward, and cuk).

The Si9112 is available in both standard and lead (Pb)-free 14-pin plastic DIP and SOIC packages which are specified to operate over the industrial temperature range of  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

### FUNCTIONAL BLOCK DIAGRAM



Applications information, see AN703.

## ABSOLUTE MAXIMUM RATINGS

Voltages Referenced to  $-V_{IN}$  ( $V_{CC} < +V_{IN} + 0.3$  V)

|                                                                                  |                            |
|----------------------------------------------------------------------------------|----------------------------|
| $V_{CC}$ .....                                                                   | 15 V                       |
| $+V_{IN}$ .....                                                                  | 80 V                       |
| Logic Inputs<br>(RESET, SHUTDOWN, OSC IN) .....                                  | -0.3 V to $V_{CC} + 0.3$ V |
| Linear Inputs (FEEDBACK, SENSE) .....                                            | -0.3 V to $V_{CC} + 0.3$ V |
| HV Pre-Regulator Input Current (continuous)<br>(Power Dissipation Limited) ..... | 25 mA                      |
| Storage Temperature .....                                                        | -65 to 150°C               |
| Operating Temperature .....                                                      | -40 to 85°C                |

|                                                  |         |
|--------------------------------------------------|---------|
| Junction Temperature ( $T_J$ ) .....             | 150°C   |
| Power Dissipation (Package) <sup>a</sup>         |         |
| 14-Pin Plastic DIP (J Suffix) <sup>b</sup> ..... | 750 mW  |
| 14-Pin SOIC (Y Suffix) <sup>c</sup> .....        | 900 mW  |
| Thermal Impedance ( $\Theta_{JA}$ )              |         |
| 14-Pin Plastic DIP .....                         | 167°C/W |
| 14-Pin SOIC .....                                | 140°C/W |

### Notes

- Device mounted with all leads soldered or welded to PC board.
- Derate 6 mW/°C above 25°C.
- Derate 7.2 mW/°C above 25°C.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## RECOMMENDED OPERATING RANGE

Voltages Referenced to  $-V_{IN}$

|                 |                 |
|-----------------|-----------------|
| $V_{CC}$ .....  | 9 V to 13.5 V   |
| $+V_{IN}$ ..... | 9 V to 80 V     |
| $f_{OSC}$ ..... | 40 kHz to 1 MHz |

|                      |                               |
|----------------------|-------------------------------|
| $R_{OSC}$ .....      | 25 k $\Omega$ to 1 M $\Omega$ |
| Linear Inputs .....  | 0 to $V_{CC} - 3$ V           |
| Digital Inputs ..... | 0 to $V_{CC}$                 |

| SPECIFICATIONS <sup>a</sup>           |                   |                                                                                                                                                                                                    |                           |                                |                  |                  |        |
|---------------------------------------|-------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------|--------------------------------|------------------|------------------|--------|
| Parameter                             | Symbol            | Test Conditions<br>Unless Otherwise Specified<br><br>DISCHARGE = -V <sub>IN</sub> = 0 V<br>V <sub>CC</sub> = 9 V, +V <sub>IN</sub> = 12 V<br>R <sub>BIAS</sub> = 270 kΩ, R <sub>OSC</sub> = 330 kΩ | Temp <sup>b</sup>         | Limits<br>D Suffix -40 to 85°C |                  |                  | Unit   |
|                                       |                   |                                                                                                                                                                                                    |                           | Min <sup>d</sup>               | Typ <sup>c</sup> | Max <sup>e</sup> |        |
| Reference                             |                   |                                                                                                                                                                                                    |                           |                                |                  |                  |        |
| Output Voltage                        | V <sub>R</sub>    | OSC IN = - V <sub>IN</sub> (OSC Disabled)<br>R <sub>L</sub> = 10 MΩ                                                                                                                                | Room<br>Full <sup>e</sup> | 3.88<br>3.82                   | 4.0              | 4.12<br>4.14     | V      |
| Output Impedance <sup>e</sup>         | Z <sub>OUT</sub>  |                                                                                                                                                                                                    | Room                      | 15                             | 30               | 45               | kΩ     |
| Short Circuit Current                 | I <sub>SREF</sub> | V <sub>REF</sub> = -V <sub>IN</sub>                                                                                                                                                                | Room                      | 70                             | 100              | 130              | μA     |
| Temperature Stability <sup>e</sup>    | T <sub>REF</sub>  |                                                                                                                                                                                                    | Full                      |                                | 0.5              | 1.0              | mV/°C  |
| Oscillator                            |                   |                                                                                                                                                                                                    |                           |                                |                  |                  |        |
| Maximum Frequency <sup>e</sup>        | f <sub>MAX</sub>  | R <sub>OSC</sub> = 0                                                                                                                                                                               | Room                      | 1                              | 3                |                  | MHz    |
| Initial Accuracy                      | f <sub>OSC</sub>  | R <sub>OSC</sub> = 330 k, See Note f                                                                                                                                                               | Room                      | 80                             | 100              | 120              | kHz    |
|                                       |                   | R <sub>OSC</sub> = 150 k, See Note f                                                                                                                                                               | Room                      | 160                            | 200              | 240              |        |
| Voltage Stability                     | Δf/f              | Δf/f = f(13.5 V) - f(9.5 V) / f(9.5 V)                                                                                                                                                             | Room                      |                                | 9                | 15               | %      |
| Temperature Coefficient <sup>e</sup>  | T <sub>OSC</sub>  |                                                                                                                                                                                                    | Full                      |                                | 200              | 500              | ppm/°C |
| Error Amplifier                       |                   |                                                                                                                                                                                                    |                           |                                |                  |                  |        |
| Feedback Input Voltage                | V <sub>FB</sub>   | FB Tied to COMP<br>OSC IN = - V <sub>IN</sub> (OSC Disabled)                                                                                                                                       | Room                      | 3.92                           | 4.00             | 4.08             | V      |
| Input Offset Voltage                  | V <sub>OS</sub>   | OSC IN = - V <sub>IN</sub> (OSC Disabled)                                                                                                                                                          | Room                      |                                | ± 15             | ± 40             | mV     |
| Input BIAS Current                    | I <sub>FB</sub>   | OSC IN = - V <sub>IN</sub> , V <sub>FB</sub> = 4 V                                                                                                                                                 | Room                      |                                | 25               | 500              | nA     |
| Open Loop Voltage Gain <sup>e</sup>   | A <sub>VOL</sub>  | OSC IN = - V <sub>IN</sub>                                                                                                                                                                         | Room                      | 60                             | 80               |                  | dB     |
| Unity Gain Bandwidth <sup>e</sup>     | BW                | OSC IN = - V <sub>IN</sub> (OSC Disabled)                                                                                                                                                          | Room                      | 1                              | 1.5              |                  | MHz    |
| Dynamic Output Impedance <sup>e</sup> | Z <sub>OUT</sub>  | Error Amp Configured for 60 dB gain                                                                                                                                                                | Room                      |                                | 1000             | 2000             | Ω      |
| Output Current                        | I <sub>OUT</sub>  | Source V <sub>FB</sub> = 3.4 V                                                                                                                                                                     | Room                      |                                | -2.0             | -1.4             | mA     |
|                                       |                   | Sink V <sub>FB</sub> = 4.5 V                                                                                                                                                                       | Room                      | 0.12                           | 0.15             |                  |        |
| Power Supply Rejection <sup>e</sup>   | PSRR              | 9 V ≤ V <sub>CC</sub> ≤ 13.5 V                                                                                                                                                                     | Room                      | 50                             | 70               |                  | dB     |



| SPECIFICATIONS <sup>a</sup>                              |                     |                                                                                                                                                                                                    |                   |                                |                  |                  |      |
|----------------------------------------------------------|---------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------|--------------------------------|------------------|------------------|------|
| Parameter                                                | Symbol              | Test Conditions<br>Unless Otherwise Specified<br><br>DISCHARGE = −V <sub>IN</sub> = 0 V<br>V <sub>CC</sub> = 9 V, +V <sub>IN</sub> = 12 V<br>R <sub>BIAS</sub> = 270 kΩ, R <sub>OSC</sub> = 330 kΩ | Temp <sup>b</sup> | Limits<br>D Suffix −40 to 85°C |                  |                  | Unit |
|                                                          |                     |                                                                                                                                                                                                    |                   | Min <sup>d</sup>               | Typ <sup>c</sup> | Max <sup>e</sup> |      |
| Current Limit                                            |                     |                                                                                                                                                                                                    |                   |                                |                  |                  |      |
| Threshold Voltage                                        | V <sub>SOURCE</sub> | V <sub>FB</sub> = 0 V                                                                                                                                                                              | Room              | 1.1                            | 1.3              | 1.5              | V    |
| Delay to Output <sup>e</sup>                             | t <sub>d</sub>      | V <sub>SENSE</sub> = 1.5 V, See Figure 1                                                                                                                                                           | Room              |                                | 100              | 150              | ns   |
| Pre-Regulator/Start-Up                                   |                     |                                                                                                                                                                                                    |                   |                                |                  |                  |      |
| Input Voltage                                            | +V <sub>IN</sub>    | I <sub>IN</sub> = 10 μA                                                                                                                                                                            | Room              | 80                             |                  |                  | V    |
| Input Leakage Current                                    | +I <sub>IN</sub>    | V <sub>CC</sub> ≥ 9.4 V                                                                                                                                                                            | Room              |                                |                  | 10               | μA   |
| Pre-Regulator Start-Up Current                           | I <sub>START</sub>  | +V <sub>IN</sub> = 48 V                                                                                                                                                                            | Room              | 12                             | 20               |                  | mA   |
| Pre-Regulator Dropout Voltage                            | V <sub>CC</sub>     | +V <sub>IN</sub> = 10 V, R <sub>LOAD</sub> = 4 k at Pin 6                                                                                                                                          | Room              | V <sub>UVLO</sub><br>+0.1      |                  |                  | V    |
| V <sub>CC</sub> Pre-Regulator Turn-Off Threshold Voltage | V <sub>REG</sub>    | I <sub>PRE-REGULATOR</sub> = 10 μA                                                                                                                                                                 | Room              | 8.0                            | 8.7              | 9.4              |      |
| Undervoltage Lockout                                     | V <sub>UVLO</sub>   | See Detailed Description                                                                                                                                                                           | Room              | 7.2                            | 8.1              | 8.9              |      |
| V <sub>REG</sub> −V <sub>UVLO</sub>                      | V <sub>DELTA</sub>  |                                                                                                                                                                                                    | Room              | 0.3                            | 0.6              |                  |      |
| Supply                                                   |                     |                                                                                                                                                                                                    |                   |                                |                  |                  |      |
| Supply Current                                           | I <sub>CC</sub>     | C <sub>L</sub> ≤ 75 pF (Pin 4)                                                                                                                                                                     | Room              |                                | 0.6              | 1.0              | mA   |
| Bias Current                                             | I <sub>BIAS</sub>   |                                                                                                                                                                                                    | Room              |                                | 15               |                  | μA   |
| Logic                                                    |                     |                                                                                                                                                                                                    |                   |                                |                  |                  |      |
| SHUTDOWN Delay <sup>e</sup>                              | t <sub>SD</sub>     | C <sub>L</sub> = 500 pF<br>V <sub>SENSE</sub> = −V <sub>IN</sub> , See Figure 2                                                                                                                    | Room              |                                | 50               | 100              | ns   |
| SHUTDOWN Pulse Width <sup>e</sup>                        | t <sub>SW</sub>     | See Figure 3                                                                                                                                                                                       | Room              | 50                             |                  |                  |      |
| RESET Pulse Width <sup>e</sup>                           | t <sub>RW</sub>     |                                                                                                                                                                                                    | Room              | 50                             |                  |                  |      |
| Latching Pulse Width SHUTDOWN and RESET Low <sup>e</sup> | t <sub>LW</sub>     |                                                                                                                                                                                                    | Room              | 25                             |                  |                  |      |
| Input Low Voltage                                        | V <sub>IL</sub>     |                                                                                                                                                                                                    | Room              |                                |                  | 2.0              | V    |
| Input High Voltage                                       | V <sub>IH</sub>     |                                                                                                                                                                                                    | Room              | 7.0                            |                  |                  |      |
| Input Current Input Voltage High                         | I <sub>IH</sub>     | V <sub>LOGIC</sub> = V <sub>CC</sub>                                                                                                                                                               | Room              |                                | 1                | 5                | μA   |
| Input Current Input Voltage Low                          | I <sub>IL</sub>     | V <sub>IN</sub> = 0 V                                                                                                                                                                              | Room              | −35                            | 25               |                  |      |
| Output                                                   |                     |                                                                                                                                                                                                    |                   |                                |                  |                  |      |
| Output High Voltage                                      | V <sub>OH</sub>     | I <sub>OUT</sub> = −10 mA                                                                                                                                                                          | Room Full         | 8.7<br>8.5                     |                  |                  | V    |
| Output Low Voltage                                       | V <sub>OL</sub>     | I <sub>OUT</sub> = 10 mA                                                                                                                                                                           | Room Full         |                                |                  | 0.3<br>0.5       |      |
| Output Resistance <sup>e</sup>                           | R <sub>OUT</sub>    | I <sub>OUT</sub> = 10 mA, Source or Sink                                                                                                                                                           | Room Full         |                                | 20<br>25         | 30<br>50         | Ω    |
| Rise Time <sup>e</sup>                                   | t <sub>r</sub>      | C <sub>L</sub> = 500 pF                                                                                                                                                                            | Room              |                                | 40               | 75               | ns   |
| Fall Time <sup>e</sup>                                   | t <sub>f</sub>      |                                                                                                                                                                                                    | Room              |                                | 40               | 75               |      |

## Notes

- Refer to PROCESS OPTION FLOWCHART for additional information.
- Room =  $25^\circ\text{C}$ , Full = as determined by the operating temperature suffix.
- Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- The algebraic convention whereby the most negative value is a minimum and the most positive a maximum.
- Guaranteed by design, not subject to production test.
- $C_{STRAY}$  Pin 8 =  $\leq 5\text{ pF}$ .

## TIMING WAVEFORMS

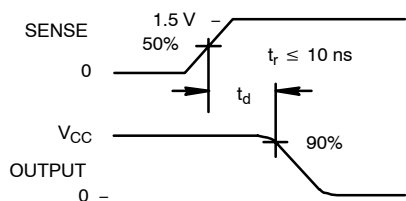


FIGURE 1.

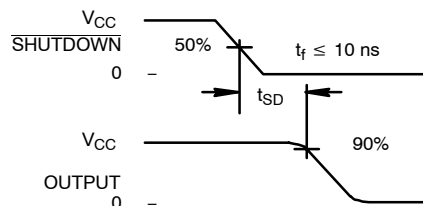


FIGURE 2.

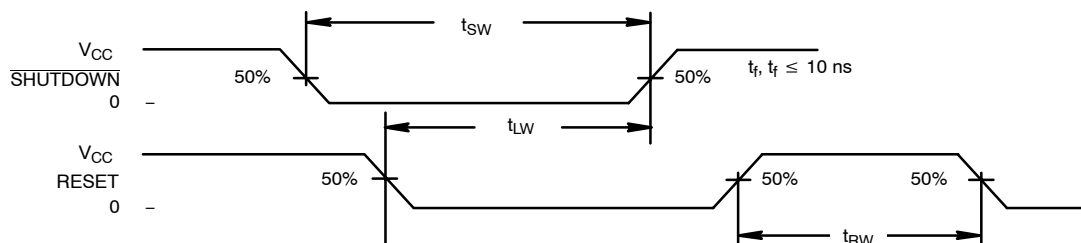


FIGURE 3.

## TYPICAL CHARACTERISTICS

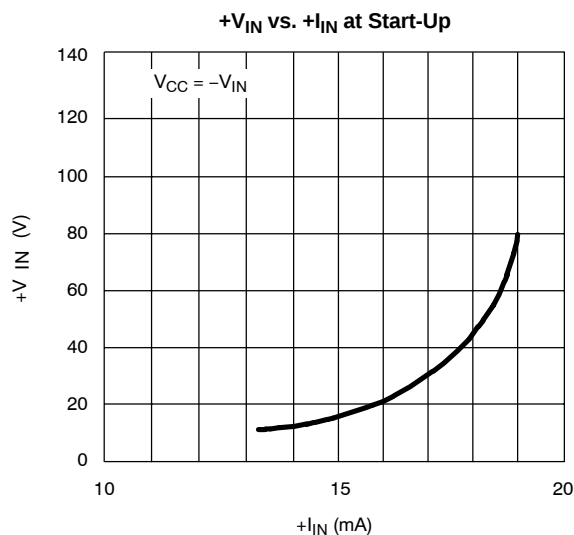


FIGURE 4.

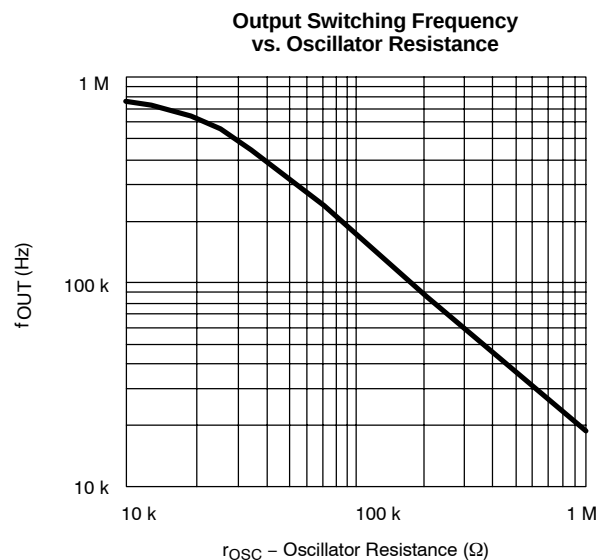
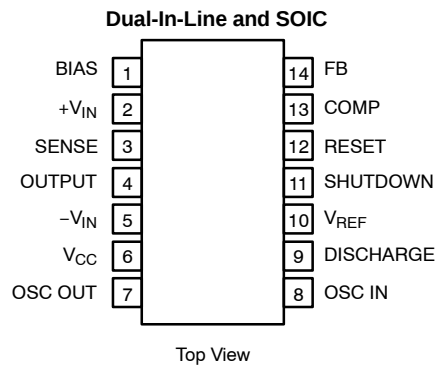


FIGURE 5.

**PIN CONFIGURATIONS AND ORDERING INFORMATION**

**ORDERING INFORMATION**

| Part Number    | Temperature Range | Package |
|----------------|-------------------|---------|
| Si9112DY       | -40 to 85°C       | SOIC-14 |
| Si9112DY-T1    |                   |         |
| Si9112DY-T1-E3 |                   |         |
| Si9112DJ       |                   | PDIP-14 |
| Si9112DJ-E3    |                   |         |

**DETAILED DESCRIPTION**
**Pre-Regulator/Start-Up Section**

Due to the low quiescent current requirement of the Si9112 control circuitry, bias power can be supplied from the unregulated input power source, from an external regulated low-voltage supply, or from an auxiliary “bootstrap” winding on the output inductor or transformer.

When power is first applied during start-up,  $+V_{IN}$  (pin 2) will draw a constant current. The magnitude of this current is determined by a high-voltage depletion MOSFET device which is connected between  $+V_{IN}$  and  $V_{CC}$  (pin 6). This start-up circuitry provides initial power to the IC by charging an external bypass capacitance connected to the  $V_{CC}$  pin. The charging current is disabled when  $V_{CC}$  exceeds 8.7 V. If  $V_{CC}$  is not forced to exceed the 8.7-V threshold, then  $V_{CC}$  will be regulated to a nominal value of 8.7 V by the pre-regulator circuit.

As the supply voltage rises toward the normal operating conditions, an internal undervoltage (UV) lockout circuit keeps the output driver disabled until  $V_{CC}$  exceeds the UV lockout threshold (typically 8.1 V). This guarantees that the control logic will be functioning properly and that sufficient gate drive voltage is available before the MOSFET turns on. The design of the IC is such that the undervoltage lockout threshold will be at least 300 mV less than the pre-regulator turn-off voltage. Power dissipation can be minimized by providing an external power source to  $V_{CC}$  such that the pre-regulator circuit is disabled.

**BIAS**

To properly set the bias for the Si9112, a 270-k $\Omega$  resistor should be tied from BIAS (pin 1) to  $-V_{IN}$  (pin 5). This

determines the magnitude of bias current in all of the analog sections and the pull-up current for the SHUTDOWN and RESET pins. The current flowing in the bias resistor is nominally 15  $\mu$ A.

**Reference Section**

The reference section of the Si9112 consists of a temperature compensated buried zener and trimmable divider network. The output of the reference section is connected internally to the non-inverting input of the error amplifier. Nominal reference output voltage is 4 V. The trimming procedure that is used on the Si9112 brings the output of the error amplifier (which is configured for unity gain during trimming) to within  $\pm 2\%$  of 4 V. This automatically compensates for input offset voltage in the error amplifier.

The output impedance of the reference section has been purposely made high so that a low impedance external voltage source can be used to override the internal voltage source, if desired, without otherwise altering the performance of the device.

**Error Amplifier**

Closed-loop regulation is provided by the error amplifier. The emitter follower output has a typical dynamic output impedance of 1000  $\Omega$ , and is intended for use with “around-the-amplifier” compensation. A MOS differential input stage provides low input leakage current. The noninverting input to the error amplifier ( $V_{REF}$ ) is internally connected to the output of the reference supply and should be bypassed with a small capacitor to ground.



## DETAILED DESCRIPTION (CONT'D)

### Oscillator Section

The oscillator consists of a ring of CMOS inverters, capacitors, and a capacitor discharge switch. Frequency is set by an external resistor between the OSC IN and OSC OUT pins. (See Typical Characteristics for details of resistor value vs. frequency.) The DISCHARGE pin should be tied to  $-V_{IN}$  for normal internal oscillator operation. A frequency divider in the logic section limits switch duty cycle to  $\leq 50\%$  by locking the switching frequency to one half of the oscillator frequency.

Remote synchronization can be accomplished by capacitive coupling of a SYNC pulse into the OSC IN (pin 8) terminal. For a 5-V pulse amplitude and 0.5- $\mu$ s pulse width, typical values would be 100 pF in series with 3 k $\Omega$  to pin 8.

### SHUTDOWN and RESET

SHUTDOWN (pin 11) and RESET (pin 12) are intended for overriding the output MOSFET switch via external control logic. The two inputs are fed through a latch preceding the output switch. Depending on the logic state of RESET, SHUTDOWN can be either a latched or unlatched input. The output is off whenever SHUTDOWN is low. By simultaneously having SHUTDOWN and RESET low, the latch is set and SHUTDOWN has no effect until RESET goes high. The truth table for these inputs is given in Table 1.

**Table 1:** Truth Table for the SHUTDOWN and RESET Pins

| SHUTDOWN | RESET | Output                       |
|----------|-------|------------------------------|
| H        | H     | Normal Operation             |
| H        |       | Normal Operation (No Change) |
| L        | H     | Off (Not Latched)            |
| L        | L     | Off (Latched)                |
|          | L     | Off (Latched, No Change)     |

Both pins have internal current source pull-ups and should be left disconnected when not in use. An added feature of the current sources is the ability to connect a capacitor and an open-collector driver to the SHUTDOWN or RESET pins to provide variable shutdown time.

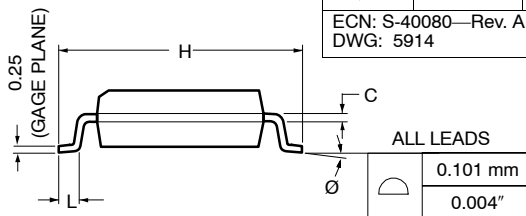
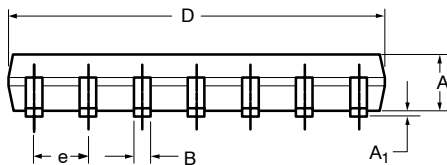
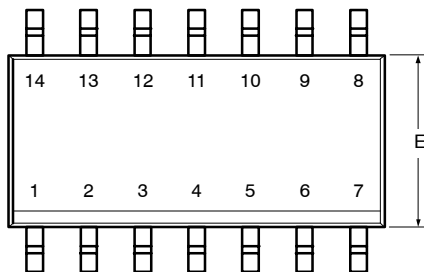
### Output Driver

The push-pull driver output has a typical on-resistance of 20  $\Omega$ . Maximum switching times are specified at 75 ns for a 500 pF load. This is sufficient to directly drive 60-V, 25-A MOSFETs. Larger devices can be driven, but switching times will be longer, resulting in higher switching losses.

For applications information refer to AN703.



**SOIC (NARROW): 14-LEAD (POWER IC ONLY)**

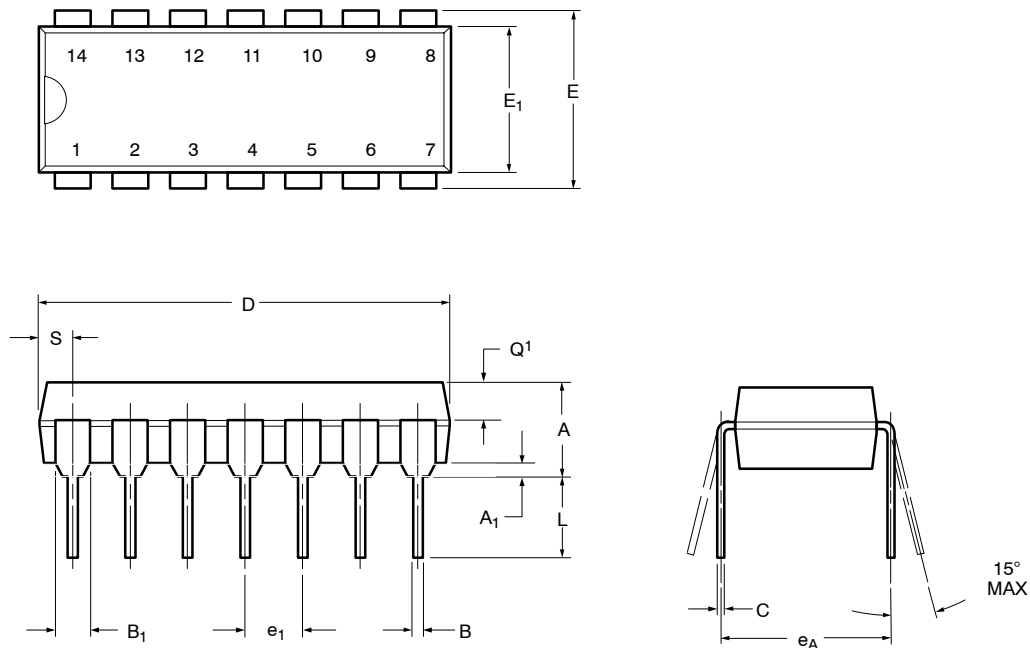


| Dim            | MILLIMETERS |      | INCHES    |       |
|----------------|-------------|------|-----------|-------|
|                | Min         | Max  | Min       | Max   |
| A              | 1.35        | 1.75 | 0.053     | 0.069 |
| A <sub>1</sub> | 0.10        | 0.20 | 0.004     | 0.008 |
| B              | 0.38        | 0.51 | 0.015     | 0.020 |
| C              | 0.18        | 0.23 | 0.007     | 0.009 |
| D              | 8.55        | 8.75 | 0.336     | 0.344 |
| E              | 3.8         | 4.00 | 0.149     | 0.157 |
| e              | 1.27 BSC    |      | 0.050 BSC |       |
| H              | 5.80        | 6.20 | 0.228     | 0.244 |
| L              | 0.50        | 0.93 | 0.020     | 0.037 |
| Ø              | 0°          | 8°   | 0°        | 8°    |

ECN: S-40080—Rev. A, 02-Feb-04  
DWG: 5914



**PDIP: 14-LEAD (POWER IC ONLY)**



| Dim            | MILLIMETERS |       | INCHES |       |
|----------------|-------------|-------|--------|-------|
|                | Min         | Max   | Min    | Max   |
| A              | 3.81        | 5.08  | 0.150  | 0.200 |
| A <sub>1</sub> | 0.38        | 1.27  | 0.015  | 0.050 |
| B              | 0.38        | 0.51  | 0.015  | 0.020 |
| B <sub>1</sub> | 0.89        | 1.65  | 0.035  | 0.065 |
| C              | 0.20        | 0.30  | 0.008  | 0.012 |
| D              | 17.27       | 19.30 | 0.680  | 0.760 |
| E              | 7.62        | 8.26  | 0.300  | 0.325 |
| E <sub>1</sub> | 5.59        | 7.11  | 0.220  | 0.280 |
| e <sub>1</sub> | 2.29        | 2.79  | 0.090  | 0.110 |
| e <sub>A</sub> | 7.37        | 7.87  | 0.290  | 0.310 |
| L              | 2.79        | 3.81  | 0.110  | 0.150 |
| Q <sub>1</sub> | 1.27        | 2.03  | 0.050  | 0.080 |
| S              | 1.02        | 2.03  | 0.040  | 0.080 |

ECN: S-40081—Rev. A, 02-Feb-04  
DWG: 5919



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