Datasheet

Serial EEPROM Series Standard EEPROM

WLCSP EEPROM

BU9844GUL-W (16Kbit)

General Description

BU9844GUL-W series is a serial EEPROM of I^{2}C BUS interface method. 1.7V single power source action and actions available at 400kHz.

Features

- Completely Conforming to the World Standard I^{2}C BUS. All Controls Available by 2 Ports of Serial Clock (SCL) and Serial Data(SDA)
- Other Devices than EEPROM can be Connected to the Same Port, Saving Microcontroller Port.
- Actions Available at 400kHz Clock (1.7V to 5.5V)
- 1.7V to 5.5V Single Power Source Action Most Suitable for Battery Use.
- Up to 16Byte in Page Write Mode.
- Bit Format 2048×8
- Auto Erase and Auto End Function at Data Rewrite.
- Low Current Consumption
  - At Write Action (5V) : 1.2mA (Typ.)
  - At Read Action (5V) : 0.2mA (Typ.)
  - At Standby Action (5V) : 0.1μA (Typ.)
- Write Mistake Prevention Function
  - Write (write protect) Function Added.
  - Write Mistake Prevention Function at Low Voltage.
- Data Rewrite up to 1,000,000 Times.
- Data Kept for 40 Years.
- Noise Filter Built in SCL / SDA Terminal
- Shipment Data all Address FFh.

Package W(Typ.) x D(Typ.) x H(Max.)
VCSP50L1:1.60mm x 1.84mm x 0.6mm

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Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Ratings	Unit	Remarks
Impressed Voltage	V_{CC}	-0.3 to +6.5	V	
Permissible Dissipation	Pd	0.22	W	When using at Ta=25°C or higher, 2.2mW to be reduced per 1°C
Storage Temperature Range	Tstg	-65 to +125	°C	
Operating Temperature Range	Topr	-40 to +85	°C	
Terminal voltage	-	-0.3 to Vcc+1.0	V	

Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Memory Cell Characteristics (Ta=25°C, Vcc=1.7V to 5.5V)

Parameter	Limits			Unit
	Min	Typ.	Max	
Number of Data rewrite times (Note1)	1,000,000	-	-	Times
Data hold years (Note)	40	-	-	Years

(Note1) Not 100% TESTED

Recommended Operating Ratings

Parameter	Symbol	Ratings	Unit
Power Source Voltage	Vcc	1.7 to 5.5	V
Input Voltage	Vin	0 to V_{CC}	

Electrical Characteristics (Unless otherwise specified, Ta=-40°C to +85°C, V_{CC}=1.7V to 5.5V)

Parameter	Symbol	Limits			Unit	Conditions
		Min.	Typ.	Max.		
“HIGH” Input Voltage1	V_{IH1}	$0.7V_{CC}$	-	-	V	$2.5V \leq V_{CC} \leq 5.5V$
“LOW” Input Voltage1	V_{IL1}	-	-	$0.3V_{CC}$	V	$2.5V \leq V_{CC} \leq 5.5V$
“HIGH” Input Voltage2	V_{IH2}	$0.9V_{CC}$	-	-	V	$1.7V \leq V_{CC} < 2.5V$
“LOW” Input Voltage2	V_{IL2}	-	-	$0.1V_{CC}$	V	$1.7V \leq V_{CC} < 2.5V$
“LOW” Output Voltage1	V_{OL1}	-	-	0.3	V	I_{OL}=3.0mA, $2.5V \leq V_{CC} \leq 5.5V$, (SDA)
“LOW Output Voltage2	V_{OL2}	-	-	0.2	V	I_{OL}=1.5mA, $1.7V \leq V_{CC} < 2.5V$, (SDA)
Input Leak Current	I_{LI}	-1	-	1	μA	V_{IN}=0V to V_{CC}
Output Leak Current	I_{LO}	-1	-	1	μA	V_{OUT}=0V to V_{CC}(SDA)
Current Consumption at Action	I_{CC1}	-	-	2.0	mA	V_{CC}=5.5V, f_{SCL}=400kHz, t_{WR}=5ms, Byte write, Page write
	I_{CC2}	-	-	0.5	mA	V_{CC}=5.5V, f_{SCL}=400kHz Random read, Current read, sequential read
Standby Current	I_{SB}	-	-	2.0	μA	V_{CC}=5.5V, SDA·SCL=V_{CC}, A2=GND, WP=GND

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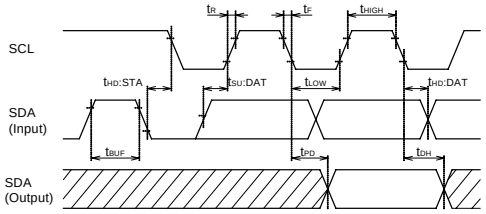
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Action timing characteristics (Unless otherwise specified, Ta=-40°C to +85°C, V_{CC} =1.7V to 5.5V)

Parameter	Symbol	FAST-MODE 2.5V≤V_{CC}≤5.5V			STANDARD-MODE 1.7V≤V_{CC}≤5.5V			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
SCL Frequency	f_{SCL}	-	-	400	-	-	100	kHz
Data Clock “HIGH” Time	t_{HIGH}	0.6	-	-	4.0	-	-	µs
Data Clock “LOW” Time	t_{LOW}	1.2	-	-	4.7	-	-	µs
SDA, SCL Rise Time (Note1)	t_R	-	-	0.3	-	-	1.0	µs
SDA< SCL Fall Time (Note1)	t_F	-	-	0.3	-	-	0.3	µs
Start Condition Hold Time	$t_{HD:STA}$	0.6	-	-	4.0	-	-	µs
Start Condition Setup Time	$t_{SU:STA}$	0.6	-	-	4.7	-	-	µs
Input Data Hold Time	$t_{HD:DAT}$	0	-	-	0	-	-	ns
Input Data Setup Time	$t_{SU:DAT}$	100	-	-	250	-	-	ns
Output Data Delay Time	t_{PD}	0.1	-	0.9	0.2	-	3.5	µs
Output Data Hold Time	t_{DH}	0.1	-	-	0.2	-	-	µs
Stop Condition Setup Time	$t_{SU:STO}$	0.6	-	-	4.7	-	-	µs
Bus Release Time Before Transfer Start	t_{BUF}	1.2	-	-	4.7	-	-	µs
Internal Write Cycle Time	t_{WR}	-	-	5	-	-	5	ms
Noise Removal Valid Period (SDA, SCL terminal)	t_I	-	-	0.1	-	-	0.1	µs
WP Hold Time	$t_{HD:WP}$	0	-	-	0	-	-	ns
WP Setup Time	$t_{SU:WP}$	0.1	-	-	0.1	-	-	µs
WP Valid Time	$t_{HIGH:WP}$	1.0	-	-	1.0	-	-	µs

(Note1) Not 100% tested.

Sync Data Input / Output Timing



○Input read at the rise edge of SCL
○Data output in sync with the fall of SCL

Figure 1-(a) Sync data input / output timing

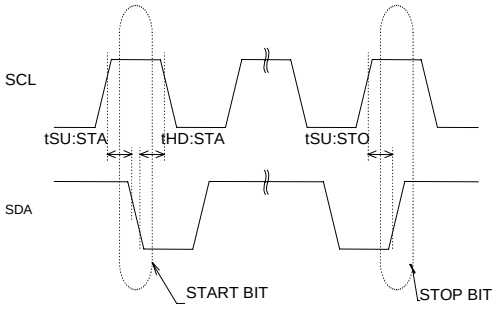


Figure 1-(b) Start – stop bit timing

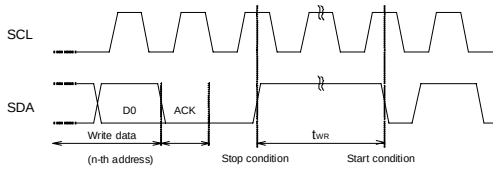


Figure 1-(c) Write cycle timing

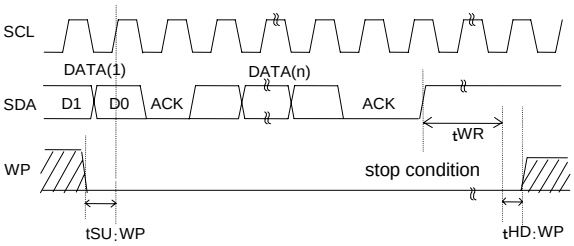


Figure 1-(d) WP timing at write execution

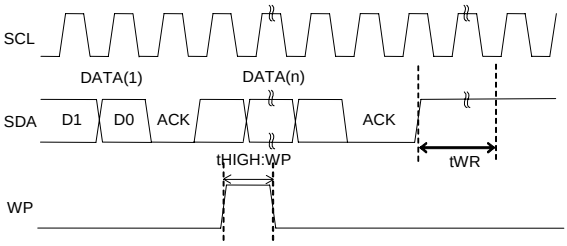


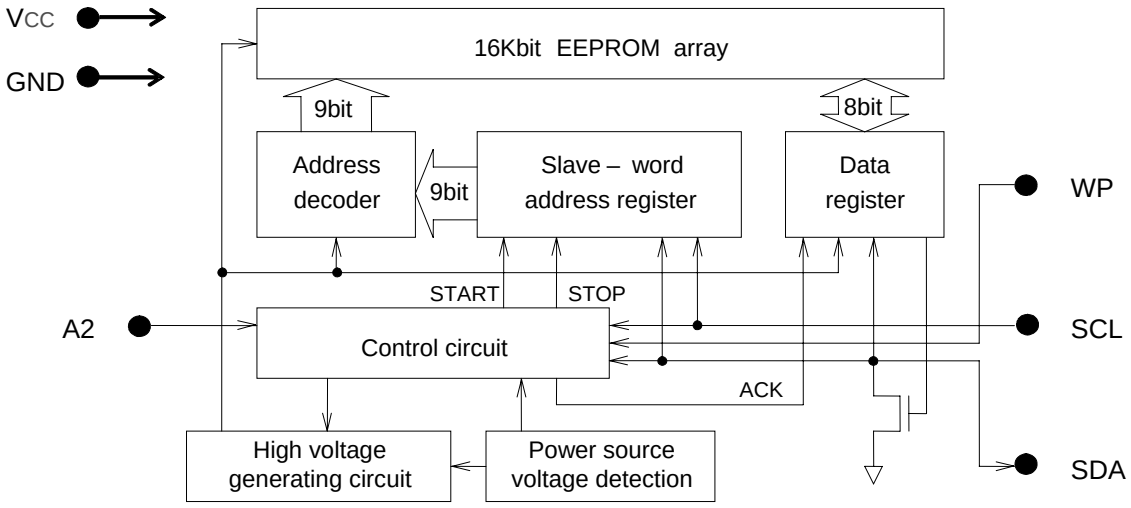
Figure 1-(e) WP timing at write cancel

○At write execution, in the area from the DO taken clock rise of the first DATA (1), to tWR, set WP=”LOW”
○By setting WP “HIGH” in the area, write can be cancelled.
When it is set WP=”HIGH” during tWR, write is forcibly ended, and data of address under access is not guaranteed, therefore write it once again.

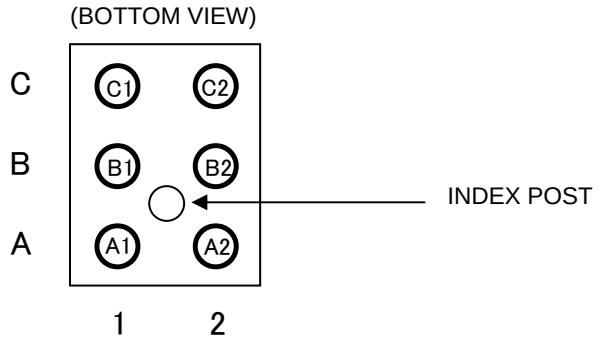
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Block Diagram



Pin Configuration



Pin Descriptions

Land No.	Terminal Name	Input/ Output	Function
A1	Vcc	–	Power Supply
A2	A2	Input	Out of Use (Vcc or GND or OPEN)
B1	WP	Input	Write Protect Input
B2	GND	Input	Ground (0V)
C1	SCL	Input	Serial Clock Input
C2	SDA (Note1)	Input /Output	Slave and Word Address, Serial Data Input, Serial Data Output (Note1)

(Note1) An open drain output requires a pull-up resister.

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Typical Performance Curves

(The following values are Typ. ones.)

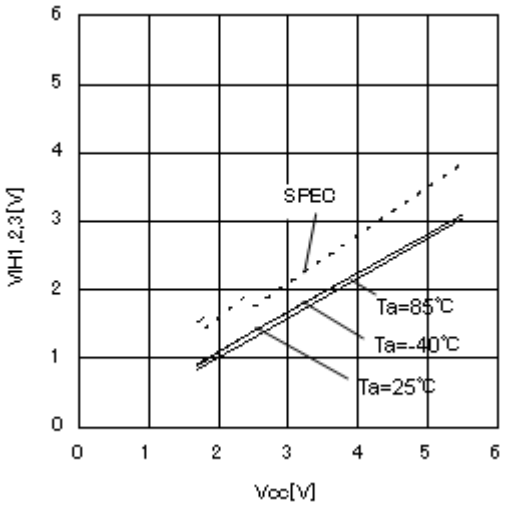


Figure 2. H input voltage VIH1,2,3
(A2, SCL, SDA, WP)

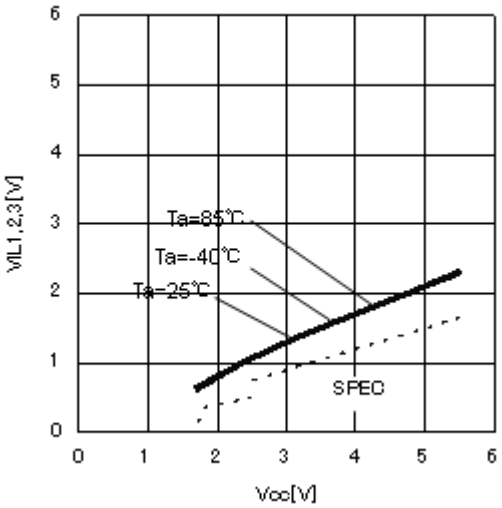


Figure 3. L input voltage VIL1,2,3
(A2, SCL, SDA, WP)

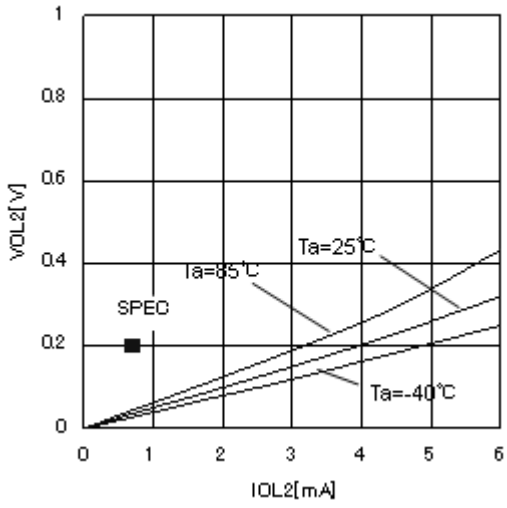


Figure 4. L output voltage VOL2-IOL2
(V_{CC}=1.7V)

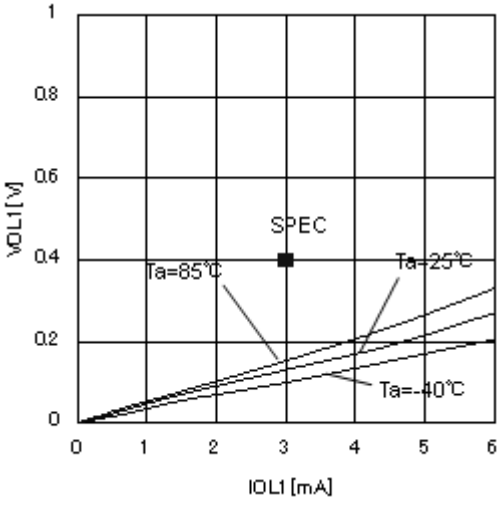


Figure 5. L input voltage
V_{OL1}-I_{OL1} (Vcc=2.5V)

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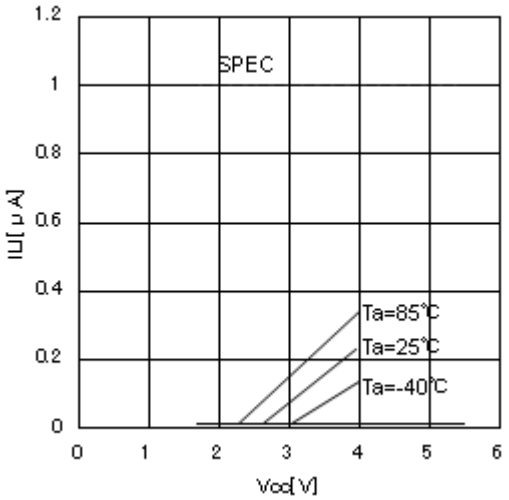


Figure 6. Input leak current
ILI (A2, SCL, WP)

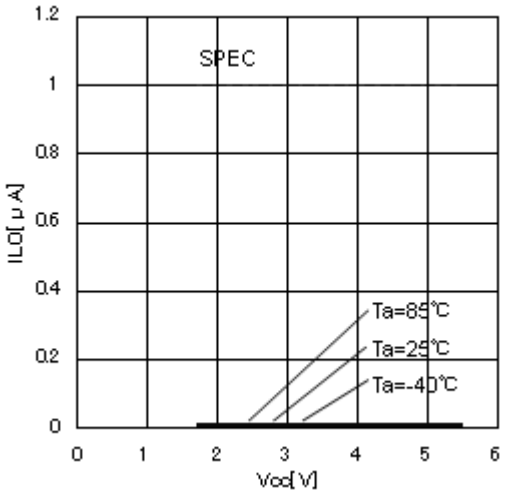


Figure 7. Output leak current
ILO (SDA)

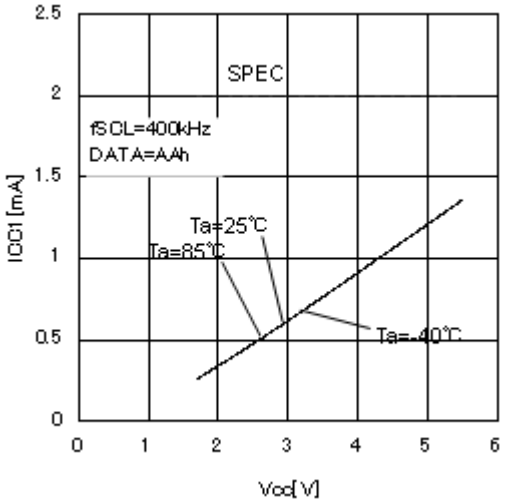


Figure 8. Consumption current
at write action Icc1 (fSCL=400kHz)

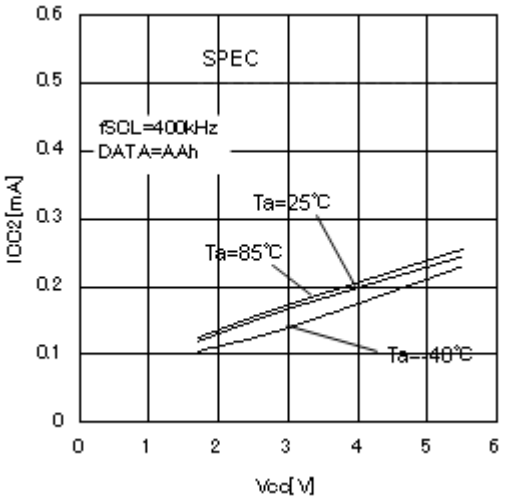


Figure 9. Consumption current
at write action Icc2 (fSCL=400kHz)

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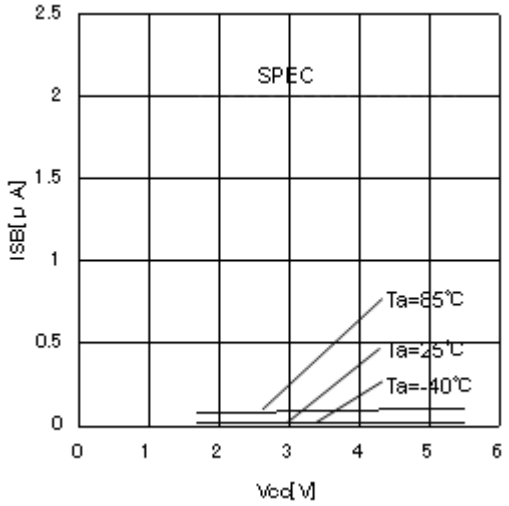


Figure 10. Standby current
I_{SB}

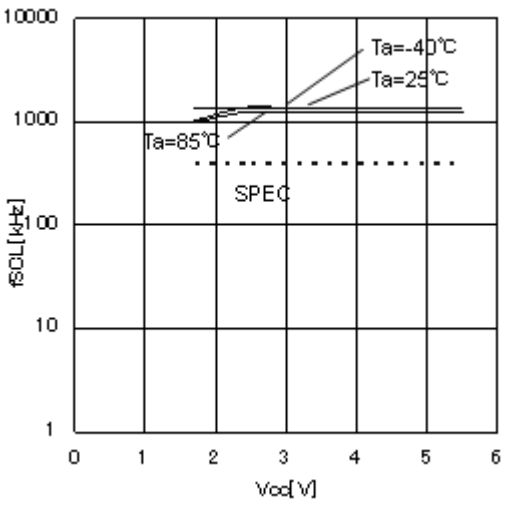


Figure 11. SCL frequency
f_{SCL}

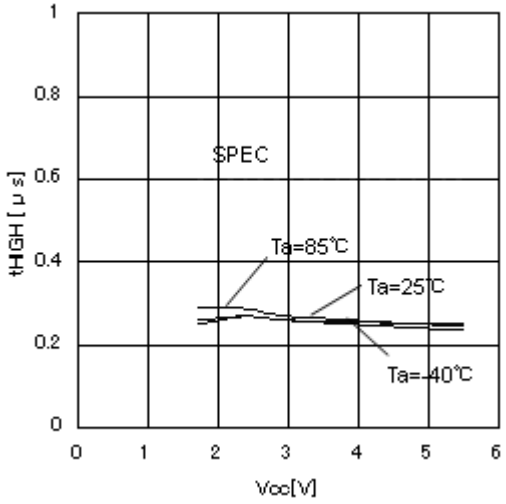


Figure 12. Data clock “H” time
tHIGH

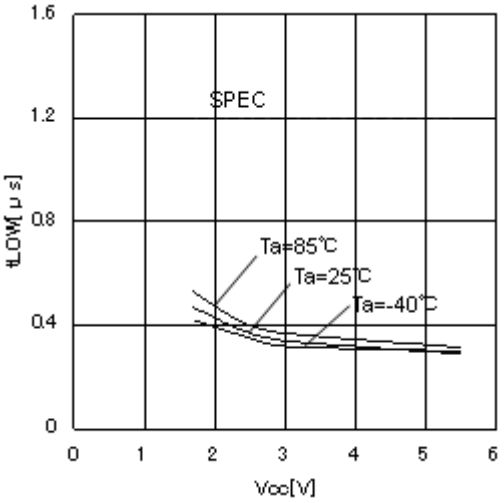


Figure 13. Data clock “L” time
tLOW

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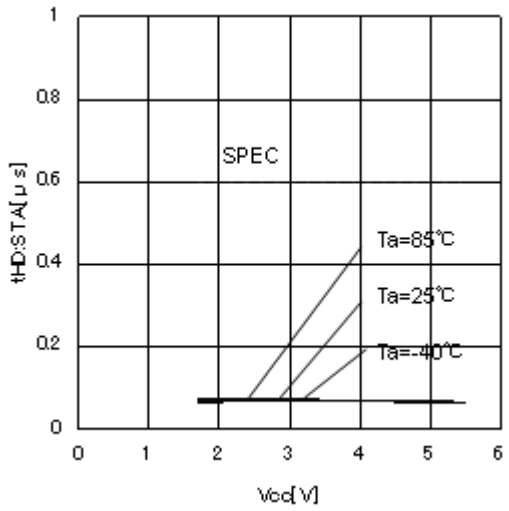


Figure 14. Start condition hold time
tHD:STA

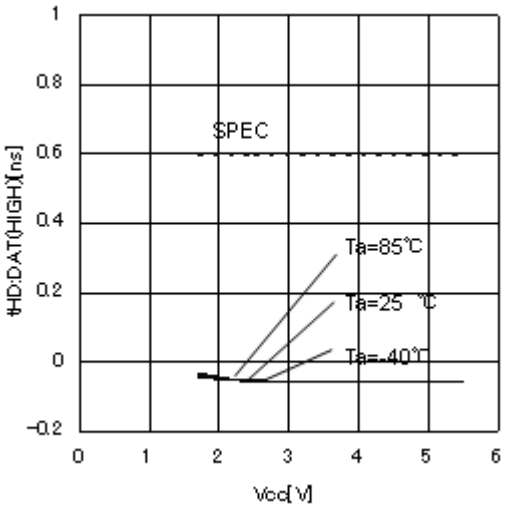


Figure 15. Start condition setup time
tSU:STA

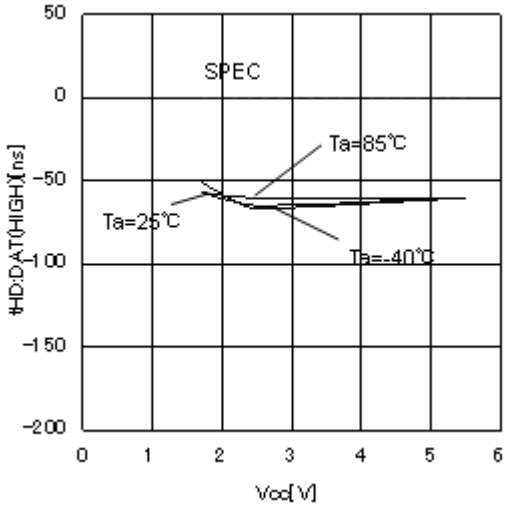


Figure 16. Input data hold time
tHD:DAT

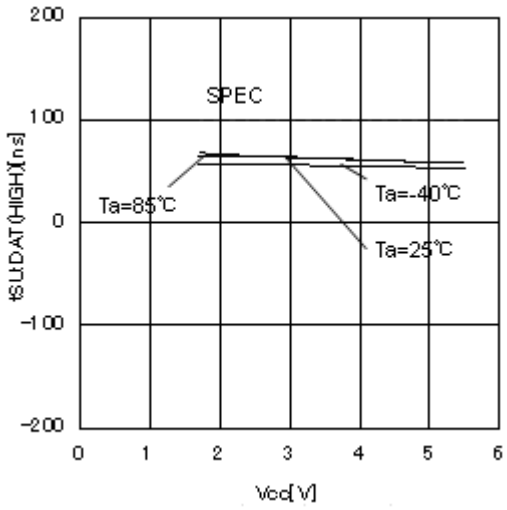


Figure 17. Input data setup time
tSU:DAT

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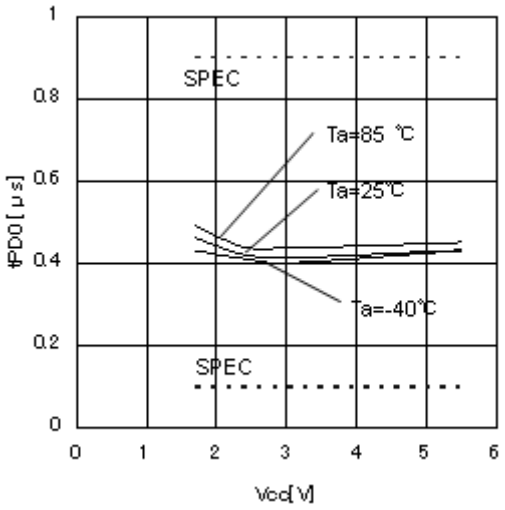


Figure 18. Output data delay time
tPD0

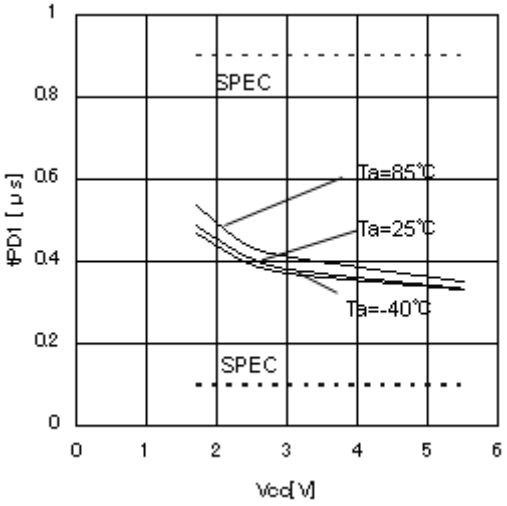


Figure 19. Output data delay time
tPD1

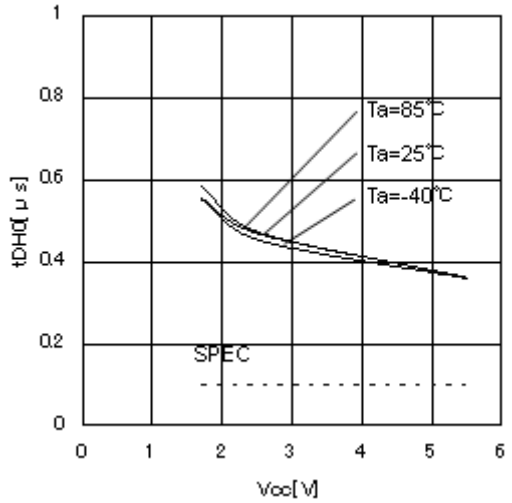


Figure 20. Output data hold time
tDH1

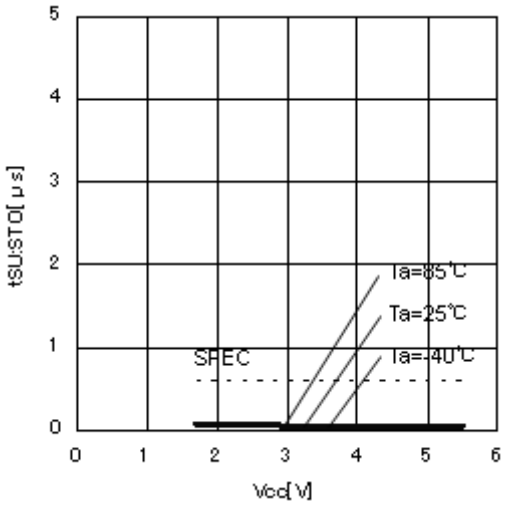


Figure 21. Stop condition setup time
tSU:STO

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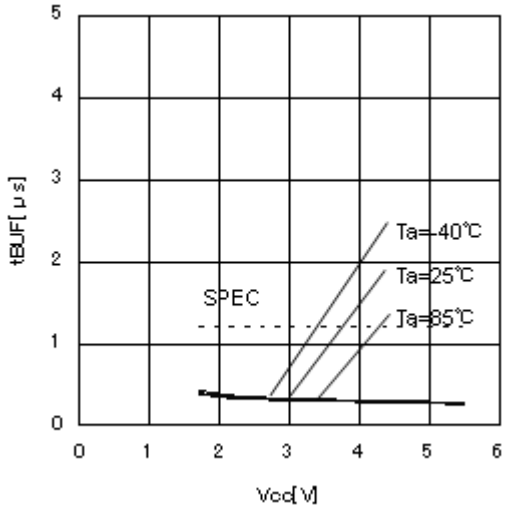


Figure 22. Bus release time before transfer start tBUF

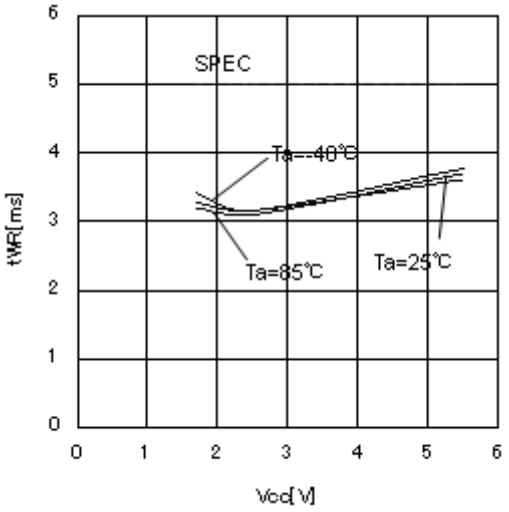


Figure 23. Internal write cycle time tWR

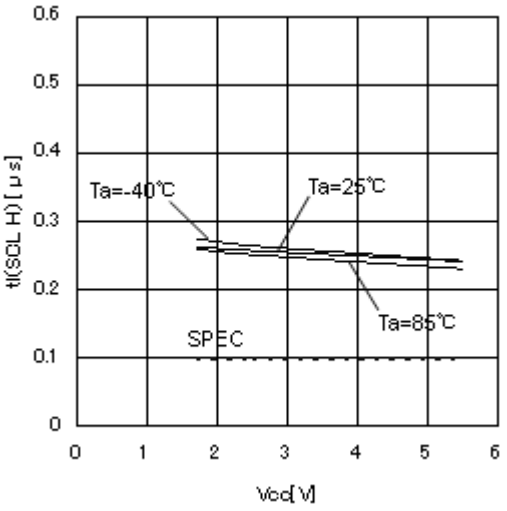


Figure 24. Noise removal time tI (SCL H)

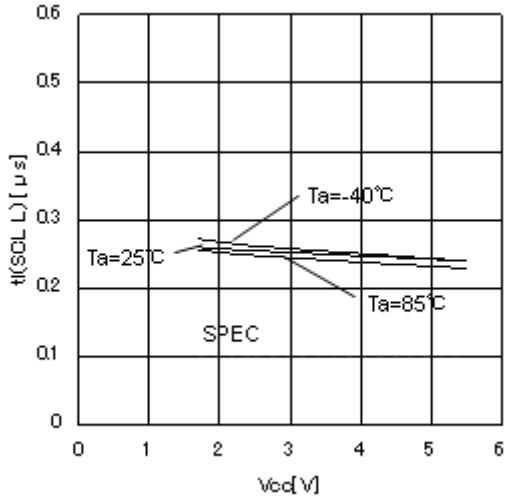


Figure 25. Noise removal time tI (SCL L)

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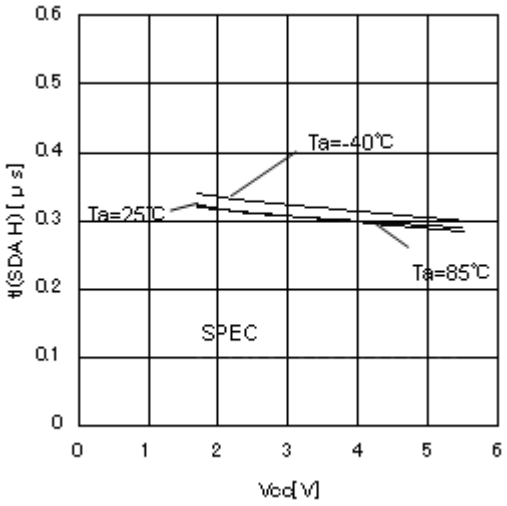


Figure 26. Noise removal time
tI (SDA H)

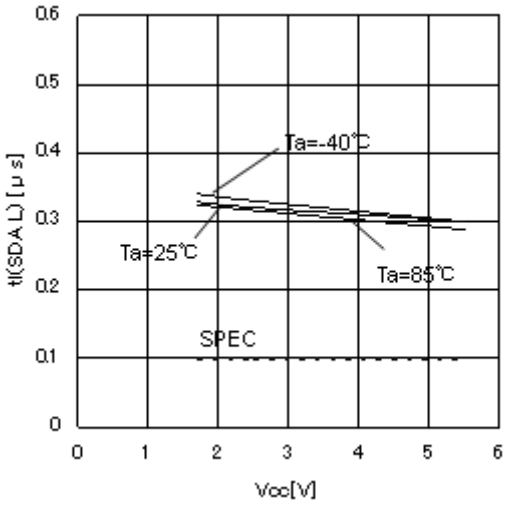


Figure 27. Noise removal time
tI (SDA L)

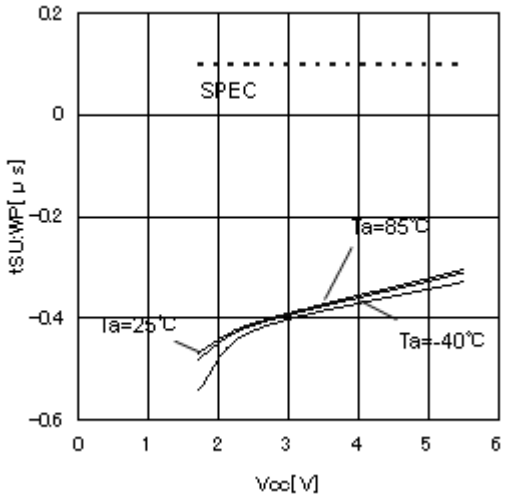


Figure 28. WP setup time
tSU:WP

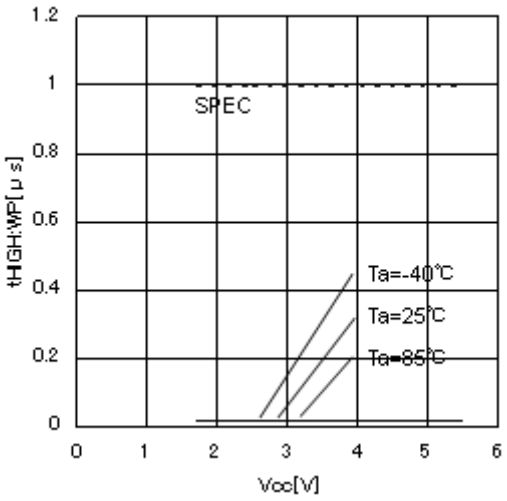


Figure 29. WP valid time
tHIGH: WP

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I²C BUS communication

1. I²C BUS data communication

I²C BUS data communication starts by start condition input, and ends by stop condition input. Data is always 8bit long, and acknowledge is always required after each byte.

I²C BUS carries out data transmission with plural devices connected by 2 communication lines of serial data (SDA) and serial clock (SCL).

Among devices, there are “master” that generates clock and control communication start and end, and “slave” that is controlled by addresses peculiar to devices.

EEPROM becomes “slave”. And the device that outputs data to bys during data communication is called “transmitter”, and the device that receives data is called “receiver “.

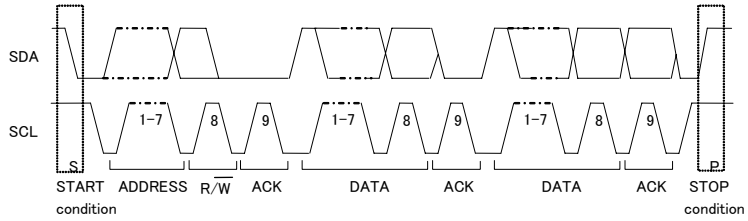


Figure 30. Data transfer timing

2. Start condition (start bit recognition)
   (1) Before executing each command, start condition (start bit) where SDA goes from “HIGH” down to “LOW” when SCL is “HIGH” is necessary.
   (2) This IC always detects whether SDA and SCL are in start condition (start bit) of not, therefore, unless this condition is satisfied, any command is executed.

3. Stop condition (stop bit recognition)
   (1) Each command can be ended by SDA rising from “LOW” to “HIGH” when stop condition (stop bit), namely, SCL is “HIGH”.

4. Acknowledge (ACK) signal
   (1) This acknowledge (ACK) signal is a software rule to show whether data transfer has been made normally or not. In master and slave, the device (µ-COM at slave address input of write command, read command, and this IC at data output of read command) at the transmitter (sending) side releases the bus after output of 8bit data.
   (2) This device (this IC at slave address input of write command , read command , and µ-COM at data output of read command) at the receiver (receiving) side sets SDA “LOW” during 9 clock cycles, and outputs acknowledge signal (ACK signal) showing that it has received the 8bit data.
   (3) This IC, after recognizing start condition and slave address (8bit), outputs acknowledge signal (ACK signal) “LOW”.
   (4) Each write action outputs acknowledge signal (ACK signal) “LOW”, at receiving 8bit data (word address and write data).
   (5) Each read action outputs 8bit data (read data), and detects acknowledge signal (ACK signal) “LOW”.
   (6) When acknowledge signal (ACK signal) is detected, and stop condition is not sent from the master (µ-COM) side, this IC continues data output. When acknowledge signal (ACK signal) is not detected, this IC stops data transfer, and recognizes stop condition (stop bit), and ends read action.
   And this IC gets in standby status.

5. Device addressing
   (1) Output slave address after start condition from master.
   (2) The significant 4 bits of slave address are used for recognizing a device type.
   The device code of this IC is fixed to “1010”.
   (3) Next slave addresses (P2 P1 P0) are upper 3bit of word address, put these and word address (WA0 to WA7) together, 11bit word address (2048byte) of the device specified.
   (4) The most insignificant bit (R / $\overline{W}$ --- READ / $\overline{WRITE}$) of slave address is used for designating write or read action, and is as shown below.

Setting R / $\overline{W}$ to 0 --- write (setting 0 to word address setting of random read)

Setting R / $\overline{W}$ to 1 --- read

Type	Slave Address	Maximum number of Connected Buses
BU9844GUL-W	1 0 1 0 P2 P1 P0 R / $\overline{W}$	1

P0 to P2 are page select bits (Upper 3bit of word address).

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Command

1. Write cycle

(1) Arbitrary data is written to EEPROM. When to write only 1 byte, byte write is normally used, and when to write continuous data of 2 bytes or more, simultaneous write is possible by page write cycle.

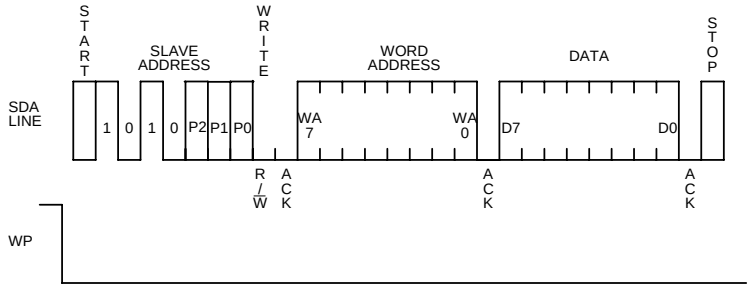


Figure 31. Byte write cycle

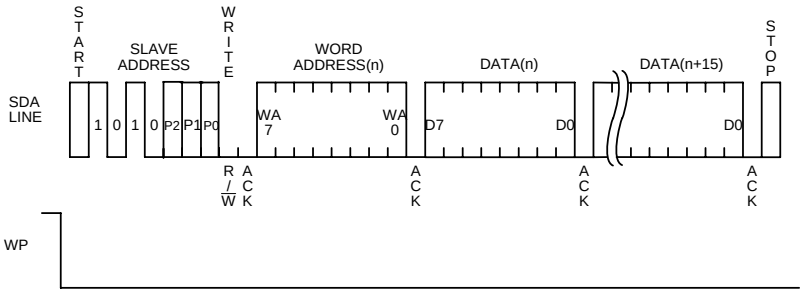


Figure 32. Page write cycle

(2) Data is written to the address designated by word address (n-th address).
(3) By issuing stop bit after 8bit data input, write to memory cell inside starts.
(4) When internal write is started, command is not accepted for tWR (5ms at maximum).
(5) By page write cycle, the following can be written in bulk. Up to 16 bytes.
And when data of the maximum bytes or higher is sent, data from the first byte is overwritten.
(Refer to “Internal address increment” in Page 14.)
(6) As for page write cycle of BU9844GUL-W, after page select bit (PS) of slave address is designated arbitrarily, by continuing data input of 2 bytes or more, the address of insignificant 4 bits is incremented internally, and data up to 16 bytes can be written.

Note)

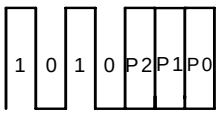


Figure 33. Difference of slave address of each type

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2. Notes on write cycle continuous input

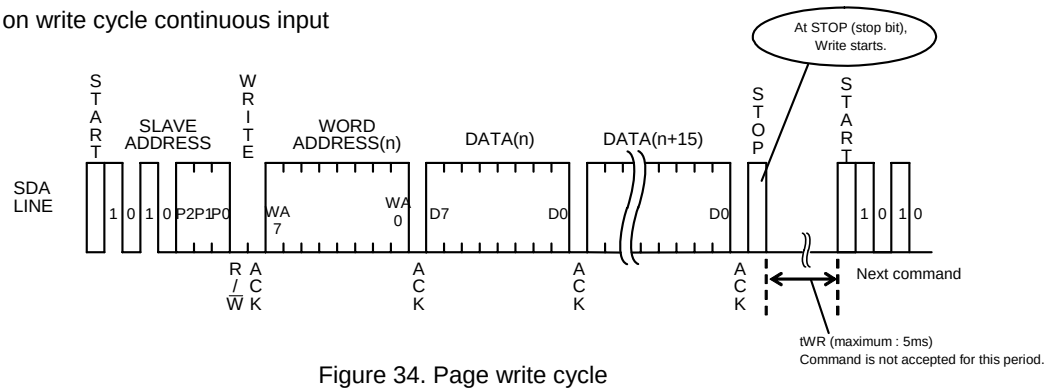


Figure 34. Page write cycle

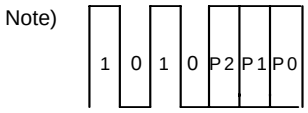


Figure 35. Difference of each type of slave address

3. Notes on page write cycle

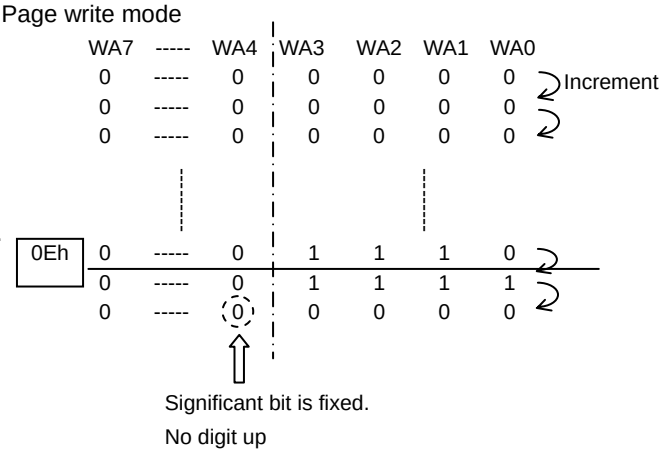
List of numbers of page write

Number of Pages	16Byte
Product number	BU9844GUL-W

The above numbers are maximum bytes for respective types.
Any types below these can be written.

1page = 16 bytes, but the page write cycle write time is 5ms at maximum for 16byte bulk write.
It does not stand 5ms at maximum x 16 bytes = 80ms (Max.).

○Internal address increment
Page write mode



For example, when it is started from address 0Eh, therefore, increment is made as below,
0Eh→0Fh→00h→01h ---, which please note.
*0Eh --- 0E in hexadecimal, therefore, 00001110 becomes a binary number.

4. Write protect terminal (WP)

(1) Write protect function

When WP terminal is set Vcc (H level), data rewrite of all addresses is prohibited. When it is set GND (L level), data rewrite of all addresses is enabled. Be sure to connect this terminal to Vcc or GND, or control it to H level or L level. Do not use it open.

At extremely low voltage at power ON/OFF, by setting the WP terminal “H”, mistake write can be prevented.

During tWR, set the WP terminal always to “L”. If it is set “H”, write is forcibly terminated.

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Command

1. Read cycle

Data of EEPROM is read. In read cycle, there are random read cycle and current read cycle.
Random read cycle is a command to read data by designating address, and is used generally.
Current read cycle is a command to read data of internal address register without designating address, and is used when to verify just after write cycle. In both the read cycles, sequential read cycle is available, and the next address data next address data can be read in succession.

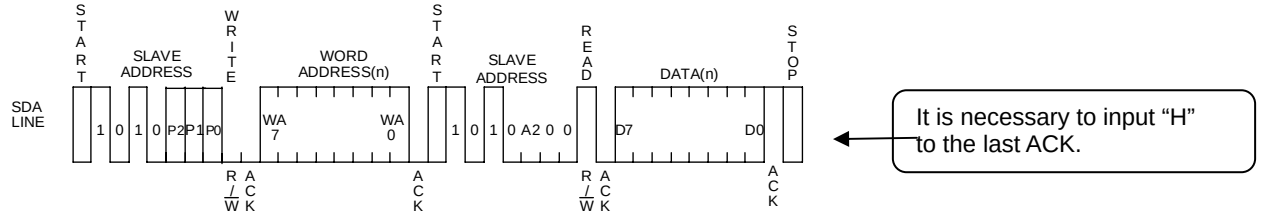


Figure 36. Random Read cycle

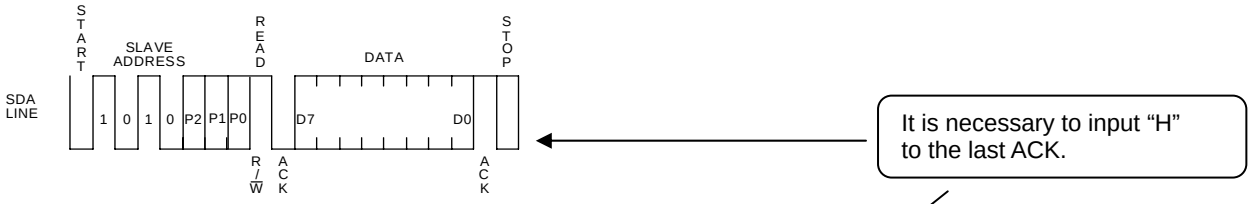


Figure 37. Current read cycle

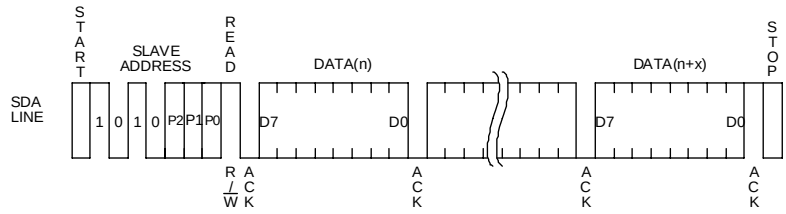


Figure 38. Sequential read cycle

(1) In random read cycle, data of designated word address can be read.
(2) When the command just before current read cycle is random read cycle, current read cycle (each including sequential read cycle), data of incremented last read address (n-th) address, i.e., data of the (n+1)-th address is output.
(3) When ACK signal “LOW” after D0 is detected, and stop condition is not sent from the master (μ-COM) side, the next address data can be read in succession.
(4) Read cycle is ended by stop condition where “H” is input to ACK signal after D0 and SDA signal is started at SCL signal “H”.
(5) When “H” is not input to ACK signal after D0, sequential read gets in, and the next data is output.
Therefore, read command cycle cannot be ended. When to end read command cycle, be sure input stop condition to input “H” to ACK signal after D0, and to start SDA at SCL signal “H”.
(6) Sequential read is ended by stop condition where “H” is input to ACK signal after arbitrary D0 and SDA is started at SCL signal “H”.

Note)

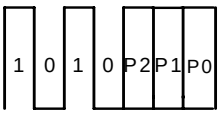


Figure 39. Difference of slave address of each type

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Software reset

Software reset is executed when to avoid malfunction after power on, and to reset during command input. Software reset has several kinds, and 3 kinds of them are shown in the figure below. (Refer to Figure 40-(a), Figure 40-(b) and Figure 40-(c).) In dummy clock input area, release the SDA bus (“H” by pull up). In dummy clock area, ACK output and read data “0” (both “L” level) may be output from EEPROM, therefore, if “H” is input forcibly, output may conflict and over current may flow, leading to instantaneous power failure of system power source or influence upon devices.

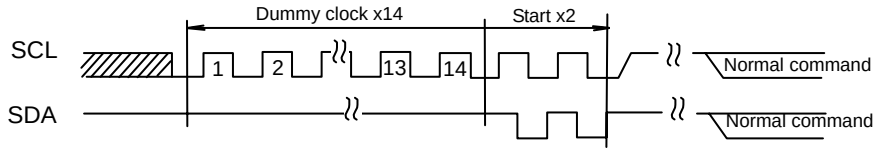


Figure 40-(a) The case of dummy clock + START + START + command input

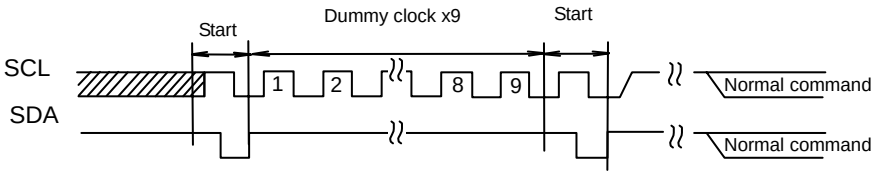


Figure 40-(b) The case of START + 9 dummy clocks + START + command input

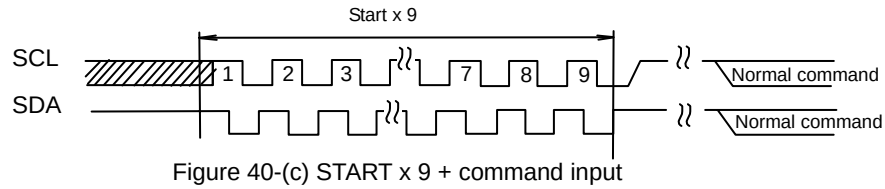


Figure 40-(c) START x 9 + command input

* Start normal command from START input.

Acknowledge polling

During internal write execution, all input commands are ignored, therefore ACK is not sent back. During internal automatic write execution after write cycle input, next command (slave address) is sent, and if the first ACK signal sends back “L”, then it means end of write action, while if it sends back “H”, it means now in writing. By use of acknowledge polling, next command can be executed without waiting for tWR=5ms.

When to write continuously, $R/\overline{W}$ = 0, when to carry out current read cycle after write, slave address $R/\overline{W}$ = 1 is sent, and if ACK signal sends back “L”, then execute word address input and data output and so forth.

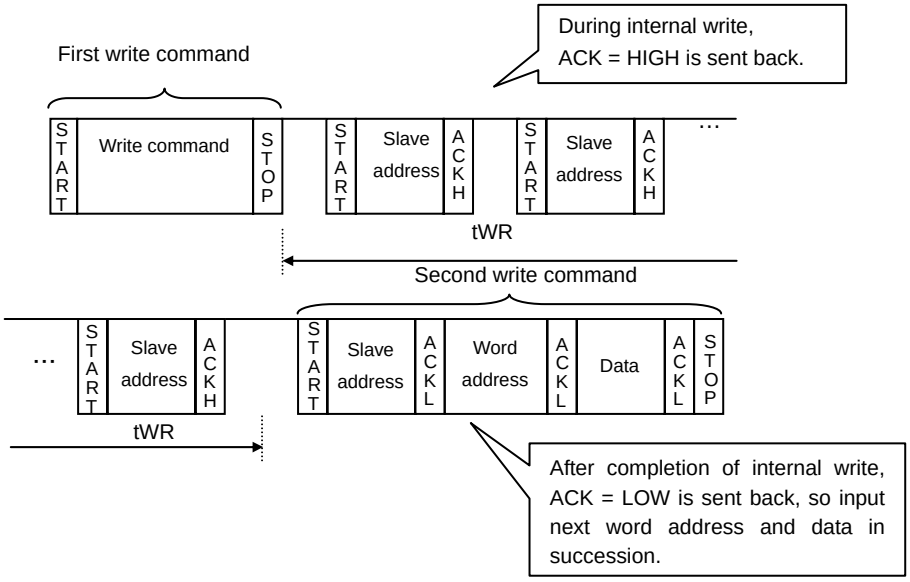


Figure 41. Case to continuously write by acknowledge polling

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WP valid timing (write cancel)

WP is usually to “H” or “L”, but when WP is used to cancel write cycle and so forth, pay attention to the following WP valid timing.

During write cycle execution, in cancel valid area, by setting WP = “H”, write cycle can be cancelled. In both byte write cycle and page write cycle, the area from the first start condition of command to the rise of clock to taken in D0 of data (in page write cycle, the first byte data) is cancel invalid area.

WP input in this area becomes don’t care. Set the setup time to rise of D0 taken SCL 100ns or more. The area from the rise of SCL to take in D0 to the end of internal automatic write (tWR) is cancel valid area. And, when it is set WP = “H” during tWR, write is ended forcibly, data of address under access is not guaranteed, therefore, write it once again. (Refer to Figure 42.) After execution of forced end by WP, standby status gets in, so there is no need to wait for tWR (5ms at maximum).

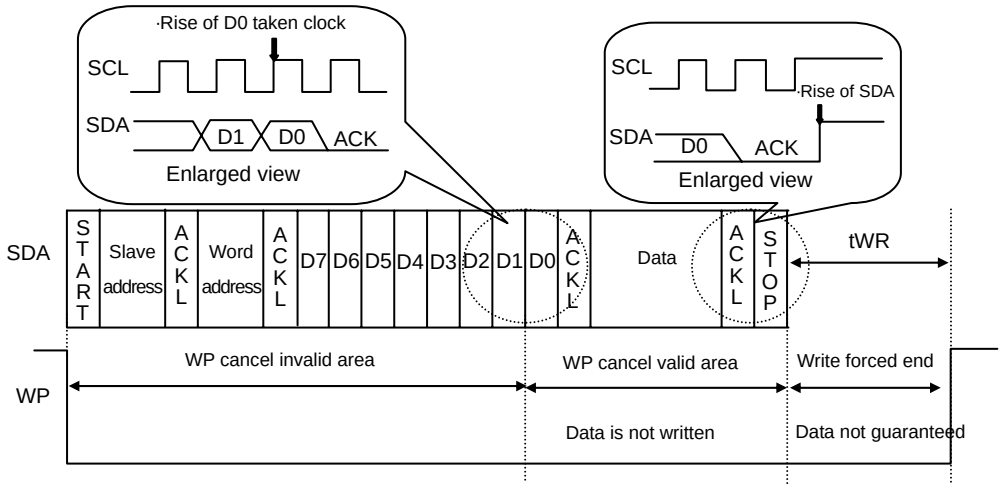


Figure 42. WP valid timing

Command cancel by start condition and stop condition

During command input, by continuously inputting start condition and stop condition, command can be cancelled. (Refer to Figure 43.)

However, in ACK output area and during data read, SDA bus may output “L”, and in this case, start condition and stop condition cannot be input, so reset is not available. Therefore, execute software reset. And when command is cancelled by start, stop condition, during random read cycle, sequential read cycle, or current read cycle, internal setting address is not determined, therefore, it is not possible to carry out current read cycle in succession. When to carry out read cycle in succession, carry out random read cycle.

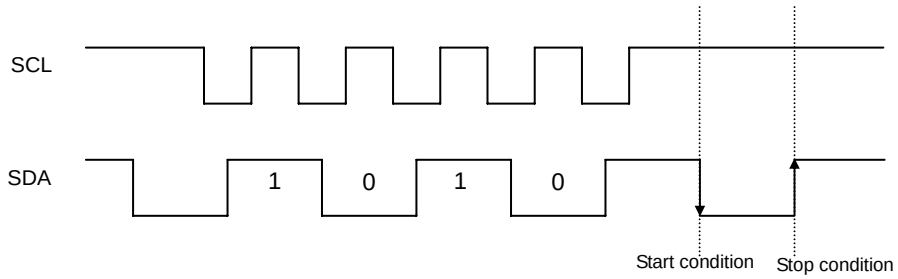


Figure 43. Case of cancel by start, stop condition during slave address input

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I/O peripheral circuit

1. Pull up resistance of SDA terminal

SDA is NMOS open drain, so requires pull up resistance. As for this resistance value (R_{PU}), select an appropriate value to this resistance value from microcontroller V_{IL}, I_L, and V_{OL}-I_{OL} characteristics of this IC. If R_{PU} is large, action frequency is limited. The smaller the R_{PU}, the larger the consumption current at action.

2. Maximum value of R_{PU}

The maximum value of R_{PU} is determined by the following factors.

(1) SDA rise time to be determined by the capacity (CBUS) of bus line of R_{PU} and SDA should be t_R or below. And AC timing should be satisfied even when SDA rise time is late.

(2) The bus electric potential Ⓐ to be determined by input leak total (I_L) of device connected to bus at output of "H" to SDA bus and R_{PU} should sufficiently secure the input "H" level (V_{IH}) of microcontroller and EEPROM including recommended noise margin 0.2Vcc.

$$V_{CC} - I_L R_{PU} - 0.2V_{CC} \geq V_{IH}$$

$$\therefore R_{PU} \leq \frac{0.8V_{CC} - V_{IH}}{I_L}$$

Ex.) When V_{CC} =3V, I_L=10μA, V_{IH}=0.7 Vcc
from (2)

$$\therefore R_{PU} \leq \frac{0.8 \times 3 - 0.7 \times 3}{10 \times 10^{-6}}$$

$$\leq 300 \ [k\Omega]$$

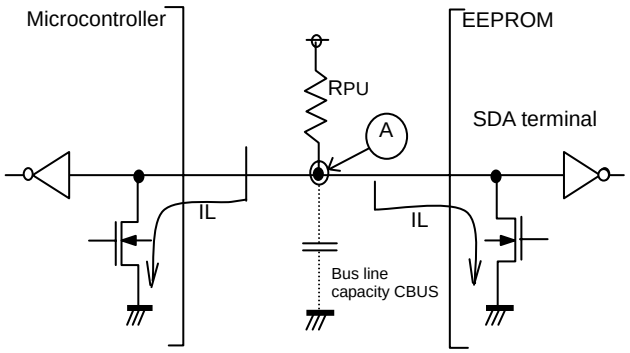


Figure 44. I/O circuit diagram

3. Minimum value of R_{PU}

The minimum value of R_{PU} is determined by the following factors.

(1) When IC outputs LOW, it should be satisfied that V_{OLMAX} = 0.4V and I_{OLMAX} = 3mA.

$$\frac{V_{CC} - V_{OL}}{R_{PU}} \leq I_{OL}$$

$$\therefore R_{PU} \geq \frac{V_{CC} - V_{OL}}{I_{OL}}$$

(2) V_{OLMAX} = 0.4V should secure the input "L" level (V_{IL}) of microcontroller and EEPROM including recommended noise margin 0.1V_{CC}.

$$V_{OLMAX} \leq V_{IL} - 0.1V_{CC}$$

Ex.) When V_{CC} = 3V, V_{OL} = 0.4V, I_{OL} = 3mA, microcontroller, EEPROM V_{IL} = 0.3V_{CC}
From (1),

$$\therefore R_{PU} \geq \frac{3 - 0.4}{3 \times 10^{-3}}$$

$$\geq 867 \quad [\Omega]$$

And $V_{OL} = 0.4 \quad [V]$

$$V_{IL} = 0.3 \times 3$$

$$= 0.9 \quad [V]$$

Therefore, the condition (2) is satisfied.

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4. Pull up resistance of SCL terminal
When SCL control is made at CMOS output port, there is no need, but in the case there is timing where SCL becomes "Hi-Z", add a pull up resistance. As for the pull up resistance, one of several kΩ to several ten kΩ is recommended in consideration of drive performance of output port of microcontroller.

A2, WP process

1. Process of device address terminals (A2)
Check whether the set device address coincides with device address input sent from the master side or not, and select one among plural devices connected to a same bus. Connect this terminal to pull up of pull down, or V_{CC} or GND.

2. Process of WP terminal
WP terminal is the terminal that prohibits and permits write in hardware manner. In "H" status, only READ is available and WRITE of all addresses is prohibited. In the case of "L", both are available. In the case to use it as an ROM, it is recommended to connect it to pull up or V_{CC}. In the case to use both READ and WRITE, control WP terminal or connect it to pull down or GND.

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Cautions on microcontroller connection

1. Rs

In I²C BUS, it is recommended that SDA port is of open drain input / output. However, when to use COMS input / output of tri state to SDA port, insert a series resistance Rs between the pull up resistance R_{PU} and the SDA terminal of EEPROM. This controls over protection of SDA terminal against surge. Therefore, even when SDA port is open drain input / output, Rs can be used.

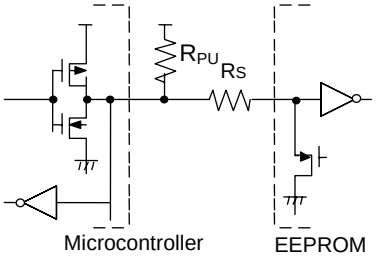


Figure 45. I/O circuit diagram

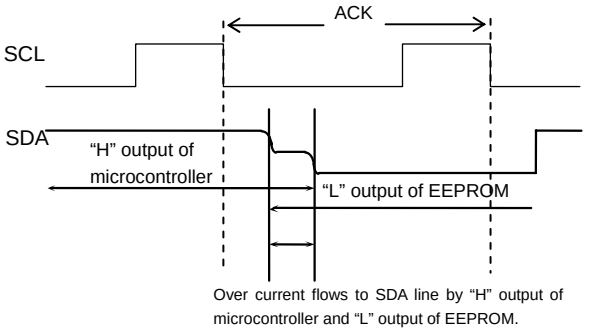


Figure 46. Input / output collision timing

2. Maximum value of Rs

The maximum value of Rs is determined by the following relations.

(1) SDA rise time to be determined by the capacity (CBUS) of bus line of R_{PU} and SDA should be t_R or below. And AC timing should be satisfied even when SDA rise time is late.

(2) The bus electric potential Ⓐ to be determined by R_{PU} and Rs at the moment when EEPROM outputs "L" to SDA bus should sufficiently secure the input "L" level (V_{IL}) of microcontroller including recommended noise margin $0.1V_{CC}$.

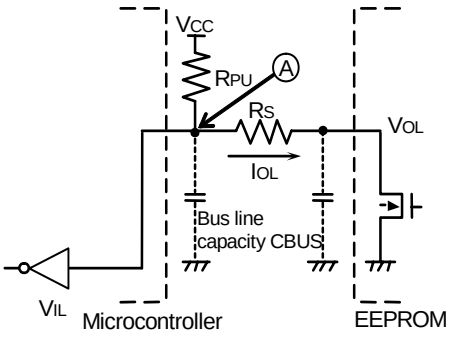


Figure 47. I/O circuit diagram

$$\frac{(V_{CC}-V_{OL})\times R_S}{R_{PU}+R_S}+V_{OL}+0.1V_{CC}\le V_{IL}$$

$$\therefore R_S \le \frac{V_{IL}-V_{OL}-0.1V_{CC}}{1.1V_{CC}-V_{IL}}\times R_{PU}$$

Ex.) When V_{CC}=3V V_{IL}=0.3V_{CC} V_{OL}=0.4V R_{PU}=20kΩ

$$R_S \le \frac{0.3\times 3-0.4-0.1\times 3}{1.1\times 3-0.3\times 3}\times 20\times 10^3$$

$$\le 1.67 \quad [k\Omega]$$

3. Minimum value of Rs

The minimum value of Rs is determined by over current at bus collision. When over current flows, noises in power source line, and instantaneous power failure of power source may occur. When allowable over current is defined as I, the following relation must be satisfied. Determine the allowable current in consideration of impedance of power source line in set and so forth. Set the over current to EEPROM 10mA or below.

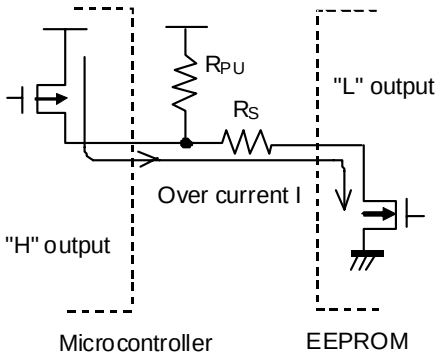


Figure 48. I/O Circuit diagram

$$\frac{V_{CC}}{R_S}\le I$$

$$\therefore Rs \ge \frac{V_{CC}}{I}$$

Ex.) When V_{CC}=3V I=10mA

$$Rs \ge \frac{3}{10\times 10^{-3}}$$

$$\ge 300 \quad [\Omega]$$

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I²C BUS input / output circuit

1. Input (A2, SCL)

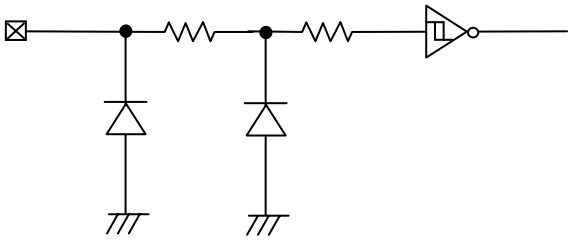


Figure 49. Input pin circuit diagram

2. Input / output (SDA)

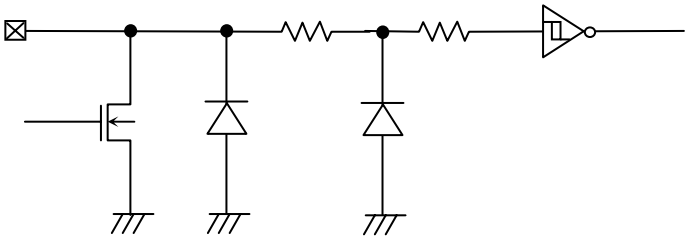


Figure 50. Input / output pin circuit diagram

3. Input (WP)

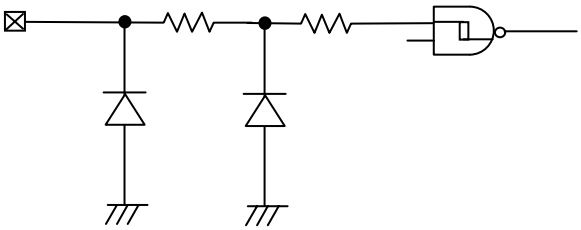


Figure 51. Input pin circuit diagram

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Notes on power ON

At power on, in IC internal circuit and set, Vcc rises through unstable low voltage area, and IC inside is not completely reset, and malfunction may occur. To prevent this, function of POR circuit and LVCC circuit are equipped. To assure the action, observe the following conditions at power on.

1. Set SDA= “H” and SCL = “L” or “H”.
2. Start power source so as to satisfy the recommended conditions of tR, tOFF, and Vbot for operating POR circuit.

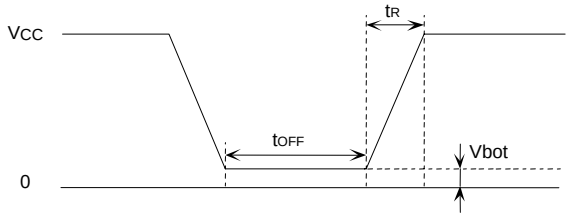


Figure 52. Rise waveform diagram

Recommended conditions of tR, tOFF, Vbot

tR	tOFF	Vbot
10ms or below	10ms or higher	0.3V or below
100ms or below	10ms or higher	0.2V or below

3. Set SDA and SCL so as not to become “Hi-Z”.
   When the above conditions 1 and 2 cannot be observed, take the following countermeasures.
   a) In the case when the above condition 1 cannot be observed. When SDA becomes “L” at power on.
   → Control SCL and SDA as shown below, to make SCL and, “H” and “H”.

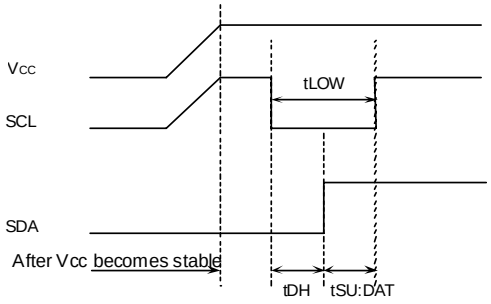


Figure 53. When SCL =”H” and SDA = “L”

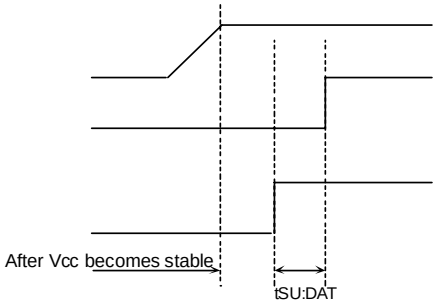


Figure 54. When SCL = “H” and SDA = “L”

   b) In the case when the above condition 2 cannot be observed.
   → After power source becomes stable, execute software reset (Page16).

   c) In the case when the above conditions 1 and 2 cannot be observed.
   → Carry out a), and then carry out b).

Low voltage malfunction prevention function

LVCC circuit prevents data rewrite action at low power, and prevents wrong write. At LVCC voltage (Typ. = 1.2V) or below, it prevent data rewrite.

Vcc noise countermeasures

1. Bypass capacitor
   When noise or surge gets in the power source line, malfunction may occur, therefore, for removing these, it is recommended to attach a by pass capacitor (0.1μF) between IC Vcc and GND. At that moment, attach it as close to IC as possible. And, it is also recommended to attach a bypass capacitor between board Vcc and GND.

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Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Thermal Consideration**
   Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. The absolute maximum rating of the Pd stated in this specification is when the IC is mounted on a 70mm x 70mm x 1.6mm glass epoxy board. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.

6. **Recommended Operating Conditions**
   These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. **Operation Under Strong Electromagnetic Field**
   Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

10. **Inter-pin Short and Mounting Errors**
    Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

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Operational Notes – continued

11. Unused Input Pins

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

12. Regarding the Input Pin of the IC

In the construction of this IC, P-N junctions are inevitably formed creating parasitic diodes or transistors. The operation of these parasitic elements can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions which cause these parasitic elements to operate, such as applying a voltage to an input pin lower than the ground voltage should be avoided. Furthermore, do not apply a voltage to the input pins when no power supply voltage is applied to the IC. Even if the power supply voltage is applied, make sure that the input pins have voltages within the values specified in the electrical characteristics of this IC.

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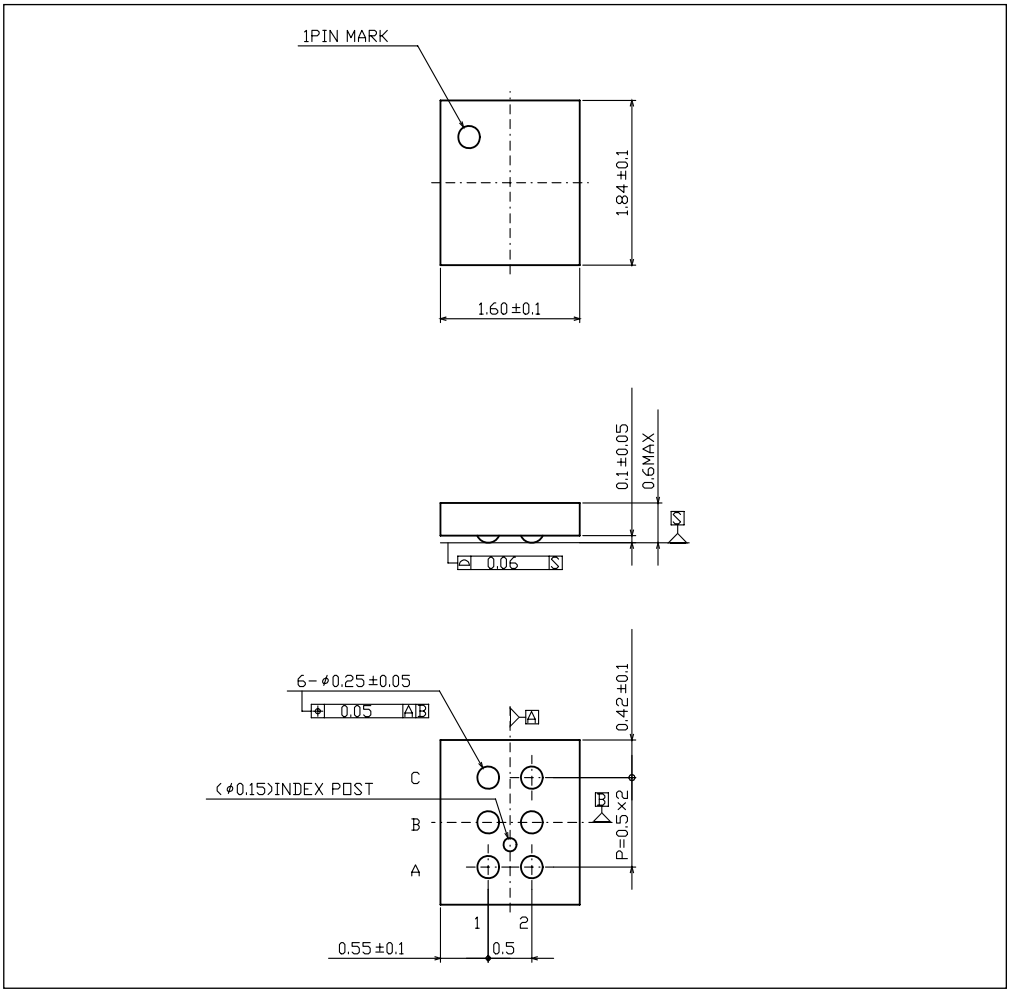
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Ordering Information

B U 9 8 4 4 G U L - W	E 2
Part Number	Package GUL: VCSP50L1(BU9844GUL-W)
	Packaging and forming specification E2: Embossed tape and reel

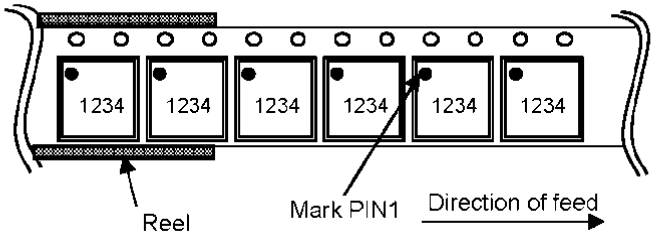
Physical Dimension, Tape and Reel Information

Package Name	VCSP50L1



< Tape and Reel Information >

Tape	Embossed carrier tape
Quantity	3000pcs
Direction of need	E2 The direction is the pin 1 of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand



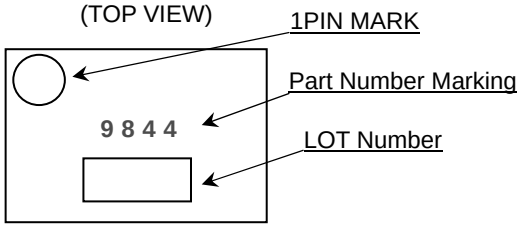
∗ Order quantity needs to be multiple of the minimum quantity.

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Marking Diagram

VCSP50L1(BU9844GUL-W)
(TOP VIEW)



Revision History

Date	Revision	Changes
05.Sep.2012	001	New Release
17.Sep.2013	002	P.1, P.25 Change package height from 0.55MAX to 0.6MAX P.12 Change comment and table of Device addressing. All page document converted to new format.

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(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

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   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

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   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation (Pd) depending on Ambient temperature (Ta). When used in sealed area, confirm the actual ambient temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used; if flow soldering method is preferred, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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Precautions Regarding Application Examples and External Circuits

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2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   - [a] the Products are exposed to sea winds or corrosive gases, including Cl2, H2S, NH3, SO2, and NO2
   - [b] the temperature or humidity exceeds those recommended by ROHM
   - [c] the Products are exposed to direct sunshine or condensation
   - [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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Precaution for Disposition

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