3.3V CMOS Low Jitter XO

FK

3.2 x 2.5mm Ceramic SMD

Product Features

- 1 to 106.25 MHz Frequency Range
- <1 ps RMS jitter
- 3.3V CMOS compatible logic levels
- Designed for standard reflow and washing techniques
- Low power standby mode
- Pb-free and RoHS/Green compliant

Product Description

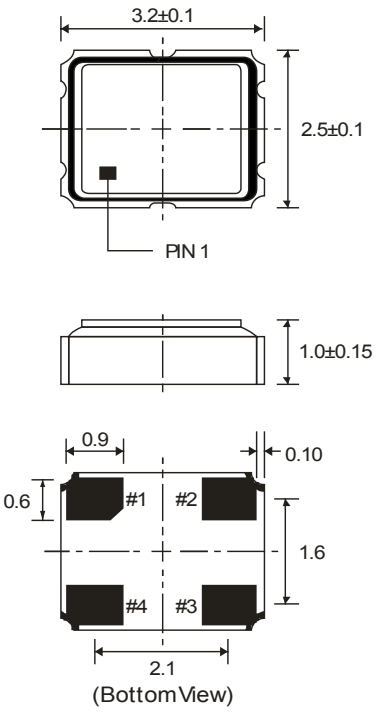
The FK Series 3.3V crystal clock oscillator achieves superb stability and low power consumption over a broad range of operating conditions and frequencies. The low jitter output clock signal, generated internally with a non-PLL oscillator design, is compatible with LVCMOS logic levels. The device, available on tape and reel, is contained in a 3.2 x 2.5mm surface-mount ceramic package.

Applications

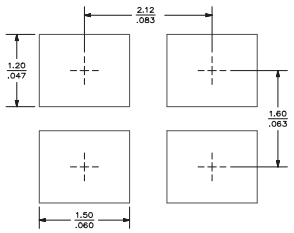
Ideal for compact, high-density applications requiring low power or tight stability, including:

- Network adapter cards
- Portable Multimedia Devices
- Hard Disk Drives
- GPS/Navigation
- Bluetooth
- 802.11a/b/g WiFi

Package:



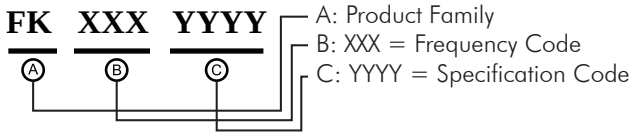
Recommended Land Pattern:



Pin Functions:

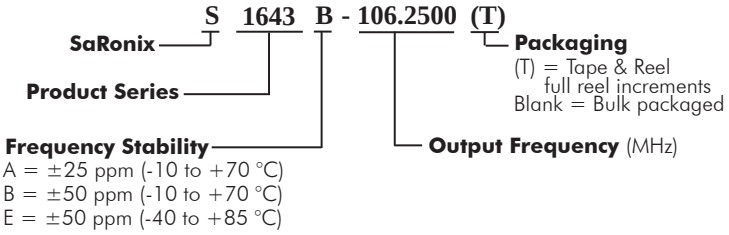
Pin	Function
1	OE Function
2	Ground
3	Clock Output
4	V_{DD}

Part Ordering Information:



Following the above format, Saronix-eCera part numbers will be assigned upon confirmation of exact customer requirements.

Legacy Ordering Information - For Reference Only:



Electrical Performance

Parameter		Min.	Typ.	Max.	Units	Notes
Output Frequency		1		106.25	MHz	As specified
Supply Voltage		2.97	3.3	3.63	V	
Supply Current, Output Enabled				10	mA	1 to 50 MHz
				18		50 to 106.25 MHz
Supply Current, Standby Mode				10	µA	Output Hi-Z
Frequency Stability				±20 to ±50	ppm	See Note 1 below
Operating Temperature Range		-20		+70	°C	Commercial (standard)
		-40		+85		Industrial (standard)
Output Logic 0, V_{OL}				10% V_{DD}	V	
Output Logic 1, V_{OH}		90% V_{DD}			V	
Output Load				15	pF	
Duty Cycle		45		55	%	Measured 50% V_{DD}
Rise and Fall Time				5	ns	Measured 10/90% of waveform
Jitter, Phase	1 to 106.25 MHz			1	ps RMS (1-σ)	10kHz to 20 MHz frequency band
Jitter, Accumulated	up to 75 MHz			5	ps RMS (1-σ)	20.000 adjacent periods
	75 to 106.25 MHz			3		
Jitter, Total	up to 75 MHz			50	ps pk-pk	100.000 random periods
	75 to 106.25 MHz			30		

Notes:
1. Stability includes all combinations of operating temperature, load changes, rated input (supply) voltage changes, initial calibration tolerance (25°C), aging (1 year at 25°C average effective ambient temperature), shock and vibration.
2. For specifications othere than those listed, please contact sales.

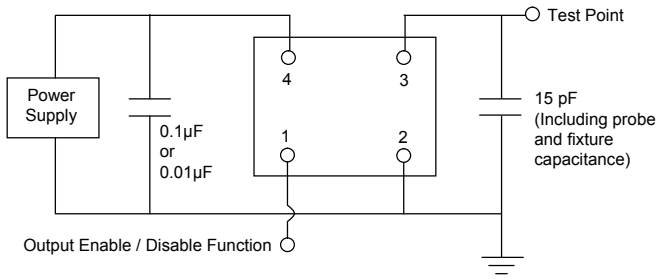
Output Enable / Disable Function

Parameter	Min.	Typ.	Max.	Units	Notes
Input Voltage (pin 1), Output Enable	0.7 V_{DD}			V	or open
Input Voltage (pin 1), Output Disable (low power standby)			0.3 V_{DD}	V	Output is Hi-Z
Internal Pullup Resistance	50			kΩ	
Output Disable Delay			100	ns	
Output Enable Delay			10	ms	

Absolute Maximum Ratings

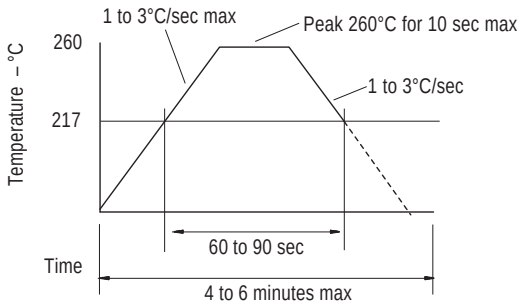
Parameter	Min.	Typ.	Max.	Units	Notes
Storage Temperature	-55		+125	°C	

Test Circuit



Reflow Soldering Profile

As per IPC/JEDEC J-STD-020C



Reliability Test Ratings

This product is rated to meet the following test conditions:

Type	Parameter	Test Condition
Mechanical	Shock	MIL-STD-883, Method 2002, Condition B
Mechanical	Solderability	JESD22-B102-D Method 2 (Preconditioning E)
Mechanical	Terminal strength	MIL-STD-883, Method 2004, Condition D
Mechanical	Gross leak	MIL-STD-883, Method 1014, Condition C
Mechanical	Fine leak	MIL-STD-883, Method 1014, Condition A2 ($R_1 = 2x10^{-8}$ atm cc/s)
Mechanical	Solvent resistance	MIL-STD-202, Method 215
Environmental	Thermal shock	MIL-STD-883, Method 1011, Condition A
Environmental	Moisture resistance	MIL-STD-883, Method 1004
Environmental	Vibration	MIL-STD-883, Method 2007, Condition A
Environmental	Resistance to soldering heat	J-STD-020C Table 5-2 Pb-free devices (2 cycles max)