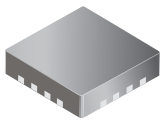
Single LNB Supply and Control Voltage Regulator

Features and Benefits

- Integrated boost MOSFET, current sensing, and compensation
- Supplies up to 500 mA continuously
- Adjustable LNB output current limit from 300 to 500 mA
- Boost peak current limit scales with LNB current limit setting
- 8 programmable LNB output voltage (DAC) levels
- LNB overcurrent limiter with shutdown timer
- Tracking boost converter minimizes power dissipation
- LNB transition times configurable by external capacitor
- Push-pull LNB output stage maintains 13→18 V and 8→13 V transition times, even with highly capacitive loads
- Built-in 22 kHz tone oscillator facilitates DiSEqC™ tone encoding, even at no-load
- Tone generation does not require additional external components
- Diagnostic features: PNG
- Extensive protection features: UVLO, OCP, TSD, CPOK
- 2-wire I²C-compatible interface

Package: 16-contact MLP/QFN (suffix ES)

3 mm × 3 mm × 0.75 mm



Description

Intended for analog and digital satellite receivers, this single low noise block converter regulator (LNBR) is a monolithic linear and switching voltage regulator, specifically designed to provide the power and the interface signals to an LNB down converter via coaxial cable. The A8296 requires few external components, with the boost switch and compensation circuitry integrated inside of the device.

The A8296 has been designed for high efficiency, utilizing the Allegro® advanced BCD process. The integrated boost switch has been optimized to minimize both switching and static losses. To further enhance efficiency, the voltage drop across the tracking regulator has been minimized.

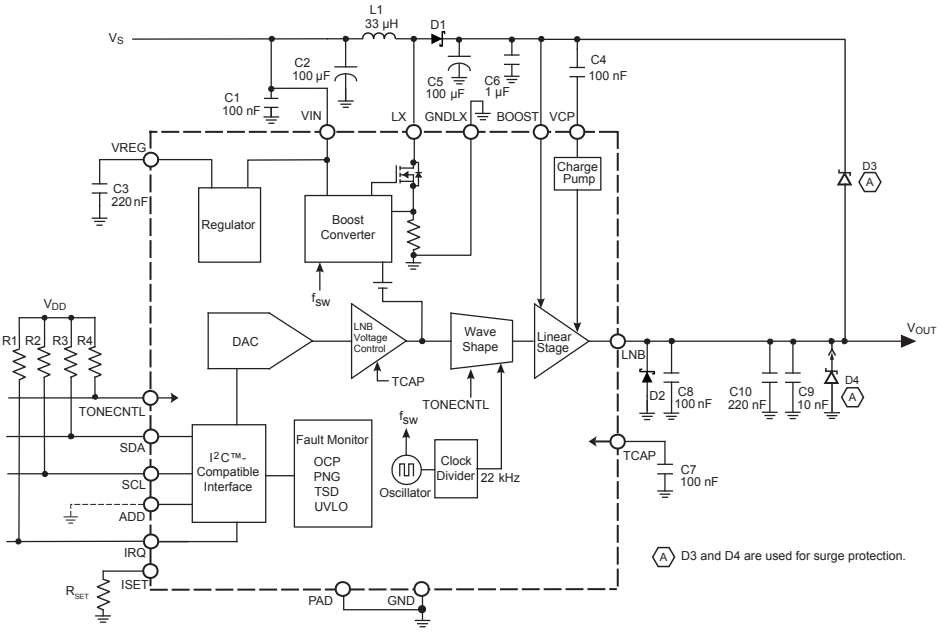
For DiSEqC™ communications, a tone control pin is provided to gate the internally-generated 22 kHz tone on-and-off.

A comprehensive set of fault registers are provided, which comply with all the common standards, including: overcurrent, thermal shutdown, undervoltage, and power not good. Furthermore, design methodology and structure ensure the highest level of robustness against transients and component failures.

The device uses a 2-wire bidirectional serial interface, compatible with the I²C™ standard, that operates up to 400 kHz.

The A8296 is supplied in a lead (Pb) free package.

Functional Block Diagram



For recommended external components, refer to table 5

Selection Guide

Part Number	Packing[a]	Description
A8296SESTR-T[b]	7 in. reel, 1500 pieces/reel 12 mm carrier tape	MLP/QFN surface mount 3 mm × 3 mm × 0.75 mm nominal height

[a]Contact Allegro for additional packing options.

[b]Leadframe plating 100% matte tin.

Absolute Maximum Ratings

Characteristic	Symbol	Conditions	Rating	Units
Load Supply Voltage, VIN pin	V_{IN}		30	V
Output Current*	I_{OUT}		Internally Limited	A
Output Voltage; LNB and BOOST pins			–0.3 to 33	V
Output Voltage; LX pin			–0.3 to 30	V
Output Voltage; VCP pin			–0.3 to 41	V
Logic Input Voltage			–0.3 to 5.5	V
Logic Output Voltage			–0.3 to 5.5	V
Operating Ambient Temperature	T_A	Range S	–20 to 85	°C
Junction Temperature	T_J(max)		150	°C
Storage Temperature	T_{stg}		–55 to 150	°C

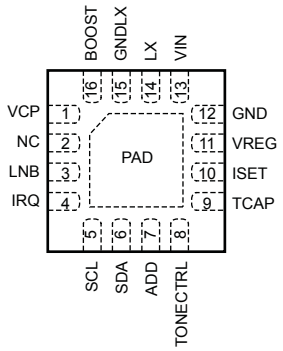
*Output current rating may be limited by duty cycle, ambient temperature, and heat sinking. Under any set of conditions, do not exceed the specified current ratings, or a junction temperature, T_J, of 150°C.

Package Thermal Characteristics*

Package	$R_{\theta JA}$ (°C/W)	PCB
ES	47	4-layer

* Additional information is available on the Allegro website.

Device Pin-out Diagram



Terminal List Table

Name	Number	Function
ADD	7	Address select
BOOST	16	Tracking supply voltage to linear regulator
GND	12	Signal ground
GNDLX	15	Boost switch ground
IRQ	4	Interrupt request
ISET	10	Output current limit set via external resistor
LNB	3	Output voltage to LNB
LX	14	Inductor drive point
NC	2	No connection
PAD	Pad	Exposed pad; connect to the ground plane, for thermal dissipation
SCL	5	I²C™-compatible clock input
SDA	6	I²C™-compatible data input/output
TCAP	9	Capacitor for setting the rise and fall time of the LNB output
TONECTRL	8	Gates the 22 kHz tone on-and-off
VCP	1	Gate supply voltage
VIN	13	Supply input voltage
VREG	11	Analog supply

ELECTRICAL CHARACTERISTICS[1] at T_A = 25°C, V_{IN} = 10 to 16 V, • as noted[2]; unless noted otherwise

Characteristics	Symbol	Test Conditions		Min.	Typ.	Max.	Units
General							
Output Voltage Accuracy	V_{OUT}	V_{IN} = 12 V, I_{OUT} = 50 mA, see table 2 for DAC settings	•	–2.6	–	2.6	%
Load Regulation	$\Delta V_{OUT(Load)}$	V_{IN} = 12 V, V_{OUT} = 13.667 V, ΔI_{OUT} = 50 to 450 mA	•	–	38	76	mV
		V_{IN} = 12 V, V_{OUT} = 19.000 V, ΔI_{OUT} = 50 to 450 mA	•	–	45	90	mV
Line Regulation	$\Delta V_{OUT(Line)}$	V_{IN} = 10 to 16 V, V_{OUT} = 13.667 V, I_{OUT} = 50 mA	•	–10	0	10	mV
		V_{IN} = 10 to 16 V, V_{OUT} = 19.000 V, I_{OUT} = 50 mA	•	–10	0	10	mV
Supply Current	$I_{IN(OFF)}$	ENB = 0, V_{IN} = 12 V	•	–	4	7	mA
	$I_{IN(ON)}$	ENB = 1, V_{IN} = 12 V, V_{OUT} = 19 V, I_{LOAD} = 0 mA, TONECTRL = 0	•	–	9	12	mA
		ENB = 1, V_{IN} = 12 V, V_{OUT} = 19 V, I_{LOAD} = 0 mA, TONECTRL = 1	•	–	15	23	mA
Boost Switch On Resistance	$R_{DS(on)BOOST}$	I_{LOAD} = 450 mA		–	300	–	mΩ
Switching Frequency	f_{SW}			320	352	384	kHz
Linear Regulator Voltage Drop	ΔV_{REG}	$V_{BOOST} - V_{LNB}$, no tone signal, I_{LOAD} = 425 mA		600	800	1000	mV
TCAP Pin Current	I_{CHG}	TCAP capacitor (C7) charging		–13	–10	–7	µA
	I_{DISCHG}	TCAP capacitor (C7) discharging		7	10	13	µA
Output Voltage Rise Time[3]	$t_{r(VLNB)}$	For V_{LNB} 13→19 V; C_{TCAP} = 100 nF, I_{LOAD} = 500 mA		–	10	–	ms
Output Voltage Pull-Down Time[3]	$t_{f(VLNB)}$	For V_{LNB} 19→13 V; C_{LOAD} = 100 µF, I_{LOAD} = 0 mA		–	20	–	ms
Output Reverse Current	I_{RLNB}	ENB = 0, VLNB = 21 V, Boost capacitor fully charged		–	2	4	mA
		ENB = 1, $VSEL_{2,1,0}$ = 001 (13.667 V), VLNB = 21 V, TONECNTL = 0 or 1		–	9	12	mA
		ENB = 1, $VSEL_{2,1,0}$ = 100 (19.000 V), VLNB = 21 V, TONECNTL = 0 or 1		–	9	12	mA
		ENB = 1, $VSEL_{2,1,0}$ = 001 (13.667 V), 13.4 V < VLNB <14.9 V, TONECNTL = 0 or 1		–	–	150	mA
		ENB = 1, $VSEL_{2,1,0}$ =100 (19.000 V), 18.6 V < VLNB < 20.4 V, TONECNTL = 0 or 1		–	–	150	mA

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ELECTRICAL CHARACTERISTICS[1] (continued) at T_A = 25°C, V_{IN} = 10 to 16 V, • as noted[2]; unless noted otherwise

Characteristics	Symbol	Test Conditions		Min.	Typ.	Max.	Units
General (continued)							
Ripple and Noise on LNB Output[4]	$V_{rip,n(pp)}$	20 MHz BWL; reference circuit shown in Functional Block diagram; contact Allegro for additional information on application circuit board design		–	30	–	mV_{PP}
VREG Voltage	V_{VREG}	V_{IN} = 10 V		4.97	5.25	5.53	V
ISET Voltage	V_{ISET}	V_{IN} = 10 V		3.4	3.5	3.6	V
TCAP Voltage	V_{TCAP}	V_{IN} = 10 V, V_{OUT} = 13.667 V		2.18	2.25	2.32	V
		V_{IN} = 10 V, V_{OUT} = 19.000 V		3.05	3.14	3.23	V
Protection Circuitry							
Output Overcurrent Limit[5]	$I_{OUT(MAX)}$	R_{SET} = 100 kΩ	•	250	300	350	mA
		R_{SET} = 60.4 kΩ	•	450	500	550	mA
Overcurrent Disable Time	t_{DIS}			–	45	–	ms
Boost MOSFET Current Limit	$I_{BOOST(MAX)}$	R_{SET} = 100 kΩ		1850	2250	2650	mA
		R_{SET} = 60.4 kΩ		2500	3000	3500	mA
VIN Undervoltage Lockout Threshold	V_{UVLO}	V_{IN} falling		8.05	8.35	8.65	V
VIN Turn On Threshold	$V_{IN(th)}$	V_{IN} rising		8.40	8.70	9.00	V
Undervoltage Hysteresis	$V_{UVLOHYS}$			–	350	–	mV
Thermal Shutdown Threshold[3]	T_J			–	165	–	°C
Thermal Shutdown Hysteresis[3]	ΔT_J			–	20	–	°C
Power Not Good (Low)	PNG_{LOSET}	With respect to V_{LNB} setting; V_{LNB} low, PNG set to 1		88	91	94	%
	$PNG_{LORESET}$	With respect to V_{LNB} setting; V_{LNB} low, PNG reset to 0		92	95	98	%
Power Not Good (Low) Hysteresis	PNG_{LOHYS}	With respect to V_{LNB} setting		–	4	–	%
Power Not Good (High)	PNG_{HISET}	With respect to V_{LNB} setting; V_{LNB} high, PNG set to 1		106	109	112	%
	$PNG_{HIRESET}$	With respect to V_{LNB} setting; V_{LNB} high, PNG reset to 0		102	105	108	%
Power Not Good (High) Hysteresis	PNG_{HIHYS}	With respect to V_{LNB} setting		–	4	–	%
Tone							
Amplitude	$V_{TONE(PP)}$	I_{LNB} = 0 to 425 mA, C_{LNB} = 750 nF	•	400	650	900	mV_{PP}
Frequency	f_{TONE}		•	20	22	24	kHz
Duty Cycle	DC_{TONE}			40	50	60	%
Rise Time	$t_{R(TONE)}$			5	10	15	µs
Fall Time	$t_{F(TONE)}$			5	10	15	µs

Continued on the next page…

ELECTRICAL CHARACTERISTICS[1] (continued) at T_A = 25°C, V_{IN} = 10 to 16 V, • as noted[2]; unless noted otherwise

Characteristics	Symbol	Test Conditions		Min.	Typ.	Max.	Units
Tone Control (TONECTRL)							
Logic Input	V_H			2.0	–	–	V
	V_L			–	–	0.8	V
Input Leakage				–1	–	1	µA
I²C™-Compatible Interface							
Logic Input (SDA,SCL) Low Level	$V_{SCL(L)}$			–	–	0.8	V
Logic Input (SDA,SCL) High Level	$V_{SCL(H)}$			2.0	–	–	V
Logic Input Hysteresis	$V_{I2CIHYS}$			–	150	–	mV
Logic Input Current	I_{I2CI}	V_{I2CI} = 0 to 5 V		–10	<±1.0	10	µA
Logic Output Voltage SDA and IRQ	$V_{t2COut(L)}$	I_{LOAD} = 3 mA		–	–	0.4	V
Logic Output Leakage SDA and IRQ	V_{t2CLKG}	V_{t2COut} = 0 to 5 V		–	–	10	µA
SCL Clock Frequency	f_{CLK}			–	–	400	kHz
I²C™ Address Setting							
ADD Voltage for Address 0001,000	Address1			0	–	0.7	V
ADD Voltage for Address 0001,001	Address2			1.3	–	1.7	V
ADD Voltage for Address 0001,010	Address3			2.3	–	2.7	V
ADD Voltage for Address 0001,011	Address4			3.3	–	5.0	V

[1]Operation at 16 V may be limited by power loss in the linear regulator.
[2]Indicates specifications guaranteed from $0 \le T_J \le 125^\circ C_{MIN}$, (design goal is $0 \le T_J \le 150^\circ C$).
[3]Guaranteed by worst case process simulations and system characterization. Not production tested.
[4]LNB output ripple and noise are dependent on component selection and PCB layout. Refer to the Application Schematic and PCB layout recommendations. Not production tested.
[5]Current from the LNB output may be limited by the choice of Boost components.

Functional Description

Protection

The A8296 has a wide range of protection features and fault diagnostics which are detailed in the Status Register section.

Boost Converter/Linear Regulator

The A8296 solution contains a tracking current-mode boost converter and linear regulator. The boost converter tracks the requested LNB voltage to within 800 mV, to minimize power dissipation. Under conditions where the input voltage, V_{BOOST}, is greater than the output voltage, V_{LNB}, the linear regulator must drop the differential voltage. When operating in these conditions, care must be taken to ensure that the safe operating temperature range of the A8296 is not exceeded.

The boost converter operates at 352 kHz typical: 16 times the internal 22 kHz tone frequency. All the loop compensation, current sensing, and slope compensation functions are provided internally.

The A8296 has internal pulse-by-pulse current limiting on the boost converter and DC current limiting on the LNB output to protect the IC against short circuits. When the LNB output is shorted, the LNB output current is limited and the IC will be shut down if the overcurrent condition lasts for more than 48 ms. If this occurs, the A8296 must be reenabled for normal operation. The system should provide sufficient time between successive restarts to limit internal power dissipation; a minimum of 5 s is recommended.

At extremely light loads, the boost converter operates in a pulse-skipping mode. Pulse skipping occurs when the BOOST voltage rises to approximately 450 mV above the BOOST target output voltage. Pulse skipping stops when the BOOST voltage drops 200 mV below the pulse skipping level.

In the case that two or more set top box LNB outputs are connected together by the customer (e.g., with a splitter), it is possible that one output could be programmed at a higher voltage than the other. This would cause a voltage on one output that is higher than its programmed voltage (e.g., 19 V on the output of a 13 V programmed voltage). The output with the highest voltage will effectively turn off the other outputs. As soon as this voltage is reduced below the value of the other outputs, the A8296 output will auto-recover to their programmed levels.

Charge Pump. Generates a supply voltage above the internal tracking regulator output to drive the linear regulator control.

LNB and BOOST Current Limits. The LNB output current limit, $I_{OUT(MAX)}$ can be set by connecting a resistor (RSET) from the ISET pin to GND as shown in the applications schematic. The LNB current limit can be set from 300 to 500 mA, corresponding to an R_{SET} value of 100 to 60.4 kΩ, respectively. If the LNB current limit is exceeded for more than the Overcurrent Disable Time (t_{DIS}) then the A8296 will be shut down and the OCP bit set, as shown in figure 1. The LNB output current limit can be set as high as 600 mA (R_{SET} = 49.9 kΩ) but care should be taken not to exceed the thermal limit of the package or thermal shutdown (TSD) will occur. The A8296 is guaranteed to support $I_{OUT} \geq 425$ mA continuously at 70ºC ambient with V_{IN} = 10 V and V_{OUT} = 20 V. The typical LNB output current limit can be set according to the following equation:

$$I_{OUT(MAX)} = 29{,}925 / R_{SET} \ ,$$

where $I_{OUT(MAX)}$ is in mA and R_{SET} is in kΩ. If the voltage at the ISET pin is 0 V (that is, shorted to GND), $I_{OUT(MAX)}$ will be clamped to a moderately high value (approximately 1.5 A). Care should be taken to ensure that ISET is not inadvertently grounded. If no resistor is connected to the ISET pin (that is, if ISET is open-circuit), $I_{OUT(MAX)}$ will be set to approximately 0 A and the A8296 will not support any load (OCP will occur prematurely).

The BOOST pulse-by-pulse current limit, $I_{BOOST(MAX)}$, is automatically scaled along with the LNB output current limit. The typical BOOST current limit is set according to the following equation:

$$I_{BOOST(MAX)} = 3.0 \times I_{OUT(MAX)} + 900 \text{ mA} \ ,$$

where both $I_{BOOST(MAX)}$ and $I_{OUT(MAX)}$ are in mA.

Automatically scaling the BOOST current limit allows the designer to choose the lowest possible saturation current of the boost inductor, reducing its physical size and PCB area, thus minimizing cost.

Slew Rate Control. During either start-up, or when the output voltage at the LNB pin is transitioning, the output voltage rise and fall times can be set by the value of the capacitor connected from the TCAP pin to GND (C_{TCAP} or C7 in the Applications Schematic). Note that during start-up, the BOOST pin is pre-

charged to the input voltage minus a voltage drop. As a result, the slew rate control for the BOOST pin occurs from this voltage.

The value of C_{TCAP} can be calculated using the following formula:

$$C_{TCAP} = (I_{TCAP} \times 6) / SR \ ,$$

where SR is the required slew rate of the LNB output voltage, in V/s, and I_{TCAP} is the TCAP pin current specified in the data sheet. The recommended value for C_{TCAP}, 100 nF, should provide satisfactory operation for most applications.

The minimum value of C_{TCAP} is 10 nF. There is no theoretical maximum value of C_{TCAP} however too large a value will probably cause the voltage transition specification to be exceeded. Tone generation is unaffected by the value of C_{TCAP}.

Pull-Down Rate Control. In applications that have to operate at very light loads and that require large load capacitances (in the order of tens to hundreds of microfarads), the output linear stage provides approximately 40 mA of pull-down capability. This ensures that the LNB output voltage is ramped from 18 to 13 V in a reasonable amount of time. When the tone is on (TONECNTL = 1), the output linear stage must increase its pull-down capability to approximately 70 mA. This ensures that the tone signal meets all specifications, even with no load on the on the LNB output.

ODT (Overcurrent Disable Time)

If the LNB output current exceeds the set output current, for more than 48 ms, then the LNB output will be disabled and the OCP bit will be set. See figure 1.

Short Circuit Handling

If the LNB output is shorted to ground, the LNB output current will be clamped to $I_{OUT(MAX)}$. If the short circuit condition lasts for more than 48 ms, the A8296 will be disabled and the OCP bit will be set.

Auto-Restart

After a short circuit condition occurs, the host controller should periodically reenable the A8296 to check if the short circuit has been removed. Consecutive startup attempts should allow at least 5 s of delay between restarts.

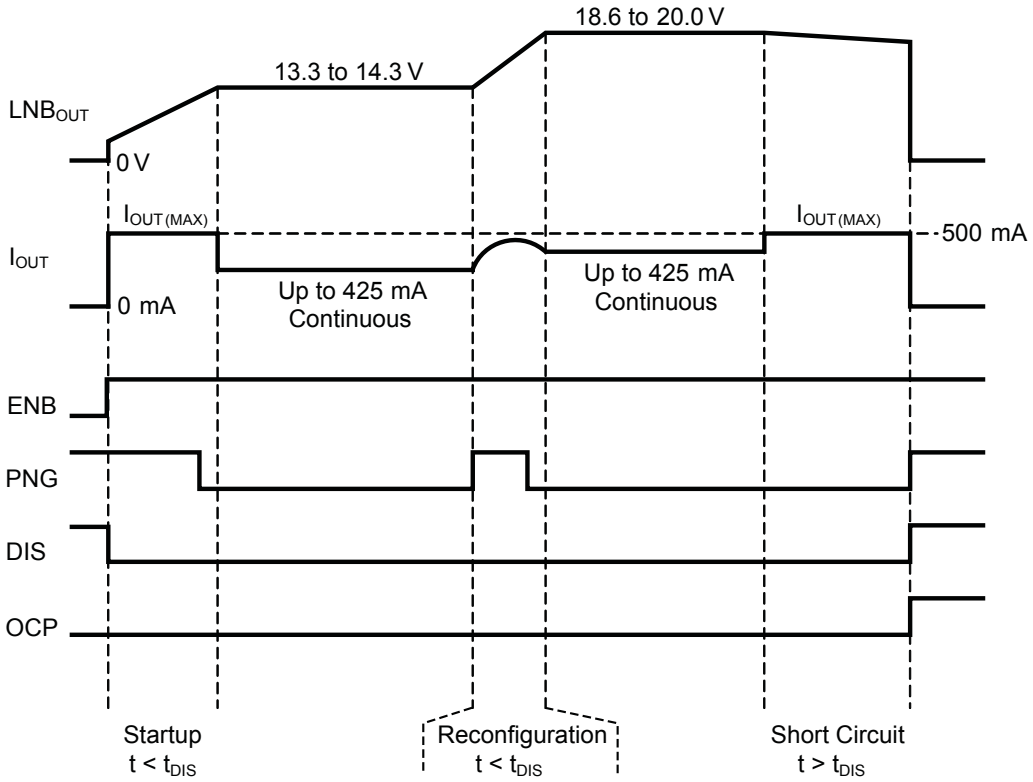


Figure 1. Startup, Reconfiguration, and Short Circuit operation using $I_{OUT(MAX)}$ = 500 mA, R_{SET} = 86.6 kΩ, and a capacitive load.

In-Rush Current

At start-up or during an LNB reconfiguration event, a transient surge current above the normal DC operating level can be provided by the A8296. This current increase can be as high as the set output current, for as long as required, up to a maximum of 48 ms.

Tone Generation

A 22 kHz tone is generated internally, and can be controlled on and off via the TONECTRL pin as shown in figure 2. Note this tone can be generated under no-load conditions, and does not require the use of an external DiSEqC filter.

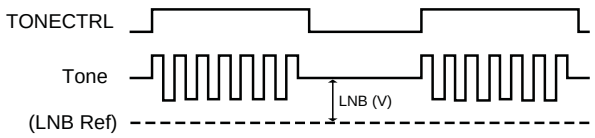


Figure 2. Internal tone, gated by TONECTRL pin

Component Selection

Boost Inductor

The A8296 is designed to operate with a boost inductor value of 33 µH ±50%. The error amplifier loop compensation, current sense gain, and PWM slope compensation were chosen for this value of inductor. The boost inductor must be able to support the peak currents required to maintain the maximum LNB output current without saturating. Figure 3 can be used to determine the peak current in the inductor given the LNB load current. The "typical" curve uses V_{IN} = 12 V, V_{OUT} = 19 V, L = 33 µH, and f = 352 kHz, while the "maximum" curve assumes V_{IN} = 9 V, V_{OUT} = 20 V, L = 26 µH, and f = 282 kHz.

Boost Electrolytic Capacitor

The A8296 is designed to operate with a low-ESR electrolytic boost capacitor of 100 µF ±25%. The ESR of the boost capacitor must be less than 100 mΩ or the boost converter will be unstable. General purpose electrolytic capacitors that do not specify an ESR should be avoided. Allegro recommends an electrolytic capacitor that is rated to support at least 35 V and has an rms current rating to support the maximum LNB load. Figure 4 can be used to determine the necessary rms current rating of the boost capacitor given the LNB load current. The "typical" curve uses

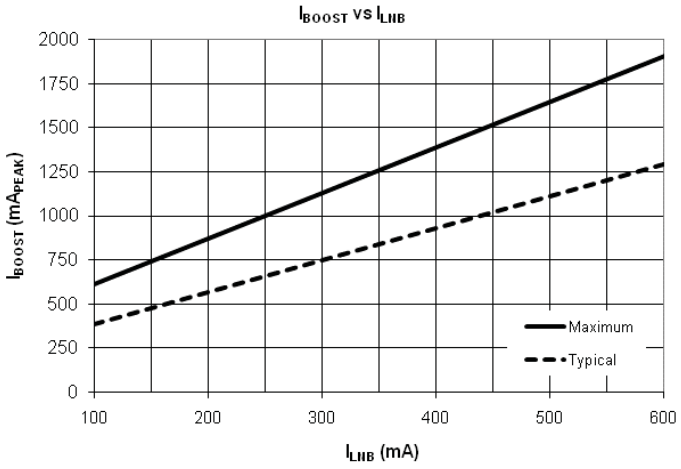


Figure 3. Boost inductor characteristic for the A8296.

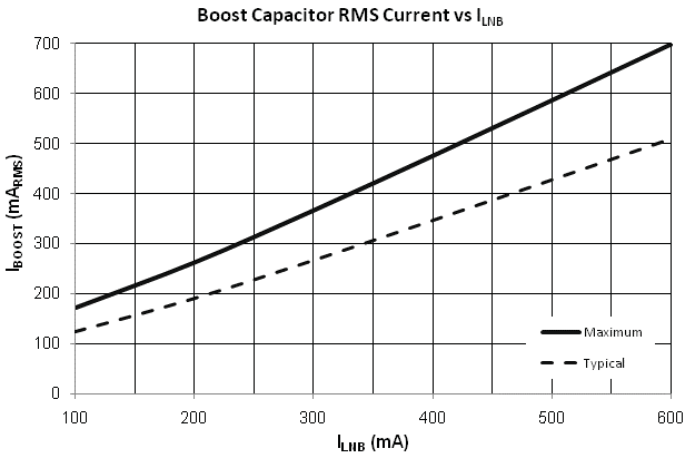


Figure 4. Boost electrolytic capacitor characteristic for the A8296.

V_{IN} = 12 V, V_{OUT} = 19 V, L = 33 µH, and f = 352 kHz while the "maximum" curve assumes V_{IN} = 9 V, V_{OUT} = 20 V, L = 26 µH, and f = 282 kHz.

Boost Filtering and LNB Noise

The LNB output noise depends on the amount of high-frequency noise at the BOOST pin. To minimize the high-frequency noise at the BOOST pin, a high quality ceramic capacitor should be placed as close as possible to the BOOST pin. Allegro recommends a 1 µF, 10% or 20%, X5R or X7R, 1206 size capacitor, with at least a 25 V rating.

For very noise-sensitive applications, a secondary boost inductor can be added between the 100 µF and the 1 µF boost capacitors, as shown in figure 5. This inductor should be approximately 1 µH and have a DC current rating of at least 1 ADC. Adding the 1 µH inductor has been shown to reduce the LNB output noise by as much as 50%. Allegro strongly recommends having provisions for this 1 µH inductor in the PCB layout, but only populating it if the LNB output is found to have too much noise after measuring at the set-top box F-connector, at full-load.

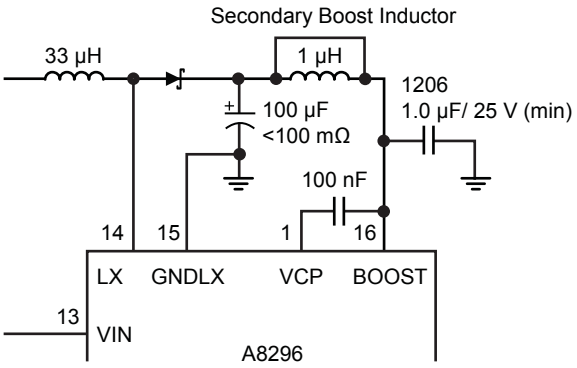


Figure 5. Application of the secondary boost inductor

Surge Components

The circuit shown on page 1 of this datasheet includes D3 and D4 for surge protection. Component recommendations for D3 and D4 are given in the bill-of-materials at the end of this datasheet. This configuration and these components have successfully passed surge tests up to ±1000 V/500 A, with a 1.2/50 µs − 8/20 µs combination wave. Every application will have its own surge requirements and the surge solution can be changed. However, Allegro strongly recommends incorporating a form of surge protection to prevent any pin of the A8296 from exceeding its Absolute Maximum voltage ratings shown in this datasheet.

I²C™-Compatible Interface

The I²C™ interface is used to access the internal Control and Status registers of the A8296. This is a serial interface that uses two lines, serial clock (SCL) and serial data (SDA), connected to a positive supply voltage via a current source or a pull-up resistor. Data is exchanged between a microcontroller (master) and the A8296 (slave). The master always generates the SCL signal. Either the master or the slave can generate the SDA signal. The SDA and SCL lines from the A8296 are open-drain signals so multiple devices may be connected to the I²C™ bus. When the bus is free, both the SDA and the SCL lines are high.

SDA and SCL Signals. SDA can only be changed while SCL is low. SDA must be stable while SCL is high. However, an exception is made when the I²C™ Start or Stop condition is encountered. See the I²C™ Communication section for further details.

Acknowledge (AK) Bit. The Acknowledge (AK) bit indicates a "good transmission" and can be used two ways. First, if the slave has successfully received eight bits of either an address or control data, it will pull the SDA line low (AK = 0) for the ninth SCL pulse to signal "good transmission" to the master. Second, if the master has successfully received eight bits of status data from the A8296, it will pull the SDA line low for the ninth SCL pulse to

signal “good transmission” to the slave. The receiver (either the master or the slave) should set the AK bit high (AK = 1 or NAK) for the ninth SCL pulse if eight bits of data are not received successfully.

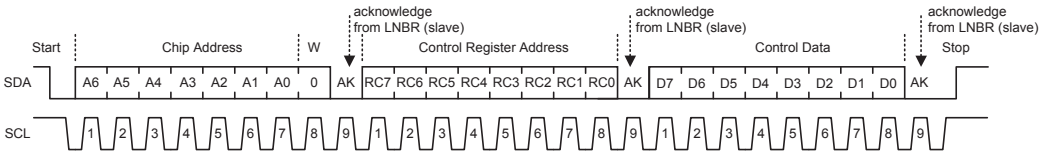
AK Bit During a Write Sequence. When the master sends control data (writes) to the A8296 there are three instances where AK bits are toggled by the A8296. First, the A8296 uses the AK bit to indicate reception of a valid seven-bit chip address plus a read/write bit (R/W = 0 for write). Second, the A8296 uses the AK bit to indicate reception of a valid eight-bit Control register address. Third, the A8296 uses the AK bit to indicate reception of eight bits of control data. This protocol is shown in figure 6(a).

AK Bit During a Read Sequence. When the master reads status data from the A8296 there are four instances where AK bits are sent–three sent by the A8296 and one sent by the master. First, the A8296 uses the AK bit to indicate reception of a valid seven-bit chip address plus a read/write bit (R/W = 0 for write). Second, the A8296 uses the AK bit to indicate reception of a valid eight-bit status register address. Third, the A8296 uses the AK bit to indicate reception of a valid seven-bit chip address plus a read/write bit (R/W = 1 for read). Finally, the master uses the AK bit to indicate receiving eight bits of status data from the A8296. This protocol is shown in figure 6(b).

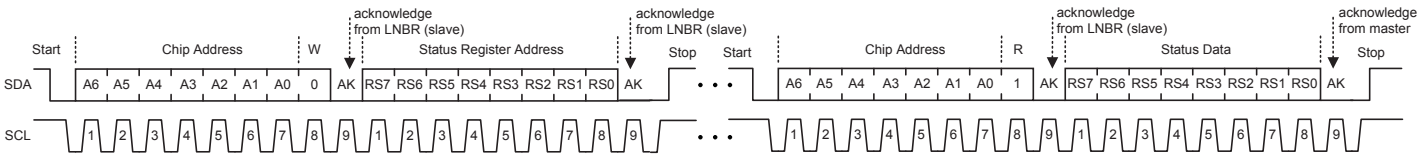
I²C™ Communications

I²C™ Start and Stop Conditions. The I²C™ Start condition is defined by a negative edge on the SDA line while SCL is high. Conversely, the Stop condition is defined by a positive edge on the SDA line while SCL is high. The Start and Stop conditions are shown in figure 6. It is possible for the Start or Stop condition to occur at any time during a data transfer. If either a Start or Stop condition is encountered during a data transfer, the A8296 will respond by resetting the data transfer sequence.

I²C™ Write Cycle Description. Writing to the A8296 Control register requires transmission of a total of 27 bits–three 8-bit bytes of data plus an Acknowledge bit after each byte. Writing to the A8296 Control register is shown in figure 6(a). Writing to the A8296 Control register requires a chip address with R/W = 0, a



(A) Write to Control Register



(B) Read from Status Register

Figure 6. I²C™ Interface Read and Write Sequences. (A) for the I²C™ Write cycle and (B) for the I²C™ Read cycle.

Control register address, and the control data, as follows:

- The Chip Address cycle consists of a total of nine bits–seven bits of chip address (A6 to A0) plus one read/write bit (R/W = 0) to indicate a write from the master followed by an Acknowledge bit (AK = 0 for reception of a valid chip address) from the slave. The chip address must be transmitted MSB (A6) first. The first five bits of the A8296 chip address (A6 to A2) are fixed as 00010. The remaining two bits (A1 and A0) are used to select one of four possible A8296 chip addresses. The DC voltage on the ADD pin programs the chip address. See the Electrical Characteristics table for the ADD pin voltages and the corresponding chip addresses.

- The Control Register Address cycle consists of a total of nine bits–eight bits of control register address (RC7 to RC0) from the master followed by an Acknowledge bit from the slave. The Control register address must be transmitted MSB (RC7) first. The A8296 only has one Control register so the Control register address is fixed as 00000000.

- The Control Data cycle consists of a total of nine bits–eight bits of control data (D7 to D0) from the master followed by an Acknowledge bit from the slave. The control data must be transmitted MSB first (D7). The Control register bits are identified in the Control Registers section of this datasheet.

I²C™ Read Cycle Description. Reading from the A8296 Status register requires transmission of a total of 36 bits–four 8-bit bytes of data plus an Acknowledge bit after each byte. Reading the A8296 Status register requires a chip address with R/W = 0, a Status register address, an I²C™ Stop condition, an I²C™ Start condition, a "repeated" chip address with R/W=1, and finally the status data from the A8296. Reading from the A8296 Status register is shown in figure 6(b).

- This 9-bit Chip Address cycle is identical to the Chip Address cycle previously described for the Write Control register sequence. It consists of A6 to A0, plus one read/write bit (R/W = 0) from the master, followed by an Acknowledge bit from the slave and finally an I²C™ Stop condition.

- The Status Register Address cycle consists of a total of nine bits–eight bits of Status register address (RS7 to RS0) from the master, followed by an Acknowledge bit from the slave. The Status register address must be transmitted MSB (RS7) first. The A8296 only has one Status register, so the Status register address is fixed at 00000000.

- The "Repeated" Chip Address cycle begins with an I²C™ Start condition followed by a 9-bit cycle identical to the Chip Address cycle previously described for the Write Control Register sequence. It consists of A6 to A0, plus one read/write bit (R/W = 1) from the master, followed by an Acknowledge bit from the slave.

- The Status Data cycle consists of a total of nine bits–eight bits of status data (RD7 to RD0) from the slave, followed by an Acknowledge bit from the master. The status data is transmitted MSB (RD7) first. The Status register bits are identified in the Status Register section of this datasheet.

Interrupt Request (IRQ) pin

The A8296 provides an interrupt request pin (IRQ), which is an open-drain, active low output. This output may be connected to a common IRQ line with a suitable external pull-up resistor and can be used with other I²C™ compatible devices to request attention from the master controller.

The IRQ output becomes active (logic low) when the A8296 recognizes a fault condition. The fault conditions that will force IRQ active include undervoltage lockout (UVLO), overcurrent protection (OCP), and thermal shutdown (TSD). The UVLO, OCP, and TSD faults are latched in the Status register and will not be unlatched until the A8296 Status register is successfully transmitted to the master controller (an AK bit must be received from the master). See the description in the Status Register section and figure 7 for further details.

When the master device receives an interrupt, it should address all slaves connected to the interrupt line in sequence and read the status register of each to determine which device is requesting attention. As shown in figure 7, the A8296 latches all conditions in the Status register and sets the IRQ to logic low when a fault occurs. The IRQ bit is reset to logic high and the Status register is unlatched when the master acknowledges the status data from the A8296 (an AK bit must be received from the master).

The disable (DIS) and Power Not Good (PNG) conditions do not cause an interrupt and are not latched in the Status register.

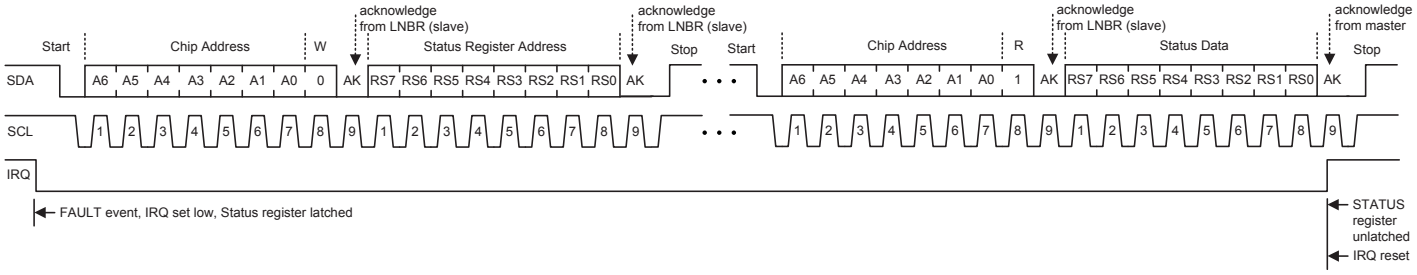
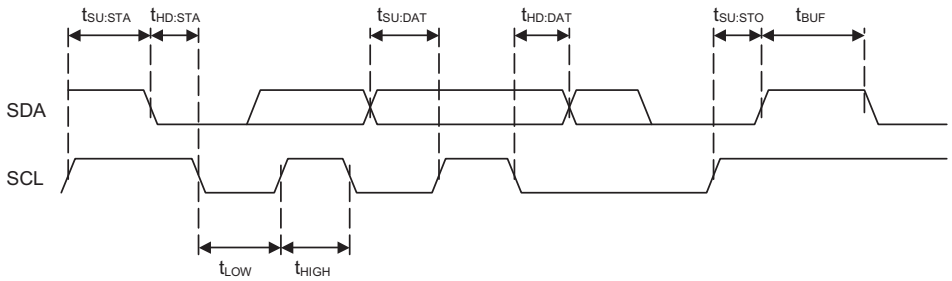


Figure 7. Fault, IRQ, and Status Register Timing. When a FAULT occurs, the IRQ bit is set to low and the Status register is latched. The IRQ bit is reset to high when the A8296 acknowledges it is being read. The Status register is unlatched when the master acknowledges the status data from the A8296.

I²C™-Compatible Interface Timing Diagram



I²C™-Compatible Timing Requirements

Characteristics	Symbol	Min.	Typ.	Max.	Units
Bus Free Time Between Stop/Start	t_{BUF}	1.3	–	–	µs
Hold Time Start Condition	$t_{HD:STA}$	0.6	–	–	µs
Setup Time for Start Condition	$t_{SU:STA}$	0.6	–	–	µs
SCL Low Time	t_{LOW}	1.3	–	–	µs
SCL High Time	t_{HIGH}	0.6	–	–	µs
Data Setup Time	$t_{SU:DAT}$	100	–	–	ns
Data Hold Time	$t_{HD:DAT}$	0	–	900	ns
Setup Time for Stop Condition	$t_{SU:STO}$	0.6	–	–	µs
Output Fall Time ($V_{fI2COut(H)}$ to $V_{fI2COut(L)}$)	$t_{fI2COut}$	–	–	250	ns

Control Registers (I²C™-Compatible Write Register)

All main functions of the A8296 are controlled through the I²C™ compatible interface via the 8-bit Control register. Table 1 shows the functionality and bit definitions of the Control register. At power-up, the Control register is initialized to all 0s.

Table 1. Control Register Definition

Bit	Name	Function	Description
0	VSEL0	LNB output voltage control See Table 2 for available output voltage selections	The available voltages provide levels for all the common standards plus the ability to add line compensation. VSEL0 is the LSB and VSEL2 is the MSB to the internal DAC.
1	VSEL1		
2	VSEL2		
3	ENB	0: Disable LNB Output 1: Enable LNB Output	Turns the LNB output on or off.
4	–	Set to 0	Unused
5	–		
6	–		
7	–		

Table 2. Output Voltage Amplitude Selection

VSEL2	VSEL1	VSEL0	LNB (V)
0	0	0	13.333
0	0	1	13.667
0	1	0	14.000
0	1	1	14.333
1	0	0	18.667
1	0	1	19.000
1	1	0	19.667
1	1	1	20.000

Status Registers (I²C™-Compatible Read Register)

The main fault conditions: undervoltage lockout (UVLO), overcurrent (OCP), and thermal shutdown (TSD) are all indicated by setting the relevant bits in the Status register. In all fault cases, after the bit is set, it remains latched until the I²C™ master has successfully read the A8296, assuming the fault has been resolved.

The undervoltage lockout (UVLO) bit indicates either the input voltage at the VIN pin is too low or the A8296 internal supply voltage (VREG) is too low.

The Disable bit (DIS) indicates the status of the LNB output. The DIS is set when either a fault occurs (UVLO, OCP, TSD, or CPOK) or when the LNB output is turned off using the Enable bit (ENB) via the I²C™ interface. The DIS bit is latched and is only reset when there are no faults and the A8296 output is turned back on using the Enable (ENB) bit via the I²C™ interface.

The Power Not Good (PNG) and Charge Pump OK (CPOK) bits are set based on the conditions sensed at the LNB output and VCP pins, respectively. These bits are not latched and, unlike the other fault bits, may become reset without an I²C™ read sequence. The PNG and CPOK bits are continuously updated.

There are three methods to detect when the Status register changes: responding to the interrupt request (IRQ) pin going low, continuously polling the Status register via the I²C™ interface, or detecting a fault condition external to the A8296 and performing a diagnostic poll of the A8296. In any case, the master should read and re-read the Status register until the status changes.

Table 3. Status Register Description and IRQ Operation

Bit	Name	Function	Latched?	Reset Condition	Effect on IRQ Pin
0	DIS	LNB output disabled	Yes	LNB enabled and no faults	None
1	CPOK	Charge pump OK	No	$V_{CP} > V_{BOOST} + 5V$	None
2	OCP	Overcurrent	Yes	I²C™ read and fault removed	IRQ set low
3	TRIMS	Trim bits locked	Yes	None	None
4	PNG	Power Not Good	No	LNB voltage within range	None
5	–	Not used	–	–	–
6	TSD	Thermal shutdown	Yes	I²C™ read and fault removed	IRQ set low
7	UVLO	VIN or VREG undervoltage	Yes	I²C™ read and fault removed	IRQ set low

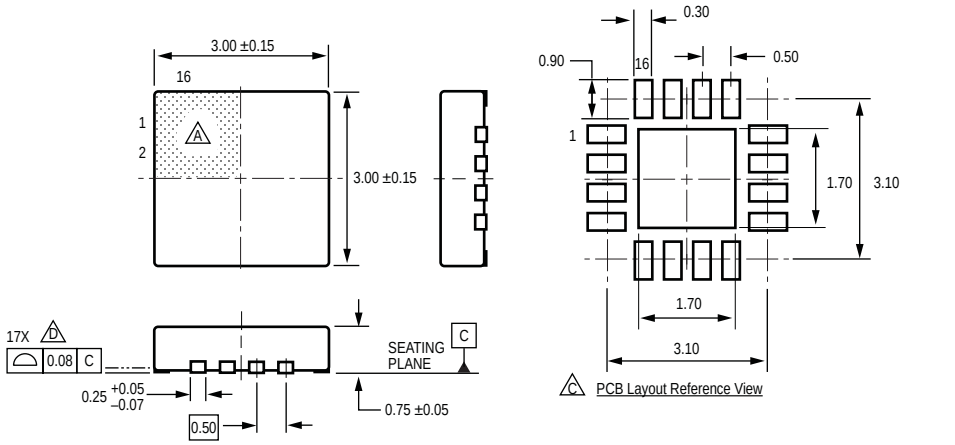
Table 4. Status Register Bit Descriptions

Bit	Name	Description
0	DIS	The DIS bit is set to 1 when the A8296 is disabled, (ENB = 0) or there is a fault: UVLO, OCP, CPOK, or TSD.
1	CPOK	If this bit is set low, the internal charge pump is not operating correctly (VCP). If the charge pump voltage is too low, the LNB output is disabled and the DIS bit is set.
2	OCP	This bit will be set to a 1 if the LNB output current exceeds the overcurrent threshold ($I_{OUT(MAX)}$) for more than the overcurrent disable time (t_{DIS}). If the OCP bit is set to 1, then the DIS bit is also set to 1.
3	TRIMS	Factory use only.
4	PNG	Set to 1 when the A8296 is enabled and the LNB output voltage is either too low or too high (nominally ±9% from the LNB DAC setting). Set to 0 when the A8296 is enabled and the LNB voltage is within the acceptable range (nominally ±5% from the LNB DAC setting).
5	–	Not used.
6	TSD	The TSD bit is set to 1 if the A8296 has detected an overtemperature condition. If the TSD bit is set to 1, then the DIS bit is also set to 1.
7	UVLO	The UVLO bit is set to 1 if either the voltage at the VIN pin or the voltage at the VREG pin is too low. If the UVLO bit is set to 1, then the DIS bit is also set to 1.

Table 5. Component Selection Table

Component	Characteristics	Manufacturer Device
C1, C4, C7, C8	100 nF, 50 V, X5R or X7R, 0603	
C2, C5	100 µF, 35 V_{MIN}, ESR < 100 mΩ, I_{RIPPLE} > 550 mA	Panasonic: EEU-FM1H101B ChemiCon: EKZE500ELL101MHB5D Nichicon: UHC1V101MPT
C3	220 nF, 10 V_{MIN}, X5R or X7R, 0402 or 0603	
C6	1.0 µF, 25 V_{MIN}, X5R or X7R, 1206	TDK: C3216X7R1E105K Murata: GRM31MR71E105KA01 Taiyo Yuden: TMK316BJ105KL-T Kemet: C1206C105K3RACTU
C9	10 nF, 50 V, X5R or X7R, 0402 or 0603	
C10	220 nF, 50 V, X5R or X7R, 0805	
D1, D2	Schottky diode, 40 V, 1 A, SOD-123	Diodes, Inc: B140HW-7 Central Semi: CMMSH1-40
D3	Schottky diode, 40 V, 3 A, SMA	Sanken: SFPB-74 Vishay: B340A-E3/5AT Diodes, Inc.: B340A-13-F Central Semi: CMSH3-40MA
D4	TVS, 20 V_{RM}, 32 V_{CL} at 500 A (8/20 µs), 3000 W	ST: LNBTVS6-221S, Littelfuse: 3.0SMCJ20A
L1	33 µH, I_{SAT} > 1.3 A, DCR < 130 mΩ	TDK: TSL0808RA-330K1R4-PF Taiyo Yuden: LHLC08TB330K Coilcraft: DR0608-333L
R1 to R4	Determined by V_{DD}, bus capacitance, etc.	

Package ES 16-Pin MLP/QFN



For reference only, not for tooling use (reference JEDEC MO-220WEED)
Dimensions in millimeters
Exact case and lead configuration at supplier discretion within limits shown

A Terminal #1 mark area

B Exposed thermal pad (reference only, terminal #1 identifier appearance at supplier discretion)

C Reference land pattern layout (reference IPC7351 QFN50P300X300X80-17W4M);
All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

D Coplanarity includes exposed thermal pad and terminals

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