



TPS22969 5.5-V, 6-A, 4.4-mΩ On-Resistance Load Switch

1 Features

- Integrated Single Channel Load Switch
- VBIAS Voltage Range: 2.5 V to 5.5 V
- VIN Voltage Range: 0.8 V to 5.5 V
- Ultra Low R_{ON} Resistance
 - R_{ON} = 4.4 mΩ at V_{IN} = 1.05 V (V_{BIAS} = 5 V)
- 6 A Maximum Continuous Switch Current
- Low Quiescent Current
 - (20 μA (Typ) for V_{BIAS} = 5 V)
- Low Shutdown Current
 - (1 μA (Typ) for V_{BIAS} = 5 V)
- Low Control Input Threshold Enables Use of 1.2 V or Higher GPIO
- Controlled and Fixed Slew Rate Across V_{BIAS} and V_{IN}
 - t_R = 599 μs at V_{IN} = 1.05 V (V_{BIAS} = 5 V)
- Quick Output Discharge (QOD)
- SON 8-Pin Package with Thermal Pad
- ESD Performance Tested per JESD 22
 - 2-kV Human-Body Model (HBM)
 - 1-kV Charged-Device Model (CDM)

2 Applications

- Ultrabook™/Notebooks
- Desktop PC
- Industrial PC
- Chromebook
- Servers
- Set-top Boxes
- Telecom Systems
- Tablet PC

3 Description

The TPS22969 is a small, ultra-low R_{ON}, single channel load switch with controlled turn on. The device contains an N-channel MOSFET that can operate over an input voltage range of 0.8 V to 5.5 V and can support a maximum continuous current of 6 A.

The combination of ultra-low R_{ON} and high current capability of the device makes it ideal for driving processor rails with very tight voltage dropout tolerances. The controlled rise time of the device greatly reduces inrush current caused by large bulk load capacitances, thereby reducing or eliminating voltage droop on the power supply. The switch can be independently controlled via the ON pin, which is capable of interfacing directly with low-voltage control signals originating from microcontrollers or low voltage discrete logic. The device further reduces the total solution size by integrating a 224-Ω pull-down resistor for quick output discharge (QOD) when the switch is turned off.

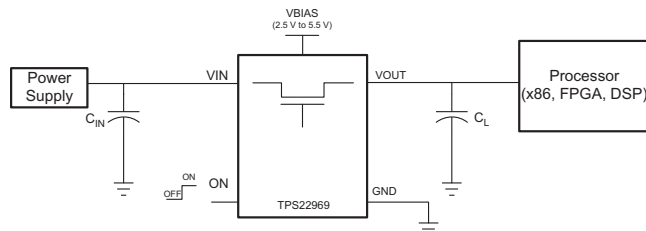
The TPS22969 is available in a small 3.00 mm x 3.00 mm SON-8 package (DNY). The DNY package integrates a thermal pad which allows for high power dissipation in high current and high temperature applications. The device is characterized for operation over the free-air temperature range of –40°C to 105°C.

Device Information⁽¹⁾

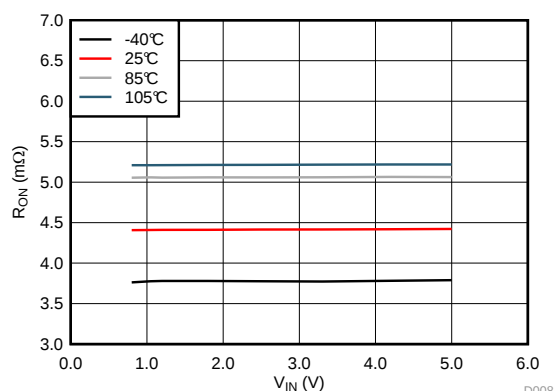
ORDER NUMBER	PACKAGE	BODY SIZE (NOM)
TPS22969	WSO8 (8)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Driving High Current Core Rails For a Processor



R_{ON} vs V_{IN} (V_{BIAS} = 5 V, I_{OUT} = –200 mA)



D008



Table of Contents

1 Features	1	7.2 Functional Block Diagram	14
2 Applications	1	7.3 Feature Description	15
3 Description	1	8 Applications and Implementation	16
4 Revision History	2	8.1 Application Information	16
5 Pin Configuration and Functions	3	8.2 Typical Application	16
6 Specifications	3	9 Power Supply Recommendations	19
6.1 Absolute Maximum Ratings	3	10 Layout	19
6.2 ESD Ratings	4	10.1 Layout Guidelines	19
6.3 Recommended Operating Conditions	4	10.2 Layout Example	20
6.4 Thermal Information	4	11 Device and Documentation Support	21
6.5 Electrical Characteristics, $V_{BIAS} = 5.0\text{ V}$	5	11.1 Community Resources	21
6.6 Electrical Characteristics, $V_{BIAS} = 2.5\text{ V}$	6	11.2 Trademarks	21
6.7 Switching Characteristics	7	11.3 Electrostatic Discharge Caution	21
6.8 Typical Characteristics	9	11.4 Glossary	21
7 Detailed Description	14	12 Mechanical, Packaging, and Orderable Information	21
7.1 Overview	14		

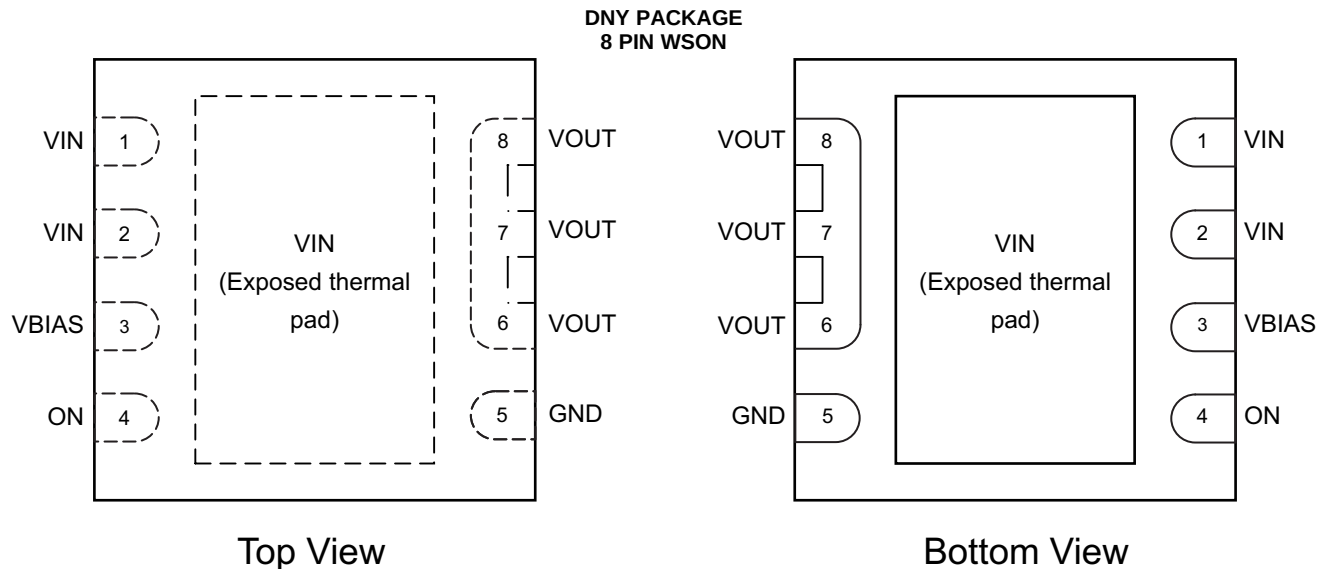
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (February 2014) to Revision B	Page
• Updated T_A ratings in datasheet from 85°C to 105°C.	1

Changes from Original (February 2014) to Revision A	Page
• Initial release of full version.	1

5 Pin Configuration and Functions



Pin Functions

Pin		I/O	DESCRIPTION
NAME	NO.		
VIN	1, 2	I	Switch input. Place ceramic bypass capacitor(s) between this pin and GND. See the Detailed Description section for more information.
VIN	Exposed thermal Pad	I	Switch input. Place ceramic bypass capacitor(s) between this pin and GND. See the Detailed Description section for more information.
VBIAS	3	I	Bias voltage. Power supply to the device.
ON	4	I	Active high switch control input. Do not leave floating.
GND	5	–	Ground.
VOUT	6, 7, 8	O	Switch output. Place ceramic bypass capacitor(s) between this pin and GND. See the Detailed Description section for more information.

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted) ⁽¹⁾

		MIN	MAX	UNIT
V _{IN}	Input voltage range	–0.3	6	V
V _{BIAS}	Bias voltage range	–0.3	6	V
V _{OUT}	Output voltage range	–0.3	6	V
V _{ON}	ON pin voltage range	–0.3	6	V
I _{MAX}	Maximum Continuous Switch Current		6	A
I _{PLS}	Maximum Pulsed Switch Current, pulse < 300-μs, 2% duty cycle		8	A
T _A	Operating free-air temperature range	–40	105	°C
T _J	Maximum junction temperature		125	°C
T _{STG}	Storage temperature range	–65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under [Recommended Operating Conditions](#). Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

		VALUE	UNIT
V _(ESD) Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions.

6.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V _{IN}	Input voltage range		0.8	V _{BIAS}	V
V _{BIAS}	Bias voltage range		2.5	5.5	V
V _{ON}	ON voltage range		0	5.5	V
V _{OUT}	Output voltage range			V _{IN}	V
V _{IH, ON}	High-level voltage, ON	V _{BIAS} = 2.5V to 5.5V	1.2	5.5	V
V _{IL, ON}	Low-level voltage, ON	V _{BIAS} = 2.5V to 5.5V	0	0.5	V
C _{IN}	Input Capacitor		1 ⁽¹⁾		μF

- (1) Refer to [Detailed Description](#) section.

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TPS22969	UNIT
		DNY (WSON)	
		8 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	44.6	°C/W
R _{θJctop}	Junction-to-case (top) thermal resistance	44.4	°C/W
R _{θJB}	Junction-to-board thermal resistance	17.6	°C/W
ψ _{JT}	Junction-to-top characterization parameter	0.4	°C/W
ψ _{JB}	Junction-to-board characterization parameter	17.4	°C/W
R _{θJcbot}	Junction-to-case (bottom) thermal resistance	1.1	°C/W

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

6.5 Electrical Characteristics, $V_{BIAS} = 5.0\text{ V}$

Unless otherwise noted, the specification in the following table applies over the operating ambient temperature $-40^{\circ}\text{C} \leq T_A \leq 105^{\circ}\text{C}$. Typical values are for $T_A = 25^{\circ}\text{C}$ (unless otherwise noted).

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
CURRENTS AND THRESHOLDS							
I_Q , V_{BIAS}	V_{BIAS} quiescent current	$I_{OUT} = 0$, $V_{IN} = V_{BIAS}$, $V_{ON} = 5.0\text{ V}$	-40°C to 85°C		20.4	26.0	μA
			-40°C to 105°C			27.0	
I_{SD} , V_{BIAS}	V_{BIAS} shutdown current	$V_{ON} = 0\text{ V}$, $V_{OUT} = 0\text{ V}$	-40°C to 85°C		1.1	1.5	μA
			-40°C to 105°C			1.6	
I_{SD} , V_{IN}	V_{IN} shutdown current	$V_{ON} = 0\text{ V}$, $V_{OUT} = 0\text{ V}$	$V_{IN} = 5.0\text{ V}$	-40°C to 85°C		0.1	μA
				-40°C to 105°C		0.5	
			$V_{IN} = 3.3\text{ V}$	-40°C to 85°C		0.1	
				-40°C to 105°C		0.5	
			$V_{IN} = 1.8\text{ V}$	-40°C to 85°C		0.1	
				-40°C to 105°C		0.5	
			$V_{IN} = 1.05\text{ V}$	-40°C to 85°C		0.1	
				-40°C to 105°C		0.5	
			$V_{IN} = 0.8\text{ V}$	-40°C to 85°C		0.1	
				-40°C to 105°C		0.5	
I_{ON}	ON pin leakage current	$V_{ON} = 5.5\text{ V}$	-40°C to 105°C			0.1	μA
$V_{HYS, ON}$	ON pin hysteresis	$V_{BIAS} = V_{IN}$	25°C		113		mV
RESISTANCE CHARACTERISTICS							
R_{ON}	On-state resistance	$I_{OUT} = -200\text{ mA}$, $V_{BIAS} = 5.0\text{ V}$	$V_{IN} = 5.0\text{ V}$	25°C	4.4	5.0	m Ω
				-40°C to 85°C		5.6	
				-40°C to 105°C		5.8	
			$V_{IN} = 3.3\text{ V}$	25°C	4.4	5.0	m Ω
				-40°C to 85°C		5.6	
				-40°C to 105°C		5.8	
			$V_{IN} = 2.5\text{ V}$	25°C	4.4	5.0	m Ω
				-40°C to 85°C		5.6	
				-40°C to 105°C		5.8	
			$V_{IN} = 1.8\text{ V}$	25°C	4.4	5.0	m Ω
				-40°C to 85°C		5.6	
				-40°C to 105°C		5.8	
			$V_{IN} = 1.05\text{ V}$	25°C	4.4	5.0	m Ω
				-40°C to 85°C		5.6	
				-40°C to 105°C		5.8	
			$V_{IN} = 0.8\text{ V}$	25°C	4.4	5.0	m Ω
				-40°C to 85°C		5.6	
				-40°C to 105°C		5.8	
		$I_{OUT} = -6\text{ A}$, $V_{BIAS} = 5.0\text{ V}$	$V_{IN} = 1.05\text{ V}$	-40°C to 85°C	4.6	5.8 ⁽¹⁾	m Ω
				-40°C to 105°C		6.0 ⁽¹⁾	
R_{PD}	Output pulldown resistance	$V_{IN} = 5.0\text{ V}$, $V_{ON} = 0\text{ V}$, $V_{OUT} = 1\text{ V}$	-40°C to 105°C		224	233	Ω

(1) Parameter verified by design and characterization, but not tested in production.

6.6 Electrical Characteristics, $V_{BIAS} = 2.5\text{ V}$

Unless otherwise noted, the specification in the following table applies over the operating ambient temperature $-40^{\circ}\text{C} \leq T_A \leq 105^{\circ}\text{C}$. Typical values are for $T_A = 25^{\circ}\text{C}$ unless otherwise noted.

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
CURRENTS AND THRESHOLDS							
$I_{Q, VBIAS}$	V_{BIAS} quiescent current	$I_{OUT} = 0$, $V_{IN} = V_{BIAS}$, $V_{ON} = 5.0\text{ V}$	-40°C to 85°C		9.9	12.5	μA
			-40°C to 105°C			12.7	
$I_{SD, VBIAS}$	V_{BIAS} shutdown current	$V_{ON} = 0\text{ V}$, $V_{OUT} = 0\text{ V}$	-40°C to 85°C		0.5	0.65	μA
			-40°C to 105°C			0.7	
$I_{SD, VIN}$	V_{IN} shutdown current	$V_{ON} = 0\text{ V}$, $V_{OUT} = 0\text{ V}$	$V_{IN} = 2.5\text{ V}$	-40°C to 85°C		0.1	μA
				-40°C to 105°C		0.5	
			$V_{IN} = 1.8\text{ V}$	-40°C to 85°C		0.1	
				-40°C to 105°C		0.5	
			$V_{IN} = 1.05\text{ V}$	-40°C to 85°C		0.1	
				-40°C to 105°C		0.5	
			$V_{IN} = 0.8\text{ V}$	-40°C to 85°C		0.1	
				-40°C to 105°C		0.5	
I_{ON}	ON pin input leakage current	$V_{ON} = 5.5\text{ V}$	-40°C to 105°C			0.1	μA
$V_{HYS, ON}$	ON pin hysteresis	$V_{BIAS} = V_{IN}$	25°C		83		mV
RESISTANCE CHARACTERISTICS							
R_{ON}	On-state resistance	$I_{OUT} = -200\text{ mA}$, $V_{BIAS} = 2.5\text{ V}$	$V_{IN} = 2.5\text{ V}$	25°C	4.7	5.3	m Ω
				-40°C to 85°C		6.0	
				-40°C to 105°C		6.2	
			$V_{IN} = 1.8\text{ V}$	25°C	4.6	5.2	m Ω
				-40°C to 85°C		5.8	
				-40°C to 105°C		6.0	
			$V_{IN} = 1.05\text{ V}$	25°C	4.5	5.1	m Ω
				-40°C to 85°C		5.7	
				-40°C to 105°C		5.9	
			$V_{IN} = 0.8\text{ V}$	25°C	4.5	5.1	m Ω
				-40°C to 85°C		5.7	
				-40°C to 105°C		5.9	
R_{PD}	Output pulldown resistance	$V_{IN} = 2.5\text{ V}$, $V_{ON} = 0\text{ V}$, $V_{OUT} = 1\text{ V}$	-40°C to 105°C		224	233	Ω

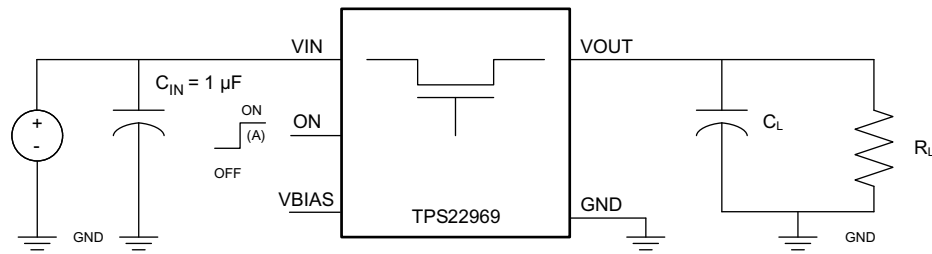
6.7 Switching Characteristics

Refer to the timing test circuit in [Figure 1](#) (unless otherwise noted) for references to external components used for the test condition in the switching characteristics table. Switching characteristics shown below are only valid for the power-up sequence where VIN and VBIAS are already in steady state condition before the ON pin is asserted high.

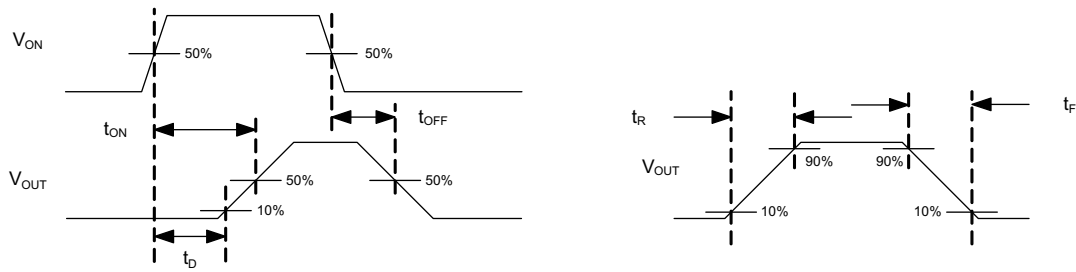
PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
V _{IN} = 5 V, V _{ON} = V _{BIAS} = 5 V, T _A = 25°C (unless otherwise noted)						
t _{ON}	Turn-on time	R _L = 10 Ω, C _L = 0.1 μF		2397		μs
t _{OFF}	Turn-off time			4		
t _R	V _{OUT} rise time			2663		
t _F	V _{OUT} fall time			2		
t _D	Delay time			1009		
V _{IN} = 1.05 V, V _{ON} = V _{BIAS} = 5 V, T _A = 25°C (unless otherwise noted)						
t _{ON}	Turn-on time	R _L = 10 Ω, C _L = 0.1 μF		1064		μs
t _{OFF}	Turn-off time			4		
t _R	V _{OUT} rise time			599		
t _F	V _{OUT} fall time			2		
t _D	Delay time			727		
V _{IN} = 0.8 V, V _{ON} = V _{BIAS} = 5 V, T _A = 25°C (unless otherwise noted)						
t _{ON}	Turn-on time	R _L = 10 Ω, C _L = 0.1 μF		981		μs
t _{OFF}	Turn-off time			4		
t _R	V _{OUT} rise time			500		
t _F	V _{OUT} fall time			2		
t _D	Delay time			714		
V _{IN} = 2.5 V, V _{ON} = 5 V, V _{BIAS} = 2.5 V, T _A = 25°C (unless otherwise noted)						
t _{ON}	Turn-on time	R _L = 10 Ω, C _L = 0.1 μF		1576		μs
t _{OFF}	Turn-off time			8		
t _R	V _{OUT} rise time			1372		
t _F	V _{OUT} fall time			2		
t _D	Delay time			865		
V _{IN} = 1.05 V, V _{ON} = 5V, V _{BIAS} = 2.5 V, T _A = 25°C (unless otherwise noted)						
t _{ON}	Turn-on time	R _L = 10 Ω, C _L = 0.1 μF		1080		μs
t _{OFF}	Turn-off time			8		
t _R	V _{OUT} rise time			604		
t _F	V _{OUT} fall time			2		
t _D	Delay time			738		
V _{IN} = 0.8 V, V _{ON} = 5V, V _{BIAS} = 2.5 V, T _A = 25°C (unless otherwise noted)						
t _{ON}	Turn-on time	R _L = 10 Ω, C _L = 0.1 μF		994		μs
t _{OFF}	Turn-off time			8		
t _R	V _{OUT} rise time			502		
t _F	V _{OUT} fall time			2		
t _D	Delay time			723		

TPS22969

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Timing Test Circuit

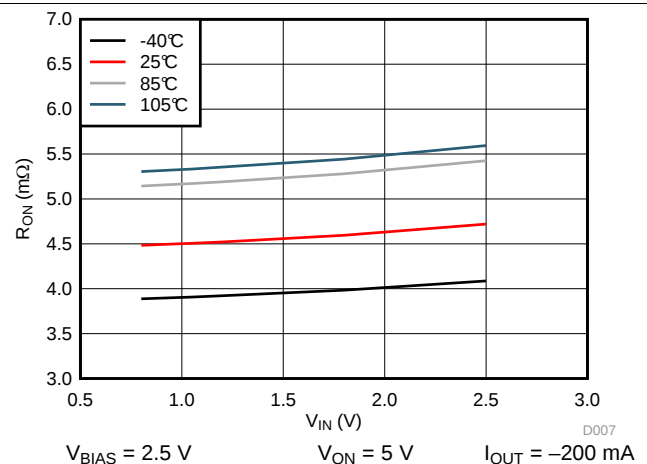
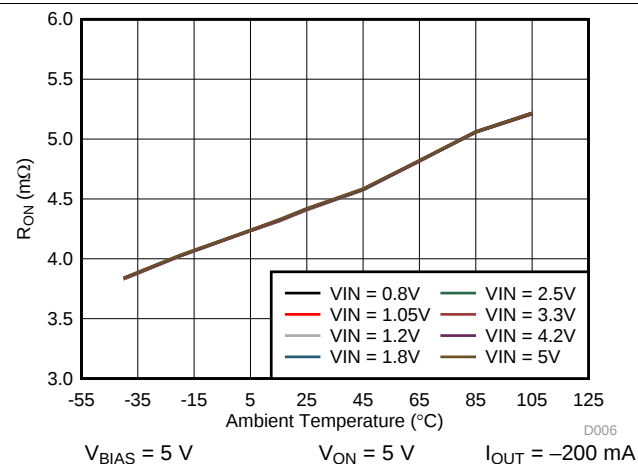
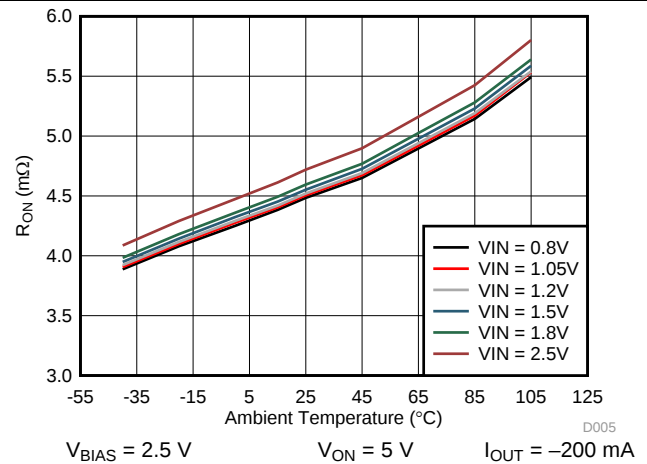
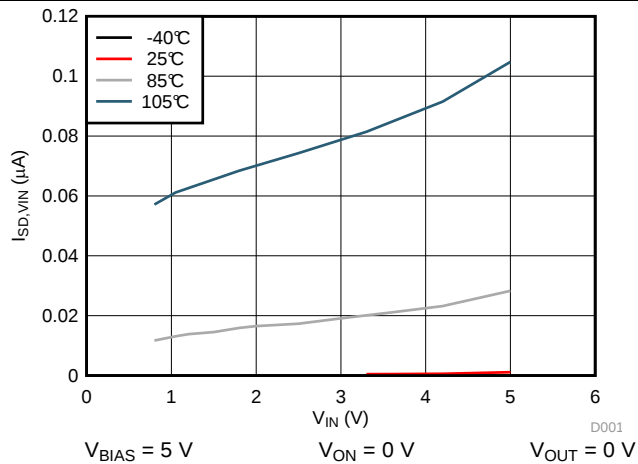
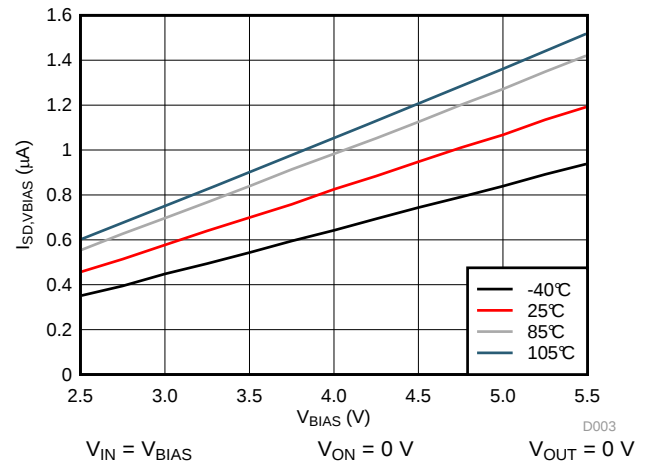
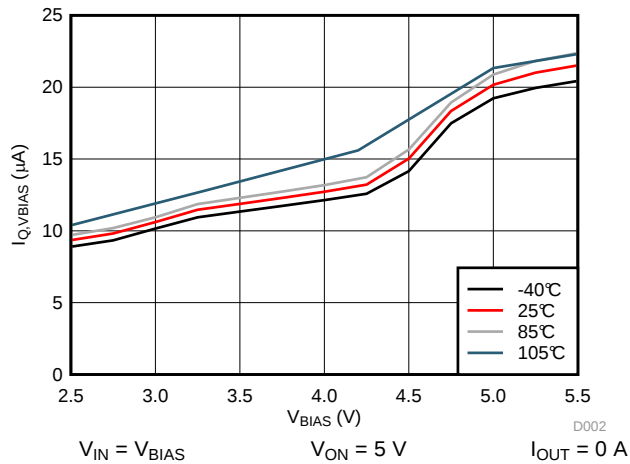


Timing Waveforms

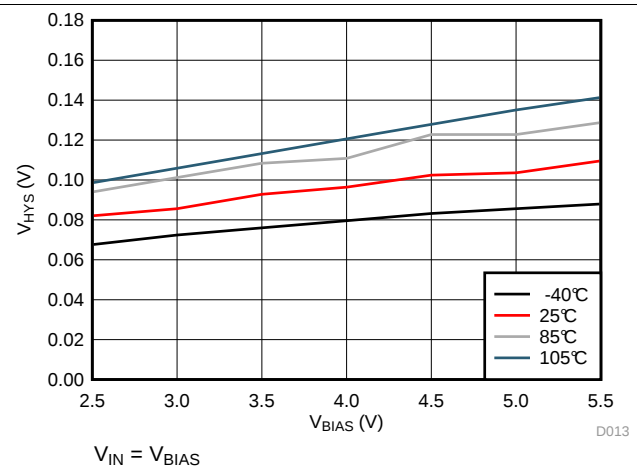
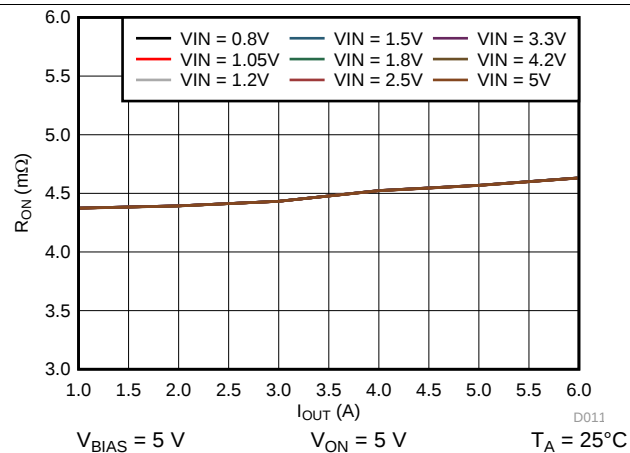
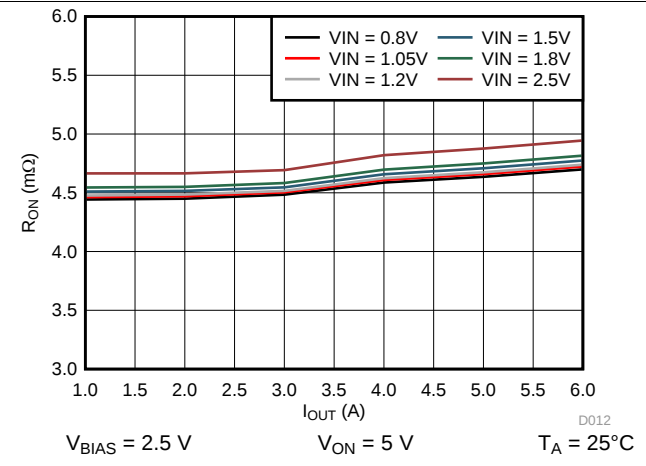
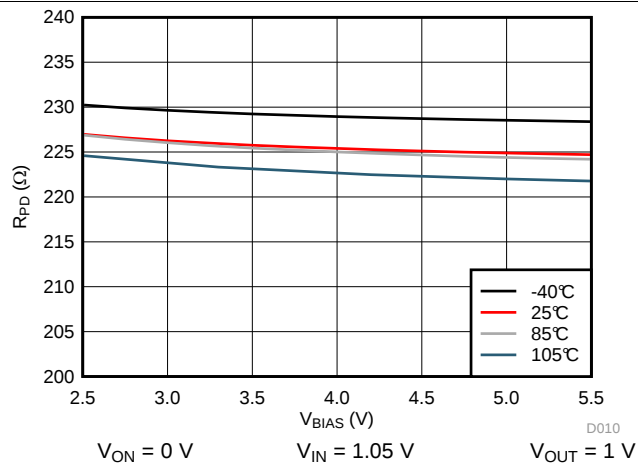
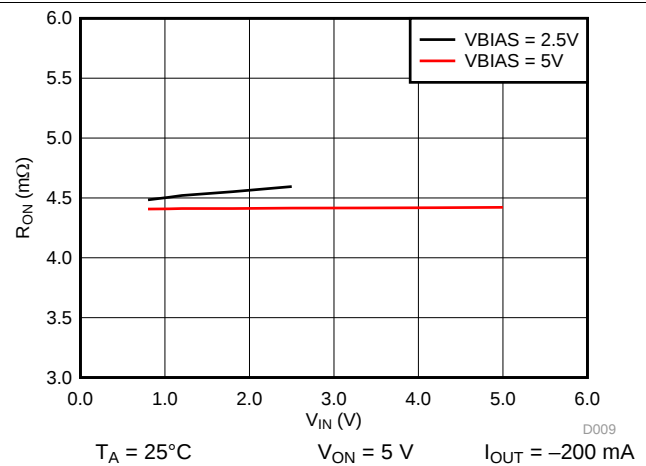
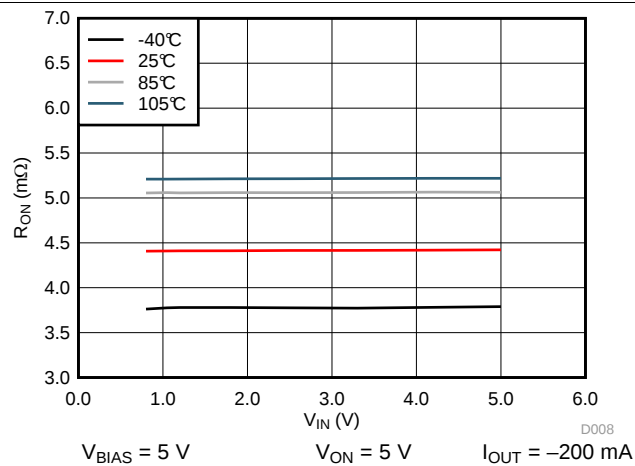
(A) Rise and fall times of the control signal is 100 ns.

Figure 1. Switching Characteristics Measurement Setup and Definitions

6.8 Typical Characteristics



Typical Characteristics (continued)



Typical Characteristics (continued)

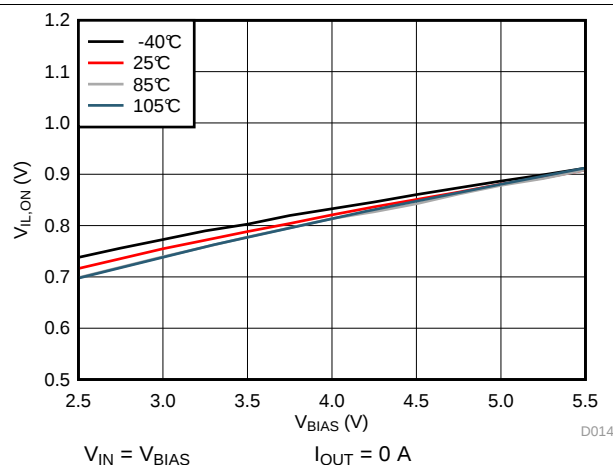


Figure 14. $V_{IL,ON}$ vs V_{BIAS}

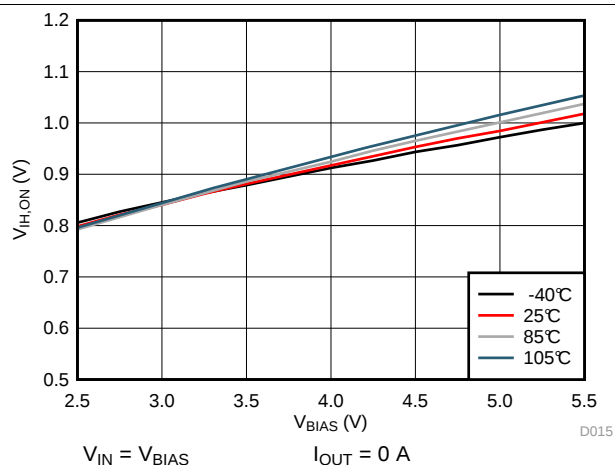


Figure 15. $V_{IH,ON}$ vs V_{BIAS}

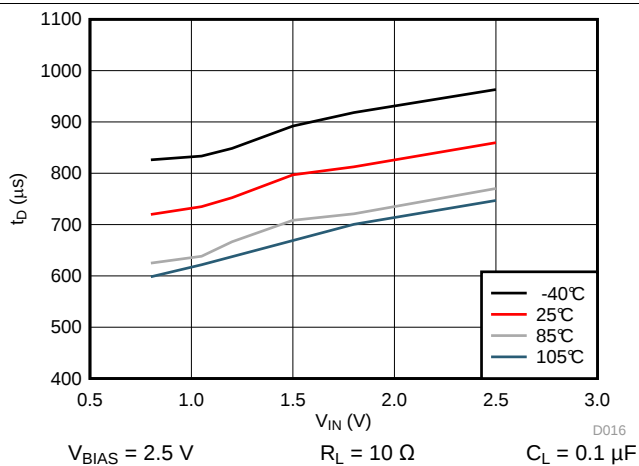


Figure 16. t_D vs V_{IN}

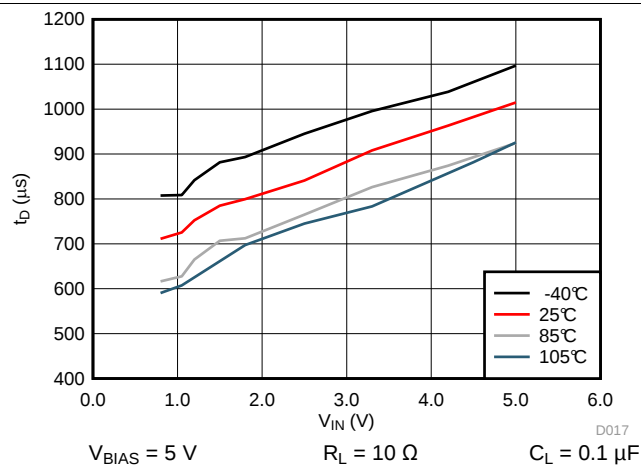


Figure 17. t_D vs V_{IN}

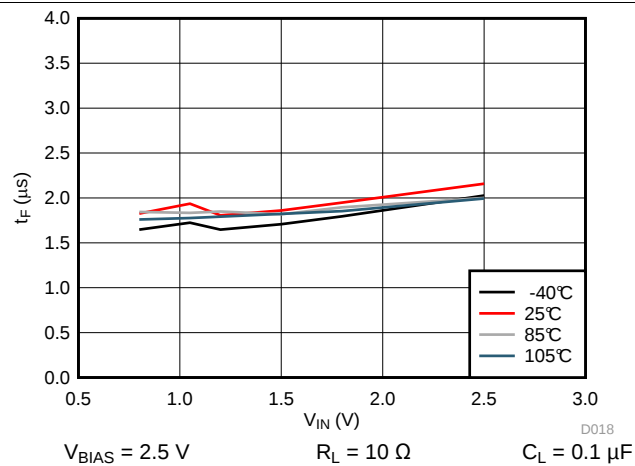


Figure 18. t_F vs V_{IN}

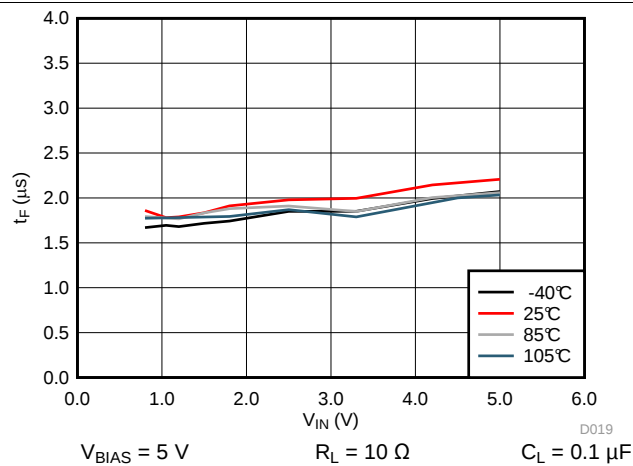
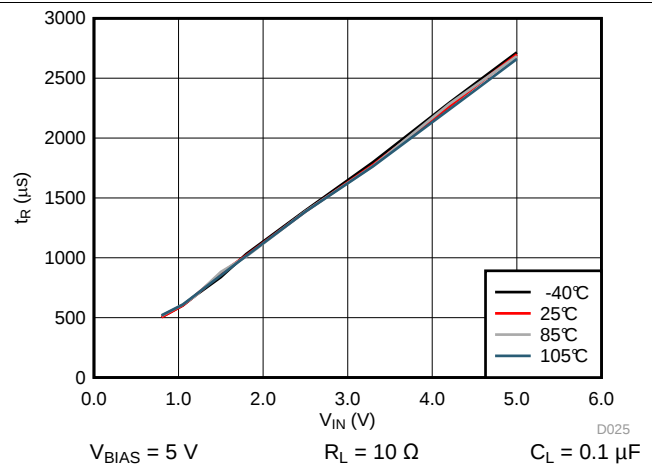
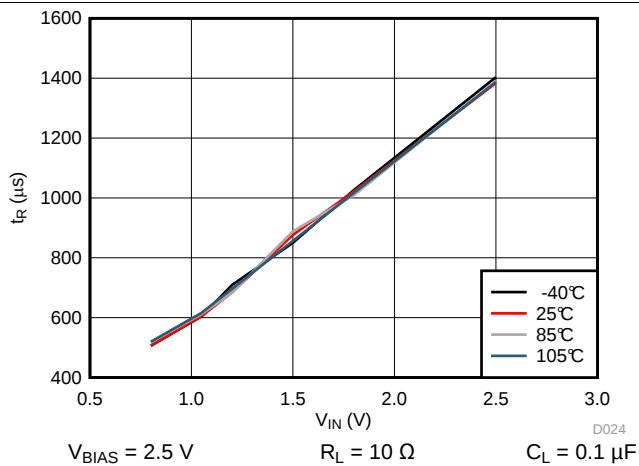
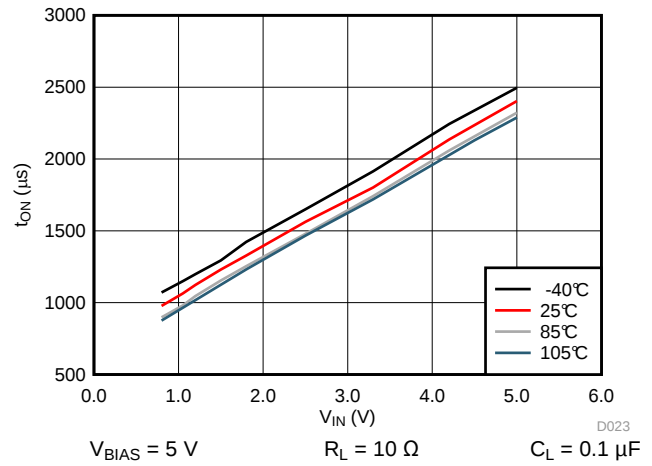
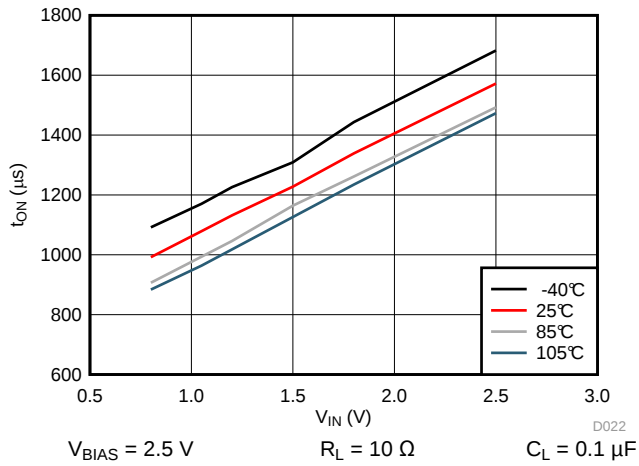
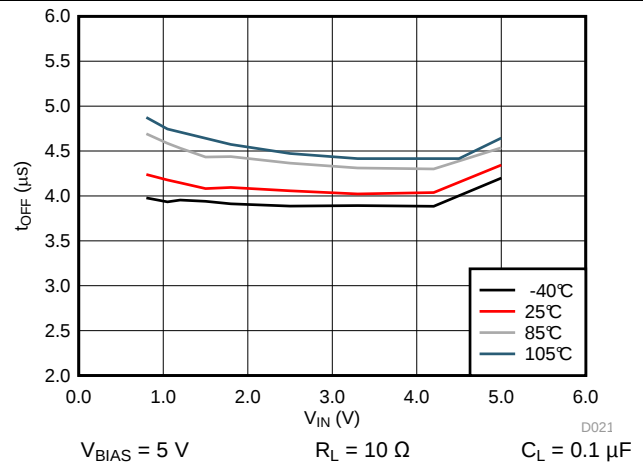
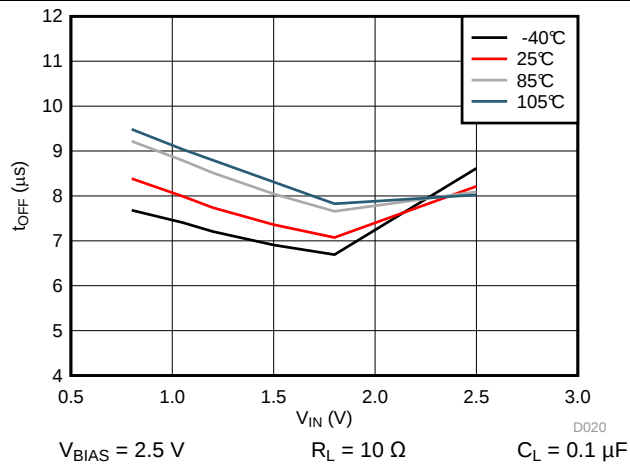
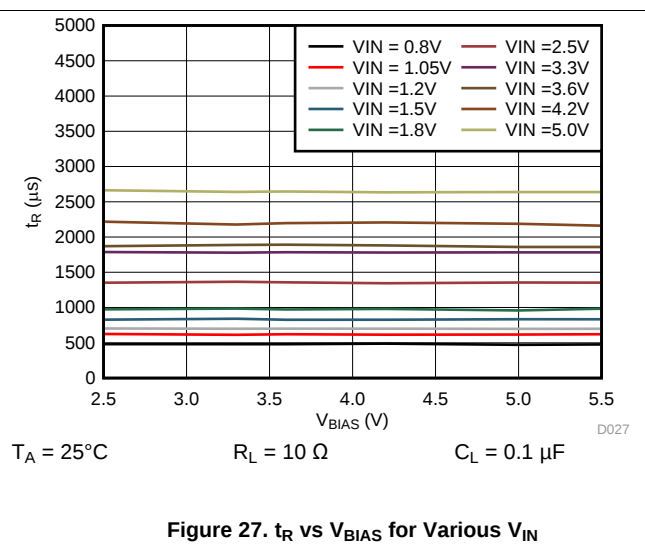
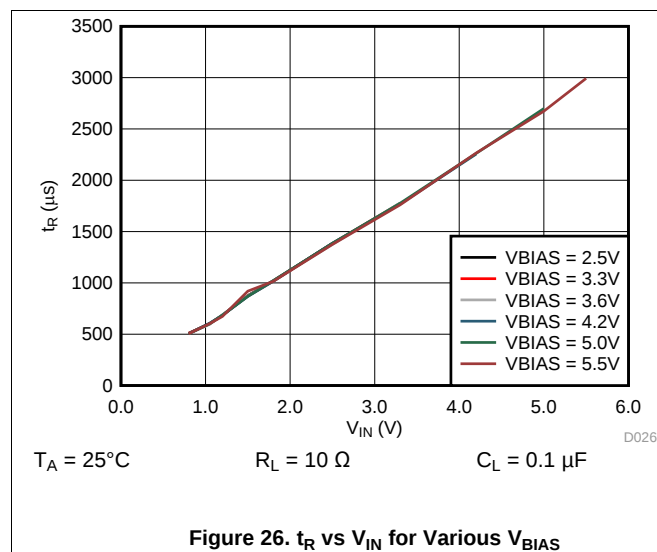


Figure 19. t_F vs V_{IN}

Typical Characteristics (continued)



Typical Characteristics (continued)



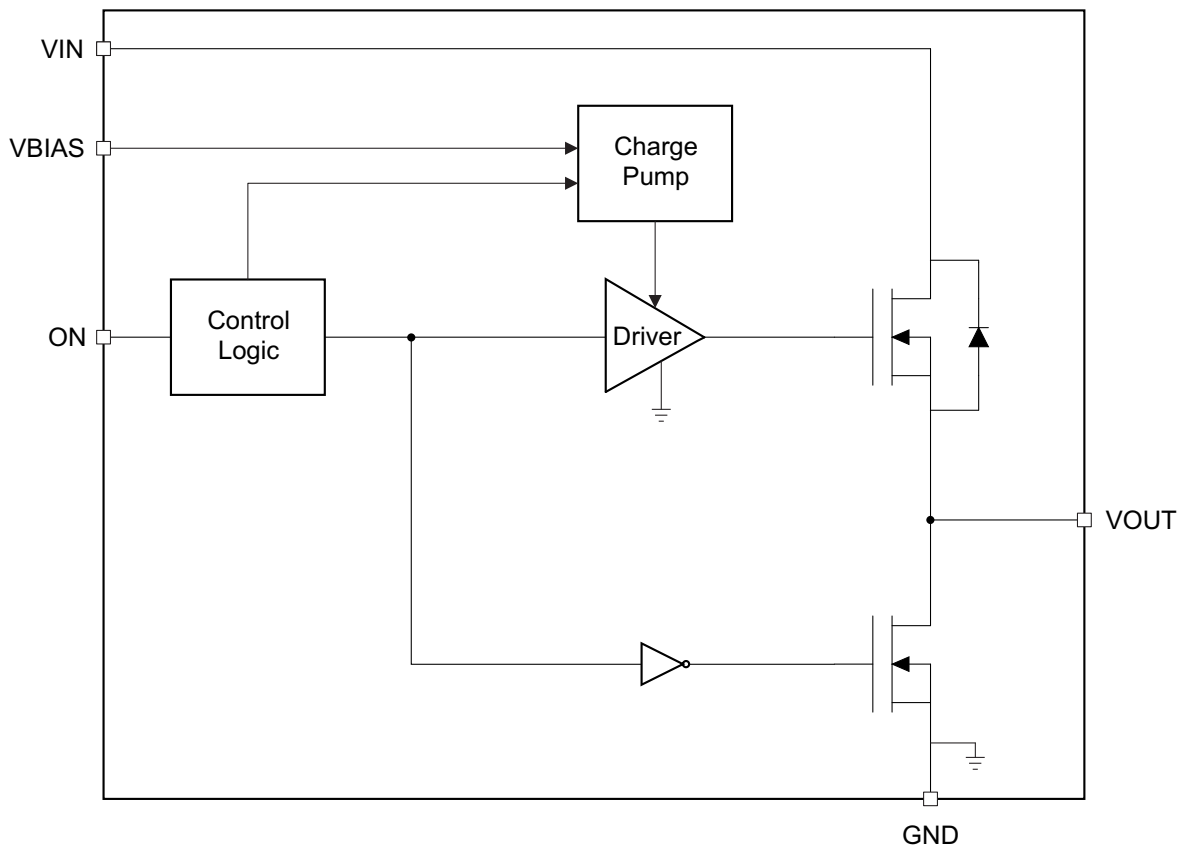
7 Detailed Description

7.1 Overview

The device is a 5.5 V, 6 A load switch in a 8-pin SON package. To reduce voltage drop for low voltage and high current rails, the device implements an ultra-low resistance N-channel MOSFET which reduces the drop out voltage through the device.

The device has a controlled and fixed slew rate which helps reduce or eliminate power supply droop due to large inrush currents. During shutdown, the device has very low leakage currents, thereby reducing unnecessary leakages for downstream modules during standby. Integrated control logic, driver, charge pump, and output discharge FET eliminates the need for any external components, which reduces solution size and BOM count.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 On/off Control

The ON pin controls the state of the load switch, and asserting the pin high (active high) enables the switch. The ON pin is compatible with standard GPIO logic threshold and can be used with any microcontroller or discrete logic with 1.2-V or higher GPIO voltage. This pin cannot be left floating and must be tied either high or low for proper functionality.

7.3.2 Input Capacitor (C_{IN})

To limit the voltage drop on the input supply caused by transient in-rush currents when the switch turns on into a discharged load capacitor or short-circuit, a capacitor needs to be placed between VIN and GND. A 1- μ F ceramic capacitor, C_{IN} , placed close to the pins, is usually sufficient. Higher values of C_{IN} can be used to further reduce the voltage drop in high-current application. When switching heavy loads, it is recommended to have an input capacitor 10 times higher than the output capacitor to avoid excessive voltage drop; however, a 10 to 1 ratio for capacitance is not required for proper functionality of the device, but a ratio smaller than 10 to 1 (such as 1 to 1) could cause a V_{IN} dip upon turn-on due to inrush currents based on external factor such as board parasitics and output bulk capacitance.

7.3.3 Output Capacitor (C_L)

Due to the integrated body diode in the N-channel MOSFET, a C_{IN} greater than C_L is highly recommended. A C_L greater than C_{IN} can cause V_{OUT} to exceed V_{IN} when the system supply is removed. This could result in current flow through the body diode from VOUT to VIN. A C_{IN} to C_L ratio of 10 to 1 is recommended for minimizing V_{IN} dip caused by inrush currents during startup, however a 10 to 1 ratio for capacitance is not required for proper functionality of the device. A ratio smaller than 10 to 1 (such as 1 to 1) could cause a V_{IN} dip upon turn-on due to inrush currents based on external factor such as board parasitics and output bulk capacitance.

7.3.4 V_{IN} and V_{BIAS} Voltage Range

For optimal R_{ON} performance, make sure $V_{IN} \leq V_{BIAS}$. The device may still be functional if $V_{IN} > V_{BIAS}$ but it will exhibit R_{ON} greater than what is listed in the Electrical Characteristics table. See Figure 28 for an example of a typical device. Notice the increasing R_{ON} as V_{IN} increases. Be sure to never exceed the maximum voltage rating for V_{IN} and V_{BIAS} . Performance of the device is not guaranteed for $V_{IN} > V_{BIAS}$.

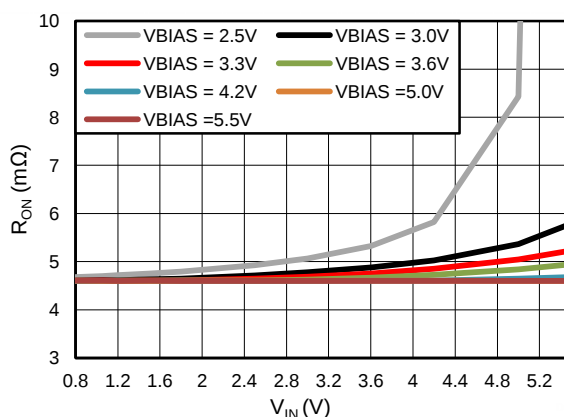


Figure 28. R_{ON} vs V_{IN} ($V_{IN} > V_{BIAS}$)

8 Applications and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

This section will highlight some of the design considerations when implementing this device in various applications. A PSPICE model for this device is also available in the product page of this device.

8.2 Typical Application

This application demonstrates how the TPS22969 can be used to power downstream modules with large capacitances. The example below is powering a 100-μF capacitive output load.

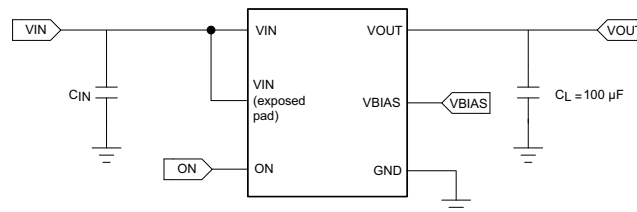


Figure 29. Typical Application Schematic for Powering a Downstream Module

8.2.1 Design Requirements

For this design example, use [Table 1](#) as the input parameters.

Table 1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
V_{IN}	1.05 V
V_{BIAS}	5.0 V
Load current	6 A

8.2.2 Detailed Design Procedure

To begin the design process, the designer needs to know the following:

- V_{IN} voltage
- V_{BIAS} voltage
- Load current

8.2.2.1 V_{IN} to V_{OUT} Voltage Drop

The V_{IN} to V_{OUT} voltage drop in the device is determined by the R_{ON} of the device and the load current. The R_{ON} of the device depends upon the V_{IN} and V_{BIAS} conditions of the device. Refer to the R_{ON} specification of the device in the [Electrical Characteristics, \$V_{BIAS} = 5.0\$ V](#) tables of this datasheet. Once the R_{ON} of the device is determined based upon the V_{IN} and V_{BIAS} conditions, use [Equation 1](#) to calculate the V_{IN} to V_{OUT} voltage drop:

$$\Delta V = I_{LOAD} \times R_{ON} \quad (1)$$

where

- ΔV = voltage drop from V_{IN} to V_{OUT}
- I_{LOAD} = load current
- R_{ON} = on-resistance of the device for a specific V_{IN} and V_{BIAS} combination

An appropriate I_{LOAD} must be chosen such that the I_{MAX} specification of the device is not violated.

8.2.2.2 Inrush Current

To determine how much inrush current will be caused by the C_L capacitor, use Equation 2:

$$I_{\text{INRUSH}} = C_L \times \frac{dV_{\text{OUT}}}{dt} \quad (2)$$

where

- I_{INRUSH} = amount of inrush caused by C_L
- C_L = capacitance on VOUT
- dt = time it takes for change in V_{OUT} during the ramp up of VOUT when the device is enabled
- dV_{OUT} = change in V_{OUT} during the ramp up of VOUT when the device is enabled

An appropriate C_L value should be placed on VOUT such that the I_{MAX} and I_{PLS} specifications of the device are not violated.

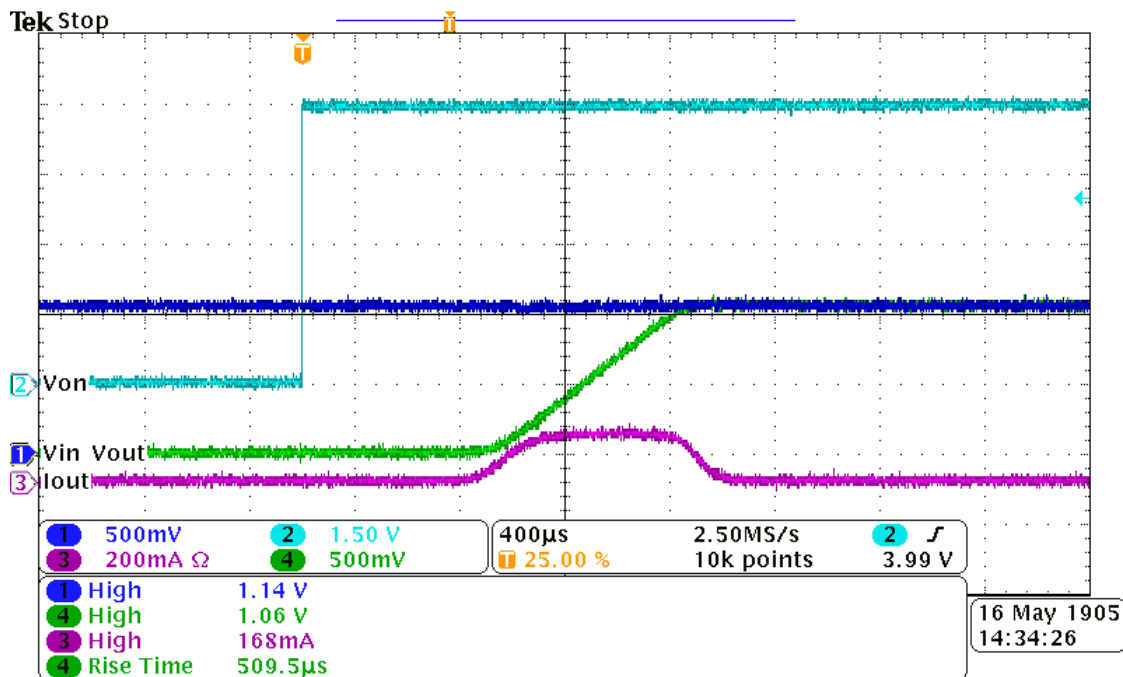


Figure 30. Inrush current ($V_{\text{BIAS}} = 5 \text{ V}$, $V_{\text{IN}} = 1.05 \text{ V}$, $C_L = 100 \mu\text{F}$)

8.2.2.3 Thermal Considerations

The maximum IC junction temperature should be restricted to 125°C under normal operating conditions. To calculate the maximum allowable dissipation, $P_{\text{D(max)}}$ for a given output current and ambient temperature, use Equation 3.

$$P_{\text{D(MAX)}} = \frac{T_{\text{J(MAX)}} - T_{\text{A}}}{R_{\theta\text{JA}}} \quad (3)$$

where

- $P_{\text{D(max)}}$ = maximum allowable power dissipation
- $T_{\text{J(max)}}$ = maximum allowable junction temperature (125°C for the TPS22969)
- T_{A} = ambient temperature of the device
- θ_{JA} = junction to air thermal impedance. See Thermal Information section. This parameter is highly dependent upon board layout.

8.2.3 Application Curves

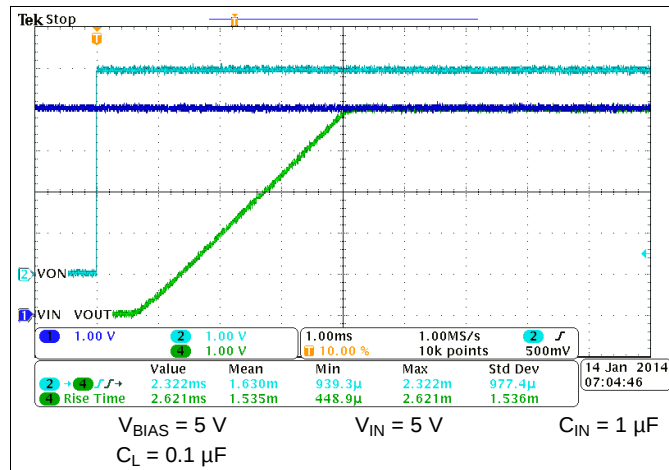


Figure 31. t_R at $V_{BIAS} = 5\text{ V}$

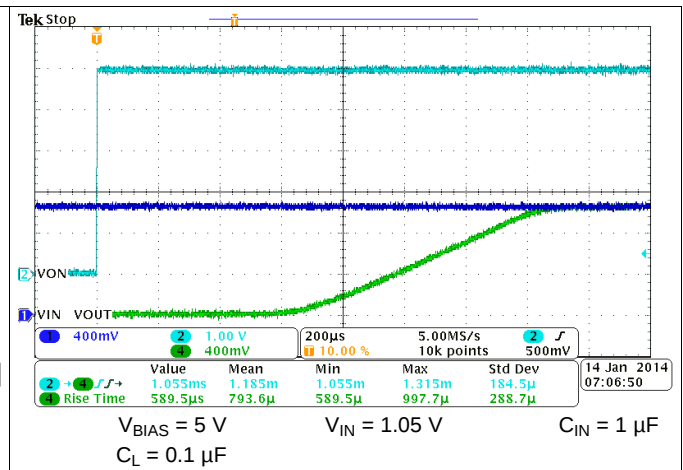


Figure 32. t_R at $V_{BIAS} = 5\text{ V}$

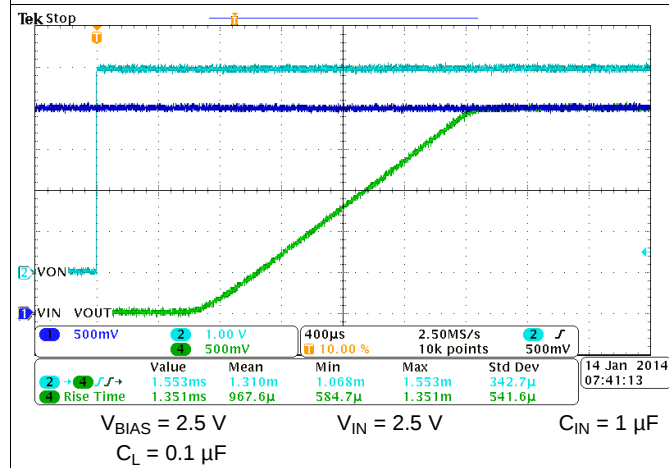


Figure 33. t_R at $V_{BIAS} = 2.5\text{ V}$

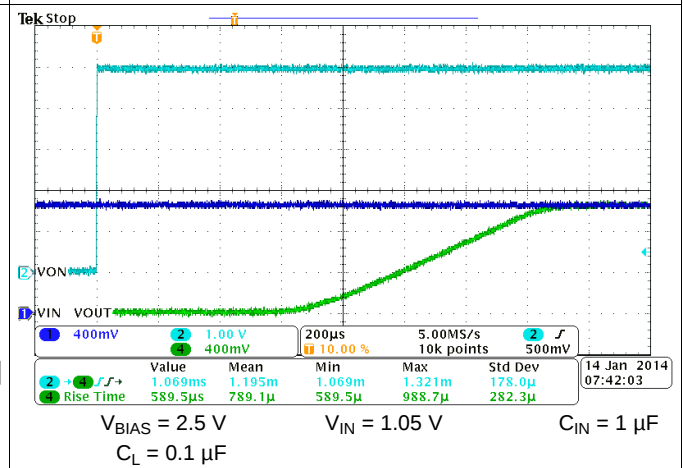


Figure 34. t_R at $V_{BIAS} = 2.5\text{ V}$

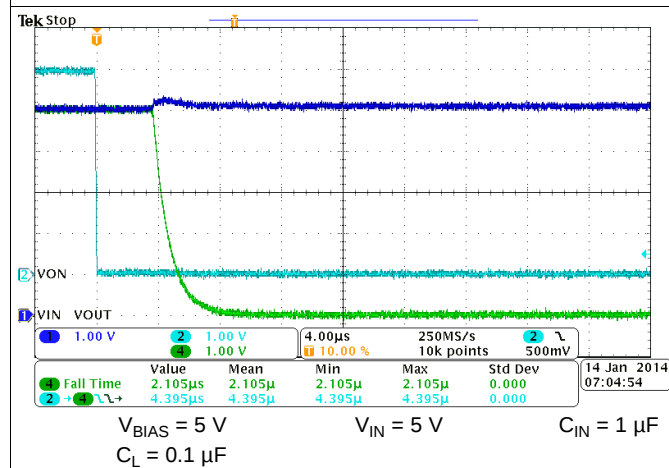


Figure 35. t_F at $V_{BIAS} = 5\text{ V}$

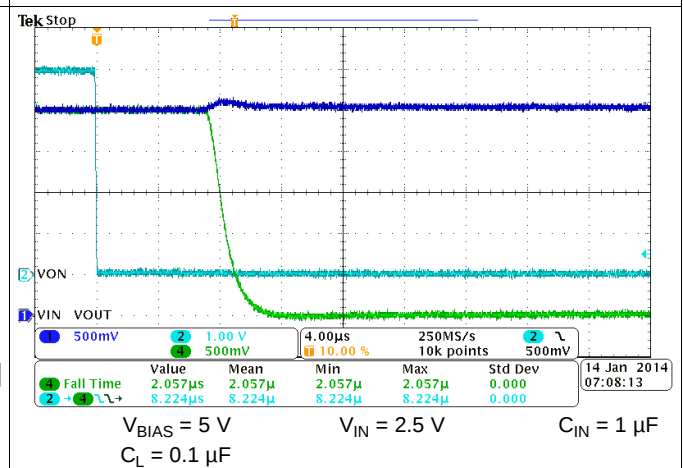


Figure 36. t_F at $V_{BIAS} = 5\text{ V}$

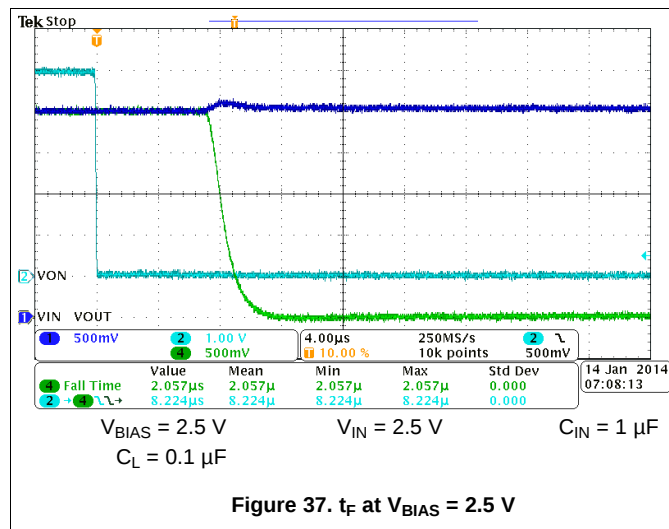


Figure 37. t_F at V_{BIAS} = 2.5 V

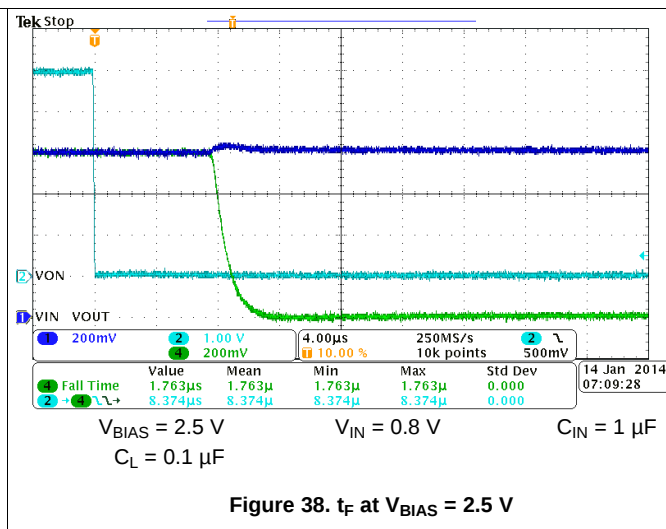


Figure 38. t_F at V_{BIAS} = 2.5 V

9 Power Supply Recommendations

The device is designed to operate from a V_{BIAS} range of 2.5 V to 5.5 V and V_{IN} range of 0.8 V to 5.5 V. This supply must be well regulated and placed as close to the device pin as possible with the recommended 1-μF bypass capacitor. If the supply is located more than a few inches from the device pins, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. If additional bulk capacitance is required, an electrolytic, tantalum, or ceramic capacitor of 10 μF may be sufficient.

10 Layout

10.1 Layout Guidelines

- VIN and VOUT traces should be as short and wide as possible to accommodate for high current.
- Use vias under the exposed thermal pad for thermal relief for high current operation.
- The VIN pin should be bypassed to ground with low ESR ceramic bypass capacitors. The typical recommended bypass capacitance is 1-μF ceramic with X5R or X7R dielectric. This capacitor should be placed as close to the device pins as possible.
- The VOUT pin should be bypassed to ground with low ESR ceramic bypass capacitors. The typical recommended bypass capacitance is one-tenth of the VIN bypass capacitor of X5R or X7R dielectric rating. This capacitor should be placed as close to the device pins as possible.
- The VBIAS pin should be bypassed to ground with low ESR ceramic bypass capacitors. The typical recommended bypass capacitance is 0.1-μF ceramic with X5R or X7R dielectric.

10.2 Layout Example

○ VIA to Power Ground Plane

⌋ VIA to VIN Plane

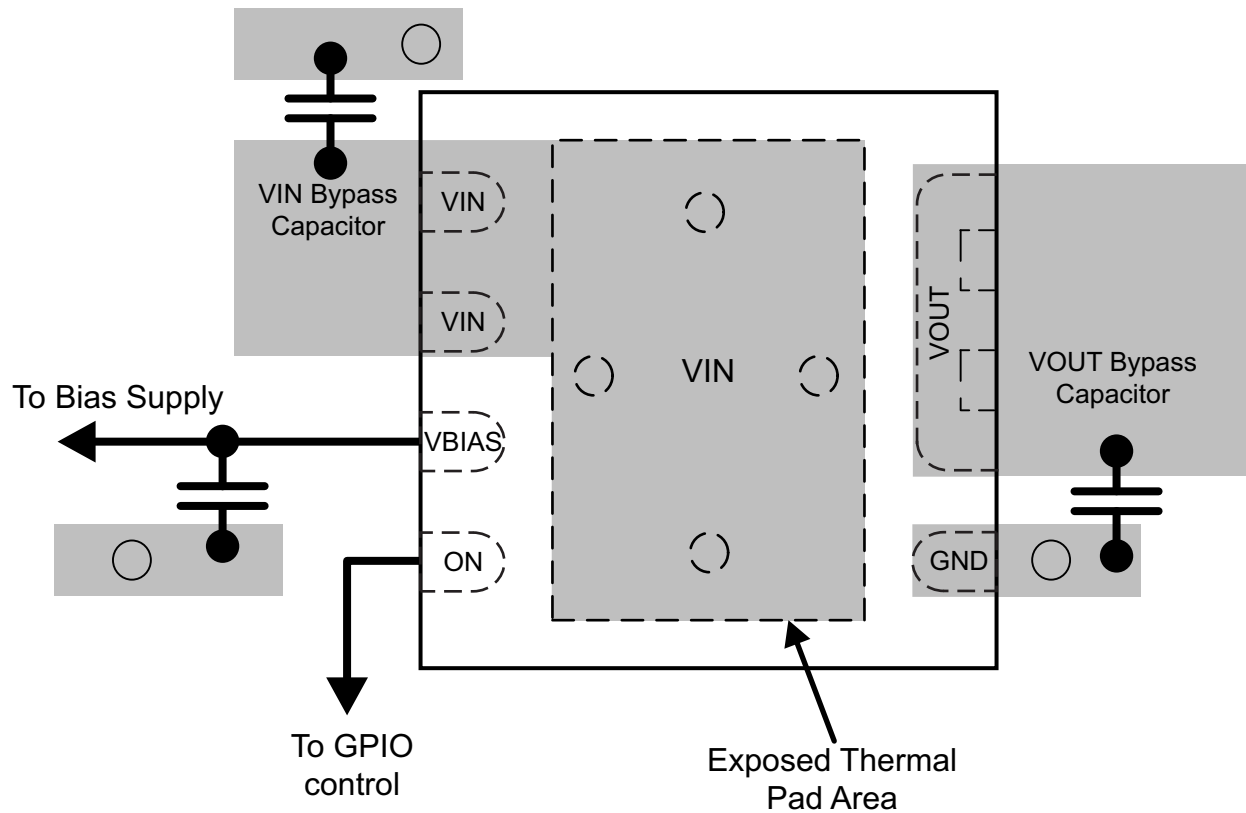


Figure 39. Recommended Board Layout

11 Device and Documentation Support

11.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.2 Trademarks

E2E is a trademark of Texas Instruments.

Ultrabook is a trademark of Intel.

All other trademarks are the property of their respective owners.

11.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.4 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS22969DNYR	Active	Production	WSO (DNY) 8	3000 LARGE T&R	Yes	Call TI Nipdau	Level-2-260C-1 YEAR	-40 to 85	969A0
TPS22969DNYT	Active	Production	WSO (DNY) 8	250 SMALL T&R	Yes	Call TI Nipdau	Level-2-260C-1 YEAR	-40 to 85	969A0

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

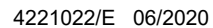
⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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PLASTIC QUAD FLATPACK- NO LEAD



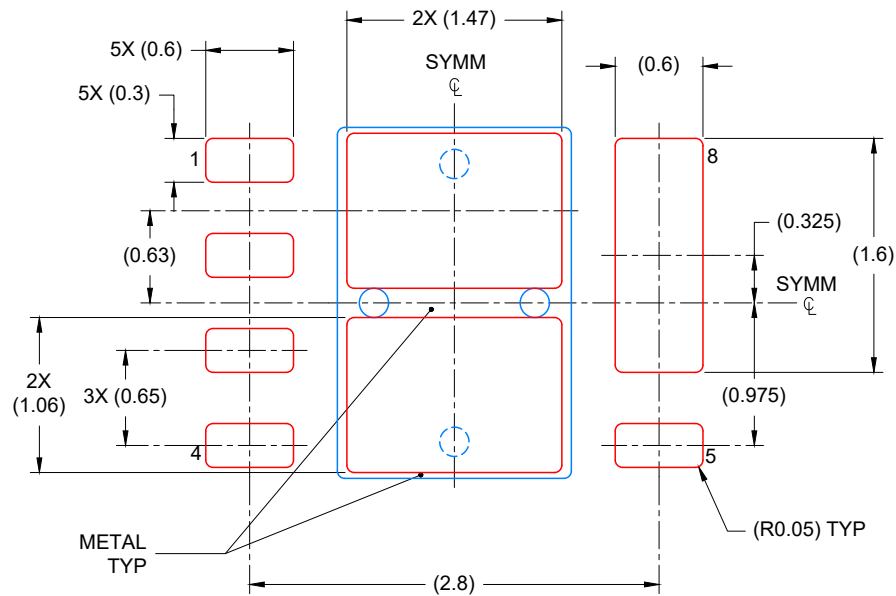
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

PLASTIC QUAD FLATPACK- NO LEAD

DNY0008A

WSN - 0.8 mm max height

PLASTIC QUAD FLATPACK- NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
81% PRINTED COVERAGE BY AREA
SCALE: 20X

4221022/E 06/2020

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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