

## Features

- High speed: 45 ns/55 ns
- Ultra-low standby power
  - Typical standby current: 3.5  $\mu$ A
  - Maximum standby current: 8.7  $\mu$ A
- Wide voltage range: 1.65 V to 2.2 V, 2.2 V to 3.6 V, 4.5 V to 5.5 V
- 1.0-V data retention
- TTL-compatible inputs and outputs
- Pb-free 48-ball VFBGA and 44-pin TSOP II packages

## Functional Description

CY62147GN and CY621472GN are high-performance CMOS low-power (MoBL) SRAM devices organized as 256K Words by 16-bits. Both devices are offered in single and dual chip enable options and in multiple pin configurations.

Devices with a single chip enable input are accessed by asserting the chip enable ( $\overline{CE}$ ) input LOW. Dual chip enable devices are accessed by asserting both chip enable inputs –  $\overline{CE}_1$  as low and  $\overline{CE}_2$  as HIGH.

Data writes are performed by asserting the Write Enable ( $\overline{WE}$ ) input LOW, while providing the data on I/O<sub>0</sub> through I/O<sub>15</sub> and address on A<sub>0</sub> through A<sub>17</sub> pins. The Byte High Enable ( $\overline{BHE}$ ) and Byte Low Enable ( $\overline{BLE}$ ) inputs control write operations to the upper and lower bytes of the specified memory location.  $\overline{BHE}$  controls I/O<sub>8</sub> through I/O<sub>15</sub> and  $\overline{BLE}$  controls I/O<sub>0</sub> through I/O<sub>7</sub>.

Data reads are performed by asserting the Output Enable ( $\overline{OE}$ ) input and providing the required address on the address lines. Read data is accessible on the I/O lines (I/O<sub>0</sub> through I/O<sub>15</sub>).

Byte accesses can be performed by asserting the required byte enable signal ( $\overline{BHE}$  or  $\overline{BLE}$ ) to read either the upper byte or the lower byte of data from the specified address location.

All I/Os (I/O<sub>0</sub> through I/O<sub>15</sub>) are placed in a HI-Z state when the device is deselected ( $\overline{CE}$  HIGH for a single chip enable device and  $\overline{CE}_1$  HIGH/ $\overline{CE}_2$  LOW for a dual chip enable device), or control signals are de-asserted ( $\overline{OE}$ ,  $\overline{BLE}$ ,  $\overline{BHE}$ ).

The device also has a unique Byte Power down feature, where, if both the Byte Enables ( $\overline{BHE}$  and  $\overline{BLE}$ ) are disabled, the devices seamlessly switch to standby mode irrespective of the state of the chip enables, thereby saving power.

The logic block diagram is provided in page 2.

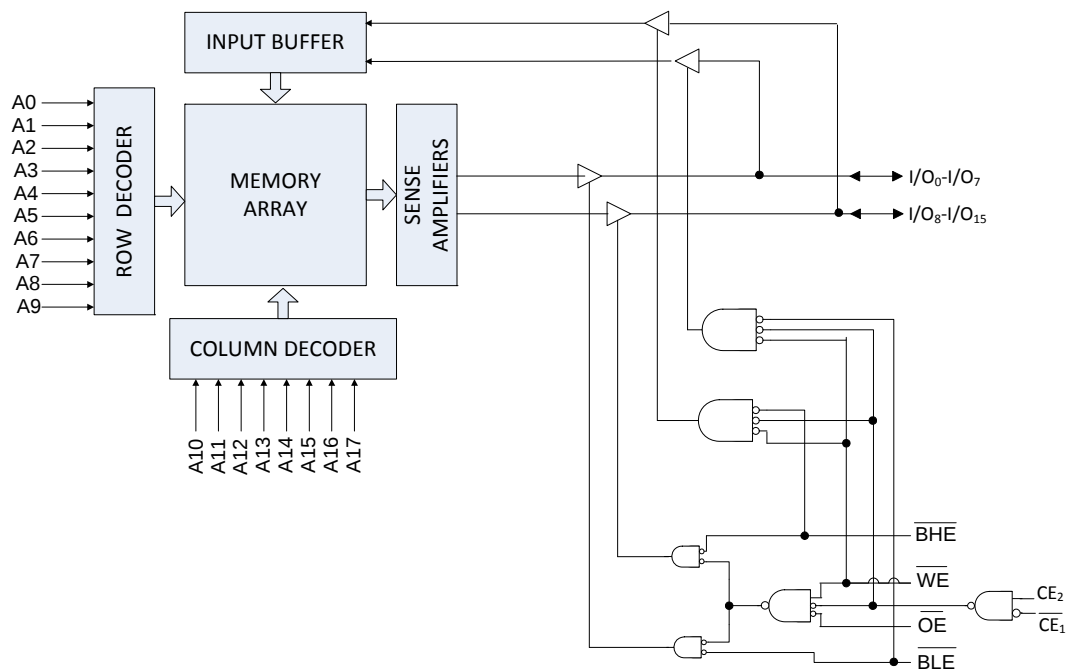
## Product Portfolio

| Product      | Features and Options<br>(see the Pin Configurations section) | Range      | V <sub>CC</sub> Range (V) | Speed (ns) | Power Dissipation                |     |                                      |     |
|--------------|--------------------------------------------------------------|------------|---------------------------|------------|----------------------------------|-----|--------------------------------------|-----|
|              |                                                              |            |                           |            | Operating I <sub>CC</sub> , (mA) |     | Standby, I <sub>SB2</sub> ( $\mu$ A) |     |
|              |                                                              |            |                           |            | f = f <sub>max</sub>             |     |                                      |     |
|              |                                                              |            |                           |            | Typ <sup>[1]</sup>               | Max | Typ <sup>[1]</sup>                   | Max |
| CY62147GN18  | Single or dual Chip Enables                                  | Industrial | 1.65 V–2.2 V              | 55         | 15                               | 20  | 3.5                                  | 10  |
| CY62147GN30  |                                                              |            | 2.2 V–3.6 V               | 45         | 15                               | 20  | 3.5                                  | 8.7 |
| CY621472GN30 |                                                              |            |                           |            |                                  |     |                                      |     |
| CY62147GN    |                                                              |            | 4.5 V–5.5 V               |            |                                  |     |                                      |     |

### Notes

- Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V<sub>CC</sub> = 1.8 V (for a V<sub>CC</sub> range of 1.65 V–2.2 V), V<sub>CC</sub> = 3 V (for V<sub>CC</sub> range of 2.2 V–3.6 V), and V<sub>CC</sub> = 5 V (for V<sub>CC</sub> range of 4.5 V–5.5 V), T<sub>A</sub> = 25 °C.

## Logic Block Diagram – CY62147GN



## Contents

|                                          |    |                                                      |           |
|------------------------------------------|----|------------------------------------------------------|-----------|
| Pin Configuration – CY62147GN .....      | 4  | Ordering Information .....                           | 16        |
| Pin Configuration – CY621472GN .....     | 5  | Ordering Code Definitions .....                      | 16        |
| Maximum Ratings .....                    | 6  | <b>Package Diagrams .....</b>                        | <b>17</b> |
| Operating Range .....                    | 6  | <b>Acronyms .....</b>                                | <b>18</b> |
| DC Electrical Characteristics .....      | 6  | <b>Document Conventions .....</b>                    | <b>18</b> |
| Capacitance .....                        | 8  | Units of Measure .....                               | 18        |
| Thermal Resistance .....                 | 8  | <b>Document History Page .....</b>                   | <b>19</b> |
| AC Test Loads and Waveforms .....        | 8  | <b>Sales, Solutions, and Legal Information .....</b> | <b>20</b> |
| Data Retention Characteristics .....     | 9  | Worldwide Sales and Design Support .....             | 20        |
| Data Retention Waveform .....            | 9  | Products .....                                       | 20        |
| AC Switching Characteristics .....       | 10 | PSoC <sup>®</sup> Solutions .....                    | 20        |
| Switching Waveforms .....                | 11 | Cypress Developer Community .....                    | 20        |
| Truth Table – CY62147GN/CY621472GN ..... | 15 | Technical Support .....                              | 20        |

## Pin Configuration – CY62147GN

Figure 1. 48-ball VFBGA pinout (Dual Chip Enable), CY62147GN<sup>[2]</sup>

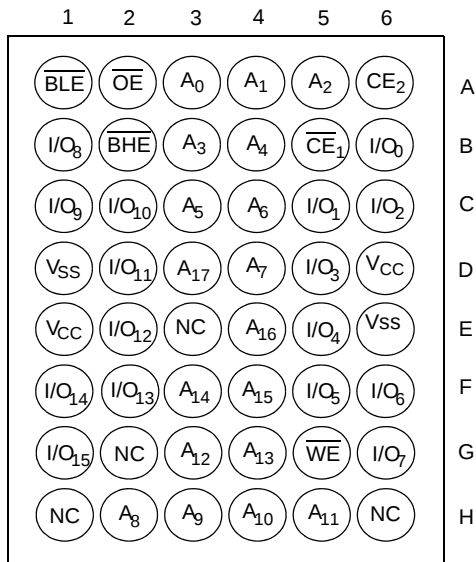


Figure 2. 48-ball VFBGA pinout (Single Chip Enable), CY62147GN<sup>[2]</sup>

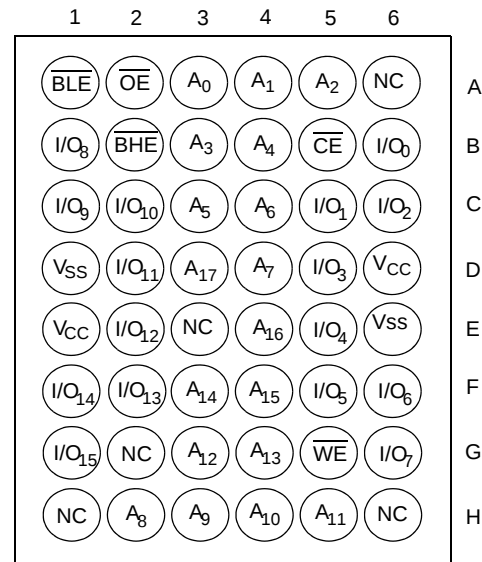
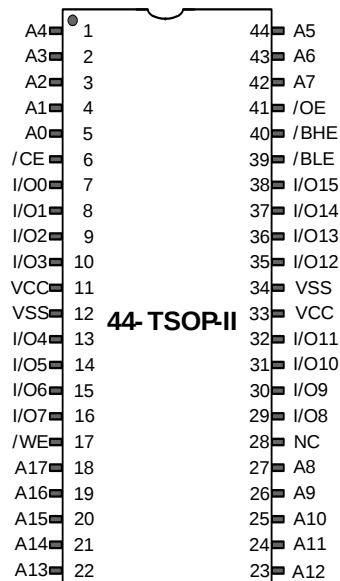


Figure 3. 44-pin TSOP II Pinout (Single Chip Enable), CY62147GN<sup>[2]</sup>

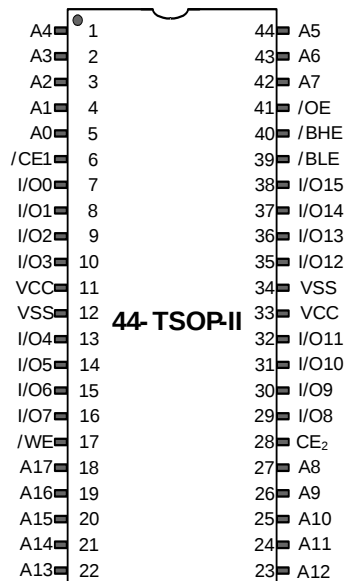


### Notes

- NC pins are not connected internally to the die and are typically used for address expansion to a higher-density device. Refer to the respective datasheets for pin configuration.

## Pin Configuration – CY621472GN

Figure 4. 44-pin TSOP II pinout (Dual Chip Enable), CY621472GN



## Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage temperature ..... –65 °C to + 150 °C

Ambient temperature  
with power applied ..... –55 °C to + 125 °C

Supply voltage  
to ground potential<sup>[3]</sup> ..... –0.5 V to  $V_{CC} + 0.5$  V

DC voltage applied to outputs  
in HI-Z state<sup>[3]</sup> ..... –0.5 V to  $V_{CC} + 0.5$  V

DC input voltage<sup>[3]</sup> ..... –0.5 V to  $V_{CC} + 0.5$  V

Output current into outputs (in low state) ..... 20 mA

Static discharge voltage  
(MIL-STD-883, Method 3015) ..... >2001 V

Latch-up current ..... >140 mA

## Operating Range

| Grade      | Ambient Temperature | $V_{CC}$                                              |
|------------|---------------------|-------------------------------------------------------|
| Industrial | –40 °C to +85 °C    | 1.65 V to 2.2 V,<br>2.2 V to 3.6 V,<br>4.5 V to 5.5 V |

## DC Electrical Characteristics

Over the operating range of –40 °C to 85 °C

| Parameter       | Description                              |                 | Test Conditions                                               |                                      | 45/55 ns |                                      |     | Unit |
|-----------------|------------------------------------------|-----------------|---------------------------------------------------------------|--------------------------------------|----------|--------------------------------------|-----|------|
|                 |                                          |                 |                                                               |                                      | Min      | Typ                                  | Max |      |
| V <sub>OH</sub> | Output HIGH voltage                      | 1.65 V to 2.2 V | V <sub>CC</sub> = Min, I <sub>OH</sub> = −0.1 mA              | 1.4                                  | –        | –                                    | V   |      |
|                 |                                          | 2.2 V to 2.7 V  | V <sub>CC</sub> = Min, I <sub>OH</sub> = −0.1 mA              | 2                                    | –        | –                                    |     |      |
|                 |                                          | 2.7 V to 3.6 V  | V <sub>CC</sub> = Min, I <sub>OH</sub> = −1.0 mA              | 2.4                                  | –        | –                                    |     |      |
|                 |                                          | 4.5 V to 5.5 V  | V <sub>CC</sub> = Min, I <sub>OH</sub> = −1.0 mA              | 2.4                                  | –        | –                                    |     |      |
|                 |                                          | 4.5 V to 5.5 V  | V <sub>CC</sub> = Min, I <sub>OH</sub> = −0.1 mA              | V <sub>CC</sub> − 0.5 <sup>[4]</sup> | –        | –                                    |     |      |
| V <sub>OL</sub> | Output LOW voltage                       | 1.65 V to 2.2 V | V <sub>CC</sub> = Min, I <sub>OL</sub> = 0.1 mA               | –                                    | –        | 0.2                                  | V   |      |
|                 |                                          | 2.2 V to 2.7 V  | V <sub>CC</sub> = Min, I <sub>OL</sub> = 0.1 mA               | –                                    | –        | 0.4                                  |     |      |
|                 |                                          | 2.7 V to 3.6 V  | V <sub>CC</sub> = Min, I <sub>OL</sub> = 2.1 mA               | –                                    | –        | 0.4                                  |     |      |
|                 |                                          | 4.5 V to 5.5 V  | V <sub>CC</sub> = Min, I <sub>OL</sub> = 2.1 mA               | –                                    | –        | 0.4                                  |     |      |
| V <sub>IH</sub> | Input HIGH voltage                       | 1.65 V to 2.2 V | –                                                             | 1.4                                  | –        | V <sub>CC</sub> + 0.2 <sup>[3]</sup> | V   |      |
|                 |                                          | 2.2 V to 2.7 V  | –                                                             | 1.8                                  | –        | V <sub>CC</sub> + 0.3 <sup>[3]</sup> |     |      |
|                 |                                          | 2.7 V to 3.6 V  | –                                                             | 2                                    | –        | V <sub>CC</sub> + 0.3 <sup>[3]</sup> |     |      |
|                 |                                          | 4.5 V to 5.5 V  | –                                                             | 2.2                                  | –        | V <sub>CC</sub> + 0.5 <sup>[3]</sup> |     |      |
| V <sub>IL</sub> | Input LOW voltage                        | 1.65 V to 2.2 V | –                                                             | −0.2 <sup>[3]</sup>                  | –        | 0.4                                  | V   |      |
|                 |                                          | 2.2 V to 2.7 V  | –                                                             | −0.3 <sup>[3]</sup>                  | –        | 0.6                                  |     |      |
|                 |                                          | 2.7 V to 3.6 V  | –                                                             | −0.3 <sup>[3]</sup>                  | –        | 0.8                                  |     |      |
|                 |                                          | 4.5 V to 5.5 V  | –                                                             | −0.5 <sup>[3]</sup>                  | –        | 0.8                                  |     |      |
| I <sub>IX</sub> | Input leakage current                    |                 | GND ≤ V <sub>IN</sub> ≤ V <sub>CC</sub>                       |                                      | −1       | –                                    | +1  | μA   |
| I <sub>OZ</sub> | Output leakage current                   |                 | GND ≤ V <sub>OUT</sub> ≤ V <sub>CC</sub> ,<br>Output disabled |                                      | −1       | –                                    | +1  | μA   |
| I <sub>CC</sub> | V <sub>CC</sub> operating supply current |                 | Max V <sub>CC</sub> , I <sub>OUT</sub> = 0 mA,<br>CMOS levels | f =<br>22.22 MHz<br>(45 ns)          | –        | 15                                   | 20  | mA   |
|                 |                                          |                 |                                                               | f =<br>18.18 MHz<br>(55 ns)          | –        | 15                                   | 20  | mA   |
|                 |                                          |                 |                                                               | f = 1 MHz                            | –        | 3.5                                  | 6   | mA   |

### Notes

3.  $V_{IL(\text{min})} = -2.0 \text{ V}$  and  $V_{IH(\text{max})} = V_{CC} + 2 \text{ V}$  for pulse durations of less than 20 ns.

4. This parameter is guaranteed by design and not tested.

**DC Electrical Characteristics** (continued)

Over the operating range of –40 °C to 85 °C

| Parameter       | Description                                                                                                             | Test Conditions                                                                                                                                                                                                                                                                                                                            |                      | 45/55 ns |     |     | Unit          |
|-----------------|-------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|----------|-----|-----|---------------|
|                 |                                                                                                                         |                                                                                                                                                                                                                                                                                                                                            |                      | Min      | Typ | Max |               |
| $I_{SB1}^{[5]}$ | Automatic power down current – CMOS inputs;<br>$V_{CC} = 2.2\text{ V to }3.6\text{ V and }4.5\text{ V to }5.5\text{ V}$ | $\overline{CE}_1 \geq V_{CC} - 0.2\text{ V or }CE_2 \leq 0.2\text{ V or }(\overline{BHE} \text{ and } \overline{BLE}) \geq V_{CC} - 0.2\text{ V},$<br>$V_{IN} \geq V_{CC} - 0.2\text{ V or }V_{IN} \leq 0.2\text{ V},$<br>$f = f_{\text{max}}$ (address and data only),<br>$f = 0$ ( $\overline{OE}$ , and $\overline{WE}$ ), Max $V_{CC}$ |                      | –        | 3.5 | 8.7 | $\mu\text{A}$ |
|                 | Automatic power down current – CMOS inputs<br>$V_{CC} = 1.65\text{ V to }2.2\text{ V}$                                  |                                                                                                                                                                                                                                                                                                                                            |                      | –        | –   | 10  |               |
| $I_{SB2}^{[5]}$ | Automatic power down current – CMOS inputs<br>$V_{CC} = 2.2\text{ V to }3.6\text{ V and }4.5\text{ V to }5.5\text{ V}$  | $\overline{CE}_1 \geq V_{CC} - 0.2\text{ V or }CE_2 \leq 0.2\text{ V or }(\overline{BHE} \text{ and } \overline{BLE}) \geq V_{CC} - 0.2\text{ V},$<br>$V_{IN} \geq V_{CC} - 0.2\text{ V or }V_{IN} \leq 0.2\text{ V},$<br>$f = 0$ , Max $V_{CC}$                                                                                           | 25 °C <sup>[6]</sup> | –        | 3.5 | 3.7 | $\mu\text{A}$ |
|                 |                                                                                                                         |                                                                                                                                                                                                                                                                                                                                            | 40 °C <sup>[6]</sup> | –        | –   | 4.8 |               |
|                 |                                                                                                                         |                                                                                                                                                                                                                                                                                                                                            | 70 °C <sup>[6]</sup> | –        | –   | 7   |               |
|                 |                                                                                                                         |                                                                                                                                                                                                                                                                                                                                            | 85 °C                | –        | –   | 8.7 |               |
|                 | Automatic power down current – CMOS inputs<br>$V_{CC} = 1.65\text{ V to }2.2\text{ V}$                                  | $\overline{CE}_1 \geq V_{CC} - 0.2\text{ V or }CE_2 \leq 0.2\text{ V or }(\overline{BHE} \text{ and } \overline{BLE}) \geq V_{CC} - 0.2\text{ V},$<br>$V_{IN} \geq V_{CC} - 0.2\text{ V or }V_{IN} \leq 0.2\text{ V},$<br>$f = 0$ , Max $V_{CC}$                                                                                           | 25 °C <sup>[6]</sup> | –        | 3.5 | 4.3 |               |
|                 |                                                                                                                         |                                                                                                                                                                                                                                                                                                                                            | 40 °C <sup>[6]</sup> | –        | –   | 5   |               |
|                 |                                                                                                                         |                                                                                                                                                                                                                                                                                                                                            | 70 °C <sup>[6]</sup> | –        | –   | 7.5 |               |
|                 |                                                                                                                         |                                                                                                                                                                                                                                                                                                                                            | 85 °C                | –        | –   | 10  |               |

**Notes**

- Chip enables ( $\overline{CE}_1$  and  $CE_2$ ) must be tied to CMOS levels to meet the  $I_{SB1}$  /  $I_{SB2}$  /  $I_{CCDR}$  spec. Other inputs can be left floating.
- The  $I_{SB2}$  limits at 25 °C, 40 °C, 70 °C, and typical limit at 85 °C are guaranteed by design and not 100% tested.

## Capacitance

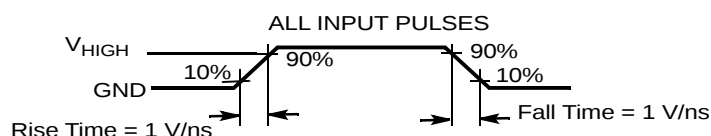
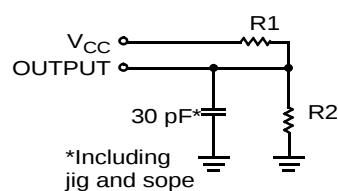
| Parameter <sup>[7]</sup> | Description        | Test Conditions                                                           | Max | Unit |
|--------------------------|--------------------|---------------------------------------------------------------------------|-----|------|
| C <sub>IN</sub>          | Input capacitance  | T <sub>A</sub> = 25 °C, f = 1 MHz, V <sub>CC</sub> = V <sub>CC(typ)</sub> | 10  | pF   |
| C <sub>OUT</sub>         | Output capacitance |                                                                           | 10  | pF   |

## Thermal Resistance

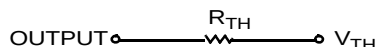
| Parameter <sup>[7]</sup> | Description                              | Test Conditions                                                         | 48-ball VFBGA | 44-pin TSOP II | Unit |
|--------------------------|------------------------------------------|-------------------------------------------------------------------------|---------------|----------------|------|
| Θ <sub>JA</sub>          | Thermal resistance (junction to ambient) | Still air, soldered on a 3 × 4.5 inch, four layer printed circuit board | 31.35         | 68.85          | °C/W |
| Θ <sub>JC</sub>          | Thermal resistance (junction to case)    |                                                                         | 14.74         | 15.97          | °C/W |

## AC Test Loads and Waveforms

Figure 5. AC Test Loads and Waveforms<sup>[8]</sup>



Equivalent to: THÉVENIN EQUIVALENT



| Parameters      | 1.8 V | 2.5 V | 3.0 V | 5.0 V | Unit |
|-----------------|-------|-------|-------|-------|------|
| R1              | 13500 | 16667 | 1103  | 1800  | Ω    |
| R2              | 10800 | 15385 | 1554  | 990   | Ω    |
| R <sub>TH</sub> | 6000  | 8000  | 645   | 639   | Ω    |
| V <sub>TH</sub> | 0.80  | 1.20  | 1.75  | 1.77  | V    |

### Notes

7. Tested initially and after any design or process changes that may affect these parameters.
8. Full-device operation requires linear V<sub>CC</sub> ramp from V<sub>DR</sub> to V<sub>CC(min)</sub> ≥ 100 μs or stable at V<sub>CC(min)</sub> ≥ 100 μs.

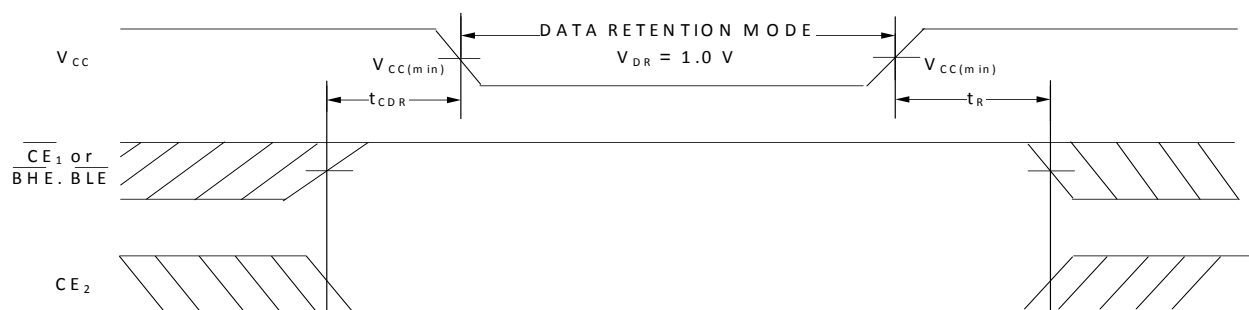
## Data Retention Characteristics

Over the Operating range

| Parameter             | Description                          | Conditions                                                                                                                                                                                                                                                         | Min   | Typ <sup>[9]</sup> | Max | Unit          |
|-----------------------|--------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|--------------------|-----|---------------|
| $V_{DR}$              | $V_{CC}$ for data retention          |                                                                                                                                                                                                                                                                    | 1     | —                  | —   | V             |
| $I_{CCDR}^{[10, 11]}$ | Data retention current               | $V_{CC} = 1.2 \text{ V}$ ,<br>$\overline{CE}_1 \geq V_{CC} - 0.2 \text{ V}$ or $CE_2 \leq 0.2 \text{ V}$<br>or $(\overline{BHE} \text{ and } \overline{BLE}) \geq V_{CC} - 0.2 \text{ V}$ ,<br>$V_{IN} \geq V_{CC} - 0.2 \text{ V}$ or $V_{IN} \leq 0.2 \text{ V}$ | —     |                    | 13  | $\mu\text{A}$ |
| $t_{CDR}^{[12]}$      | Chip deselect to data retention time |                                                                                                                                                                                                                                                                    | 0     | —                  | —   | ns            |
| $t_R^{[13]}$          | Operation recovery time              |                                                                                                                                                                                                                                                                    | 45/55 | —                  | —   | ns            |

## Data Retention Waveform

Figure 6. Data Retention Waveform<sup>[14]</sup>



### Notes

9. Typical values are included only for reference and are not guaranteed or tested. Typical values are measured at  $V_{CC} = 1.8 \text{ V}$  (for  $V_{CC}$  range of 1.65 V–2.2 V),  $V_{CC} = 3 \text{ V}$  (for  $V_{CC}$  range of 2.2 V–3.6 V), and  $V_{CC} = 5 \text{ V}$  (for  $V_{CC}$  range of 4.5 V–5.5 V),  $T_A = 25^\circ\text{C}$ .
10. Chip enables ( $\overline{CE}_1$  and  $CE_2$ ) must be tied to CMOS levels to meet the  $I_{SB1}$  /  $I_{SB2}$  /  $I_{CCDR}$  spec. Other inputs can be left floating.
11.  $I_{CCDR}$  is guaranteed only after device is first powered up to  $V_{CC(min)}$  and then brought down to  $V_{DR}$ .
12. These parameters are guaranteed by design.
13. Full-device operation requires linear  $V_{CC}$  ramp from  $V_{DR}$  to  $V_{CC(min)} \geq 100 \mu\text{s}$  or stable at  $V_{CC(min)} \geq 100 \mu\text{s}$ .
14.  $\overline{BHE}.\overline{BLE}$  is the AND of both  $\overline{BHE}$  and  $\overline{BLE}$ . Deselect the chip by either disabling the chip enable signals or by disabling both  $\overline{BHE}$  and  $\overline{BLE}$ .

## AC Switching Characteristics

| Parameter <sup>[15, 16]</sup>   | Description                                                                     | 45 ns |     | 55 ns |     | Unit |
|---------------------------------|---------------------------------------------------------------------------------|-------|-----|-------|-----|------|
|                                 |                                                                                 | Min   | Max | Min   | Max |      |
| READ CYCLE                      |                                                                                 |       |     |       |     |      |
| t <sub>RC</sub>                 | Read cycle time                                                                 | 45    | –   | 55    | –   | ns   |
| t <sub>AA</sub>                 | Address to data valid                                                           | –     | 45  | –     | 55  | ns   |
| t <sub>OHA</sub>                | Data hold from address change                                                   | 10    | –   | 10    | –   | ns   |
| t <sub>ACE</sub>                | $\overline{CE}_1$ LOW and CE <sub>2</sub> HIGH to data valid                    | –     | 45  | –     | 55  | ns   |
| t <sub>DOE</sub>                | $\overline{OE}$ LOW to data valid                                               | –     | 22  | –     | 25  | ns   |
| t <sub>LZOE</sub>               | $\overline{OE}$ LOW to Low impedance <sup>[17]</sup>                            | 5     | –   | 5     | –   | ns   |
| t <sub>HZOE</sub>               | $\overline{OE}$ HIGH to HI-Z <sup>[17, 18]</sup>                                | –     | 18  | –     | 18  | ns   |
| t <sub>LZCE</sub>               | $\overline{CE}_1$ LOW and CE <sub>2</sub> HIGH to Low impedance <sup>[17]</sup> | 10    | –   | 10    | –   | ns   |
| t <sub>HZCE</sub>               | $\overline{CE}_1$ HIGH and CE <sub>2</sub> LOW to HI-Z <sup>[17, 18]</sup>      | –     | 18  | –     | 18  | ns   |
| t <sub>PU</sub>                 | $\overline{CE}_1$ LOW and CE <sub>2</sub> HIGH to power-up                      | 0     | –   | 0     | –   | ns   |
| t <sub>PD</sub>                 | $\overline{CE}_1$ HIGH and CE <sub>2</sub> LOW to power-down                    | –     | 45  | –     | 55  | ns   |
| t <sub>DBE</sub>                | $\overline{BLE}$ / $\overline{BHE}$ LOW to data valid                           | –     | 45  | –     | 55  | ns   |
| t <sub>LZBE</sub>               | $\overline{BLE}$ / $\overline{BHE}$ LOW to Low impedance <sup>[17]</sup>        | 5     | –   | 5     | –   | ns   |
| t <sub>HZBE</sub>               | $\overline{BLE}$ / $\overline{BHE}$ HIGH to HI-Z <sup>[17, 18]</sup>            | –     | 18  | –     | 18  | ns   |
| WRITE CYCLE <sup>[19, 20]</sup> |                                                                                 |       |     |       |     |      |
| t <sub>WC</sub>                 | Write cycle time                                                                | 45    | –   | 55    | –   | ns   |
| t <sub>SCE</sub>                | $\overline{CE}_1$ LOW and CE <sub>2</sub> HIGH to write end                     | 35    | –   | 45    | –   | ns   |
| t <sub>AW</sub>                 | Address setup to write end                                                      | 35    | –   | 45    | –   | ns   |
| t <sub>HA</sub>                 | Address hold from write end                                                     | 0     | –   | 0     | –   | ns   |
| t <sub>SA</sub>                 | Address setup to write start                                                    | 0     | –   | 0     | –   | ns   |
| t <sub>PWE</sub>                | $\overline{WE}$ pulse width                                                     | 35    | –   | 40    | –   | ns   |
| t <sub>BW</sub>                 | $\overline{BLE}$ / $\overline{BHE}$ LOW to write end                            | 35    | –   | 45    | –   | ns   |
| t <sub>SD</sub>                 | Data setup to write end                                                         | 25    | –   | 25    | –   | ns   |
| t <sub>HD</sub>                 | Data hold from write end                                                        | 0     | –   | 0     | –   | ns   |
| t <sub>HZWE</sub>               | $\overline{WE}$ LOW to HI-Z <sup>[17, 18]</sup>                                 | –     | 18  | –     | 20  | ns   |
| t <sub>LZWE</sub>               | $\overline{WE}$ HIGH to Low impedance <sup>[17]</sup>                           | 10    | –   | 10    | –   | ns   |

### Notes

15. Test conditions assume a signal transition time (rise/fall) of 3 ns or less, timing reference levels of 1.5 V (for  $V_{CC} \geq 3$  V) and  $V_{CC}/2$  (for  $V_{CC} < 3$  V), and input pulse levels of 0 to 3 V (for  $V_{CC} \geq 3$  V) and 0 to  $V_{CC}$  (for  $V_{CC} < 3$  V). Test conditions for the read cycle use output loading shown in AC Test Loads and Waveforms section, unless specified otherwise.

16. These parameters are guaranteed by design.

17. At any temperature and voltage condition,  $t_{HZCE}$  is less than  $t_{LZCE}$ ,  $t_{HZBE}$  is less than  $t_{LZBE}$ ,  $t_{HZOE}$  is less than  $t_{LZOE}$ , and  $t_{HZWE}$  is less than  $t_{LZWE}$  for any device.

18.  $t_{HZOE}$ ,  $t_{HZCE}$ ,  $t_{HZBE}$ , and  $t_{HZWE}$  transitions are measured when the outputs enter a high-impedance state.

19. The internal write time of the memory is defined by the overlap of  $\overline{WE} = V_{IL}$ ,  $\overline{CE}_1 = V_{IL}$ ,  $\overline{BHE}$  or  $\overline{BLE}$ , or both =  $V_{IL}$ , and  $CE_2 = V_{IH}$ . All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must refer to the edge of the signal that terminates the write.

20. The minimum pulse width in Write Cycle No. 3 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW) should be equal to sum of  $t_{SD}$  and  $t_{HZWE}$ .

## Switching Waveforms

Figure 7. Read Cycle No. 1 of CY62147GN (Address Transition Controlled)<sup>[21, 22]</sup>

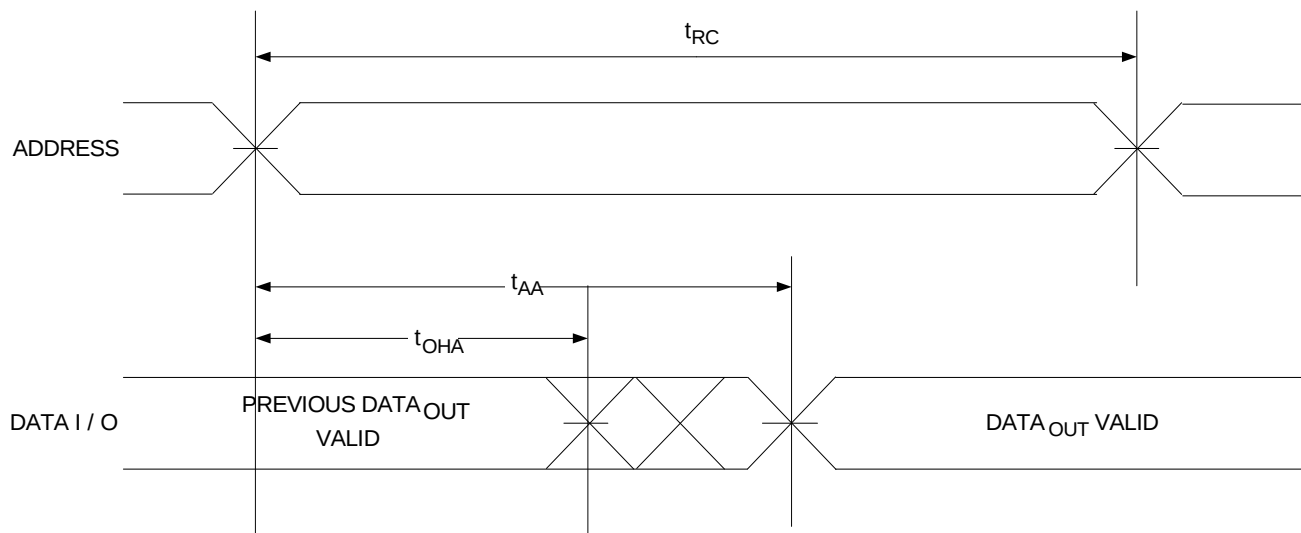
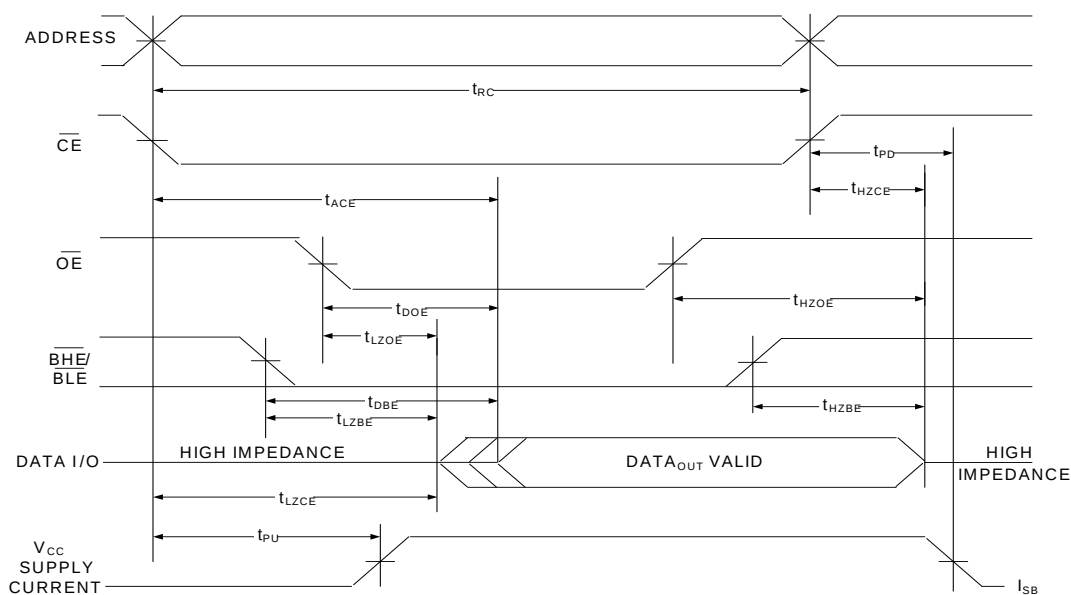


Figure 8. Read Cycle No. 2 ( $\overline{\text{OE}}$  Controlled)<sup>[21, 22, 23, 24]</sup>

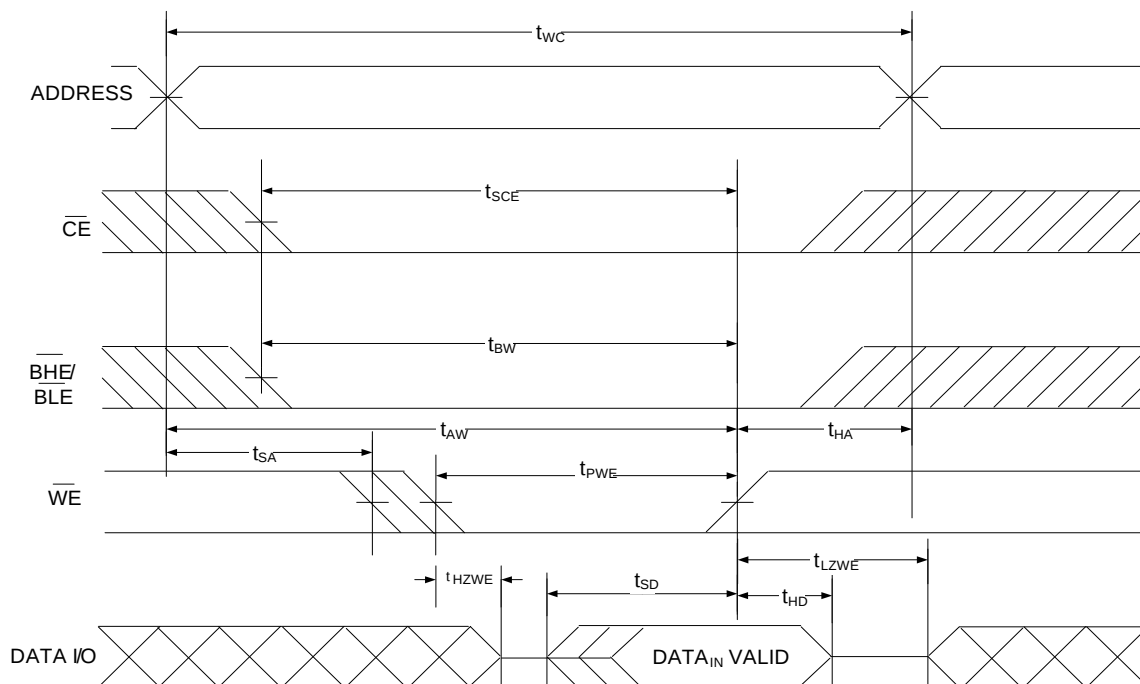


### Notes

21. The device is continuously selected.  $\overline{\text{OE}} = V_{\text{IL}}$ ,  $\overline{\text{CE}} = V_{\text{IL}}$ ,  $\overline{\text{BHE}}$  or  $\overline{\text{BLE}}$  or both =  $V_{\text{IL}}$ .
22.  $\overline{\text{WE}}$  is HIGH for Read cycle.
23. Data I/O is in a HI-Z state if  $\overline{\text{CE}} = V_{\text{IH}}$ , or  $\overline{\text{OE}} = V_{\text{IH}}$  or  $\overline{\text{BHE}}$ , and/or  $\overline{\text{BLE}} = V_{\text{IH}}$ .
24. Address valid prior to or coincident with  $\overline{\text{CE}}$  LOW transition.

## Switching Waveforms (continued)

**Figure 9. Write Cycle No. 1 ( $\overline{\text{WE}}$  Controlled)**<sup>[25, 26, 27]</sup>

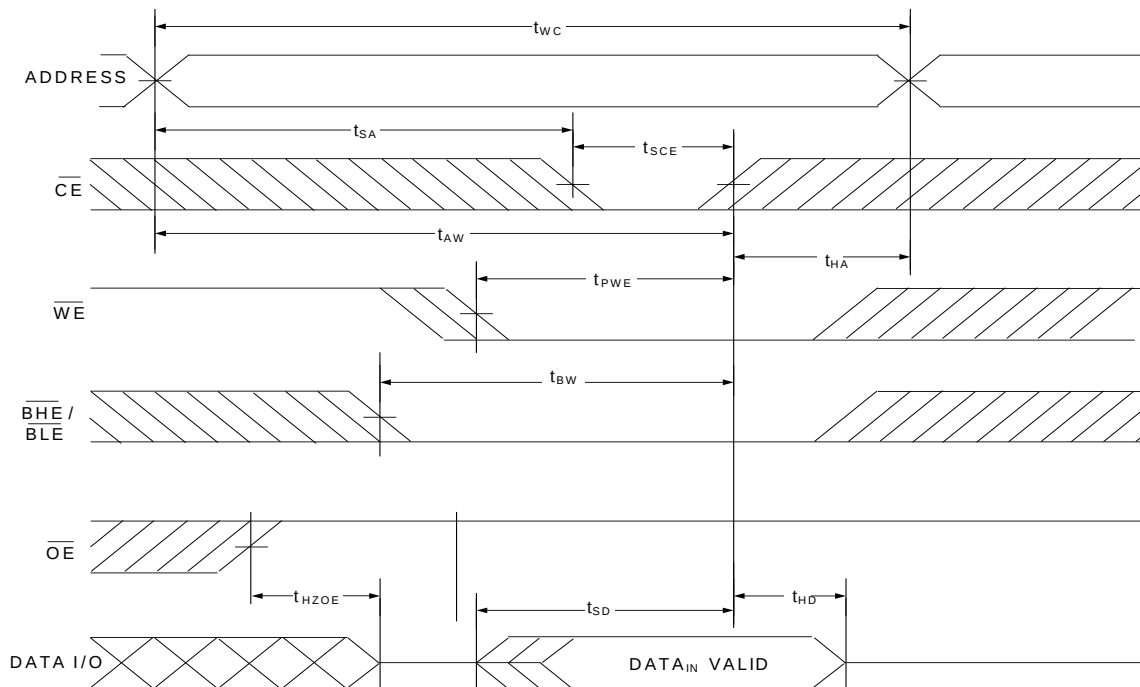


### Notes

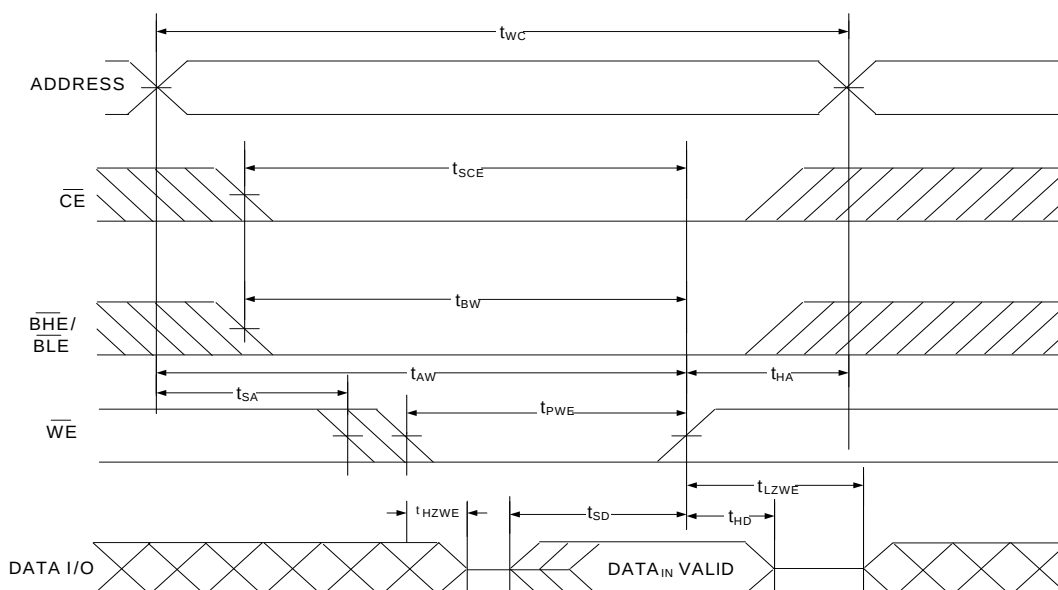
25. For all dual chip enable devices,  $\overline{\text{CE}}$  is the logical combination of  $\overline{\text{CE}}_1$  and  $\text{CE}_2$ . When  $\overline{\text{CE}}_1$  is LOW and  $\text{CE}_2$  is HIGH,  $\overline{\text{CE}}$  is LOW; when  $\overline{\text{CE}}_1$  is HIGH or  $\text{CE}_2$  is LOW,  $\overline{\text{CE}}$  is HIGH.
26. The internal write time of the memory is defined by the overlap of  $\overline{\text{WE}} = V_{\text{IL}}$ ,  $\overline{\text{CE}}_1 = V_{\text{IL}}$ ,  $\overline{\text{BHE}}$  or  $\overline{\text{BLE}}$  or both =  $V_{\text{IL}}$ , and  $\text{CE}_2 = V_{\text{IH}}$ . All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must refer to the edge of the signal that terminates the write.
27. Data I/O is in a HI-Z state if  $\overline{\text{CE}} = V_{\text{IH}}$ , or  $\overline{\text{OE}} = V_{\text{IH}}$  or  $\overline{\text{BHE}}$ , and/or  $\overline{\text{BLE}} = V_{\text{IH}}$ .

## Switching Waveforms (continued)

**Figure 10. Write Cycle No. 2 ( $\overline{\text{CE}}$  Controlled)**<sup>[28, 29, 30]</sup>



**Figure 11. Write Cycle No. 3 ( $\overline{\text{WE}}$  Controlled,  $\overline{\text{OE}}$  LOW)**<sup>[28, 29, 30, 31]</sup>



### Notes

28. For all dual chip enable devices,  $\overline{\text{CE}}$  is the logical combination of  $\overline{\text{CE}}_1$  and  $\text{CE}_2$ . When  $\overline{\text{CE}}_1$  is LOW and  $\text{CE}_2$  is HIGH,  $\overline{\text{CE}}$  is LOW; when  $\overline{\text{CE}}_1$  is HIGH or  $\text{CE}_2$  is LOW,  $\overline{\text{CE}}$  is HIGH.

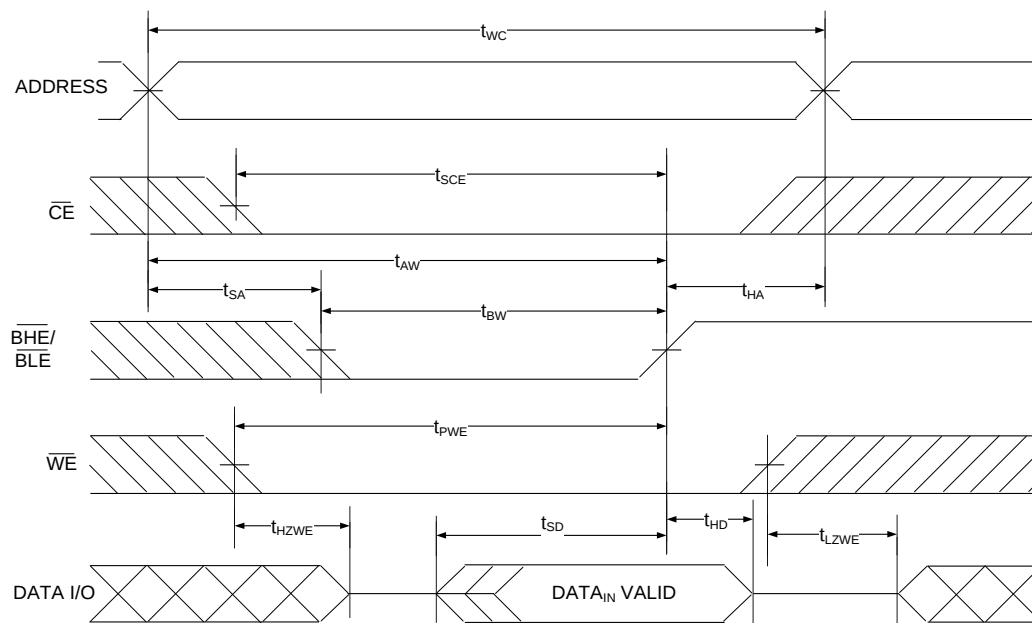
29. The internal write time of the memory is defined by the overlap of  $\overline{\text{WE}} = V_{\text{IL}}$ ,  $\overline{\text{CE}}_1 = V_{\text{IL}}$ ,  $\overline{\text{BHE}}$  or  $\overline{\text{BLE}}$  or both =  $V_{\text{IL}}$ , and  $\text{CE}_2 = V_{\text{IH}}$ . All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must refer to the edge of the signal that terminates the write.

30. Data I/O is in HI-Z state if  $\overline{\text{CE}} = V_{\text{IH}}$ , or  $\overline{\text{OE}} = V_{\text{IH}}$  or  $\overline{\text{BHE}}$ , and/or  $\overline{\text{BLE}} = V_{\text{IH}}$ .

31. The minimum write pulse width for Write Cycle No. 3 ( $\overline{\text{WE}}$  Controlled,  $\overline{\text{OE}}$  LOW) should be sum of  $t_{\text{HZWE}}$  and  $t_{\text{SD}}$ .

## Switching Waveforms (continued)

**Figure 12. Write Cycle No. 4 ( $\overline{\text{BHE}}/\overline{\text{BLE}}$  Controlled)**<sup>[32, 33, 34]</sup>



### Notes

32. For all dual chip enable devices,  $\overline{\text{CE}}$  is the logical combination of  $\overline{\text{CE}}_1$  and  $\text{CE}_2$ . When  $\overline{\text{CE}}_1$  is LOW and  $\text{CE}_2$  is HIGH,  $\overline{\text{CE}}$  is LOW; when  $\overline{\text{CE}}_1$  is HIGH or  $\text{CE}_2$  is LOW,  $\overline{\text{CE}}$  is HIGH.
33. The internal write time of the memory is defined by the overlap of  $\overline{\text{WE}} = V_{\text{IL}}$ ,  $\overline{\text{CE}}_1 = V_{\text{IL}}$ ,  $\overline{\text{BHE}}$  or  $\overline{\text{BLE}}$  or both =  $V_{\text{IL}}$ , and  $\text{CE}_2 = V_{\text{IH}}$ . All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must refer to the edge of the signal that terminates the write.
34. Data I/O is in a HI-Z state if  $\overline{\text{CE}} = V_{\text{IH}}$ , or  $\overline{\text{OE}} = V_{\text{IH}}$  or  $\overline{\text{BHE}}$ , and/or  $\overline{\text{BLE}} = V_{\text{IH}}$ .

**Truth Table – CY62147GN/CY621472GN**

| $\overline{CE_1}/\overline{CE}^{[35]}$ | $CE_2^{[35]}$     | $\overline{WE}$ | $\overline{OE}$ | $\overline{BHE}$ | $\overline{BLE}$ | Inputs/Outputs                                                   | Mode                | Power                |
|----------------------------------------|-------------------|-----------------|-----------------|------------------|------------------|------------------------------------------------------------------|---------------------|----------------------|
| H                                      | X <sup>[36]</sup> | X               | X               | X                | X                | HI-Z                                                             | Deselect/Power-down | Standby ( $I_{SB}$ ) |
| X                                      | L                 | X               | X               | X                | X                | HI-Z                                                             | Deselect/Power-down | Standby ( $I_{SB}$ ) |
| X                                      | X                 | X               | X               | H                | H                | HI-Z                                                             | Deselect/Power-down | Standby ( $I_{SB}$ ) |
| L                                      | H                 | H               | L               | L                | L                | Data Out ( $I/O_0$ – $I/O_{15}$ )                                | Read                | Active ( $I_{CC}$ )  |
| L                                      | H                 | H               | L               | H                | L                | Data Out ( $I/O_0$ – $I/O_7$ );<br>HI-Z ( $I/O_8$ – $I/O_{15}$ ) | Read                | Active ( $I_{CC}$ )  |
| L                                      | H                 | H               | L               | L                | H                | HI-Z ( $I/O_0$ – $I/O_7$ );<br>Data Out ( $I/O_8$ – $I/O_{15}$ ) | Read                | Active ( $I_{CC}$ )  |
| L                                      | H                 | H               | H               | L                | H                | HI-Z                                                             | Output disabled     | Active ( $I_{CC}$ )  |
| L                                      | H                 | H               | H               | H                | L                | HI-Z                                                             | Output disabled     | Active ( $I_{CC}$ )  |
| L                                      | H                 | H               | H               | L                | L                | HI-Z                                                             | Output disabled     | Active ( $I_{CC}$ )  |
| L                                      | H                 | L               | X               | L                | L                | Data In ( $I/O_0$ – $I/O_{15}$ )                                 | Write               | Active ( $I_{CC}$ )  |
| L                                      | H                 | L               | X               | H                | L                | Data In ( $I/O_0$ – $I/O_7$ );<br>HI-Z ( $I/O_8$ – $I/O_{15}$ )  | Write               | Active ( $I_{CC}$ )  |
| L                                      | H                 | L               | X               | L                | H                | HI-Z ( $I/O_0$ – $I/O_7$ );<br>Data In ( $I/O_8$ – $I/O_{15}$ )  | Write               | Active ( $I_{CC}$ )  |

**Notes**

35. For all dual chip enable devices,  $\overline{CE}$  is the logical combination of  $\overline{CE_1}$  and  $CE_2$ . When  $\overline{CE_1}$  is LOW and  $CE_2$  is HIGH,  $\overline{CE}$  is LOW; when  $\overline{CE_1}$  is HIGH or  $CE_2$  is LOW,  $\overline{CE}$  is HIGH

36. The 'X' (Don't care) state for the chip enables refer to the logic state (either HIGH or LOW). Intermediate voltage levels on these pins is not permitted.



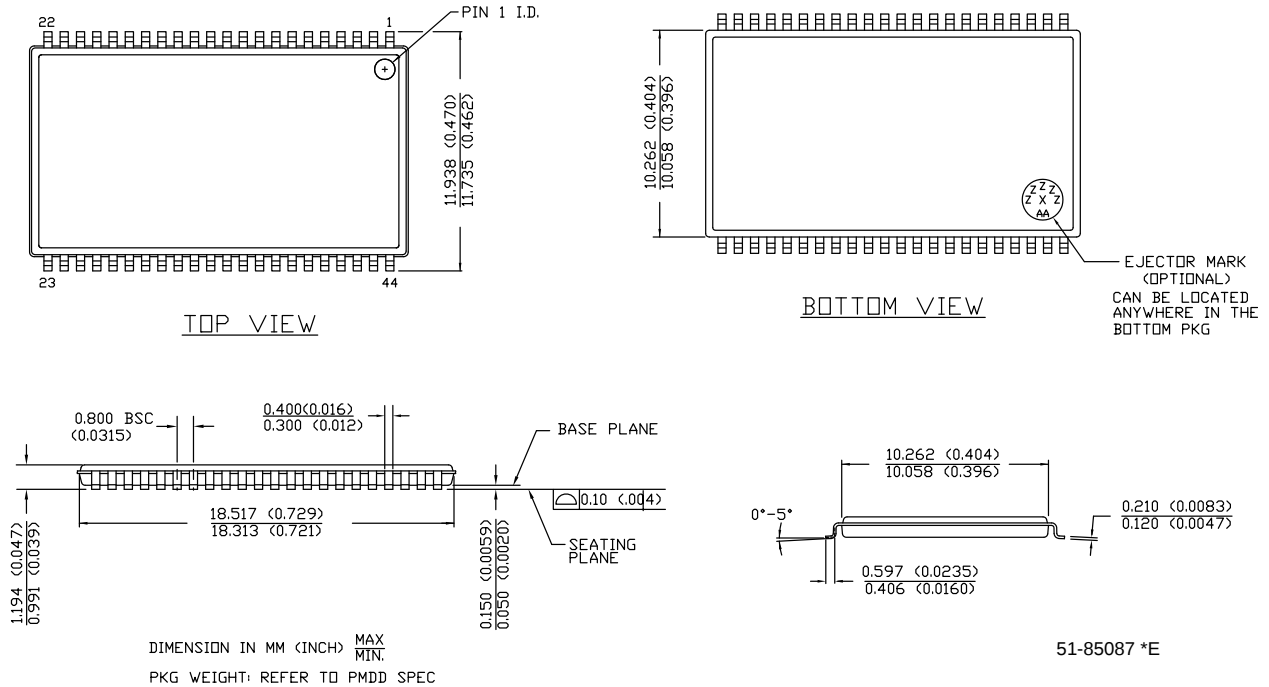
| Speed (ns) | Voltage Range | Ordering Code        | Package Diagram | Package Type                                                    | Operating Range |
|------------|---------------|----------------------|-----------------|-----------------------------------------------------------------|-----------------|
| 45         | 2.2 V–3.6 V   | CY62147GN30-45BVXI   | 51-85150        | 48-ball VFBGA (6 × 8 × 1 mm), Dual Chip Enable                  | Industrial      |
|            |               | CY62147GN30-45BVXIT  | 51-85150        | 48-ball VFBGA (6 × 8 × 1 mm), Dual Chip Enable, Tape and Reel   |                 |
|            |               | CY62147GN30-45ZSXI   | 51-85087        | 44-pin TSOP II, Single Chip Enable                              |                 |
|            |               | CY62147GN30-45ZSXIT  | 51-85087        | 44-pin TSOP II, Single Chip Enable, Tape and Reel               |                 |
|            |               | CY62147GN30-45B2XI   | 51-85150        | 48-ball VFBGA (6 × 8 × 1 mm), Single Chip Enable                |                 |
|            |               | CY62147GN30-45B2XIT  | 51-85150        | 48-ball VFBGA (6 × 8 × 1 mm), Single Chip Enable, Tape and Reel |                 |
|            |               | CY621472GN30-45ZSXI  | 51-85087        | 44-pin TSOP II, Dual Chip Enable                                |                 |
|            |               | CY621472GN30-45ZSXIT | 51-85087        | 44-pin TSOP II, Dual Chip Enable, Tape and Reel                 |                 |
| 55         | 1.65 V–2.2 V  | CY62147GN18-55BVXI   | 51-85150        | 48-ball VFBGA (6 × 8 × 1 mm), Single Chip Enable                | Industrial      |
|            |               | CY62147GN18-55BVXIT  | 51-85150        | 48-ball VFBGA (6 × 8 × 1 mm), Single Chip Enable, Tape and Reel |                 |

Diagram illustrating the breakdown of the MoBL SRAM part number: **CY 621 4 7 X GN XX - XX XX X X X**.

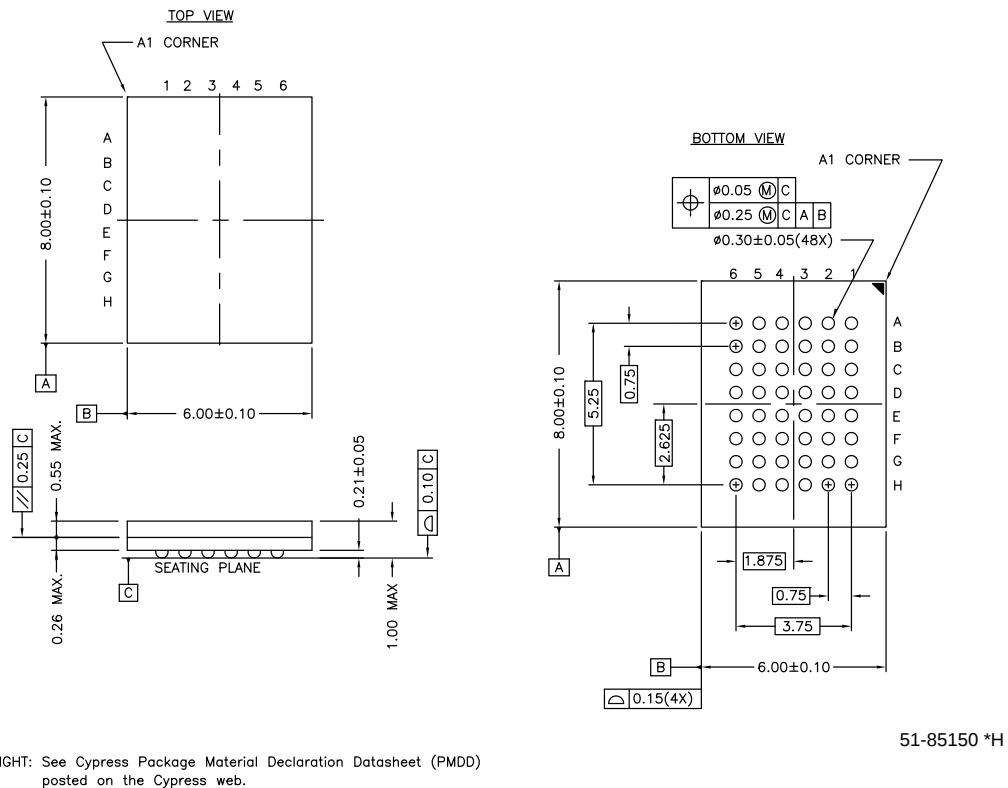
- CY**: Company ID: CY = Cypress
- 621**: Family Code: 621 = MoBL SRAM family
- 4**: Density: 4 = 4-Mbit
- 7**: Bus Width: 7 =  $\times 16$
- X**: Chip Enable: X = blank or 2  
blank = Single Chip Enable; 2 = Dual Chip Enable
- GN**: Process Technology: GN = 65 nm
- XX**: Voltage Range: 30 = 3 V typ
- : Speed Grade: XX = 45 ns or 55 ns
- XX**: Package Type: XX = BV, B2 or ZS  
BV = 48-ball VFBGA (Dual Chip Enable);  
B2 = 48-ball VFBGA (Single Chip Enable)  
ZS = 44-pin TSOP II
- XX**: Pb-free
- X**: Temperature Grade: X = I, I = Industrial
- X**: X: T = Tape and Reel; Blank = Bulk

## Package Diagrams

**Figure 13. 44-pin TSOP II (Z44) Package Outline, 51-85087**



**Figure 14. 48-ball VFBGA (6 × 8 × 1.0 mm) BV48/BZ48 Package Outline, 51-85150**



## Acronyms

**Table 1. Acronyms Used in this Document**

| Acronym | Description                             |
|---------|-----------------------------------------|
| BHE     | byte high enable                        |
| BLE     | byte low enable                         |
| CE      | chip enable                             |
| CMOS    | complementary metal oxide semiconductor |
| I/O     | input/output                            |
| OE      | output enable                           |
| SRAM    | static random access memory             |
| TSOP    | thin small outline package              |
| VFBGA   | very fine-pitch ball grid array         |
| WE      | write enable                            |

## Document Conventions

### Units of Measure

**Table 2. Units of Measure**

| Symbol | Unit of Measure |
|--------|-----------------|
| °C     | degrees Celsius |
| MHz    | megahertz       |
| μA     | microamperes    |
| μs     | microseconds    |
| mA     | milliamperes    |
| mm     | millimeters     |
| ns     | nanoseconds     |
| Ω      | ohms            |
| %      | percent         |
| pF     | picofarads      |
| V      | volts           |
| W      | watts           |

## Document History Page

| Document Title: CY62147GN/CY621472GN MoBL®, 4-Mbit (256K words × 16 bit) Static RAM<br>Document Number: 002-10624 |         |                 |                 |                                                                                                                                                                                                                                                                                                                       |
|-------------------------------------------------------------------------------------------------------------------|---------|-----------------|-----------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Rev.                                                                                                              | ECN No. | Orig. of Change | Submission Date | Description of Change                                                                                                                                                                                                                                                                                                 |
| **                                                                                                                | 5076421 | NILE            | 01/07/2016      | New data sheet.                                                                                                                                                                                                                                                                                                       |
| *A                                                                                                                | 5084145 | NILE            | 01/13/2016      | Updated <a href="#">Logic Block Diagram – CY62147GN</a> .                                                                                                                                                                                                                                                             |
| *B                                                                                                                | 5329364 | VINI            | 06/29/2016      | Updated <a href="#">Ordering Information</a> :<br>Updated part numbers.<br>Updated to new template.                                                                                                                                                                                                                   |
| *C                                                                                                                | 5429186 | NILE            | 09/07/2016      | Updated <a href="#">DC Electrical Characteristics</a> : Enhanced VIH of 2.2V - 2.7V operating range from 2.0V to 1.8V. Enhanced VOH of 2.7V - 3.6V operating range from 2.2V to 2.4V.<br>Updated <a href="#">Ordering Information</a> : Updated part numbers.<br>Updated Note 3.<br>Updated Copyright and Disclaimer. |
| *D                                                                                                                | 6002285 | AESATP12        | 12/21/2017      | Updated logo and copyright.                                                                                                                                                                                                                                                                                           |

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