1.8 V/2.5 V/3.3 V 8 GHz/14 Gbps Differential 1:4 Clock/Data CML Fanout Buffer w/ Selectable Input Equalizer

Multi−Level Inputs w/ Internal Termination

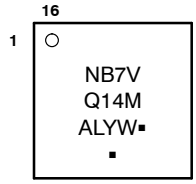
NB7VQ14M



1

QFN−16
MN SUFFIX
CASE 485G

MARKING DIAGRAM*

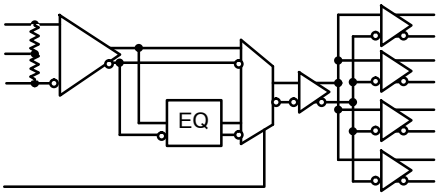


A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
▪	= Pb−Free Package

(Note: Microdot may be in either location)

*For additional marking information, refer to Application Note AND8002/D.

SIMPLIFIED BLOCK DIAGRAM



ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 9 of this data sheet.

Description

The NB7VQ14M is a high performance differential 1:4 CML fanout buffer with a selectable Equalizer receiver. When placed in series with a Clock /Data path operating up to 8 GHz or 14 Gb/s, respectively, the NB7VQ14M inputs will compensate the degraded signal transmitted across a FR4 PCB backplane or cable interconnect and output four identical CML copies of the input signal with a 1.8 V, 2.5 V or 3.3 V power supply. Therefore, the serial data rate is increased by reducing Inter−Symbol Interference (ISI) caused by losses in copper interconnect or long cables. The EQualizer ENable pin (EQEN) allows the IN/$\overline{\text{IN}}$ inputs to either flow through or bypass the Equalizer section. Control of the Equalizer function is realized by setting EQEN; When EQEN is set Low, the IN/$\overline{\text{IN}}$ inputs bypass the Equalizer. When EQEN is set High, the IN/$\overline{\text{IN}}$ inputs flow through the Equalizer. The default state at start−up is LOW. As such, NB7VQ14M is ideal for SONET, GigE, Fiber Channel, Backplane and other Clock/Data distribution applications.

The differential inputs incorporate internal 50 Ω termination resistors that are accessed through the VT pin. This feature allows the NB7VQ14M to accept various logic level standards, such as LVPECL, CML or LVDS. The 1:4 fanout design was optimized for low output skew applications.

The NB7VQ14M is a member of the GigaComm™ family of high performance clock products.

Features

- Input Data Rate > 14 Gb/s, Typical
- Input Clock Frequency > 8 GHz, Typical
- 165 ps Typical Propagation Delay
- 30 ps Typical Rise and Fall Times
- < 15 ps Maximum Output Skew
- < 0.8 ps Maximum RMS Clock Jitter
- < 10 ps pp of Data Dependent Jitter
- Differential CML Outputs, 400 mV Peak−to−Peak, Typical
- Selectable Input Equalization
- Operating Range: V_{CC} = 1.71 V to 3.6 V with GND = 0 V
- Internal Input Termination Resistors, 50 Ω
- −40°C to +85°C Ambient Operating Temperature
- These are Pb−Free Devices

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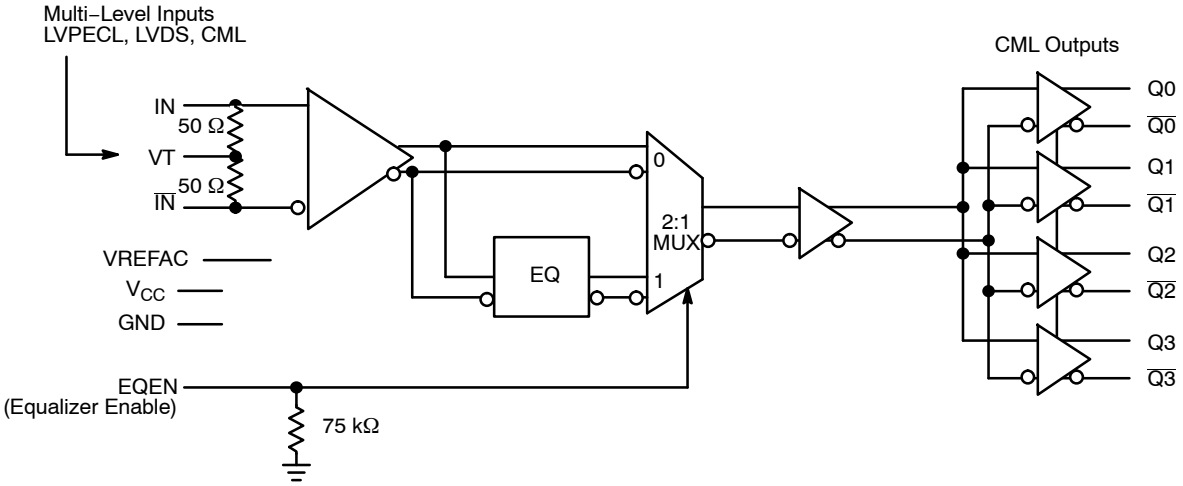


Figure 1. Detailed Block Diagram of NB7VQ14M

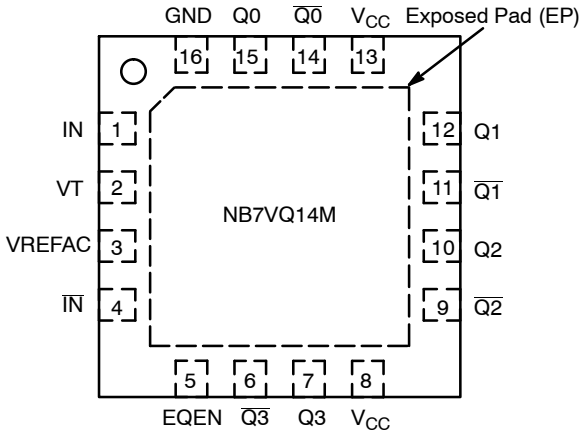


Figure 2. QFN−16 Pinout (Top View)

Table 1. EQUALIZER ENABLE FUNCTION

EQEN	Function
0	IN / $\overline{\text{IN}}$ Inputs By−pass the Equalizer section
1	Inputs flow through the Equalizer

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Table 2. PIN DESCRIPTION

Pin	Name	I/O	Description
1	IN	LVPECL, CML, LVDS Input	Non−inverted Differential Input. (Note 1)
2	VT		Internal 100 Ω Center−tapped Termination Pin for IN / $\overline{\text{IN}}$
3	VREFAC		Output Voltage Reference for Capacitor−Coupled Inputs, only
4	$\overline{\text{IN}}$	LVPECL, CML, LVDS Input	Inverted Differential Input. (Note 1)
5	EQEN	LVCMOS Input	Equalizer Enable Input; pin will default LOW when left open (has internal pull−down resistor)
6	$\overline{\text{Q3}}$	CML Output	Inverted Differential Output. Typically Terminated with 50 Ω Resistor to V_{CC}.
7	Q3	CML Output	Non−inverted Differential Output. Typically Terminated with 50 Ω Resistor to V_{CC}.
8	VCC	−	Positive Supply Voltage
9	$\overline{\text{Q2}}$	CML Output	Inverted Differential Output. Typically Terminated with 50 Ω Resistor to V_{CC}.
10	Q2	CML Output	Non−inverted Differential Output. Typically Terminated with 50 Ω Resistor to V_{CC}.
11	$\overline{\text{Q1}}$	CML Output	Inverted Differential Output. Typically Terminated with 50 Ω Resistor to V_{CC}.
12	Q1	CML Output	Non−inverted Differential Output. Typically Terminated with 50 Ω Resistor to V_{CC}.
13	VCC	−	Positive Supply Voltage
14	$\overline{\text{Q0}}$	CML Output	Inverted Differential Output. Typically Terminated with 50 Ω Resistor to V_{CC}.
15	Q0	CML Output	Non−inverted Differential Output. Typically Terminated with 50 Ω Resistor to V_{CC}.
16	GND	−	Negative Supply Voltage
−	EP	−	The Exposed Pad (EP) on the QFN−16 package bottom is thermally connected to the die for improved heat transfer out of package. The exposed pad must be attached to a heat−sinking conduit. The pad is electrically connected to the die, and must be electrically and thermally connected to GND on the PC board.

1. In the differential configuration when the input termination pin (VT) is connected to a common termination voltage or left open, and if no signal is applied on IN / $\overline{\text{IN}}$ input, then, the device will be susceptible to self−oscillation.
2. All VCC and GND pins must be externally connected to a power supply for proper operation.

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Table 3. ATTRIBUTES

Characteristics	Value
ESD Protection Human Body Model Machine Model	 > 2 kV > 200 V
R_{PD} – EQEN Input Pulldown Resistor	75 kΩ
Moisture Sensitivity (Note 3) 16–QFN	 Level 1
Flammability Rating Oxygen Index: 28 to 34	 UL 94 V–0 @ 0.125 in
Transistor Count	210
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test	

3. For additional information, see Application Note AND8003/D.

Table 4. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V_{CC}	Positive Power Supply – Core	GND = 0 V		4.0	V
V_{IO}	Positive Input/Output Voltage	GND = 0 V		–0.5 to V_{CC} + 0.5	V
V_{INPP}	Differential Input Voltage |IN – $\overline{IN}$|			1.89	V
I_{IN}	Input Current Through R_T (50 Ω Resistor)			±40	mA
I_{OUT}	Output Current Through R_T (50 Ω Resistor)			±40	mA
$I_{VFREFAC}$	VREFAC Sink/Source Current			±1.5	mA
T_A	Operating Temperature Range	16 QFN		–40 to +85	°C
T_{stg}	Storage Temperature Range			–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction–to–Ambient) (Note 4)	0 lfpm 500 lfpm	16 QFN 16 QFN	42 35	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction–to–Case) (Note 4)		16 QFN	4	°C/W
T_{sol}	Wave Solder Pb–Free			265	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

4. JEDEC standard multilayer board – 2S2P (2 signal, 2 power) with 8 filled thermal vias under exposed pad.

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Table 5. DC CHARACTERISTICS, MULTI−LEVEL INPUTS V_{CC} = 1.71 V to 3.6 V, GND = 0 V, T_A = −40°C to 85°C (Note 5)

Symbol	Characteristic	Min	Typ	Max	Unit
POWER SUPPLY CURRENT					
V_{CC}	Power Supply Voltage V_{CC} = 3.3 V V_{CC} = 2.5 V V_{CC} = 1.8 V	 3.135 2.375 1.71	 3.3 2.5 1.8	 3.6 2.625 1.89	V
I_{CC}	Power Supply Current (Inputs and Outputs Open)		170	210	mA
CML OUTPUTS (Note 6)					
V_{OH}	Output HIGH Voltage V_{CC} = 3.3 V V_{CC} = 2.5 V V_{CC} = 1.8 V	V_{CC} − 30 3270 2470 1770	V_{CC} − 5 3295 2495 1795	V_{CC} 3300 2500 1800	mV
V_{OL}	Output LOW Voltage V_{CC} = 3.3 V V_{CC} = 2.5 V V_{CC} = 1.8 V	V_{CC} − 525 2775 1975 1275	V_{CC} − 425 2875 2075 1375	V_{CC} − 325 2975 2175 1475	mV
DIFFERENTIAL INPUT DRIVEN SINGLE−ENDED (see Figures 5 and 7) (Note 7)					
V_{IH}	Single−ended Input HIGH Voltage	V_{th} + 100		V_{CC}	mV
V_{IL}	Single−ended Input LOW Voltage	GND		V_{th} −100	mV
V_{th}	Input Threshold Reference Voltage Range (Note 8)	1050		V_{CC} − 100	mV
V_{ISE}	Single−ended Input Voltage Amplitude (V_{IH} − V_{IL})	200		2800	mV
VREFAC					
V_{REFAC}	Output Reference Voltage @ 100 μA for capacitor− coupled inputs, only (Note 9) V_{CC} = 3.3 V V_{CC} = 2.5 V V_{CC} = 1.8 V	V_{CC} − 650 2650 1850 1150	V_{CC} − 500 2800 2000 1300	V_{CC} − 350 2950 2150 1450	mV
DIFFERENTIAL INPUTS DRIVEN DIFFERENTIALLY (see Figures 6 and 8) (Note 9)					
V_{IHD}	Differential Input HIGH Voltage	1200		V_{CC}	mV
V_{ILD}	Differential Input LOW Voltage	0		V_{IHD} − 100	mV
V_{ID}	Differential Input Voltage (V_{IHD} − V_{ILD})	100		1200	mV
V_{CMR}	Input Common Mode Range (Differential Configuration) (Note 10) (Figure 9)	1050		V_{CC} − 50	mV
I_{IH}	Input HIGH Current IN / $\overline{IN}$, (VT Open)	−150		150	μA
I_{IL}	Input LOW Current IN / $\overline{IN}$, (VT Open)	−150		150	μA
CONTROL INPUTS (EQEN)					
V_{IH}	Input HIGH Voltage for Control Pins	V_{CC} x 0.65		V_{CC}	V
V_{IL}	Input LOW Voltage for Control Pins	GND		V_{CC} x 0.35	V
I_{IH}	Input HIGH Current	−150		150	μA
I_{IL}	Input LOW Current	−150		150	μA
TERMINATION RESISTORS					
R_{TIN}	Internal Input Termination Resistor	45	50	55	Ω
R_{TOUT}	Internal Output Termination Resistor	45	50	55	Ω

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

5. Input and output parameters vary 1:1 with V_{CC}.
6. CML outputs loaded with 50 Ω to V_{CC} for proper operation.
7. V_{th}, V_{IH}, V_{IL}, and V_{ISE} parameters must be complied with simultaneously.
8. V_{th} is applied to the complementary input when operating in single−ended mode.
9. V_{IHD}, V_{ILD}, V_{ID}, and V_{CMR} parameters must be complied with simultaneously.
10. V_{CMR} min varies 1:1 with GND, V_{CMR} max varies 1:1 with V_{CC}. The V_{CMR} range is referenced to the crosspoint side of the differential input signal.

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Table 6. AC CHARACTERISTICS V_{CC} = 1.71 V to 3.6 V, GND = 0 V, T_A = −40°C to 85°C (Note 11)

Symbol	Characteristic		Min	Typ	Max	Unit
f_{MAX}	Maximum Input Clock Frequency;	$V_{OUT} \geq$ 200 mV	7	8.5		GHz
$f_{DATAMAX}$	Maximum Operating Data Rate NRZ, (PRBS23)		10	14		Gbps
V_{OUTPP}	Output Voltage Amplitude, EQEN = 0 or 1 (Note 15) (See Figure 10)	$f_{in} \leq$ 7 GHz	200	400		mV
t_{PLH}, t_{PHL}	Propagation Delay	IN to Q_x	125	175	225	ps
t_{SKEW}	Duty Cycle Skew (Note 12) Output – Output Within Device Skew Device to Device Skew			 3	 15 50	ps
t_{DC}	Output Clock Duty Cycle (Reference Duty Cycle = 50%)	$f_{in} \leq$ 7 GHz	40	50	60	%
Φ_N	Phase Noise, fin = 1 GHz	10 kHz 100 kHz 1 MHz 10 MHz 20 MHz 40 MHz		−134 −136 −150 −151 −151 −151		dBc
$t_{\int \Phi N}$	Integrated Phase Jitter f_{in} = 1 GHz, 12 kHz – 20 MHz Offset (RMS)			35		fs
t_{JITTER}	RMS Random Clock Jitter (Note 13) Peak−to−Peak Data Dependent Jitter (Note 14) $f_{IN} \leq$ 14 Gbps EQEN = 0 (≤ 3” FR4) $f_{IN} \leq$ 10 Gbps EQEN = 1 (12” FR4)	$f_{in} \leq$ 7 GHz		0.2	0.8 10 10	ps rms ps pk−pk ps pk−pk
V_{INPP}	Input Voltage Swing/Sensitivity (Differential Configuration) (Note 15)		100		1200	mV
t_r t_f	Output Rise/Fall Times @ 1.0 GHz (20% – 80%)	Qx, $\overline{Qx}$	15	30	45	ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

11. Measured by forcing V_{INPP} 400mV from a 50% duty cycle clock source. All loading with an external R_L = 50 Ω to V_{CC}. Input edge rates 40 ps (20% – 80%).
12. Skew is measured between outputs under identical transitions and conditions @ 0.5 GHz. Duty cycle skew is measured between differential outputs using the deviations of the sum of Tpw− and Tpw+ @ 0.5 GHz.
13. Additive RMS jitter with 50% duty cycle clock signal.
14. Additive peak−to−peak data dependent jitter with input NRZ data at PRBS23.
15. Input and output voltage swings are single−ended measurements operating in a differential mode.

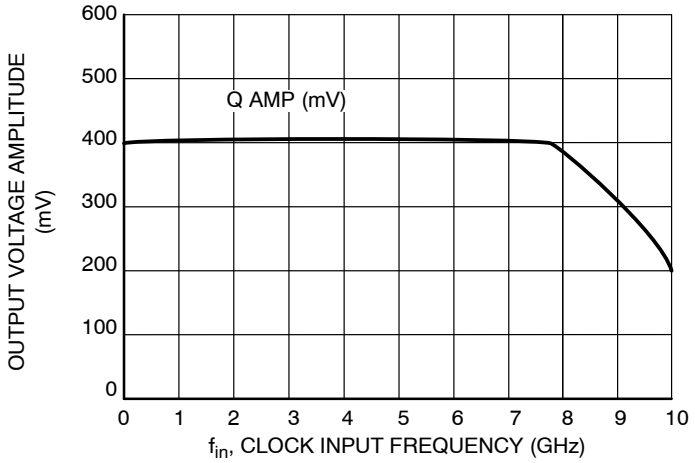


Figure 3. CLOCK Output Voltage Amplitude (V_{OUTPP}) vs. Input Frequency (f_{in}) at Ambient Temperature (Typical)

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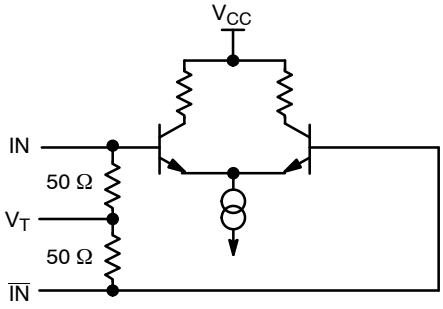


Figure 4. Input Structure

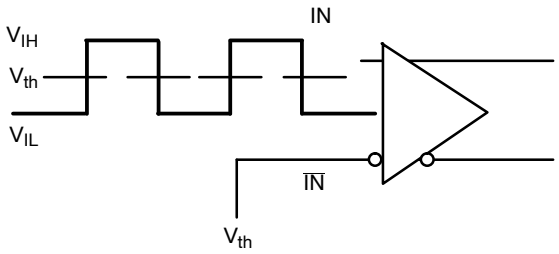


Figure 5. Differential Input Driven Single−Ended

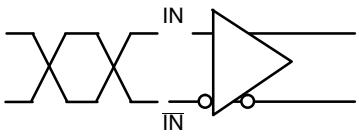


Figure 6. Differential Inputs Driven Differentially

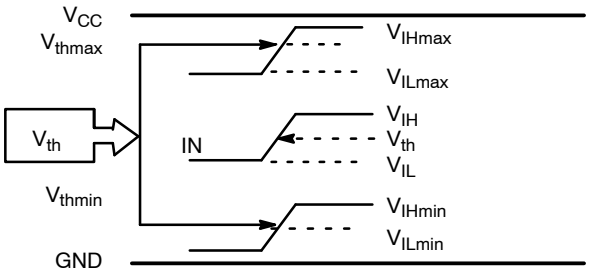


Figure 7. V_{th} Diagram

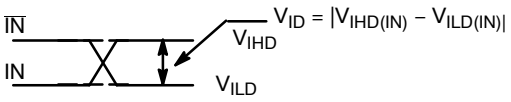


Figure 8. Differential Inputs Driven Differentially

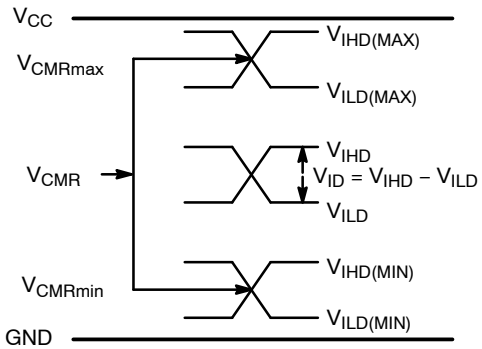


Figure 9. V_{CMR} Diagram

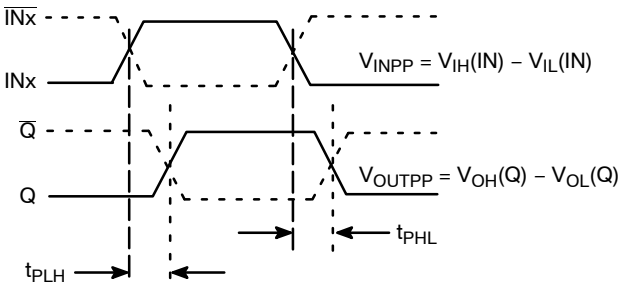


Figure 10. AC Reference Measurement

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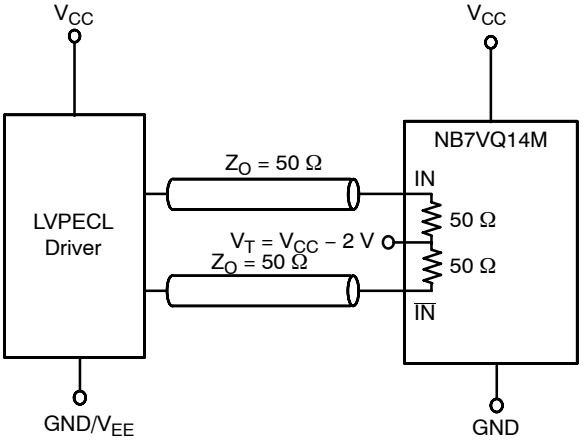


Figure 11. LVPECL Interface

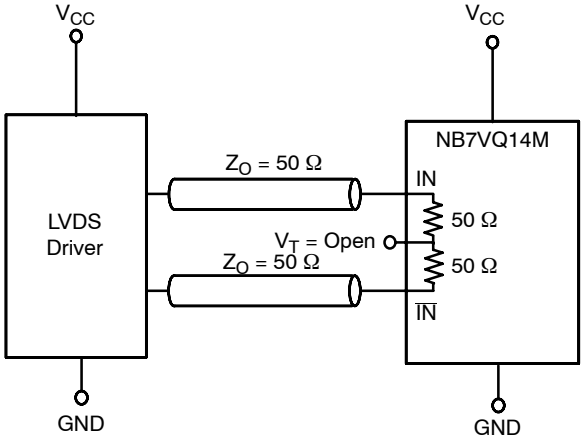


Figure 12. LVDS Interface

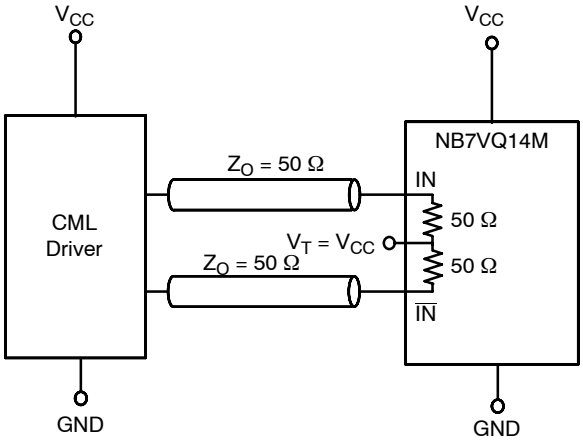


Figure 13. Standard 50 Ω Load CML Interface

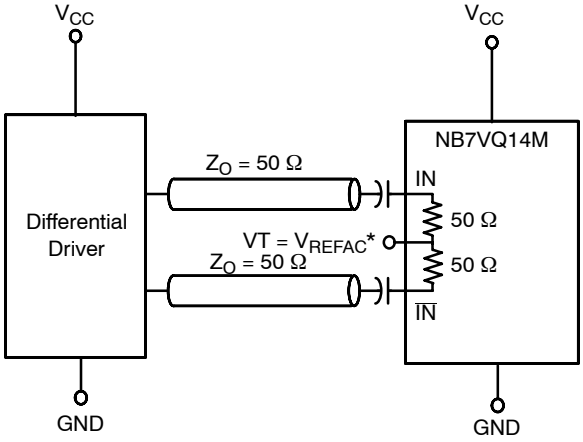


Figure 14. Capacitor−Coupled Differential Interface (V_T Connected to V_{REFAC})

*V_{REFAC} bypassed to ground with a 0.01 μF capacitor

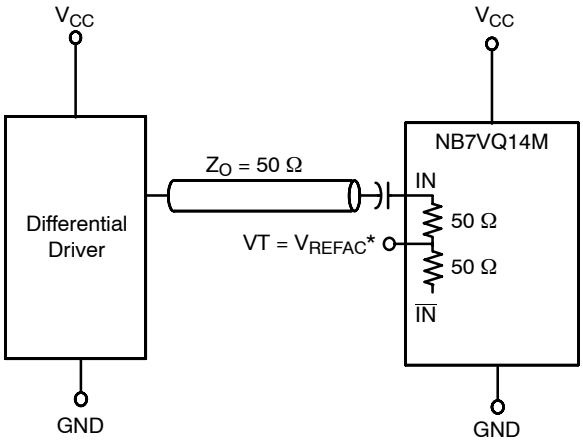


Figure 15. Capacitor−Coupled Single−Ended Interface (V_T Connected to V_{REFAC})

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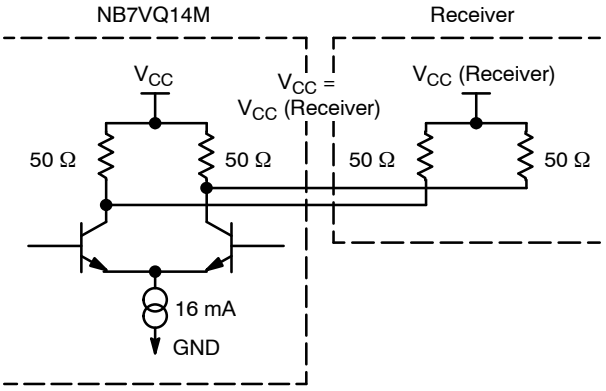


Figure 16. Typical CML Output Structure and Termination

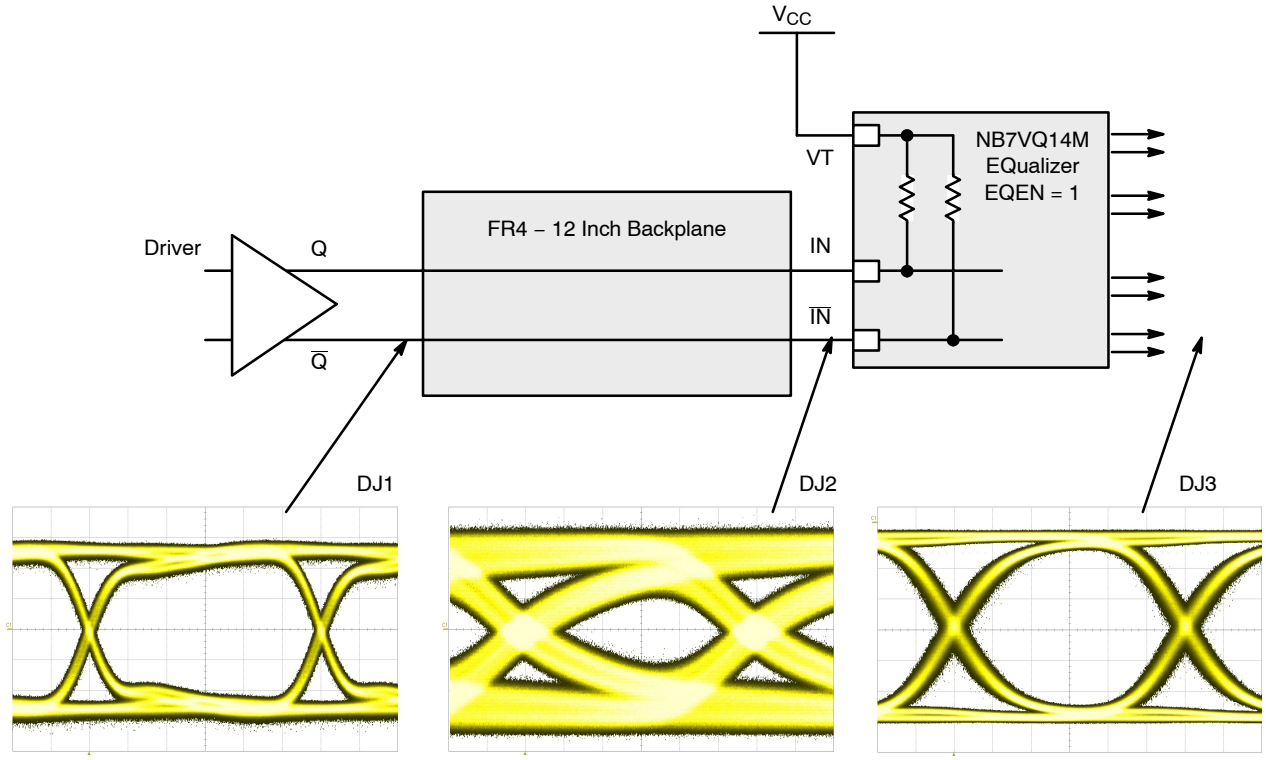


Figure 17. Typical NB7VQ14M Equalizer Application and Interconnect with PRBS23 pattern at 6.5 Gbps, EQEN = 1

ORDERING INFORMATION

Device	Package	Shipping†
NB7VQ14MMNG	QFN−16 (Pb−Free)	123 Units / Tube
NB7VQ14MMNHTBG	QFN−16 (Pb−Free)	100 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

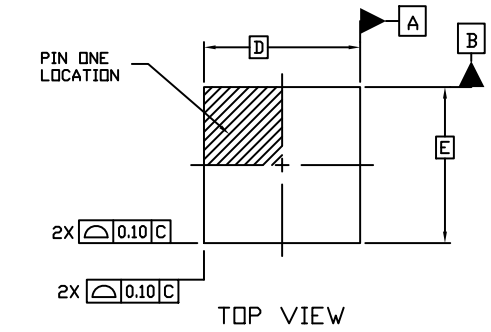
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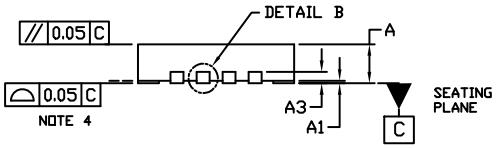
QFN16 3x3, 0.5P
CASE 485G
ISSUE G

DATE 08 OCT 2021

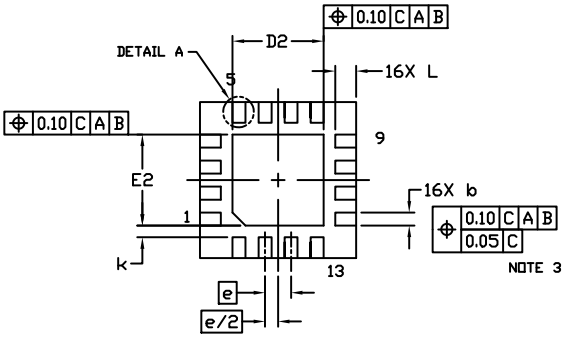
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SCALE 2:1



TOP VIEW

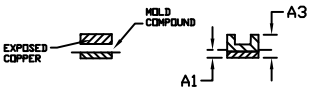


SIDE VIEW

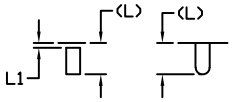


BOTTOM VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.



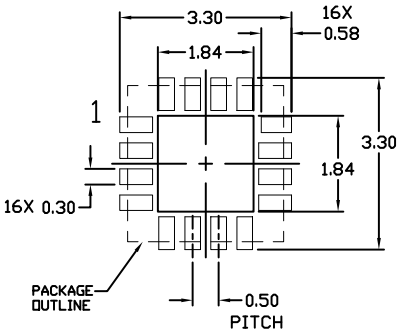
DETAIL B
ALTERNATE CONSTRUCTIONS



DETAIL A
ALTERNATE TERMINAL CONSTRUCTIONS

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.80	0.90	1.00
A1	0.00	0.03	0.05
A3		0.20 REF	
b	0.18	0.24	0.30
D		3.00 BSC	
D2	1.65	1.75	1.85
E		3.00 BSC	
E2	1.65	1.75	1.85
e		0.50 BSC	
k		0.18 TYP	
L	0.30	0.40	0.50
L1	0.00	0.08	0.15

MOUNTING FOOTPRINT



GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	**QFN16 3X3, 0.5P**		**PAGE 1 OF 1**

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