

MOSFETs Silicon N-channel MOS (U-MOSVIII-H)

TPW2900ENH

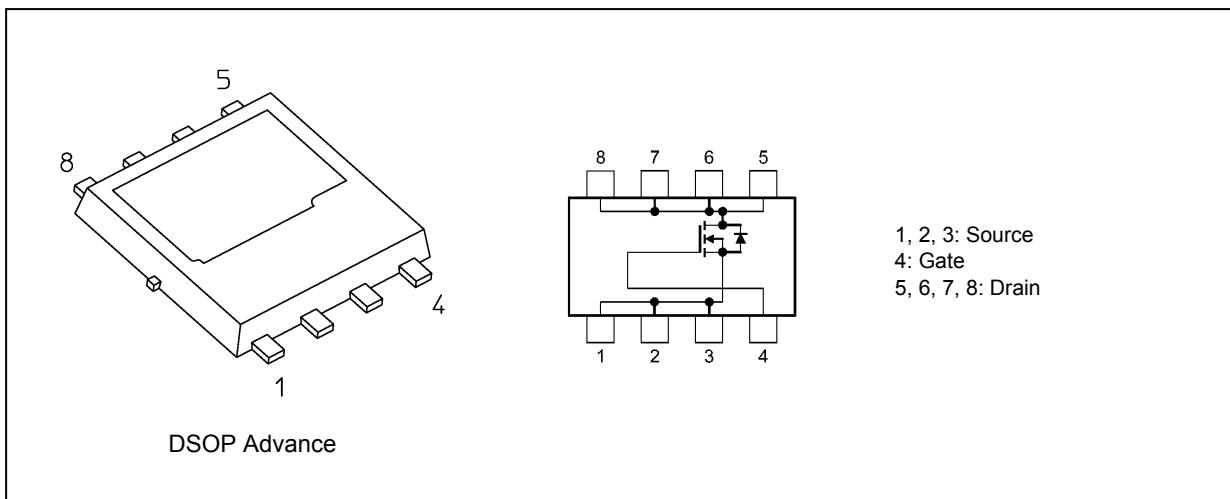
1. Applications

- High-Efficiency DC-DC Converters
- Switching Voltage Regulators

2. Features

- (1) High-speed switching
- (2) Small gate charge: $Q_{SW} = 8.2 \text{ nC}$ (typ.)
- (3) Low drain-source on-resistance: $R_{DS(ON)} = 24 \text{ m}\Omega$ (typ.) ($V_{GS} = 10 \text{ V}$)
- (4) Low leakage current: $I_{DSS} = 10 \mu\text{A}$ (max) ($V_{DS} = 200 \text{ V}$)
- (5) Enhancement mode: $V_{th} = 2.0$ to 4.0 V ($V_{DS} = 10 \text{ V}$, $I_D = 1.0 \text{ mA}$)

3. Packaging and Internal Circuit



Start of commercial production
2015-08

4. Absolute Maximum Ratings (Note) ($T_a = 25^\circ\text{C}$ unless otherwise specified)

Characteristics	Symbol	Rating	Unit
Drain-source voltage	V_{DSS}	200	V
Gate-source voltage	V_{GSS}	± 20	
Drain current (DC) ($T_c = 25^\circ\text{C}$) (Bottom drain)	I_D	33	A
Drain current (DC) (Silicon limit)	I_D	36	
Drain current (pulsed) ($t = 100\ \mu\text{s}$)	I_{DP}	150	
Power dissipation ($T_c = 25^\circ\text{C}$) (Bottom drain)	P_D	142	W
Power dissipation	P_D	2.5	
Power dissipation	P_D	0.8	
Single-pulse avalanche energy	E_{AS}	176	mJ
Single-pulse avalanche current	I_{AS}	33	A
Channel temperature	T_{ch}	150	$^\circ\text{C}$
Storage temperature	T_{stg}	-55 to 150	$^\circ\text{C}$

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc.).

5. Thermal Characteristics

Characteristics	Symbol	Max	Unit
Channel-to-case thermal resistance (Bottom drain) ($T_c = 25^\circ\text{C}$)	$R_{th(ch-c)}$	0.88	$^\circ\text{C/W}$
Channel-to-case thermal resistance (Top source) ($T_c = 25^\circ\text{C}$)	$R_{th(ch-c)}$	0.93	$^\circ\text{C/W}$
Channel-to-ambient thermal resistance ($T_a = 25^\circ\text{C}$)	$R_{th(ch-a)}$	50	$^\circ\text{C/W}$
Channel-to-ambient thermal resistance ($T_a = 25^\circ\text{C}$)	$R_{th(ch-a)}$	156	$^\circ\text{C/W}$

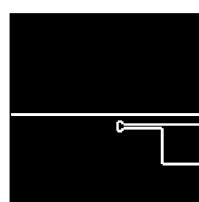
Note 1: Ensure that the channel temperature does not exceed 150 $^\circ\text{C}$.

Note 2: Limited by silicon chip capability.

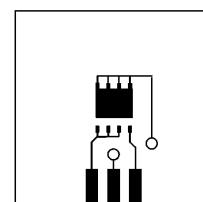
Note 3: Device mounted on a glass-epoxy board (a), Figure 5.1

Note 4: Device mounted on a glass-epoxy board (b), Figure 5.2

Note 5: $V_{DD} = 60\text{ V}$, $T_{ch} = 25^\circ\text{C}$ (initial), $L = 250\ \mu\text{H}$, $I_{AS} = 33\text{ A}$



FR-4
25.4 \times 25.4 \times 1.6
(Unit: mm)
2 oz copper



FR-4
25.4 \times 25.4 \times 1.6
(Unit: mm)
2 oz copper

Fig. 5.1 Device Mounted on a Glass-Epoxy Board (a)

Fig. 5.2 Device Mounted on a Glass-Epoxy Board (b)

Note: This transistor is sensitive to electrostatic discharge and should be handled with care.

6. Electrical Characteristics

6.1. Static Characteristics ($T_a = 25^\circ\text{C}$ unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current	I_{GSS}	$V_{GS} = \pm 20\text{ V}$, $V_{DS} = 0\text{ V}$	—	—	± 0.1	μA
Drain cut-off current	I_{DSS}	$V_{DS} = 200\text{ V}$, $V_{GS} = 0\text{ V}$	—	—	10	
Drain-source breakdown voltage	$V_{(BR)DSS}$	$I_D = 10\text{ mA}$, $V_{GS} = 0\text{ V}$	200	—	—	
	$V_{(BR)DSX}$	$I_D = 10\text{ mA}$, $V_{GS} = -20\text{ V}$	140	—	—	
Gate threshold voltage	V_{th}	$V_{DS} = 10\text{ V}$, $I_D = 1.0\text{ mA}$	2.0	—	4.0	
Drain-source on-resistance	$R_{DS(ON)}$	$V_{GS} = 10\text{ V}$, $I_D = 16.5\text{ A}$	—	24	29	$\text{m}\Omega$

6.2. Dynamic Characteristics ($T_a = 25^\circ\text{C}$ unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Input capacitance	C_{iss}	$V_{DS} = 100\text{ V}$, $V_{GS} = 0\text{ V}$, $f = 1\text{ MHz}$	—	1700	2200	pF
Reverse transfer capacitance	C_{rss}		—	7.0	50	
Output capacitance	C_{oss}		—	180	—	
Gate resistance	r_g	—	—	4.0	6.0	Ω
Switching time (rise time)	t_r	See Fig. 6.2.1	—	8.0	—	ns
Switching time (turn-on time)	t_{on}		—	20	—	
Switching time (fall time)	t_f		—	12	—	
Switching time (turn-off time)	t_{off}		—	36	—	

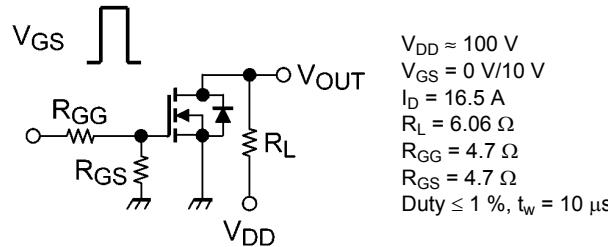


Fig. 6.2.1 Switching Time Test Circuit

6.3. Gate Charge Characteristics ($T_a = 25^\circ\text{C}$ unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Total gate charge (gate-source plus gate-drain)	Q_g	$V_{DD} \approx 100\text{ V}$, $V_{GS} = 10\text{ V}$, $I_D = 33\text{ A}$	—	22	—	nC
Gate-source charge 1	Q_{gs1}		—	9.0	—	
Gate-drain charge	Q_{gd}		—	4.4	—	
Gate switch charge	Q_{SW}		—	8.2	—	

6.4. Source-Drain Characteristics ($T_a = 25^\circ\text{C}$ unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Reverse drain current (pulsed) (Note 6)	I_{DRP}	—	—	—	150	A
Diode forward voltage	V_{DSF}	$I_{DR} = 33\text{ A}$, $V_{GS} = 0\text{ V}$	—	—	-1.2	V
Reverse recovery time	t_{rr}	$V_{DD} = 100\text{ V}$, $I_{DR} = 8.3\text{ A}$, $V_{GS} = 0\text{ V}$, $-\text{d}I_{DR}/\text{d}t = 100\text{ A}/\mu\text{s}$	—	93	—	ns
Reverse recovery charge	Q_{rr}	—	—	300	—	nC

Note 6: Ensure that the channel temperature does not exceed 150 °C.

7. Marking

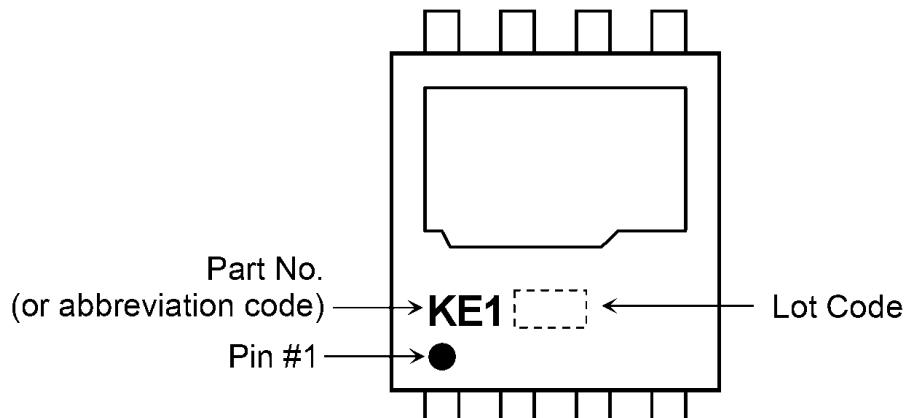
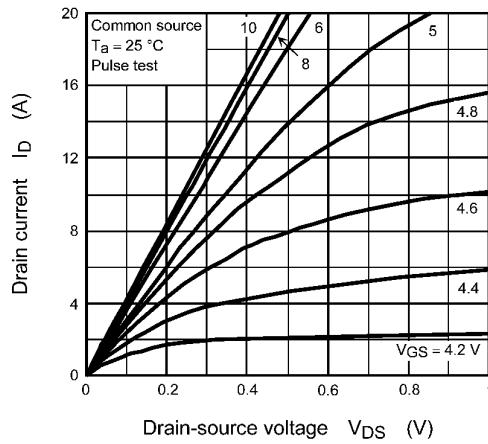
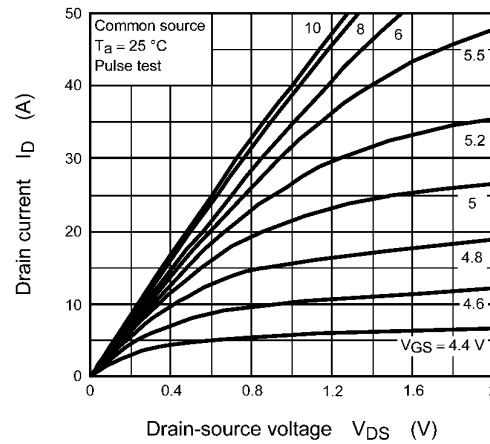
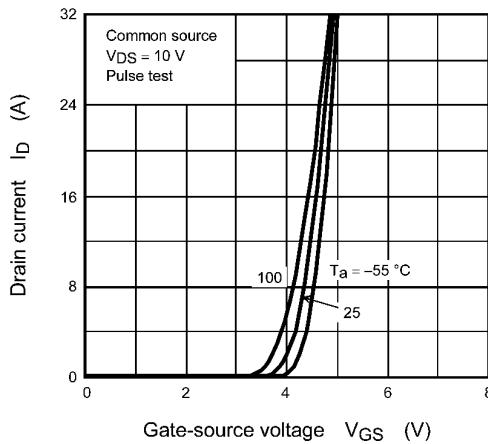
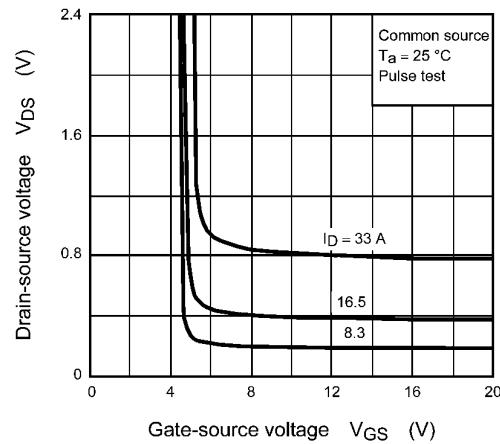
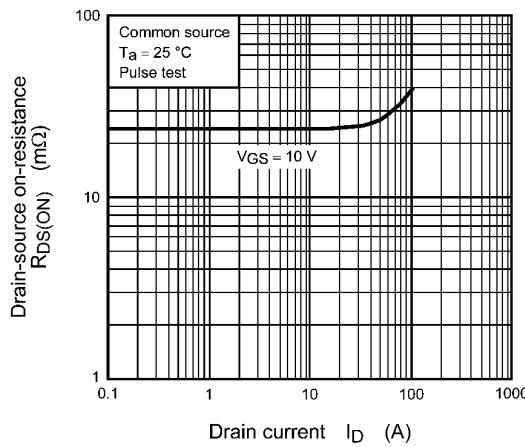
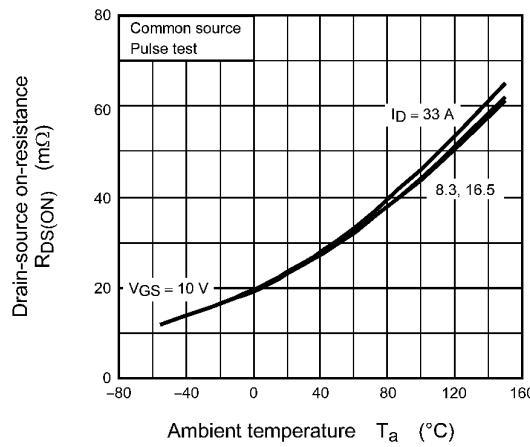


Fig. 7.1 Marking

8. Characteristics Curves (Note)

Fig. 8.1 I_D - V_{DS} Fig. 8.2 I_D - V_{DS} Fig. 8.3 I_D - V_{GS} Fig. 8.4 V_{DS} - V_{GS} Fig. 8.5 $R_{DS(ON)}$ - I_D Fig. 8.6 $R_{DS(ON)}$ - T_a

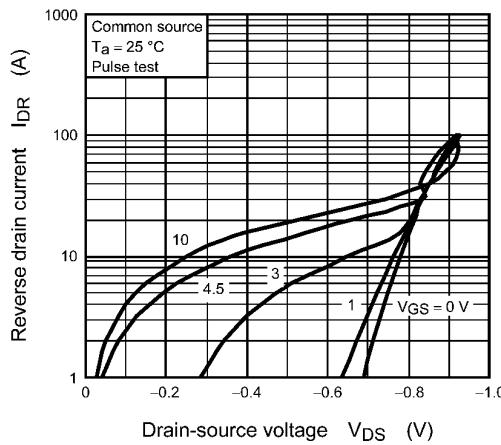


Fig. 8.7 IDR - V_{DS}

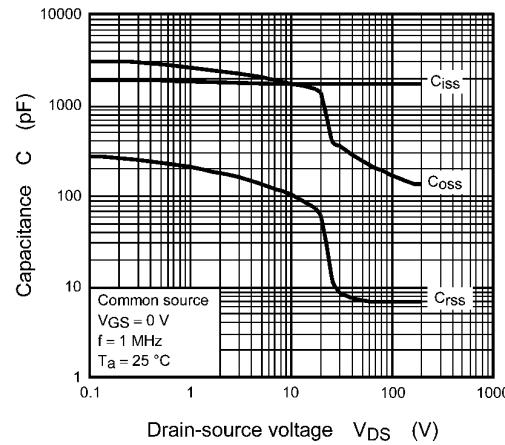


Fig. 8.8 Capacitance - V_{DS}

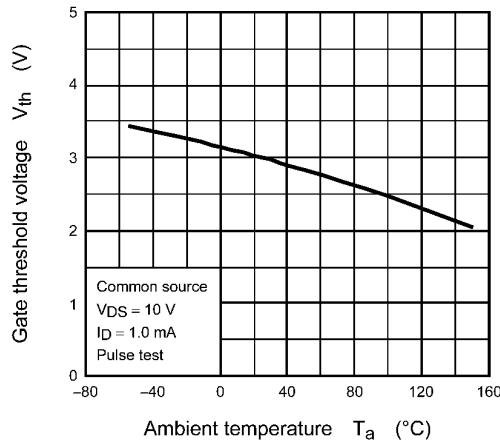


Fig. 8.9 V_{th} - T_a

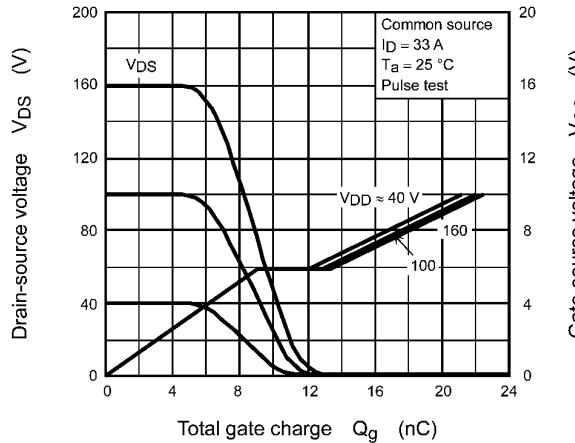


Fig. 8.10 Dynamic Input/Output Characteristics

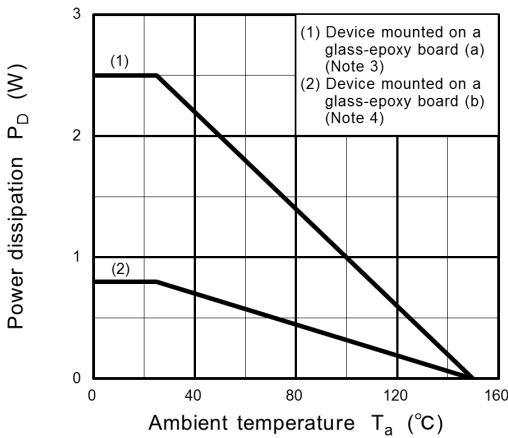


Fig. 8.11 P_D - T_a
(Guaranteed Maximum)

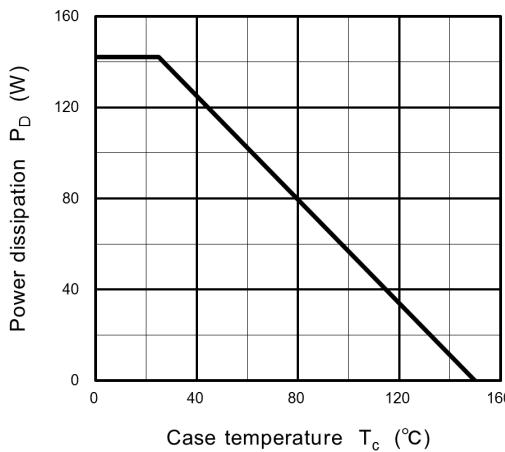
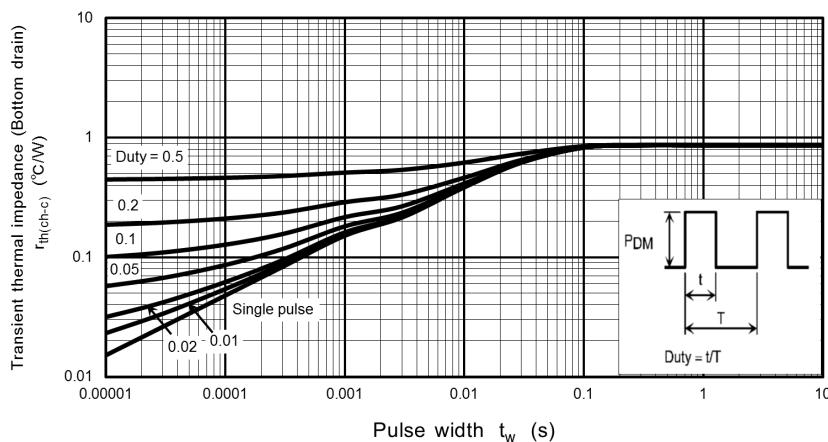
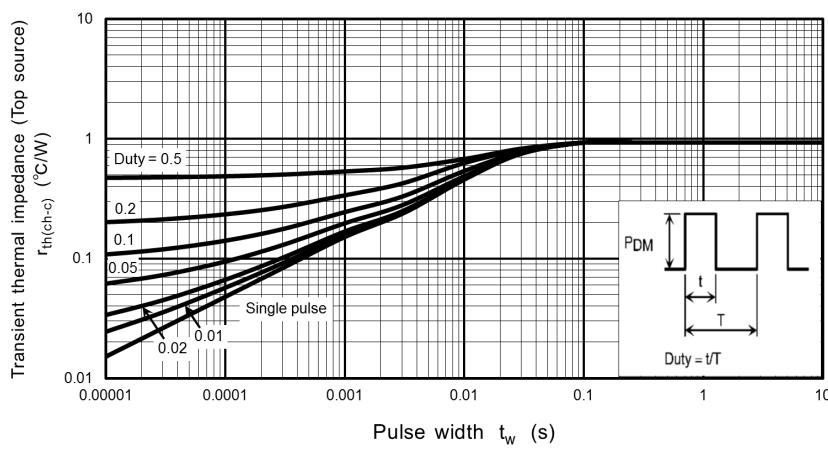


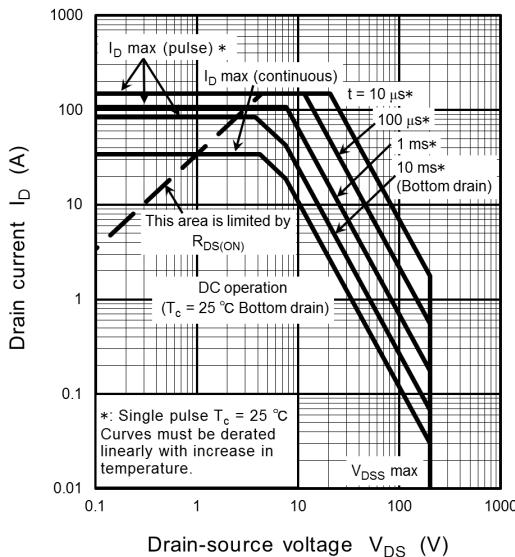
Fig. 8.12 P_D - T_c (Bottom drain)
(Guaranteed Maximum)



**Fig. 8.13 $r_{th} - t_w$ (Bottom drain)
(Guaranteed Maximum)**



**Fig. 8.14 $r_{th} - t_w$ (Top source)
(Guaranteed Maximum)**

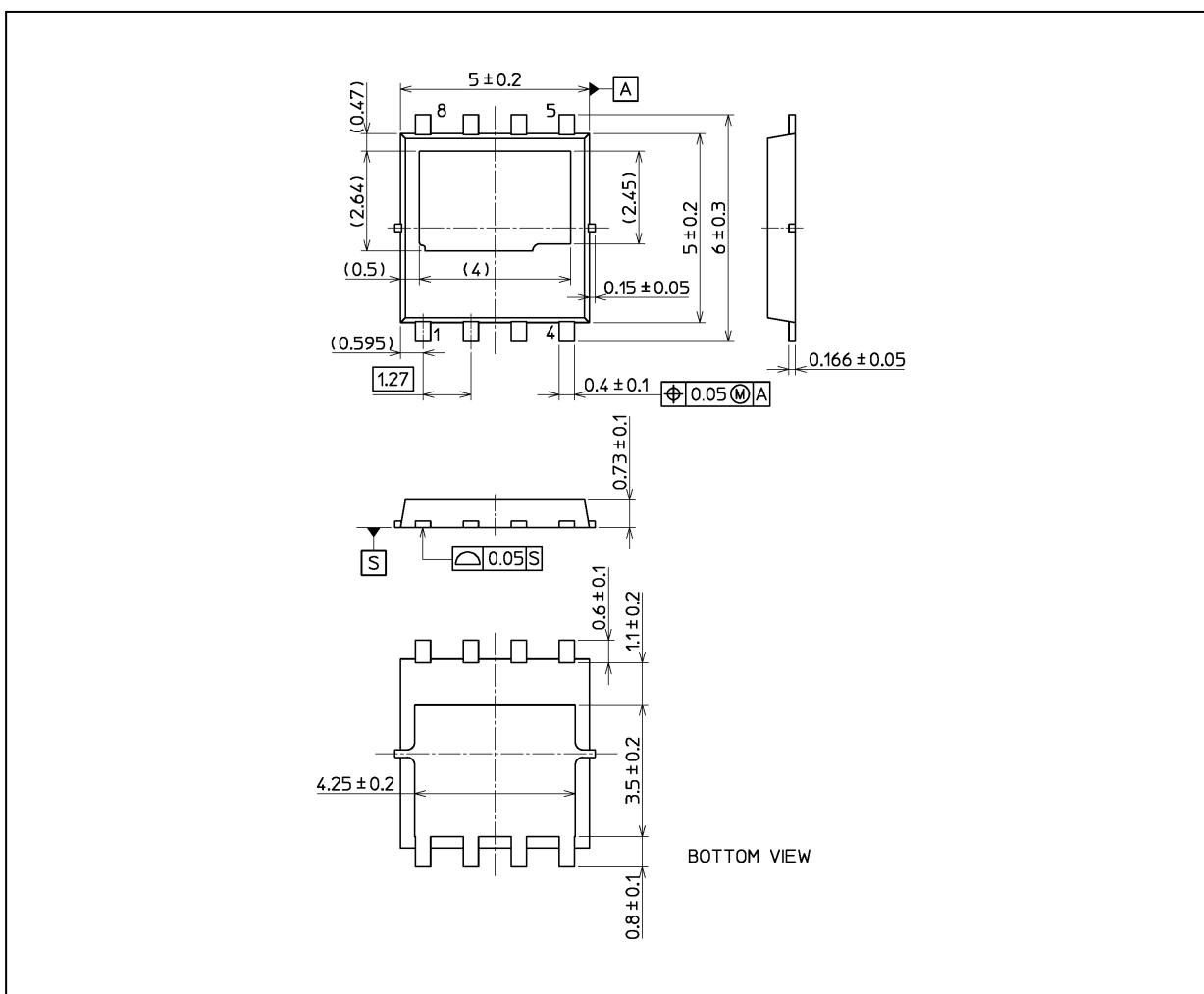


**Fig. 8.15 Safe Operating Area
(Guaranteed Maximum)**

Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

Package Dimensions

Unit: mm



Weight: 0.104 g (typ.)

Package Name(s)
TOSHIBA: 2-5S1A
Nickname: DSOP Advance

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