# XDPL8221 Digital PFC+Flyback Controller IC

## XDP™ Digital Power

**Design Guide**

**Revision 1.1**

## About this document

### Scope and purpose

This document is a step-by-step guide for designing high-performance dual-stage digital PFC+Flyback AC-DC converter using the XDPL8221 controller for LED lighting applications. The document also describes parameter handling for Infineon typical use cases using the Infineon .dp Vision tool for the Infineon XDPL8221.

### Intended audience

This document is intended for anyone wishing to design high-performance dual-stage digital PFC+Flyback AC/DC-DC converter for LED lighting based on the digital controller XDPL8221.

## Table of contents

# 1 Introduction

The digital controller IC XDPL8221 belongs to the Infineon XDP™ digital power family. It provides an independent PFC boost and Flyback dual stage control to achieve an output which combines a constant voltage (CV), constant current (CC) and limited Power (LP) for LED luminaires. The IC is available in a PG-DSO-16 package and supports many features with only a minimum requirement of external components. The digital engine of the IC offers the possibility to configure operational parameters and protection modes. This eases the design phase and allows a high product variety with a reduced number of hardware variants. Accurate primary side output voltage and current control eliminates a secondary side feedback loop.

This design guide provides detailed information how to calculate the major power stage component values, as well as the setting of parameters for general functions and protection features. Useful tips on PCB layout are included to help the developers to optimize their PCB design. Finally, the installation and usage of a Graphical User Interface – .dp Vision is described to guide the customer to set parameters for the digital IC. The numeric values below are shown for the 100W reference board with universal input voltage.

## 1.1 Product highlights

- UART Command Interface enables real-time communication for smart control applications.
- Flicker-free dimming by analog reduction of output driving current down to 1%
- Primary side regulated (PSR) constant voltage (CV), constant current (CC), limited power (LP) output.
- High current accuracy output of typical +/- 2% across universal AC/DC input voltage range (90 Vrms to 305 Vrms) with extended output voltage range from 16 VDC to 48 VDC.
- Multi-mode flyback stage control (QRM+DCM+ABM) ensures high power efficiency over the entire load range and low dimming output down to 1% of the full current.
- High power factor (PF >0.9) and low input current total harmonic distortion (iTHD < 15%) for AC and DC input up to 300 V (RMS) and load down to 30%.
- Integrated 600 V startup cell ensures fast time to light and low power consumption.
- Adapted external temperature protection.

## 1.2 Design features

- Universal AC input (120 V to 277 VAC +/- 10%) or DC input (120 V to 430 VDC +/-10%)
- Extended output voltage range from 16 V to 48 VDC
- Recommended power range from 25 W to 150 W

## 1.3 Target applications

- Driver for LED luminaires

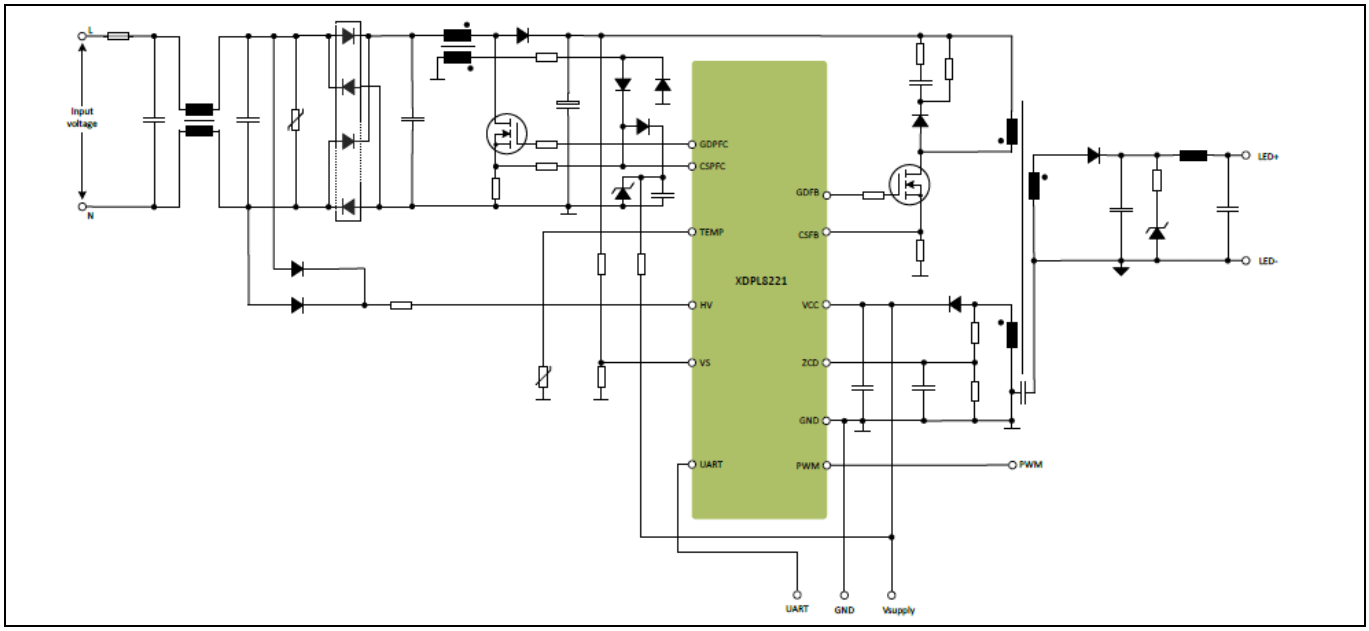



**Figure 1 XDPL8221 Typical application schematic**

## 1.4 Pin configuration and description

Pin assignments and basic pin description information are shown below.

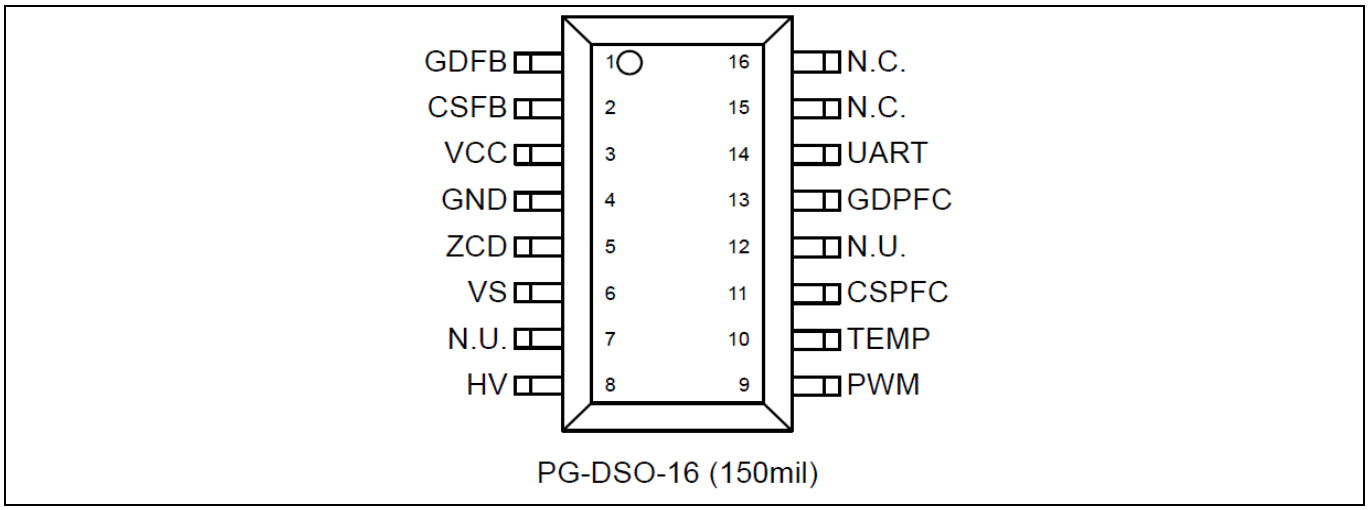



**Figure 2 Pinning of XDPL8221**

**Table 1 Pin definitions and functions**

| Name | Pin | Type | Function |
|---|---|---|---|
| GDFB | 1 | O | **Flyback Gate Drive Output**<br>Output for directly driving a power MOSFET of the Flyback converter via a resistor. |
| CSFB | 2 | I | **Flyback Current Sense Input**<br>Connected to an external shunt resistor and the source of a power MOSFET of the Flyback converter. |
| VCC | 3 | I | **Positive Power Supply** |

| | | | |
|---|---|---|---|
| | | | IC power supply |
| GND | 4 | - | **Ground**<br>IC Ground |
| ZCD | 5 | I | **Flyback Zero-crossing Detection**<br>Connected to the Flyback auxiliary winding via a resistive divider for zero-crossing detection as well as primary side output voltage sensing for output regulation and backup bus voltage sensing for safety. |
| VS | 6 | I | **PFC Voltage Sense**<br>Connected to DC bus via a resistive divider for the PFC boost converter output voltage sensing. |
| N.U. | 7 | - | **Not Used, to be connected to GND externally** |
| HV | 8 | I | **High Voltage Input**<br>Connected to the AC mains via external rectifier diode and resistor. An internal 600V HV startup-cell is used to charge VCC initially. In addition, sampled high-voltage sensing is also used for AC/DC detection and brown-out. |
| PWM | 9 | I | **PWM Dimming**<br>The PWM pin is used as a dimming input. |
| TEMP | 10 | I | **External Temperature Sensor**<br>Connected to an external NTC resistor to sense the environment temperature. |
| CSPFC | 11 | I | **PFC Current Sensing**<br>Connected to an external shunt resistor and the source of a power MOSFET of the PFC boost converter. Additionally, it is connected to the PFC aux winding for zero-crossing detection. |
| N.U. | 12 | I/O | **Not Used, to be connected to GND externally** |
| GDPFC | 13 | O | **PFC Gate Drive Output**<br>Output for directly driving a power MOSFET of the PFC boost converter via a resistor. |
| UART | 14 | - | **Universal Asynchronous Receiver Transmitter (UART) Communication**<br>The UART pin is used for the UART interface to support parameterization. |
| N.C. | 15 | - | **Not Connected. Externally to be connected to GND.** |
| N.C. | 16 | - | **Not Connected. Externally to be connected to GND.** |

# 2 Hardware design

The hardware design part provides detailed calculation of power component values as well as the setting of parameters of general functions and protection features for both PFC boost and Flyback converters. Useful tips on PCB layout are included to help the customers optimize their PCB design.

The design example used in this hardware design part is a 100 W Constant Current mode driver reference design for direct driving of LED lighting applications. The customer can easily apply their own target specifications according this example and obtain the design parameters by themselves.

## 2.1 System specification of a 100 W driver for LED lighting applications

The system specification of a 100W driver reference design for LED lighting applications is given as following:

**Table 2**

| Parameter | Symbol | Target value | Unit |
|---|---|---|---|
| **Input characteristic** | | | |
| Nominal input AC voltage (RMS) | $V_{in\_AC}$ | 120 to 300 | $V_{AC}$ |
| Nominal input DC voltage | $V_{in\_DC}$ | 120 to 300 | $V_{DC}$ |
| Nominal output DC voltage | $V_{OUT}$ | 16 to 48 | $V_{DC}$ |
| Nominal output DC current | $I_{OUT}$ | 550 to 2500 | mA |
| Nominal output power | $P_O$ | 100 | W |
| Power Factor | PF | > 0.9 | |
| THD | iTHD | < 15 | % |
| Power Efficiency | η | < 89 | % |
| **PFC stage** | | | |
| PFC MOSFET Maximum drain-source voltage | $V_{DS\_PFC}$ | 600 | V |
| Maximum PFC stage output power | $P_{O\_PFC}$ | 110 | W |
| Minimum PFC switching frequency | $f_{sw,min\_PFC}$ | 22 | kHz |
| Maximum PFC switching frequency | $f_{sw,max\_PFC}$ | 80 | kHz |
| **Flyback stage** | | | |
| Nominal Input voltage | $V_{DC}$ | 460 | $V_{DC}$ |
| Maximum output power | $P_O$ | 100 | W |
| Nominal output overvoltage threshold | $V_{OUT,OV}$ | 53 | V |
| Flyback MOSFET maximum drain-source voltage | $V_{DS\_FB}$ | 800 | V |
| Minimum switching frequency | $f_{sw,min}$ | 16 | kHz |

## 2.2 Schematic

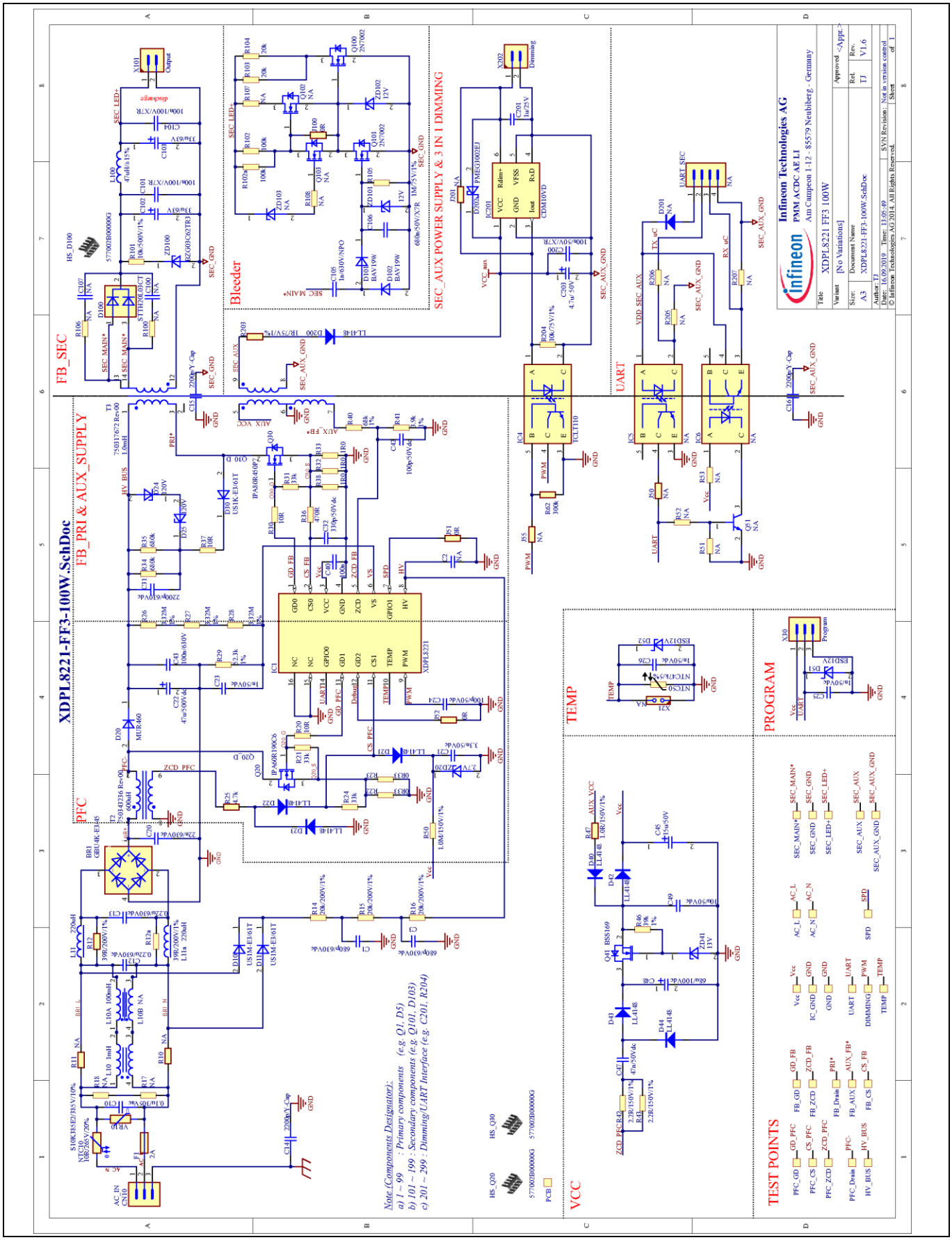



**Figure 3 XDPL8221 100 W driver schematic**

## 2.3 Bridge rectifier

The bridge rectifier usually has the highest semiconductor power loss in the PFC boost converter. Using a higher rated current bridge rectifier can reduce the forward voltage drop, which reduces the total power dissipation at a small incremental cost. The total power loss is calculated using the average input current flowing through two of the bridge rectifying diodes if the forward voltage is assumed as 1 V:

$$P_{loss\_BR} = I_{BR\_avg} * 2 * V_{F\_BR} = \frac{2\sqrt{2}}{\pi} * \frac{P_{O\_PFC\_max}}{V_{in\_rms\_min} * \eta_{PFC}} * 2 * V_{F\_BR} = 2.71\text{W}$$

With the value of power loss, an appropriate bridge rectifier based on its thermal characteristics should be selected.

## 2.4 Design PFC boost converter

Power Factor Correction (PFC) shapes the input current of the power supply to be in synchronization with the mains voltage, in order to maximize the real power drawn from the mains. In a perfect PFC circuit, the input current follows the input voltage as a pure resistor, without any input current harmonics. In the 100 W driver reference design, PFC is implemented as a boost converter which works in the Quasi-Resonant Mode (QRM) with constant on-time control. The converter provides the following flyback stage a constant high DC voltage as input which ensures flicker-free light output. This chapter describes the methodology for designing the QRM PFC Boost converter based on XDPL8221; including PFC boost inductor design, equations for power losses estimation, selection guide for power semiconductor devices and passive components.

### 2.4.1 Main PFC boost inductor

As the key magnetic component of the PFC boost converter, the boost inductor has the main function of energy storage. Its inductance is given as the following formula:

$$L_{PFC} = \frac{V_{in\_pk}^2 * (V_{bus} - V_{in\_pk}) * \eta_{PFC}}{4 * V_{bus} * P_{O\_PFC} * f_{PFC}}$$

Where

- $L_{PFC}$ -- Inductance of the PFC boost inductor
- $V_{in\_pk}$ -- Peak value of the input AC mains
- $V_{bus}$ -- Bus voltage as the PFC output
- $\eta_{PFC}$ -- Estimated power efficiency of the PFC boost converter
- $P_{O\_PFC}$ -- Output Power of the PFC boost converter
- $f_{PFC}$ -- Operation switching frequency of the PFC boost inductor

In the 100 W driver reference design, the output of the PFC boost converter is chosen as 460 V so that a high power factor is still guaranteed at the maximum AC/DC input. The minimum switching frequency limited at 22 kHz to avoid audible noise is controlled by XPDL8221 through “maximum switching period time-out” approach, which starts the next switching cycle when 45 µs of maximum switching period is reached. The detailed variables values are given in the following table:

**Table 3 PFC design specification**

| Parameter | Symbol | Value | Unit |
|---|---|---|---|
| AC/DC input under voltage threshold | $V_{UV\_rms}$ | 76 | V |
| AC/DC input overvoltage threshold | $V_{OV\_rms}$ | 320 | V |
| Maximum PFC boost converter output power | $P_{O\_PFC\_max}$ | 110 | W |
| Maximum PFC On time | $t_{on,max\_PFC}$ | 32 | µs |
| Minimum PFC On time | $t_{on,min\_PFC}$ | 200 | ns |
| Minimum switching frequency | $f_{sw,min\_PFC}$ | 22 | kHz |
| Estimated PFC boost converter power efficiency @ maximum AC input voltage | $\eta_{PFC}$ | ≤ 96 | % |
| Nominal PFC boost converter output voltage | $V_{bus}$ | 460 | V |
| Power Factor | PF | > 0.9 | - |

The maximum possible inductance should be calculated at both lowest (input under voltage threshold) and highest possible input voltage (input overvoltage threshold) with full load and minimum switching frequency.

At 76 VAC input:

$$L_{PFC\_76} = \frac{\left(76 * \sqrt{2}\right)^2 * \left(460 - 76 * \sqrt{2}\right) * 0.96}{4 * 460 * 110 * 22 * 10^3} \approx 0.88\ mH$$

At 320 VAC input:

$$L_{PFC\_320} = \frac{\left(320 * \sqrt{2}\right)^2 * \left(460 - 320 * \sqrt{2}\right) * 0.96}{4 * 460 * 110 * 22 * 10^3} \approx 1.15\ mH$$

The suitable inductance must be less than the smaller one of both.

$$L_{PFC} < min\left(L_{PFC_{76}}, L_{PFC_{320}}\right)$$

Other considerations regarding PFC choke inductance:

- The selected PFC inductance must be small enough to cover the maximum output power at the minimum input (e.g. to cover the brown-in/out feature).
- Bigger PFC inductance has the advantage at light load in comparison to smaller inductance due to longer on time. This ensures smaller minimum output power in DCM when the LED load is small (e.g. 1% dimming) and avoids unwanted bus voltage ripples due to the limited minimum on time of the IC controller.
- For the maximum output power, bigger PFC inductance has longer on time and lower switching frequency. It must be guaranteed that these two parameters are still within the limit of XDPL8221.
- Bigger PFC inductance leads to bigger choke size and more winding turns which cause more winding loss. In contrast, smaller inductance has smaller size and less winding turns but higher frequency which could lead to more switching loss.

In the reference design, $L_{PFC}$ =0.6 mH is chosen to avoid magnetic saturation in all worst cases like start-up and load transient. After the PFC choke inductance is fixed, the choke relevant parameters can be calculated as following with the assumption of the boundary concudtion mode operation:

Maximum input current (RMS) happens at minimum AC input and maximum output power:

$$I_{in\_rms\_max} = \frac{P_{O\_PFC\_max}}{V_{UV\_rms} * \eta_{PFC}} = 1.5\ A$$

Maximum input peak current:

$$I_{in\_pk\_max} = \sqrt{2} * I_{in\_rms\_max} = 2.12\ A$$

Maximum inductor peak current:

$$I_{L,pk\_PFC\_max} = 2 * I_{in\_pk\_max} = 4.24\ A$$

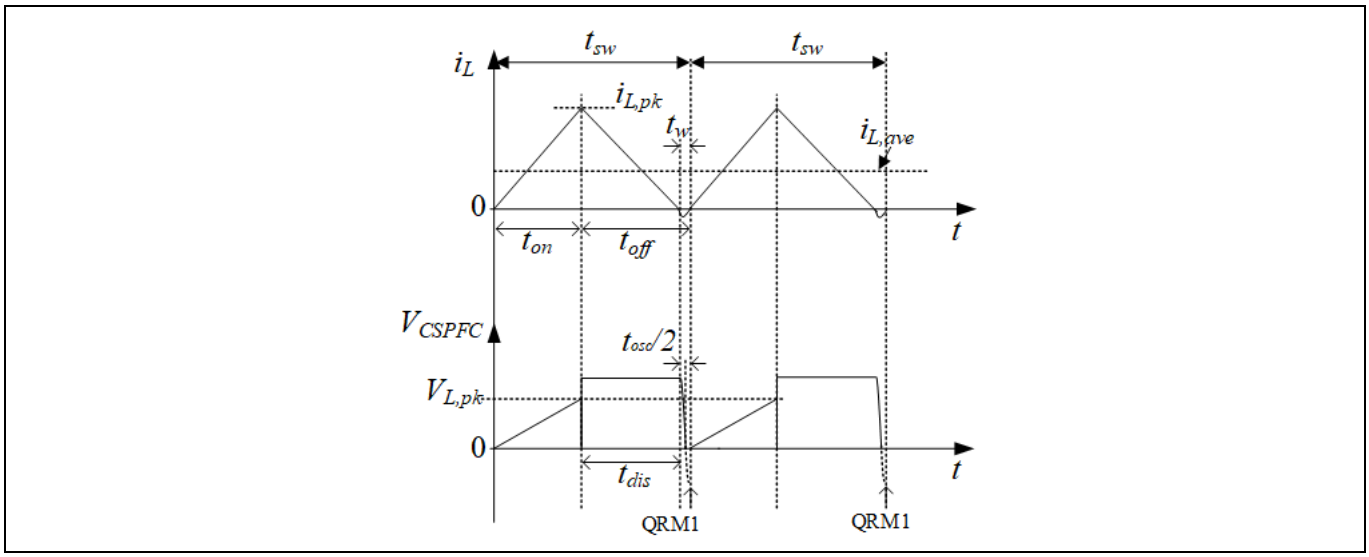



**Figure 4 Boost inductor current waveform in a switching cycle**

According to the **Figure 4** above, other important parameters of the PFC boost converter can be calculated as following if the QRM1 operation is assumed:

Maximum on-time:

$$t_{on\_max} = \frac{L_{PFC} * I_{L,pk\_PFC\_max}}{\sqrt{2} * V_{UV\_rms}} = 23\ \mu s$$

If $T_{osc}$ = 1.5 us is assumed, off time at minimum AC input and maximum output power:

$$t_{off} = \frac{L_{PFC} * I_{L,pk\_PFC\_max}}{V_{bus} - \sqrt{2} * V_{UV\_rms}} + 0.5 * T_{osc} = 7.97\ \mu s$$

the lowest frequency for maximum output power of PFC converter in QRM:

$$f_{PFC\_min} = \frac{1}{t_{on\_max} + t_{off}} = 32.3\ kHz$$

Maximum current (RMS) through the PFC inductor during on-time:

$$I_{L,PFC\_on\_rms\_max} = I_{L,pk\_PFC\_max} * \sqrt{\frac{1}{3} * t_{on\_max} * f_{PFC\_min}} = 2.11A$$

Maximum current (RMS) through the PFC inductor during off-time:

$$I_{L,PFC\_off\_rms\_max} = I_{L,pk\_PFC\_max} * \sqrt{\frac{1}{3} * t_{off} * f_{PFC\_min}} = 1.24A$$

Thus the maximum PFC inductor current (RMS):

$$I_{L\_rms\_max} = \sqrt{I^2_{L,PFC\_on\_rms\_max} + I^2_{L,PFC\_off\_rms\_max}} = 2.45\ A$$

To realize the zero crossing detection of the inductor current for the quasi-resistant mode switching, an additional auxiliary winding is introduced in the PFC inductor. It is recommended to keep the maximum voltage across the auxiliary winding below 50V which is proportional to the maximum voltage drop across the PFC inductor main winding. This must comply with the maximum voltage rating of the components which are connected to the auxiliary winding. In the 100 W reference design, a turns-ratio of 10:1 is used.

The important parameters of the PFC boost inductor are summarized in the following **Table 4**:

**Table 4 PFC boost inductor design parameters**

| PFC Boost converter | | | |
|---|---|---|---|
| **Parameter** | **Symbol** | **Value** | **Unit** |
| Main Inductance of the PFC boost inductor | $L_{PFC}$ | 600 | µH |
| Minimum switching frequency in QRM | $f_{PFC\_min}$ | 32.3 | kHz |
| Maximum inductor peak current | $I_{L,pk\_PFC\_max}$ | 4.24 | A |
| Maximum input current (RMS) | $I_{in\_rms\_max}$ | 1.5 | A |
| Maximum input peak current | $I_{in\_pk\_max}$ | 2.12 | A |
| Maximum inductor current (RMS) | $I_{L\_rms\_max}$ | 2.45 | A |
| Maximum on-time | $t_{on\_max}$ | 23 | µs |
| Turns-ratio of primary to auxiliary winding | $N_{p\_PFC}/N_{a\_PFC}$ | 10:1 | - |

Based on the calculated specifications above, the inductor can be constructed according to different design requirements like size, power efficiency and temperature etc. by selecting different bobbin and core. In order to avoid core saturation and achieve an optimized core loss, the flux density $B_{max}$ is recommended not to exceed 0.3.

In the Infineon 100 W driver reference design, the PFC boost inductor is constructed by the Würth Electronic under part no. **750343236** as a design example. The specification sheet is given as following in **Table 5**:

**Table 5 Parameters of Würth inductor 750343252**

| **Parameter** | **Value** | **Unit** |
|---|---|---|
| Inductance | 600 | µH |
| Bobbin | ETD34 | - |
| Core material | TP4A or DMR44 | - |
| Turns-ratio of primary to auxiliary winding | 10 : 1 | - |
| DC resistance primary winding | 0.13 | Ω |
| DC resistance auxiliary winding | 0.033 | Ω |
| Saturation current | 4.3 | A |

The maximum main inductor copper loss can be calculated based on the specification above as:

$$P_{loss\_L\_PFC} = I^2_{L\_rms\_max} * R_{DC\_L\_PFC} = 0.76\ \text{W}$$

## 2.4.2 PFC Boost diode

The selection of the boost diode is a major decision in the PFC boost converter design and it is related to the converter efficiency. Following considerations should be taken into account:

- Reverser break down voltage

It must be chosen higher than the bus voltage with at least 20% margin:

$$V_{RRM\_D\_PFC} < 1.2 * V_{bus\_OVP1} = 582\ V$$

A 600V diode is suitable here in the 100W reference design.

- Average rectified forward current

It must be higher than the maximum average PFC diode current calculated as following:

$$I_{D\_PFC\_avg\_max} = \frac{\sqrt{3}}{2} * I_{L,PFC\_off\_rms\_max} = 1.07\ A$$

Using a diode with high current capability will benefit the power efficiency.

- Forward voltage

It is directly related to the power efficiency. So the forward voltage should be chosen as small as possible.

- Reverse recovery time

As the PFC boost converter is controlled by XDPL8221 in the QRM+DCM mode, the PFC boost diode current goes back to zero while the PFC MOSFET turns on. So there is no current commutation between PFC diode and MOSFET and thus no switching loss by reverse recovery. It is not necessary to choose an ultra-fast diode.

- Power loss

The only power loss which should be considered is conduction loss. With a forward voltage of 0.5V assumed, the diode conduction loss can be calculated as following:

$$P_{loss\_D\_PFC} = I_{D\_PFC\_avg\_max} * V_{F\_D\_PFC} = 0.535\ \mathrm{W}$$

- Thermal characteristic

With the thermal resistance of the diode $R_{D\_PFC\_TH\_JA}$ and ambient temperature $T_A$, the PFC diode temperature without heat sink is calculated as:

$$T_{D\_PFC} = P_{loss\_D\_PFC} * R_{D\_PFC\_TH\_JA} + T_A$$

The important parameters for the boost diode which used in the 100 W driver reference design are summarized in the following **Table 6**:

**Table 6 Boost Diode Design Parameters**

| Parameter | Symbol | Value | Unit |
|---|---|---|---|
| Maximum reverse voltage | $V_{RRM\_D\_PFC}$ | 600 | V |
| Average rectified forward current | $I_{D\_PFC\_avg}$ | 4 | A |
| Maximum PFC diode RMS current | $I_{D\_PFC\_rms\_max}$ | 1.24 | A |
| Forward voltage | $V_{F\_D\_PFC}$ | 0.5 | V |

## 2.4.3 PFC Power MOSFET

The selection of the PFC power MOSFET is based mainly on the consideration of the break down voltage and power dissipation. According to the operating bus voltage, a 600 V MOSFET is suitable. In the QRM+DCM mode PFC boost converter, the overall MOSFET losses comprise:

- Conduction loss

These losses are frequency independent and do not scale significantly with frequency. It is calculated as following:

$$P_{con\_loss\_MOS\_PFC} = I_{L,PFC\_on\_rms\_max}{}^2 * R_{DS(ON)}$$

- Turn-on transition loss

As the converter works in the QRM+DCM mode, the turn-on transition loss caused by the magnetizing current can be ignored because the current rises from zero when a switching cycle starts. But to discharge the parasitic capacitors like $C_{oss}$ and $C_{can}$ through the MOSFET channel can cause significant turn-on transition loss. These losses occur every switching cycle and are thus frequency dependent.

- $E_{oss}$ and $^1/_2 \cdot C_{can} \cdot V^2$ loss

As mentioned above, the energy stored in $C_{can}$ and $C_{oss}$ at the time of turn-on must be dissipated in the MOSFET channel and current sense resistor during the turn-on transition. The energy stored in any capacitor is fundamentally a function of the square of the voltage across it, and thus the $E_{oss}$ and $½ \cdot C_{can} \cdot V^2$ losses can be very significant during high line conditions. These losses occur every switching cycle and are thus frequency dependent. To simplify the calculation, we assumed that the switching loss is approximately the half of the conduction loss:

$$P_{sw\_loss\_MOS\_PFC} = \frac{1}{2} * P_{con\_loss\_MOS\_PFC}$$

- Gate driver loss

These losses also scale linearly with frequency, but are generally a quite small contribution to the overall losses (at switching frequencies of below hundred kilohertz) and depend almost exclusively on the MOSFET $Q_g$ (total gate-charge). The gate-driver power is typically dissipated in the external gate resistor and gate-driver itself and thus does not need to be considered in the thermal calculation of MOSFET.

In the 100 W driver reference design, the 600V Infineon MOSFET IPA60R190C6 of C6 family is used. With the $R_{DS(ON)}$ of 190 mΩ, the total loss of the MOSFET is calculated as below:

$$P_{loss\_MOS\_PFC} = P_{sw\_loss\_MOS\_PFC} + P_{con\_loss\_MOS\_PFC} = 1.5 * P_{con\_loss\_MOS\_PFC} = 0.63\ W$$

The important parameters for PFC MOSFET are summarized in the following **Table 7**:

**Table 7 PFC MOSFET Design parameters**

| Parameter | Symbol | Value | Unit |
|---|---|---|---|
| Break down voltage | $V_{BR\_DSS\_PFC}$ | 650 | V |
| MOSFET on-resistance | $R_{DS(ON)}$ | 190 | mΩ |
| PFC MOSFET conduction loss | $P_{loss\_MOS\_PFC\_con}$ | 0.42 | W |
| PFC MOSFET switching loss | $P_{loss\_MOS\_PFC\_sw}$ | 0.21 | W |
| PFC MOSFET total loss | $P_{loss\_MOS\_PFC}$ | 0.63 | W |

## 2.4.4 PFC MOSFET Gate driver

The XDPL8221 PFC boost converter gate driver GDPFC offers following advanced features:

- Configurable charge current from 30 up to 118 mA for turn-on slope optimization with dpVision tool
- Configurable gate voltage from 4.5 to up to 15 V

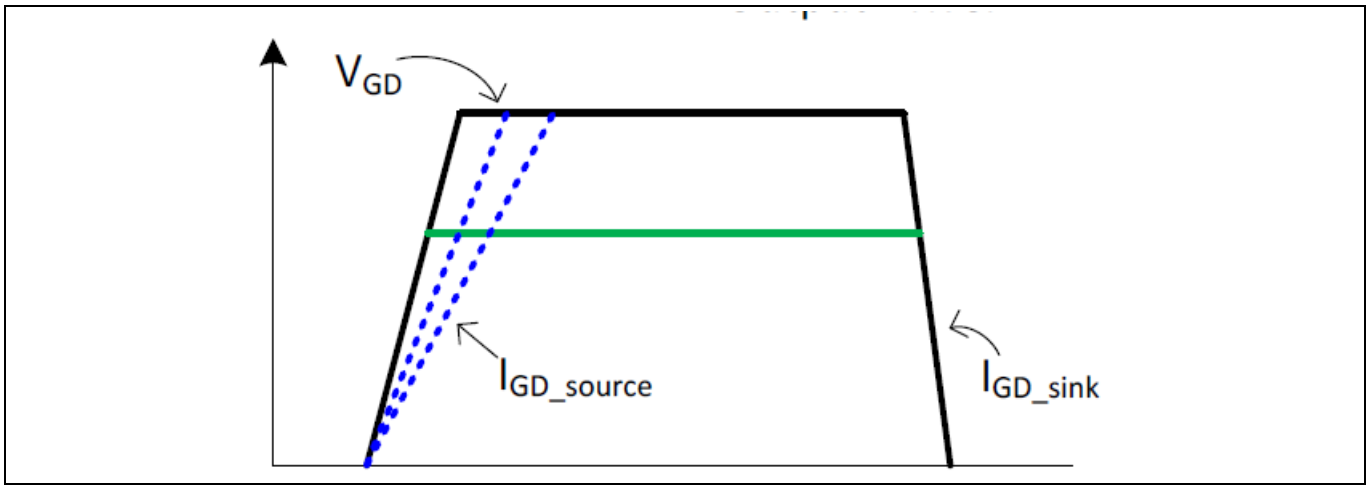



**Figure 5 Configurable gate driver with gate voltage and charge current**

Due to the configurable gate charge current and voltage, the external gate resistor should not be selected too high. A gate resistor of 10 Ω should fit for most application cases. The soft turn on for improved EMI result is guaranteed by the configurable constant current gate charging. Following table shows the recommend range of the external gate resistor for a stable gate drive operation of different MOSFET:

**Table 8 Recommended external gate resistor value**

| Parameter | Symbol | Value | | Unit |
|---|---|---|---|---|
| MOSFET Gate capacitance | $C_g$ | 1.0 to 2.0 | | nF |
| MOSFET gate source current | $I_{gs}$ | 100 | | mA |
| MOSFET gate source resistance | $R_{gs}$ | 10 | 100 | kΩ |
| Recommended external gate resistor | $R_g$ | 5 ~ 20 | 15 ~ 25 | Ω |

## 2.4.5 PFC Current sense and zero-crossing detection

The pin CSPFC of the XDPL8221 is used for two different purposes in one switching cycle. During the on time of the PFC MOSFET, it is used as current sense pin. The current sense of the PFC boost converter is used to limit the turn on time of the PFC MOSFET by sensing the peak current flowing through the MOSFET in order to protect it and also the boost inductor from the over-power situation. When the MOSFET is turned off, the pin is used as ZCD pin. The zero-crossing detection catches the moment when the boost inductor current goes back to zero and the next switching cycle can be started so that the boost converter always works in the QRM or DCM mode with minimum switching loss.

As the **Figure 6** shows below, when the PFC MOSFET turns on, the rectifier diode $D_1$ blocks the negative voltage drop across the PFC auxiliary winding so that the CSPFC pin is effectively connected only to the shunt resistor $R_{CS\_PFC}$ via the resistor $R_{ZCD2\_PFC}$ and thus only sees the peak current sense voltage signal. When the PFC MOSFET turns off, a positive voltage drop is forwarded by $D_1$. The CSPFC pin is connected effectively to a resistor divider $R_{ZCD1\_PFC}$ and $R_{ZCD2\_PFC}$. A zener diode and a capacitor are necessary to clamp the pin voltage not higher than 3.3 V. Another diode is required to decouple the current sensing signal from the clamping circuit.

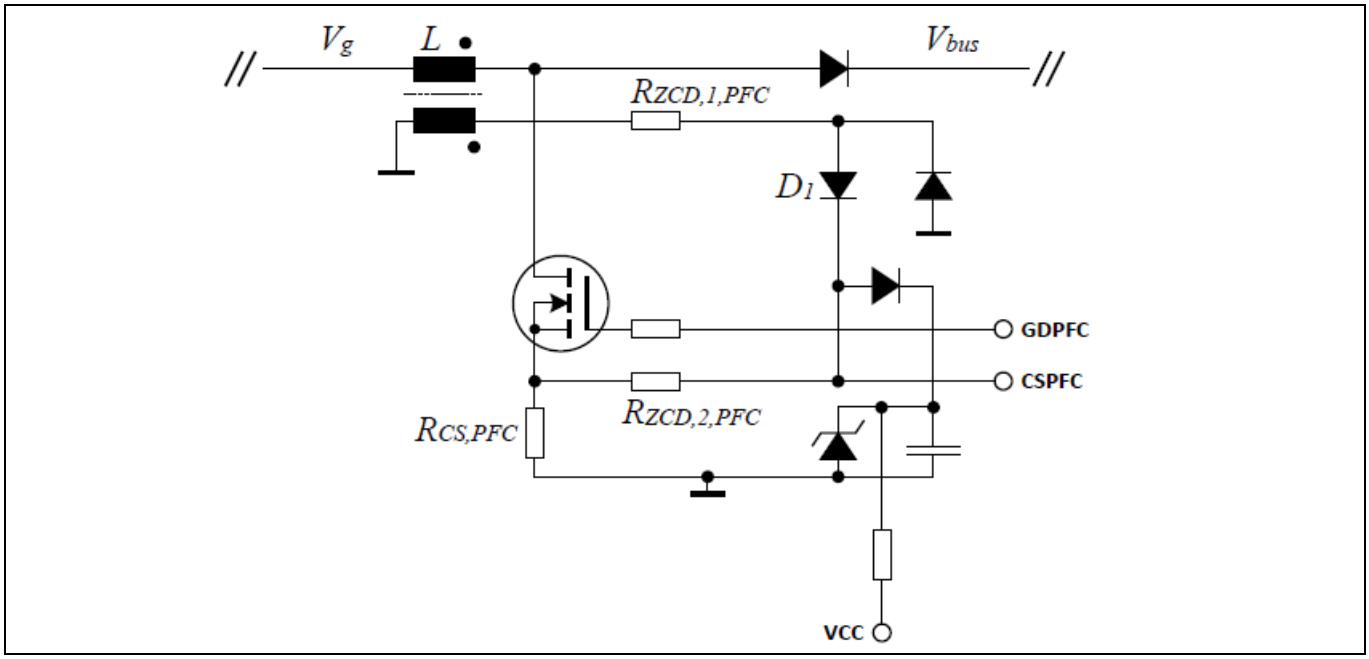



**Figure 6 Schematic of shared CS and ZCD functions at the CSPFC pin**

The ratio of the resistor divider $R_{ZCD1\_PFC}$ and $R_{ZCD2\_PFC}$ decides the amplitude of the oscillation at the CSPFC pin. So that the comparator for the zero crossing detection works correctly, the amplitude of the oscillation at the CSPFC pin must be higher than the 1.53 V as shown in the **Figure 7**. The ratio of the divider must be designed theoretically as following:

$$(V_{bus} - V_{in\_pk\_max}) * \frac{N_{a\_PFC}}{N_{p\_PFC}} * \frac{R_{ZCD2\_PFC}}{R_{ZCD1\_PFC} + R_{ZCD2\_PFC}} > 1.5 * 1.54\,V$$

***Attention:*** ***The bus voltage ripple and the parasitic resistance of the winding which leads to the damping of the amplitude should be also taken into account if necessary. Wrongly designed of the divider ratio will cause the losing of the PFC ZCD signal.***

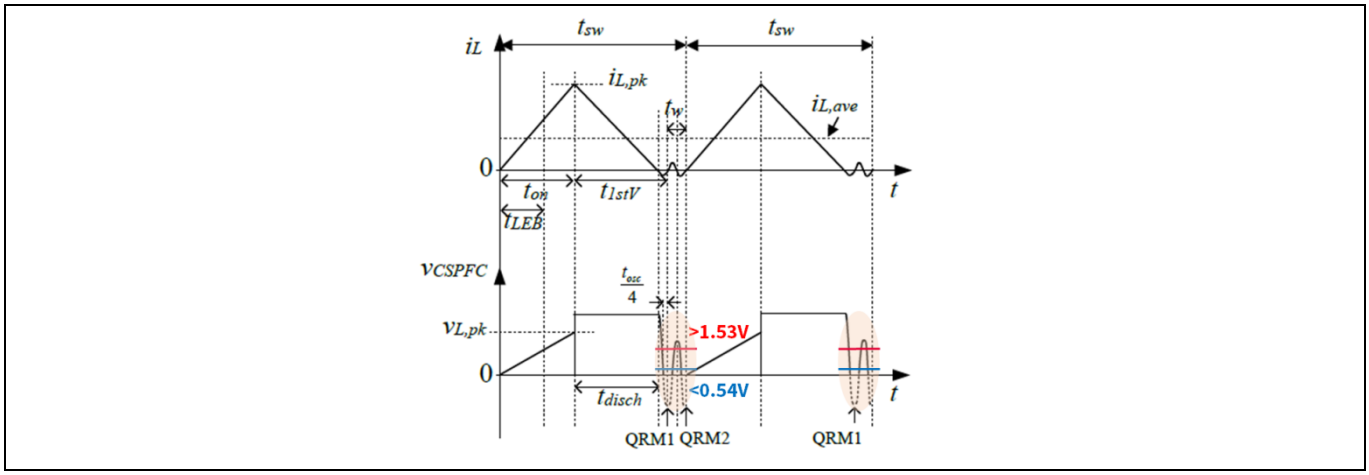



**Figure 7 Hysteretic comparator threshold for zero crossing detection**

To design the PFC current sense shunt resistor, following condition must be complied:

$$I_{L,pk\_PFC\_max} * R_{CS_{PFC}} < V_{OCP1\_PFC\_max} = 1.214\,V$$

and

$$R_{CS\_PFC} < \frac{1.214V}{I_{L,pk\_PFC\_max}} = 0.28\,\Omega$$

The value of the current sense resistor is chosen to 0.165 Ω with two resistors 0.33 Ω parallel connected. This splits the power dissipation and reduces the thermal stress. The maximum power loss of each shunt resistor is:

$$P_{loss\_shunt\_PFC\_max} = 0.5 * I^2_{L\_RMS\_max} * R_{CS\_PFC} = 0.5 * 1.71A^2 * 0.33 = 0.48\,W$$

This should be considered while selecting the proper shunt resistor type.

The important design parameters for bus voltage sensing are summarized in the following **Table 9**:

**Table 9 PFC Current sense and ZCD design parameters**

| Parameter | Symbol | Value | Unit |
|---|---|---|---|
| Upper resistor of the PFC ZCD divider | $R_{ZCD1\_PFC}$ | 4.7 | kΩ |
| Lower resistor of the PFC ZCD divider | $R_{ZCD2\_PFC}$ | 33 | kΩ |
| PFC OCP1 maximum operating range | $V_{OCP1\_PFC\_max}$ | 1.214 | V |
| PFC current sense resistor | $R_{CS\_PFC}$ | 0.33//0.33=0.165 | Ω |

## 2.4.6 PFC Output voltage sense

As shown in the **Figure 8** below, the bus voltage is measured at the VS pin of XDPL8221 through a resistor divider. This measurement is used as the input of the PFC output voltage regulator to generate the PWM control signal for PFC MOSFET and offers the protection functions for the PFC boost converter. It is strongly recommended to add a filter capacitor near the VS pin to filter the switching noise in order to get a precise and stable measurement result. The VS pin has a very low leakage current so the intolerance can be ignored.

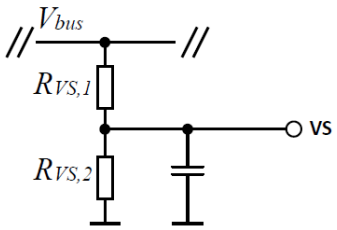



**Figure 8 Bus voltage measurement**

Inside the XDPL8221, the VS pin is connected to an 8-Bit Analog-to-Digital Converter (ADC) which utilizes two voltage ranges for the bus voltage measurement results. This gives the advantage that on the one hand, the whole voltage range started from 0V is monitored. On the other hand the operating range is sensed with a high resolution so that the regulation accuracy is guaranteed.

As shown in the **Figure 9**, the wide voltage range from 0 to $V_{REF}$ results in a low resolution. If the nominal operating bus voltage $V_{bus}$ = 460 V is assumed in the normal operation and mapped to $V_{REF}$ by the resistor divider as recommended, then a 8-Bit ADC gives the range 0 ~ 460 V a resolution of

$$Wide\ Range\ Resolution = \frac{V_{bus}}{256} \approx 1.8\,V/LSB$$

This range is used to monitor the start-up behavior or other failures.

The narrow voltage range from 5/6 $V_{REF}$ to 7/6 $V_{REF}$ gives a three times better resolution. If the nominal operating bus voltage $V_{bus}$ = 460 V is assumed and mapped to $V_{REF}$, then a 8-Bit ADC gives the range from 5/6*$V_{bus}$ = 383 V to 7/6* $V_{bus}$ = 536 V a resolution of

$$Narrow\ Range\ Resolution = \frac{1}{3} * \frac{V_{bus}}{256} \approx 0.6\ V/LSB$$

So in the steady state operation, the high-resolution range is used to get an accurate bus voltage regulation.

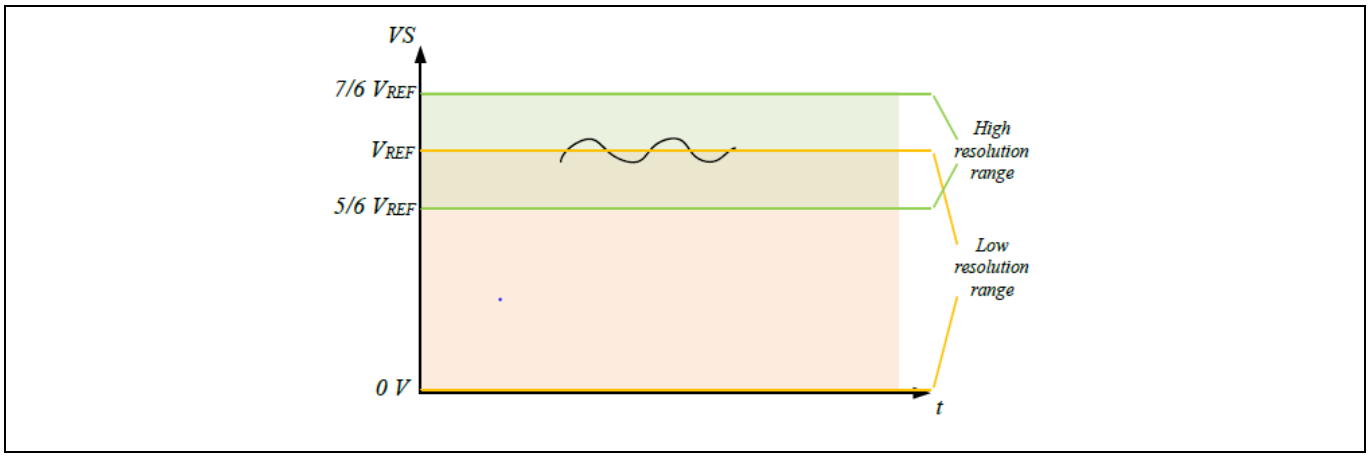



**Figure 9 Bus voltage sensing ranges**

The calculation of the resistor divider is given as following if the $V_{bus}$ = 460 V is mapped to $V_{REF}$:

$$\frac{R_{VS1\_PFC}}{R_{VS2\_PFC}} = \frac{V_{bus} - V_{REF}}{V_{REF}} = 188.46$$

To reduce the inaccuracy caused by the resistor divider, it is necessary to select the bus voltage sensing resistors with a tolerance of 1% or less. In the 100 W driver reference design, to reduce the voltage stress, the upper resistor $R_{VS1\_PFC}$ consists of three resistors of each 3.32 MΩ and the lower resistor $R_{VS1\_PFC}$ is selected as 52.3 kΩ.

*Note: As indicated in the XDPL8221 Datasheet, the Vcc pin voltage must be higher than 3.4 V before the voltage of VS exceeds 1.2 V. So it is recommended to select the divider with high impedance. This also helps to reduce the power consumption in the stand-by mode.*

The criteria to switch between these two ranges are as following if the tolerance of the resistors can be ignored:

- The PFC boost converter always starts in the narrow (high resolution) range
- In the narrow (high resolution) range, if the bus voltage $V_{bus}$< 406 V then it will be switched to wide range
- In the wide (low resolution) range, if the bus voltage $V_{bus}$ > 430 V, then it will be switched to the narrow range

*Note: In order to reduce the switching noise coupled in the Bus voltage sense signal, a filter capacitor of 1 nF is strongly recommended to be placed directly near the VS pin.*

The important design parameters for bus voltage sensing are summarized in the following **Table 10**:

**Table 10 Bus voltage sensing design parameters**

| Parameter | Symbol | Value | Unit |
|---|---|---|---|
| Nominal PFC boost converter output voltage | $V_{bus}$ | 460 | V |
| XDPL8221 internal ADC reference voltage | $V_{REF}$ | 2.428 | V |
| Bus voltage sensing divider upper resistor | $R_{VS1\_PFC}$ | 3.32 x 3 | MΩ |
| Bus voltage sensing divider lower resistor | $R_{VS2\_PFC}$ | 52.3 | kΩ |
| Bus voltage sensing filter capacitor | $C_{VS}$ | 1 | nF |
| Narrow (High Resolution) range | - | 383 ~ 536 | V |
| Resolution of narrow range | - | 0.6 | V/LSB |
| Wide (Low Resolution) range | - | 0 ~ 460 | V |
| Resolution of wide range | - | 1.8 | V/LSB |

## 2.4.7 PFC Output capacitor

The PFC bus capacitor can be calculated with the following formula if the ESR of the capacitor is small enough to be neglected and the peak to peak voltage ripple is selected as 20 V. Please note that the tolerance of 20% of the capacitance needs to be taken into account as well.

$$C_{bus} = \frac{I_{out\_PFC\_max}}{2 * \pi * f_{line\_min} * V_{bus\_ripple\_pp}} * 1.2 = 46\ \mu F$$

With

$$I_{out\_PFC\_max} = \frac{P_{O\_PFC\_max}}{V_{bus}} = 0.24\ A$$

Regarding the voltage rating with consideration of over-voltage protection threshold, a 500 V capacitor is necessary. But due to the price and size factors, it is reasonable to use two 250V rating capacitors in series. The ESR of the capacitor should be selected as small as possible and the allowed maximum ripple current should have enough margins. In the 100 W driver reference design, one 500 V capacitor of 47 µF with low ESR is selected. To symmetrize the voltage stress on the two in series connected capacitors, an in parallel connected high ohmics resistor divider is recommended, which will increase the stand by power consumption lightly nevertheless.

The important parameters for the bus capacitor selection are summarized in the following table:

**Table 11 Bus Capacitors Design Parameters**

| Parameter | Symbol | Value | Unit |
|---|---|---|---|
| Nominal PFC boost converter output voltage | $V_{bus}$ | 460 | V |
| Maximum PFC boost converter output power | $P_{out\_PFC\_max}$ | 110 | W |
| Bus voltage ripple (peak to peak) | $V_{bus\_ripple\_pp}$ | 20 | V |
| AC input line frequency | $f_{line}$ | 45 ~ 66 | Hz |
| PFC Bus capacitor | $C_{bus}$ | 47 | µF |

## 2.4.8 PFC Multi-mode control

The PFC boost converter regulates the output bus voltage through the calculated constant on-time:

$$t_{on\_PFC} = \frac{2 * P_{O\_PFC\_max} * L_{PFC}}{V_{in\_rms}^2 * \eta_{PFC}}$$

As shown from the formula above, when the inductance is fixed and the line input voltage is constant, the PFC on-time is only dependent on the converter output power. The output voltage is sensed and fed into the internal regulator for on-time calculation. With the calculated on-time and frequency law, a switching cycle is defined.

For PFC boost converter operating in the QRM (quasi resonant mode), the PFC MOSFET is turned on with constant on-time throughout the complete AC half cycle and the off-time is varying during the AC half cycle depending on the instantaneous input voltage applied. A new switching cycle starts after the inductor current reaches zero. It is ideal for full load operation, where the on-time is large. However, the on-time reduces at light load, resulting in very high switching frequency especially near the zero-crossings of the AC input. The high switching frequency increases the switching loss, resulting in poor efficiency at light load. Therefore the multi-mode control is implemented.

XDPL8221 uses QRM+DCM operation for PFC load regulation. At full load and heavy load, PFC is running with QRM1 for the best power efficiency. When the load decreases, XDPL8221 reduces the on time and switching frequency at the same time by adding an additional delay into each switching cycle through selecting further inductor current valleys to achieve QRM2 and up to maximum QRM5 (configurable) operation. **Figure 10** illustrates the QRM2 valley switching in multi-mode PFC control as an example. In case of light load e.g. deep dimming, DCM operation with fixed on time is applied to further reduce the power transfer: the adjustment of the switching period will regulate the load change and the switching frequency can be reduced.

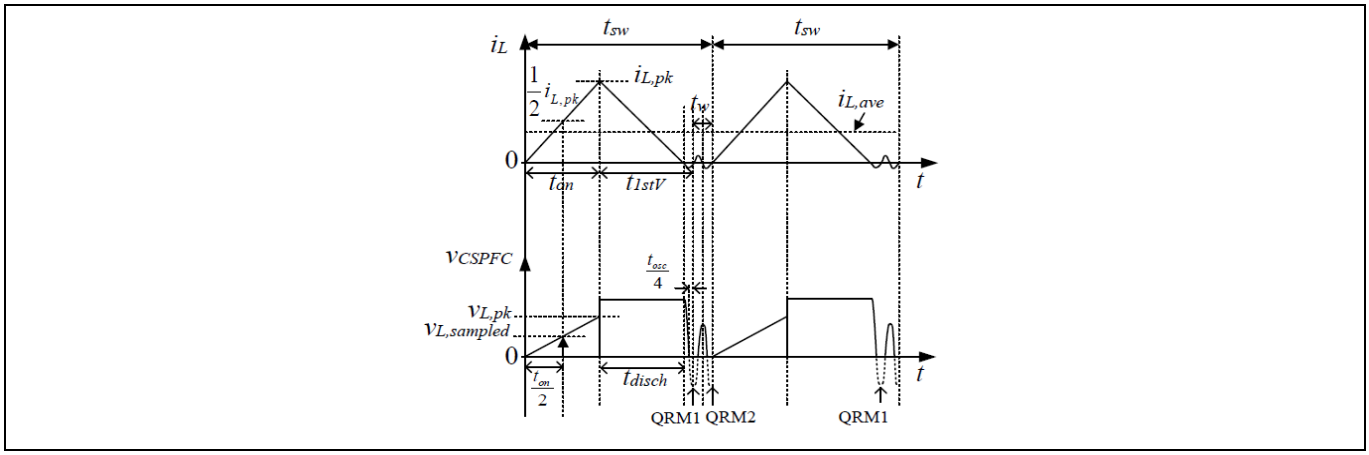



**Figure 10 PFC Boost multi-mode control with QRM2**

The multi-mode control is defined in the frequency law, which consisting of a maximum switching frequency $f_{sw\_PFC\_max}$ and a minimum switching frequency $f_{sw\_PFC\_min}$ controls the valley selection (QRMn). In this way, the switching frequency is limited within the defined range and efficiency at light load can be improved. An illustration of the frequency law is shown in **Figure 11**:

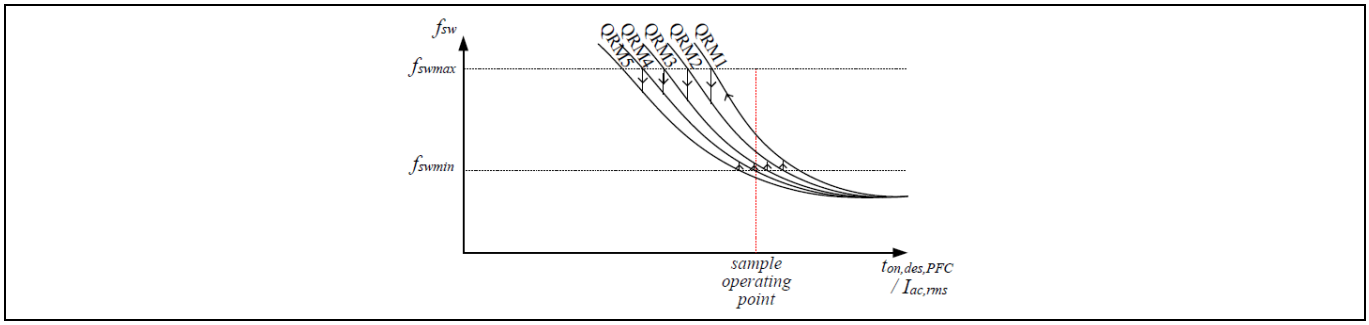



**Figure 11 Frequency law for operating mode**

The switching between QRM and DCM operation is described in the following **Figure 12**:

- PFC will enter DCM operation from QRM once the internal calculated on time is smaller than $t_{on\_dcm\_PFC}$
- PFC will leave DCM operation back to QRM once the switching frequency is higher than $f_{sw\_max\_dcm\_PFC}$

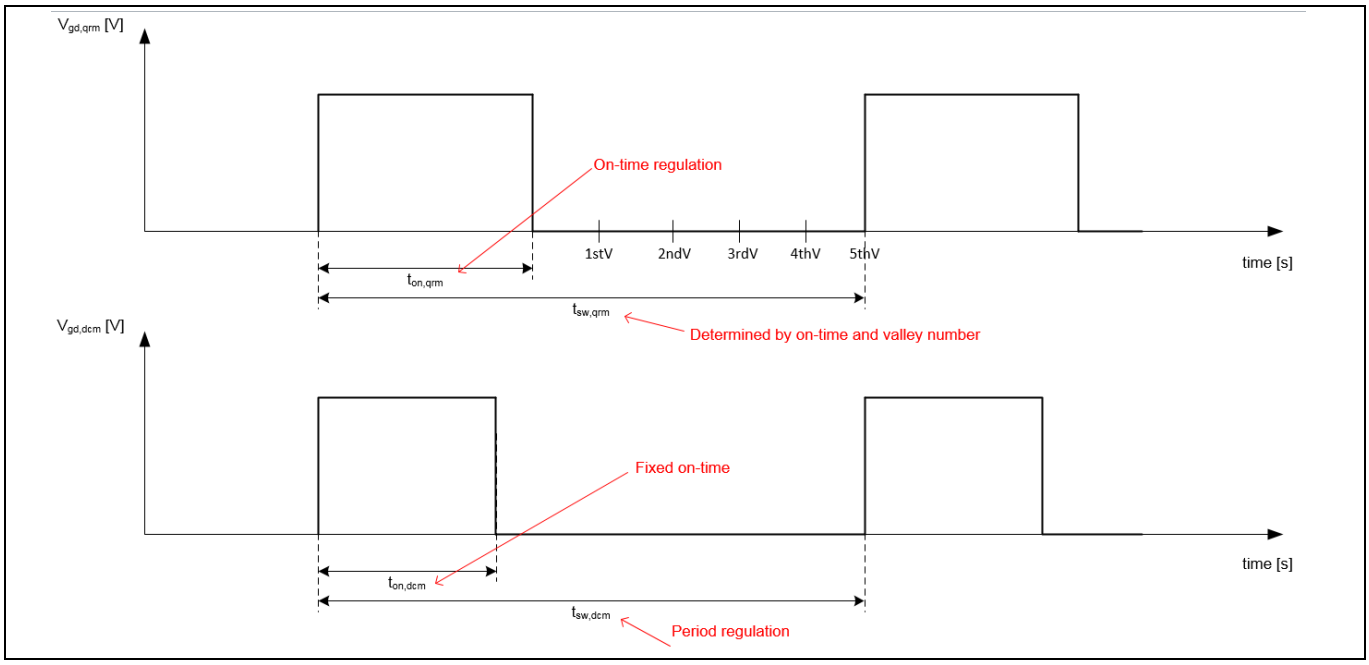



**Figure 12 Mode switching between QRMn and DCM operation**

The important design parameters for multi-mode control are summarized in the following table:

**Table 12 Input Voltage Sensing Design Parameters**

| Parameter | Symbol | Value | Unit |
|---|---|---|---|
| Maximum PFC boost converter switching frequency | $f_{sw\_max\_PFC}$ | 80 | kHz |
| Minimum PFC boost converter switching frequency | $f_{sw\_min\_PFC}$ | 22 | kHz |
| The minimum on time to enter the DCM operation | $t_{on\_dcm\_PFC}$ | 300 | ns |
| The maximum frequency to leave the DCM operation | $f_{sw\_max\_dcm\_PFC}$ | 150 | kHz |
| Maximum allowed valley | $N_{valley\_max\_PFC}$ | 8 | - |

## 2.4.9 PFC Start-up and steady state control

After the AC or DC voltage is applied at the input, the bus voltage is charged by the bridge rectifier and PFC diode. The Vcc capacitors are charged by the high voltage start-up cell till the Vcc on threshold is reached and the XDPL8221 is active. After activation, XDPL8221 checks first if the bus voltage is higher than $V_{bus\_start\_PFC}$ (brown-in condition). The PFC boost converter begins with the soft-start phase one the condition is fulfilled. After the threshold $V_{bus\_steady\_entry\_UV}$ is reached within the time $t_{start\_max\_PFC}$, the start-up phase is over and the controller will switch to the steady state operation till the operating bus voltage value $V_{bus\_set}$ is reached. Once the bus voltage is still lower than the threshold beyond the time, the PFC soft-start failure will be triggered. This is shown in the following **Figure 13**:

XDPL8221 PFC stage uses PIT1 (Proportional-Integral-T1) controller to control the bus voltage in start-up and steady state operation:

- Term P is proportional to the bus voltage error (difference between current bus voltage value and the operating nominal bus voltage value)
- Term I accounts for past values of the bus voltage error and integrates them over time to produce the I-term.
- Term T1 is a low pass filter which eliminates the noise in the error signal.

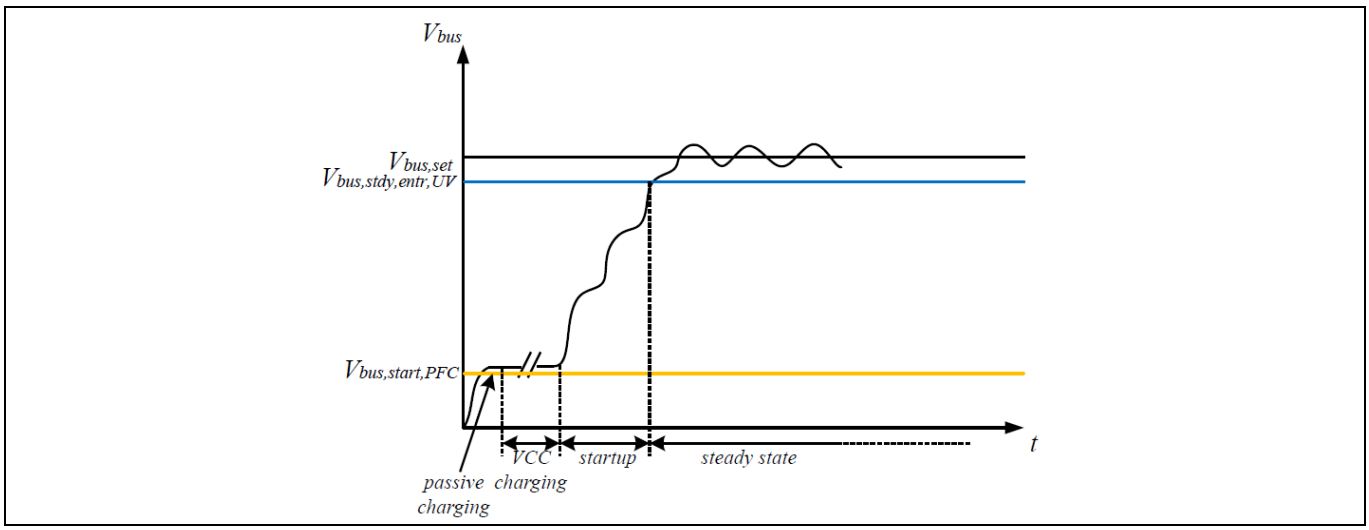



**Figure 13 PFC Boost Converter Start-Up Control**

The PIT1 controller parameters used for the start-up and steady state may be different because of different requirements of the control loop. In the start-up phase, the control loop reacts fast because a fast dynamic response is important in order to settle the bus voltage at the defined operation level as soon as possible so that the flyback stage can start quickly and take over the IC power supply. Furthermore, it also helps to reduce the time-to-light. On the contrary, a relative slow loop response in the steady state operation is desired for the stable bus voltage regulation. To reduce the PFC bus voltage ripple in the DCM operation, the controller gain can be configured, too. This eliminates the possible flicker in the deep dimming condition.

For all PIT1 controller gain parameters in XDPL8221: the higher the gain value is, the lower is the gain.

The important design parameters for PFC Boost Converter Start-up control are summarized in the table below:

**Table 13 PFC Start-up design parameters**

| Parameter | Symbol | Value | Unit |
|---|---|---|---|
| Voltage threshold to start PFC stage | $V_{bus\_start\_PFC}$ | 75 | V |
| Voltage threshold for closed loop regulation | $V_{bus\_steady\_entry\_UV}$ | 448 | V |
| Nominal PFC boost converter output voltage | $V_{bus\_set}$ | 460 | V |
| Proportional gain of PIT1 regulator in the start-up phase | $SVP_{start\_up}$ | 5 | - |
| Integral gain of PIT1 regulator in the start-up phase | $SVI_{start\_up}$ | 9 | - |
| Proportional gain of PIT1 regulator in the steady state phase | $SVP_{steady\_state}$ | 4 | - |
| Integral gain of PIT1 regulator in the steady state phase | $SVI_{steady\_state}$ | 7 | - |
| T1 filter gain in the steady state phase | SVT | 6 | - |
| Proportional gain of PIT1 regulator in the DCM operation | $SVP_{dcm}$ | 1 | - |
| Integral gain of PIT1 regulator in DCM operation | $SVI_{dcm}$ | 7 | - |

## 2.4.10 Input voltage sensing

The rectified input voltage is measured through an external current limitation resistor $R_{HV}$ at the HV pin as shown in the **Figure 14**. This path provides not only the input voltage sensing function, but also the power supply via the IC internal built HV start-up cell for XDPL8221 before the Vcc reaches the on-threshold.

The input voltage sensing distinguishes whether the AC or DC voltage is applied at input. Meanwhile, input voltage measurement provides the brown-in, brown-out and input over voltage protection. The threshold of each protection may be different for AC or DC input.

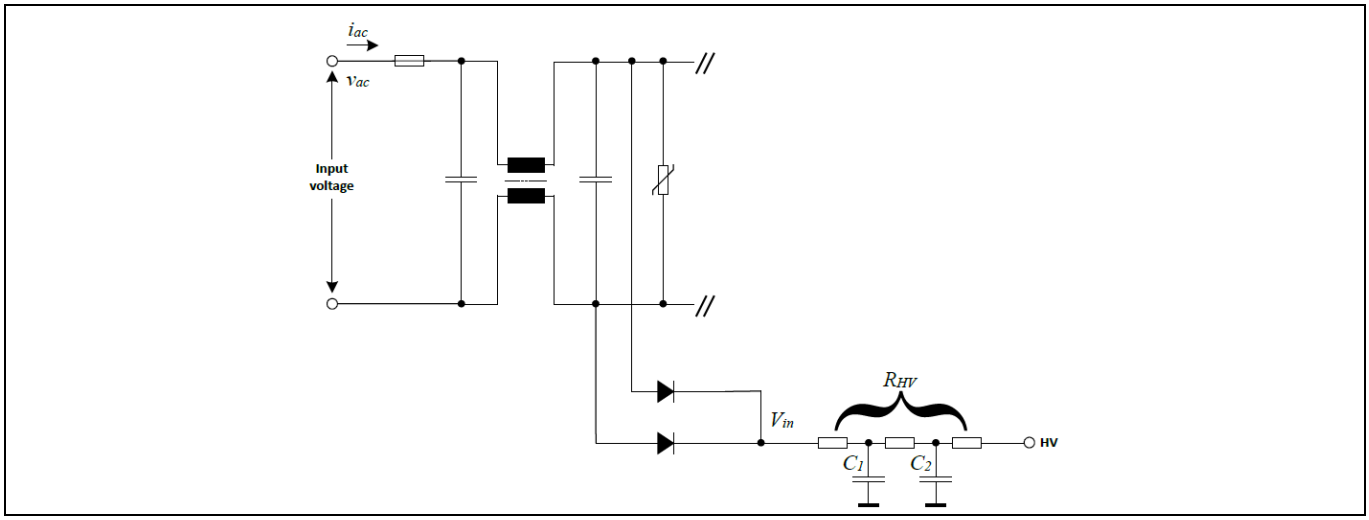



**Figure 14 Input voltage sensing**

To charge the Vcc capacitors through the IC internal start-up cell, the charge current must be limited not to over-power the start-up cell. The current limitation resistor $R_{HV}$ must fulfill the following condition:

$$R_{HV} > \frac{\sqrt{2} * V_{in\_max\_rms}}{I_{HV\_max}} = 45\ k\Omega$$

Because of internal setup of the HV pin to measure the input precisely, it is mandatory to use the HV current limitation resistor $R_{HV}$ = 99kΩ in order to limit the maximum HV pin current to 9.6 mA. To reduce the voltage and power stress of the resistor, it is strongly recommended to split it into three 1206 resistors of each 20 kΩ. To improve the accuracy of the measurement, resistors with tolerance less than 1% should be selected.

*Note: To reduce the switching due to the PFC stage at the input stage and to increase the accuracy of the input voltage measurement, it is highly recommended to add high voltage filter capacitors with typical value of 680 pF after each HV resistor as shown in the **Figure 14**.*

The important design parameters for input voltage sensing are summarized in the following table:

**Table 14 Input voltage sensing design parameters**

| Parameter | Symbol | Value | Unit |
|---|---|---|---|
| Maximum AC input Voltage | $V_{in\_AC\_max\_rms}$ | 305 | Vrms |
| Maximum DC input voltage | $V_{in\_DC\_max}$ | 305 | V |
| Maximum current of start-up cell | $I_{HV\_max}$ | 9.6 | mA |
| HV current limitation resistor | $R_{HV}$ | 20x3=60 | kΩ |

## 2.4.11 PFC Protection features

The digital controller XDPL8221 provides all around protections for both power components and input/output of the PFC boost converter. As illustrated below in the control state machine (**Figure 15**), the protections are active after the system enters the start-up checks state (when Vcc voltage reaches the on-threshold). While the start-up checks, the input/output are monitored before starts PFC to protect against possible under/over-voltage. After the system is in the soft-start state, more protections like over-current, over-power and CCM protection are also activated. An overview of which protection enabled in which operating state is given in the following **Table 15**:

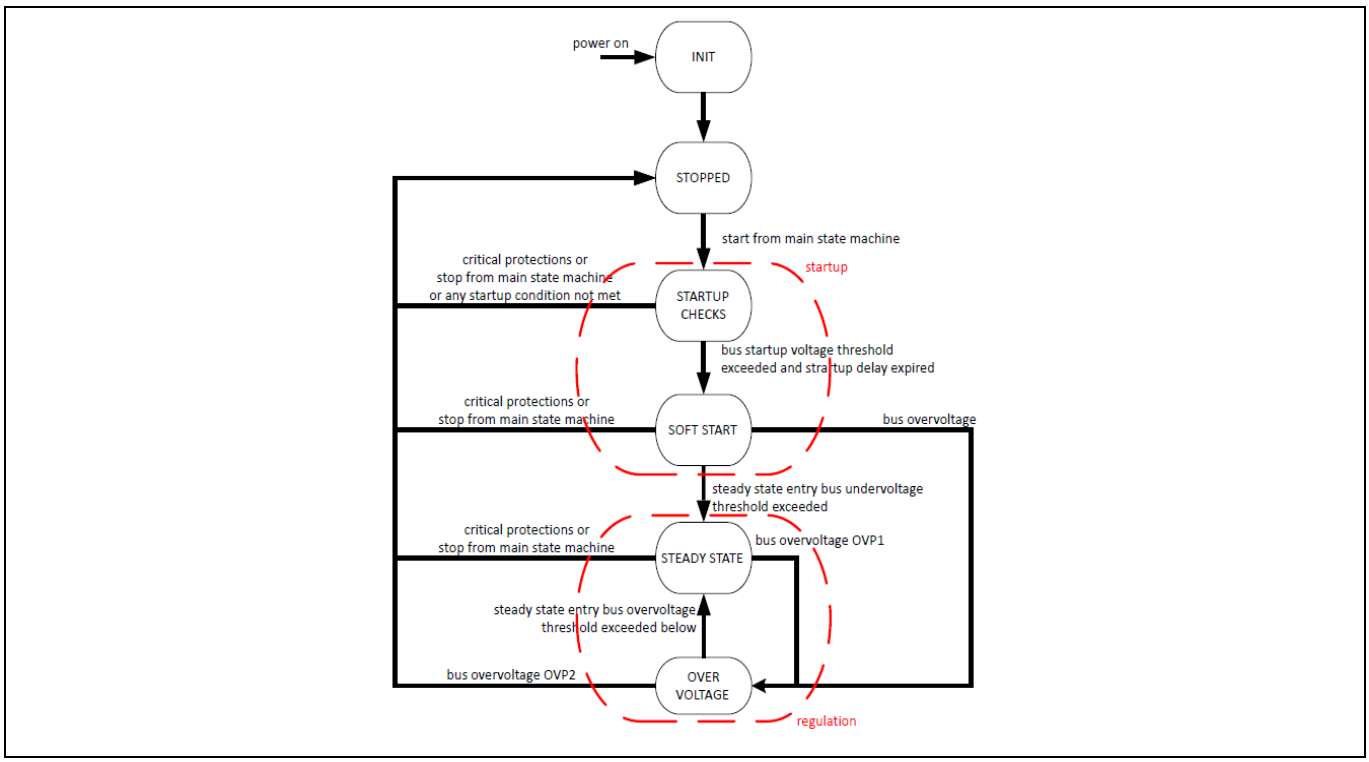



**Figure 15 PFC Boost converter control state machine**

**Table 15 PFC Protection states**

| Protection | Stopped | Soft-Start | SteadyState | Over Voltage |
|---|---|---|---|---|
| Bus Over-oltage Protection level 2 (OVP2) | Disabled | Enabled | Enabled | Enabled |
| Bus Under-voltage Protection | Disabled | Disabled | Enabled | Enabled |
| Input Over-voltage Protection | Disabled | Enabled | Enabled | Enabled |
| Input Under-voltage Protection | Disabled | Enabled | Enabled | Enabled |
| Over-current Protection level 2 | Disabled | Enabled | Enabled | Enabled |
| Soft-Start Failure | Disabled | Enabled | Disabled | Disabled |
| CCM Protection | Disabled | Disabled | Enabled | Disabled |

### 2.4.11.1 Bus voltage protection

The voltage at the VS pin which represents the bus voltage is sensed for the bus voltage protection.

Bus over-voltage protection is mandatory to protect the DC-link electrolytic capacitor, boost diode and MOSFET of the flyback converter. There are two different level protections defined:

- The OVP1 is part of the regulation loop and controlled by the firmware. When the OVP1 threshold $V_{bus\_OVP1}$ is continuously triggered beyond the configured blanking time $t_{blank\_bus\_OVP1}$, the PFC gate driver is stopped by the firmware. In this case, flyback converter should go on switching to help discharging the bus capacitor. The PFC gate driver is only enabled again when the bus voltage falls below the level $V_{bus\_steady\_entry\_OV}$. No further protection action is necessary.
- The OVP2 in contrast is a hardware protection and the gate driver is disabled if the fixed OVP2 threshold $V_{bus\_OVP2}$ is triggered beyond the defined blanking time $t_{blank\_bus\_OVP2}$ and without any firmware delay. In this case, flyback converter will also stop working and XDPL8221 will enter the latch mode. The OVP2 threshold is defined as a VS pin voltage of 2.8V, which together with the bus voltage sense divider results in the corresponding voltage at the bus.
- Bus under-voltage protection is meaningful to prevent the flyback transformer from running into saturation. When the threshold $V_{bus\_UV}$ is continuously triggered beyond the configured blanking time $t_{blank\_bus\_UV}$, both PFC and flyback converter operations are stopped and XDPL8221 will enter the auto-restart mode.

The different OVP thresholds are illustrated in the following:

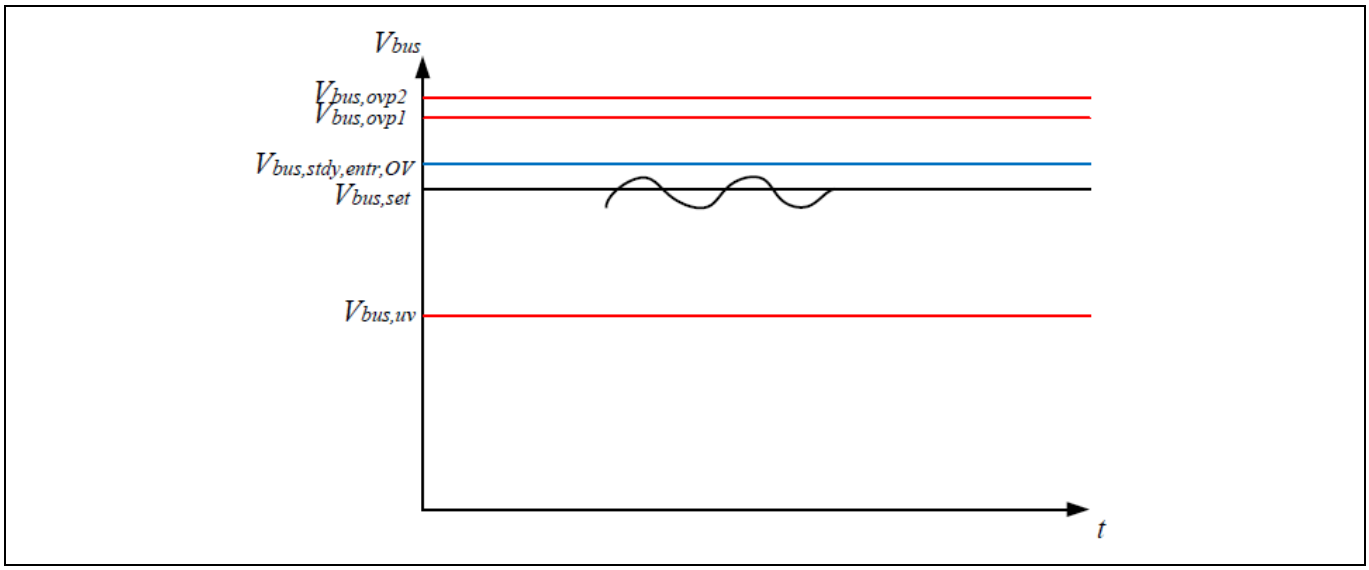



**Figure 16 PFC Bus voltage protection thresholds**

The important design parameters for bus voltage protection are summarized in the table below:

**Table 16 PFC Bus voltage protection design parameters**

| Parameter | Symbol | Value | Unit | Configurable |
|---|---|---|---|---|
| Bus over-voltage protection level 2 threshold | $V_{bus\_OVP2}$ | 536 | V | No |
| Blanking time for OVP2 | $t_{blank\_bus\_OVP2}$ | 200 | ns | Yes |
| Reaction OVP2 | - | Auto-Restart | - | Yes |
| Bus over-voltage protection level 1 threshold | $V_{bus\_OVP1}$ | 485 | V | Yes |
| Blanking time for OVP1 | $t_{blank\_bus\_OVP1}$ | 384 | µs | Yes |
| Recovery threshold from OVP1 | $V_{bus\_steady\_entry\_OV}$ | 472 | V | Yes |
| Bus under-voltage protection threshold | $V_{bus\_UV}$ | 300 | V | Yes |
| Blanking time for under-voltage | $t_{blank\_bus\_UV}$ | 500 | ms | Yes |
| Reaction bus under-voltage protection | - | Auto-Restart | - | Yes |

### 2.4.11.2 Input voltage protection

Input voltage protection is realized by monitoring the voltage at the HV pin. After the XDPL8221 is active and before the PFC boost converter is started, the input voltage is checked first. Once the input RMS voltage is between the threshold $V_{in\_start\_min}$ and $V_{in\_start\_max}$, PFC will start. After this, input will be monitored continuously. If the input voltage touches the under-voltage or over-voltage threshold beyond the blanking time, XDPL8221 will enter the auto-restart mode.

The important design parameters for input voltage protection are summarized in the table below:

**Table 17 PFC Input voltage protection design parameters**

| Parameter | Symbol | Value | Unit | Configurable |
|---|---|---|---|---|
| Minimum input voltage to start PFC Converter | $V_{in\_start\_min}$ | 88 | Vrms | Yes |
| Maximum input voltage to start PFC Converter | $V_{in\_start\_max}$ | 308 | Vrms | Yes |
| Input under-voltage protection during operation | $V_{in\_UV}$ | 76 | Vrms | Yes |
| Blanking time for input over-/under-voltage | $t_{blank\_Vin\_OV\_UV}$ | 100 | ms | Yes |
| Reaction input under-voltage protection | - | Auto-Restart | - | Yes |
| Input over-voltage protection during operation | $V_{in\_OV}$ | 320 | Vrms | Yes |
| Reaction input over-voltage protection | - | Auto-Restart | - | Yes |

*Note: The thresholds listed in the table above are related to the selected HV resistor of 60 kΩ. Different HV resistor will result in different thresholds.*

### 2.4.11.3 Over-current protection

The over-current protection is necessary to control the maximum current flowing through the PFC boost inductor and PFC MOSFET so that they are not over-powered. This is realized by monitoring the voltage across the PFC shunt resistor. If the voltage reaches the threshold and beyond the blanking time, PFC gate will be switched off. There are two level of the over-current protection:

- Over-current Protection level 1: by touching the threshold $V_{CS\_PFC\_OCP1}$ of the OCP1 beyond the blanking time $t_{blank\_OCP1\_PFC}$, PFC gate will be switched off and the next switching cycle will be started again after the zero-crossing signal is detected. No further action will be taken. This is a cycle by cycle power limitation.
- Over-current Protection level 2: by touching the threshold $V_{CS\_PFC\_OCP2}$ of the OCP2, both PFC and flyback gate drive will be switched off and XDPL8221 will enter the latch mode

The important design parameters for PFC over-current protection are summarized in the table below:

**Table 18 PFC Over-current design parameters**

| Parameter | Symbol | Value | Unit | Configurable |
|---|---|---|---|---|
| PFC Over-current protection level 1 threshold | $V_{CS\_PFC\_OCP1}$ | 0.75 | V | Yes |
| Blanking time for PFC OCP1 | $t_{blank\_OCP1\_PFC}$ | 200 | ns | Yes |
| PFC Over-current protection level 2 threshold | $V_{CS\_PFC\_OCP2}$ | 1.6 | V | No |
| Blanking time for PFC OCP2 | $t_{blank\_OCP2\_PFC}$ | 600 | ns | Yes |
| Reaction to PFC OCP2 | - | Latch | - | Yes |

### 2.4.11.4 Soft-start failure

When the input voltage is low beyond the nominal range or the output is over-loaded, the start-up time of the PFC boost converter may be extended to an unexpected long value. In both cases, the protection could be triggered and XDPL8221 will enter the auto-restart mode. The PFC soft-start time $t_{start\_PFC}$ is defined and monitored from the moment that PFC stage is started till the bus voltage reaches the threshold $V_{bus\_steady\_entry\_UV}$. If this time exceeds the maximum allowed PFC soft-start time $t_{start\_PFC\_max}$, protection will be triggered and XDPL8221 will enter the auto-restart mode.

The important design parameters for soft-start failure are summarized in the table below:

**Table 19 PFC Soft-start failure design parameters**

| Parameter | Symbol | Value | Unit | Configurable |
|---|---|---|---|---|
| Voltage threshold for start-up end | $V_{bus\_steady\_entry\_UV}$ | 448 | V | Yes |
| Maximum allowed PFC soft-start time | $t_{start\_PFC\_max}$ | 400 | ms | Yes |

### 2.4.11.5 CCM protection

Continuous conduction mode (CCM) operation occurs when the magnetizing current does not decrease to zero before the next switching cycle starts. This happens usually when the difference of the bus voltage and input voltage is very small, which is the case of start-up or boost diode short. However, when the output is over-loaded or input voltage is too low, the inductor peak current will be very high and the demagnetizing of boost inductor cannot be operated completely, too. At start-up, the CCM operation is allowed for limited time but in other conditions, XDPL8221 must enter the protection mode.

The CCM operation is monitored at the PFC CS pin. When the ZCD signal does not come till the maximum switching period time-out happens, it will be treated as a CCM cycle. If the CCM operation happens beyond the blanking time $t_{blank\_CCM\_PFC}$, XDPL8221 will enter the auto-restart mode.

The important design parameters for CCM protection are summarized in the table below:

**Table 20 PFC CCM protection design parameters**

| Parameter | Symbol | Value | Unit | Configurable |
|---|---|---|---|---|
| Blanking time for PFC CCM operation | $t_{blank\_CCM\_PFC}$ | 12 | ms | Yes |

## 2.5 Design the flyback converter

The flyback converter takes the boosted DC voltage as input and converts it to a configurable wide range DC output with the programmable constant current on the secondary side. The controller XDPL8221 provides a primary side output voltage and current control without the external regulator on the secondary side. This chapter describes the methodology for designing the multi-mode control (QRM+DCM+ABM) flyback converter based on XDPL8221, which includes the flyback transformer design, power losses estimation, selection guide for power semiconductor devices and passive components.

The design specification for the 100 W driver reference design is given in the following table:

**Table 21 Flyback converter design specification**

| Flyback converter | | | |
|---|---|---|---|
| **Parameter** | **Symbol** | **Value** | **Unit** |
| Minimum DC input voltage | $V_{bus\_min}$ | 440 | V |

| | | | |
|---|---|---|---|
| Nominal DC input voltage | $V_{bus}$ | 460 | V |
| Maximum DC input voltage | $V_{bus\_max}$ | 485 | V |
| Maximum flyback converter output power | $P_{O\_max}$ | 100 | W |
| Minimum switching frequency | $f_{sw\_FB\_min}$ | 16 | kHz |
| Estimated flyback converter power efficiency | $\eta_{FB}$ | < 93 | % |
| Flyback converter output voltage | $V_{out}$ | 16 to 48 | V |
| Flyback converter output over-voltage threshold | $V_{out\_OV}$ | 53 | V |
| Flyback converter output current | $I_{out}$ | 550 to 2500 | mA |
| Maximum flyback MOSFET drain-source voltage | $V_{DS\_max}$ | 800 | V |
| Secondary diode forward voltage | $V_F$ | 1 | V |
| Secondary diode voltage rating | $V_{RRM}$ | 400 | V |

### 2.5.1 Design the flyback transformer

For flyback converter, the transformer is the most important factor that determines the performance such as the efficiency, output regulation and EMI. Contrary to the normal transformer, the flyback transformer is inherently an inductor that provides energy storage, coupling and isolation for the flyback converter. In the general transformer, the current flows in both the primary and secondary winding at the same time. However, in the flyback transformer, the current flows only in the primary winding while the energy in the core is charged and in the secondary winding while the energy in the core is discharged. Usually a gap is introduced between the cores to increase the energy storage capacity. The general transformer design procedures are briefly described below.

#### 2.5.1.1 Transformer turns ratio

The transformer turns-ratio n decides not only the reflected voltage from the secondary side to the primary side, which affects the primary side flyback MOSFET selection, but also the maximum switching duty cycle $D_{max}$ of the flyback converter.

A higher transformer turns-ratio steps down the voltage from input to output more, such that a higher duty cycle may be employed. The maximum duty cycle is exactly defined by the turn-ratio, since magnetizing time and demagnetizing time are functions of input voltage and reflected output voltage respectively. The duty cycle of the QR mode flyback can be calculated as following:

$$D = \frac{t_{on}}{t_{on} + t_{off}} = \frac{n * (V_{out} + V_F)}{V_{bus} + n * (V_{out} + V_F)}$$

with

$$t_{off} = t_{demag} + 0.5 * T_{osc}$$

This expression for D clearly approaches 1 asymptotically when n approaches ∞ (and 0 when n approaches 0). Nevertheless, a high turns-ratio means high reflected voltage from the secondary to primary side, which requires a higher MOSFET drain-source break down voltage. Therefore, the maximum transformer turns-ratio depends on the expected maximum input voltage and reflected output voltage, since the sum of the two determines the voltage stress across drain-source of primary side MOSFET during the demagnetization period like following:

$$V_{DS\_MOS\_max\_FB} = V_{bus\_max} + n * V_{out\_max}$$

During turn-off of the primary side MOSFET, energy stored in leakage inductance will charge up the $C_{oss}$ of the primary MOSFET causing an overvoltage spike to occur on top of the steady-state stress voltage. Depending on the leakage inductance value and the $C_{oss}$ characteristics of the MOSFET employed, the snubber circuit can be tuned to guarantee operation within the voltage rating of the MOSFET, when employing a de-rating factor as is norm in the industry. In the 100 W driver reference design, 800 V MOSFET is selected with a de-rating of 85% is assumed. So the maximum turns-ratio $n_{max}$ is calculated as:

$$n \leq n_{max} = \frac{0.85 * V_{DS_{MOS_{FB}}} - V_{bus\_max}}{V_{out\_max}} = 3.67$$

A low transformer turns-ratio could be desirable for several reasons. One reason is the conduction losses on the output loop, since the primary peak current is defined independent of the transformer turns-ratio by the DCM Flyback power equation:

$$P_{out} = \frac{1}{2} * L_{FB} * i_{p\_pk}^2 * f_{FB} * \eta_{FB}$$

The output loop peak-current is the input peak current reflected across the transformer:

$$i_{s\_pk} = n * i_{p\_pk}$$

A smaller turns-ratio will reduce the secondary peak current and thus the conduction loss. One other reason could be the construction of the transformer itself. In order to get a strong coupling with accurate turns-ratio, there is a minimum practical limit to the number of physical turns on the output-side. With a minimum output winding turns-count and a maximum input winding turns-count, a practical upper limit to the transformer turns-ratio will also exist. With the electrical requirements known, the minimum transformer turns-ratio can be found similarly as the maximum, but based on voltage rating for the desired output rectifier diode $V_{RRM}$. The steady state voltage stress across the diode is the sum of the transformer winding voltage and the output voltage, both of which have known maxima from previous calculations. The MOSFET voltage rating must adhere to de-rating criteria:

$$n \geq n_{min} = \frac{V_{bus\_max}}{0.8 * V_{RRM} - V_{out\_max}} = 2.52$$

Nevertheless, a very low turns-ratio leads to a low duty cycle or smaller on-time at light load. If this small on-time is not able to be output by the controller, then the burst mode is unavoidable, which could lead to higher ripple on the output and audible noise. In the 100 W driver reference design, the turns-ratio is chosen as:

$$\frac{N_p}{N_s} = n = 3.2$$

### 2.5.1.2 Primary magnetizing inductance

The primary magnetizing inductance scaling can be done in several ways. One such way would be to ensure that at least full power can be produced at lowest bus voltage while staying in QRM operation.

As already described in the previous chapter, the maximum duty cycle occurs at minimum bus voltage and maximum output voltage:

$$D_{max\_FB} = \frac{n * (V_{out\_max} + V_{F\_D\_sec})}{V_{bus\_min} + n * (V_{out\_max} + V_{F\_D\_sec})} = 0.28$$

But as the voltage and current could change at the full output power, the more critical working point happens at the maximum output current under full load. So the possible minimum duty cycle at full power in QRM operation is:

$$D_{min\_QRM\_FB} = \frac{n * (\frac{P_{out\_max\_FB}}{I_{out\_max\_FB}} + V_{F\_D\_sec})}{V_{bus\_min} + n * (\frac{P_{out\_max\_FB}}{I_{out\_max\_FB}} + V_{F\_D\_sec})} = 0.23$$

If a minimum switching frequency for full load in the QRM of 35 kHz is assumed, the maximum possible magnetizing inductance is then calculated as:

$$L_{p\_max\_FB} = \frac{V_{bus\_min}^2 * D_{min\_QRM\_FB}^2 * \eta_{FB}}{2 * P_{o\_max\_FB} * f_{sw\_QR\_min\_FB}} = 1.18\ \mathrm{m}H$$

Thus, in the 100W reference design, the primary flyback main inductance is chosen as:

$$L_{P\_FB} = 1\mathrm{m}H < L_{p\_FB\_max}$$

Therewith the maximum reflected voltage is:

$$V_{R\_max} = n * (V_{out\_max} + V_F) = 172.8\ V$$

The minimum switching frequency in the QRM happens at full load with full output current and minimum bus voltage, if an oscillation period $T_{osc\_FB}$ in the QRM is assumed as 1.5µs:

$$f_{sw\_QR\_min\_FB} = \frac{1}{\frac{1}{\frac{V_{bus\_min}^2 * D_{min\_QRM\_FB}^2 * \eta_{FB}}{2 * P_{o\_max\_FB} * L_{p\_FB}}} + 0.5 * T_{osc\_FB}} = 40\ kHz$$

The switching frequency at full load with full output voltage and minimum bus voltage is:

$$f_{sw\_QR\_Vout\_max\_FB} = \frac{1}{\frac{1}{\frac{V_{bus\_min}^2 * D_{max\_FB}^2 * \eta_{FB}}{2 * P_{o\_max\_FB} * L_{p\_FB}}} + 0.5 * T_{osc\_FB}} = 63.9\ kHz$$

The maximum primary peak current appears at minimum bus voltage, maximum output current and full load:

$$I_{p\_pk\_max\_FB} = \sqrt{\frac{2 * P_{O\_max}}{L_{P\_FB} * \eta_{FB} * f_{sw\_FB\_QR\_min}}} = 2.37\ A$$

The maximum on-time happens at minimum bus voltage, maximum output current and full load:

$$t_{on\_max\_FB} = \frac{L_{p\_FB} * I_{p\_pk\_max\_FB}}{V_{bus\_min}} = 5.38\ \mu s$$

The maximum primary RMS current is:

$$I_{p\_rms\_max\_FB} = I_{p\_pk\_max\_FB} * \sqrt{\frac{D_{min\_QRM\_FB}}{3}} = 0.65\ A$$

The maximum primary DC current is:

$$I_{p\_DC\_max\_FB} = \frac{1}{2} * I_{p\_pk\_max\_FB} * D_{min\_QRM\_FB} = 0.26\ A$$

The maximum primary AC current is:

$$I_{p\_AC\_max\_FB} = \sqrt{I_{p\_rms\_max\_FB}^2 - I_{p\_DC\_max\_FB}^2} = 0.59\ A$$

The maximum secondary peak current is:

$$I_{s\_pk\_max\_FB} = n * I_{p\_pk\_max\_FB} = 7.6\ A$$

The maximum secondary RMS current is

$$I_{s\_rms\_max\_FB} = I_{s\_pk\_max\_FB} * \sqrt{\frac{1 - D_{min\_QRM\_FB}}{3}} = 3.85\ A$$

The maximum secondary DC current is:

$$I_{s\_DC\_max\_FB} = \frac{1}{2} * I_{s\_pk\_max\_FB} * (1 - D_{min\_QRM\_FB}) = 2.9\ A$$

The maximum secondary AC current is:

$$I_{s\_AC\_max\_FB} = \sqrt{I_{s\_rms\_max\_FB}^2 - I_{s\_DC\_max\_FB}^2} = 2.45\ A$$

### 2.5.1.3 Flyback transformer winding turns

After the primary main inductance is determined and the maximum primary peak current is calculated, the turns of each winding of the flyback transformer can be calculated after the selection of the proper core. In the 100 W reference design, the ERL35 core with an effective area $A_e$ of 103 $mm^2$ is selected. With the assumption of the saturation flux density $B_{sat}$ of 0.3 T, the minimum primary turns to avoid core saturation can be calculated as following:

$$N_{p\_FB} \geq N_{p\_min\_FB} = \frac{L_{p\_FB} * I_{p\_pk\_max\_FB}}{B_{sat} * A_e} \approx 84\ turns$$

The secondary turn's number is calculated as:

$$N_{s\_FB} \geq \frac{N_{p\_FB}}{n} \approx 26\ turns$$

The primary auxiliary winding is separated to two parts. One is the forward winding which provides the power for the controller XDPL8221. This ensures the precision of the primary side regulation. As this winding operates in the forward mode, so the winding voltage is proportional to the bus voltage when the flyback MOSFET turns on and independent from the output voltage. To make sure that the winding voltage is between 12 V and 22 V according to the Vcc voltage range, the turns-ratio of the primary to the primary aux forward winding is:

$$\frac{N_{p\_FB}}{N_{p\_aux\_FWD\_FB}} \approx 32$$

The other winding is used to sense the output voltage and the secondary side current zero-crossing moment from the primary side. As this winding operates in the flyback mode, so the winding voltage is proportional to the output voltage. The turns-ratio of the primary to the primary ZCD winding is:

$$\frac{N_{p\_FB}}{N_{p\_aux\_ZCD\_FB}} \approx 4$$

Another winding, which provides the power for the dimming circuit, is also operated in the forward mode so that the winding voltage is independent from the output voltage. To make sure that the winding voltage is between 12 V and 22 V, the turns-ratio of the primary to the secondary aux forward winding is:

$$\frac{N_{p\_FB}}{N_{s\_aux\_FWD\_FB}} \approx 32$$

The important parameters of the flyback transformer are summarized in the following table:

**Table 22 Flyback transformer design parameters**

| Parameter | Symbol | Value | Unit |
|---|---|---|---|
| Primary main inductance of the flyback transformer | $L_{p\_FB}$ | 1 | mH |
| Turns-ratio from primary to secondary winding | $N_{p\_FB}/N_{s\_FB}$ | 3.2 | - |
| Turns-ratio from primary to primary aux forward winding | $N_{p\_FB}/N_{p\_aux\_FWD\_FB}$ | 32 | - |
| Turns-ratio from primary to primary ZCD winding | $N_{p\_FB}/N_{p\_ZCD\_FB}$ | 4 | - |
| Turns-ratio from primary to secondary aux forward winding | $N_{p\_FB}/N_{s\_aux\_FWD\_FB}$ | 32 | - |
| Maximum duty cycle | $D_{max\_FB}$ | 0.28 | - |
| Maximum primary peak current | $I_{p\_pk\_max\_FB}$ | 2.37 | A |
| Maximum primary RMS current | $I_{p\_RMS\_max\_FB}$ | 0.65 | A |
| Maximum secondary peak current | $I_{s\_pk\_max\_FB}$ | 7.6 | A |
| Maximum secondary RMS current | $I_{s\_RMS\_max\_FB}$ | 3.85 | A |
| Maximum on-time | $t_{on\_max\_FB}$ | 5.38 | µs |

Based on the above calculated specifications, the flyback transformer can be constructed according to different design requirements like size, power efficiency and temperature etc. by selecting different bobbin and core. In order to avoid core saturation and achieve an optimized core loss, the flux density $B_{max}$ is recommended not to exceed 0.3 T.

In the Infineon 100 W driver reference design, the flyback transformer is constructed by the Würth Electronic under part no. **750317672-Rev00** as a design example. The specification sheet is given as following:

**Table 23 Parameters of Würth inductor 750317672-Rev00**

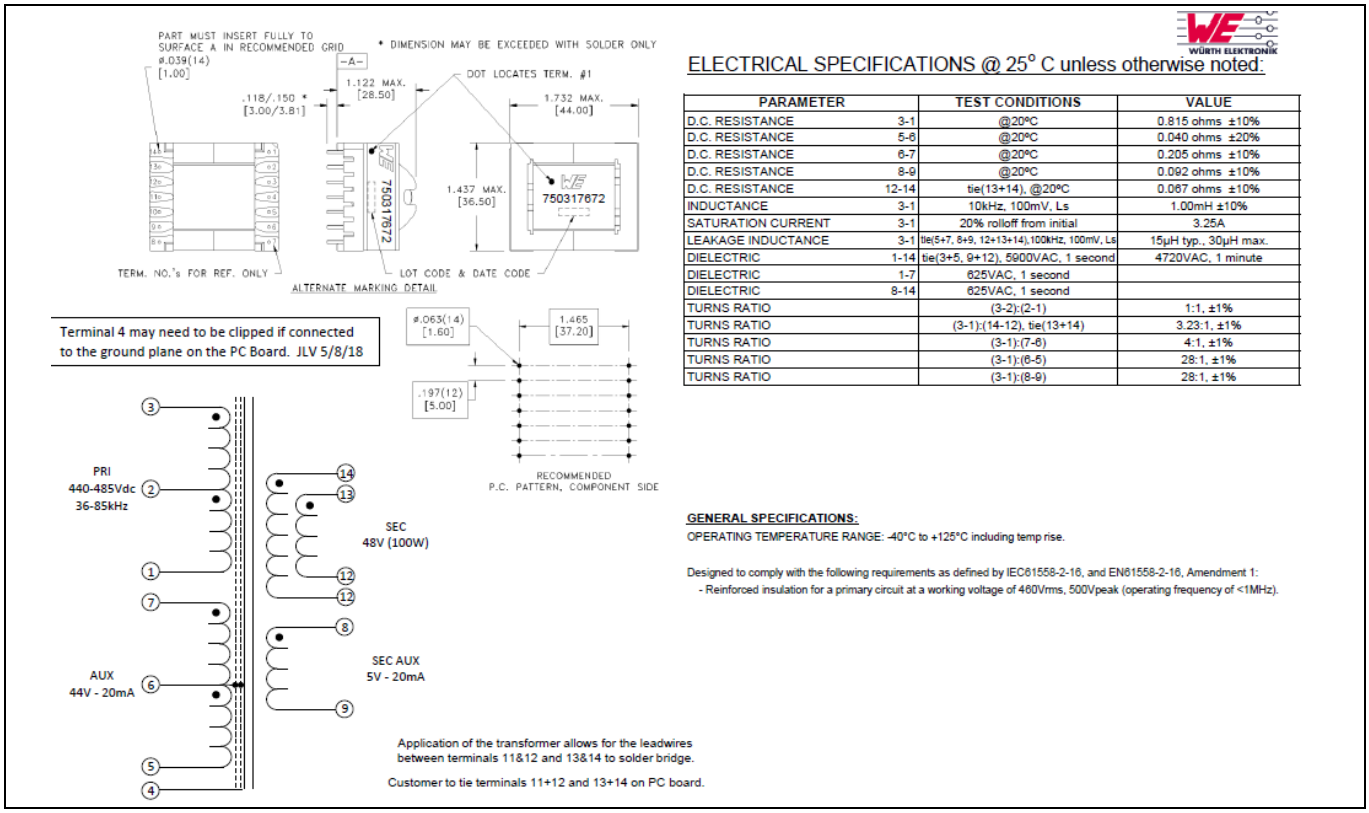
| Parameter | Value | Unit |
|---|---|---|
| Inductance | 1 | mH |
| Bobbin | ERL35 | - |
| Core material | TP4A or DMR44, N87 equivalent | - |
| Turns-ratio from primary to secondary winding | 3.23:1 | - |
| Turns-ratio from primary to primary aux forward winding | 28:1 | - |
| Turns-ratio from primary to primary ZCD winding | 4:1 | - |
| Turns-ratio from primary to secondary aux forward winding | 28:1 | - |
| DC resistance primary winding | 0.815 | Ω |
| DC resistance secondary winding | 0.067 | Ω |
| Cross section of the ERL35 core | 92.7 | $mm^2$ |
| Volume of the ERL35 core | 9548.10 | $mm^3$ |

The maximum primary side DC conduction loss can be calculated as:

$$P_{loss\_p\_FB} = I_{p\_rms\_max\_FB}^2 * R_{DC\_p\_FB} = 0.55\ \text{W}$$

The maximum secondary side DC conduction loss can be calculated as:

$$P_{loss\_s\_FB} = I_{s\_rms\_max\_FB}^2 * R_{DC\_p\_FB} = 1.24\ \text{W}$$




| PARAMETER | | TEST CONDITIONS | VALUE |
|---|---|---|---|
| D.C. RESISTANCE | 3-1 | @20ºC | 0.815 ohms ±10% |
| D.C. RESISTANCE | 5-6 | @20ºC | 0.040 ohms ±20% |
| D.C. RESISTANCE | 6-7 | @20ºC | 0.205 ohms ±10% |
| D.C. RESISTANCE | 8-9 | @20ºC | 0.092 ohms ±10% |
| D.C. RESISTANCE | 12-14 | tie(13+14), @20ºC | 0.067 ohms ±10% |
| INDUCTANCE | 3-1 | 10kHz, 100mV, Ls | 1.00mH ±10% |
| SATURATION CURRENT | 3-1 | 20% rolloff from initial | 3.25A |
| LEAKAGE INDUCTANCE | 3-1 | tie(5+7, 8+9, 12+13+14),100kHz, 100mV, Ls | 15µH typ., 30µH max. |
| DIELECTRIC | 1-14 | tie(3+5, 9+12), 5900VAC, 1 second | 4720VAC, 1 minute |
| DIELECTRIC | 1-7 | 625VAC, 1 second | |
| DIELECTRIC | 8-14 | 625VAC, 1 second | |
| TURNS RATIO | | (3-2):(2-1) | 1:1, ±1% |
| TURNS RATIO | | (3-1):(14-12), tie(13+14) | 3.23:1, ±1% |
| TURNS RATIO | | (3-1):(7-6) | 4:1, ±1% |
| TURNS RATIO | | (3-1):(6-5) | 28:1, ±1% |
| TURNS RATIO | | (3-1):(8-9) | 28:1, ±1% |

**Figure 17 Flyback transformer specification sheet**

The core loss can be looked up in the following figure with the operating frequency and the AC flux density.

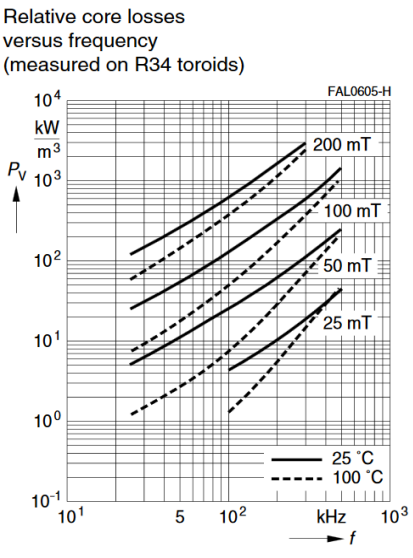



**Figure 18 Relative core losses of the N87 material**

## 2.5.2 Flyback primary power MOSFET

The selection of the flyback primary side power MOSFET is based mainly on the break down voltage and the consideration of the MOSFET power dissipation. As already mentioned in the previous chapter, an 800V MOSFET is used in the reference design. In the QRM+DCM mode flyback converter, the overall MOSFET losses comprise:

- Conduction loss

These losses are frequency independent and do not scale significantly with frequency. It is calculated as following:

$$P_{con\_loss\_MOS\_FB} = I_{p\_RMS\_max}^2 * R_{DS(ON)}$$

Due to the high bus voltage, the primary RMS current is quite low. It is recommended to use a MOSFET with a relative high $R_{DS(on)}$ but smaller $C_{oss}$.

- Turn-on transition loss

As the converter works in the QRM+DCM+ABM mode, the turn-on transition loss caused by the magnetizing current can be ignored because the current rises from zero when a switching cycle starts. But to discharge the parasitic capacitors like $C_{oss}$ and $C_{can}$ through the MOSFET channel can cause significant turn-on transition loss. These losses occur every switching cycle and are thus frequency dependent.

- $E_{oss}$ and $^1/_2 \cdot C_{can} \cdot V^2$ loss

As mentioned above, the energy stored in $C_{oss}$ and $C_{can}$ at the time of turn-on must be dissipated in the MOSFET channel and current sense resistor during the turn-on transition. The energy stored in any capacitor is fundamentally a function of the square of the voltage across it, and thus the $E_{oss}$ and $^1/_2 \cdot C_{can} \cdot V^2$ loss can be very significant during high line conditions. These losses occur every switching cycle and are thus frequency dependent. To simplify the calculation, we assumed that the switching loss is approximately the same as the conduction loss:

$$P_{sw\_loss\_MOS\_FB} = P_{con\_loss\_MOS\_FB}$$

- Gate driver loss

These losses also scale linearly with frequency, but are generally a quite small contribution to the overall losses (at switching frequencies of a few hundred kilohertz and below) and depend almost exclusively on the MOSFET $Q_g$ (total gate-charge). The gate-driver power is typically dissipated in the external gate resistor and gate-driver itself and thus does not need to be considered in the thermal calculation of MOSFET.

In the 100 W driver reference design, the 800 V Infineon MOSFET IPA80R450P7 of the P7 family is used. With the $R_{DS(ON)}$ of 0.45 Ω, the total loss of the MOSFET is calculated as below:

$$P_{loss\_MOS\_FB} = P_{sw\_loss\_MOS\_FB} + P_{con\_loss\_MOS\_FB} = 2 * P_{con\_loss\_MOS\_FB} = 0.36\,W$$

The important parameters for Flyback MOSFET are summarized in the following table:

**Table 24 Flyback MOSFET Design parameters**

| Parameter | Symbol | Value | Unit |
|---|---|---|---|
| Flyback MOSFET break down voltage | $V_{BR\_DSS\_FB}$ | 800 | V |
| Flyback MOSFET on-resistance | $R_{DS(ON)}$ | 450 | mΩ |
| Flyback MOSFET conduction loss | $P_{loss\_MOS\_FB\_con}$ | 0.18 | W |
| Flyback MOSFET switching loss | $P_{loss\_MOS\_FB\_sw}$ | 0.18 | W |

| Parameter | Symbol | Value | Unit |
|---|---|---|---|
| Flyback MOSFET total loss | $P_{loss\_MOS\_FB}$ | 0.36 | W |

## 2.5.3 Flyback MOSFET gate driver

The XDPL8221 flyback gate driver GDFB offers the following advanced features:

- Configurable charge current from 100 to 150 mA for turn-on slope optimization with dpVision tool
- Configurable gate voltage from 4.5 to 15 V

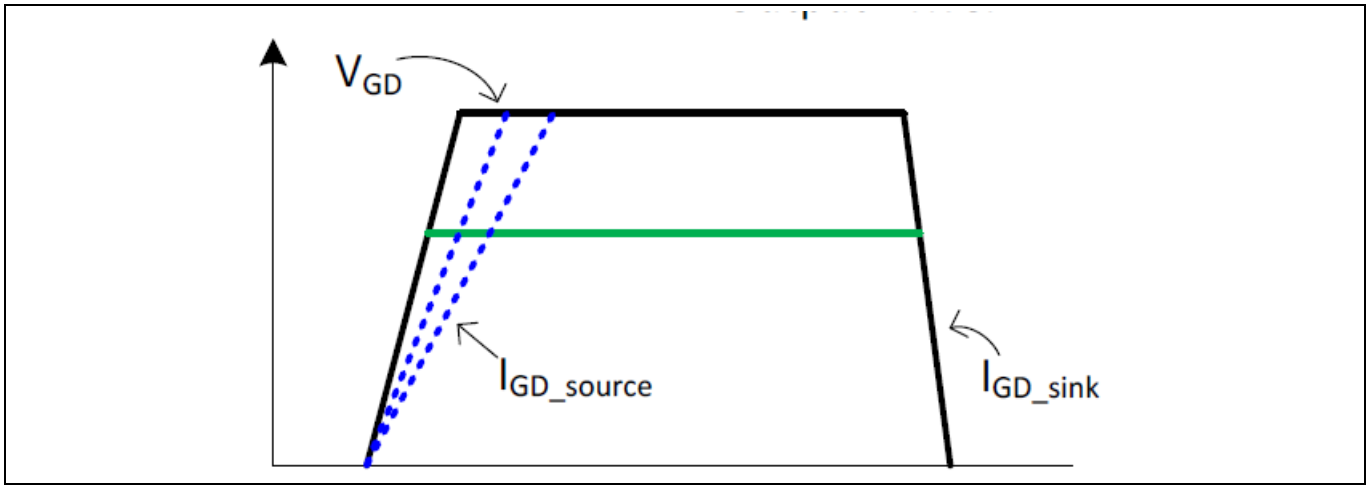



**Figure 19 Configurable gate driver with gate voltage and charge current**

Due to the configurable gate charge current and voltage, the external gate resistor should not be selected too high. A gate resistor of 10Ω should fit for most application cases. The soft turn on for improved EMI result is guaranteed by the configurable constant current gate charging. Following table shows the recommend range of the external gate resistor for a stable gate drive operation of different MOSFET:

**Table 25 Recommended external gate resistor value**

| Parameter | Symbol | Value | | Unit |
|---|---|---|---|---|
| MOSFET Gate capacitance | $C_g$ | 1.0 to 2.0 | | nF |
| MOSFET gate source current | $I_{gs}$ | 100 | | mA |
| MOSFET gate source resistance | $R_{gs}$ | 10 | 100 | kΩ |
| Recommended external gate resistor | $R_g$ | 5 to 20 | 15 to 25 | Ω |

## 2.5.4 Flyback primary snubber

When the flyback power MOSFET is turned off, there is a high voltage spike across the MOSFET drain-source due to the transformer leakage inductance $L_{LK\_FB}$ and the $C_{oss}$ of the MOSFET. This excessive voltage may lead to an avalanche break down and damage the MOSFET. Therefore, it is necessary to use an additional RCD snubber network to clamp the voltage spike in order to protect the power MOSFET.

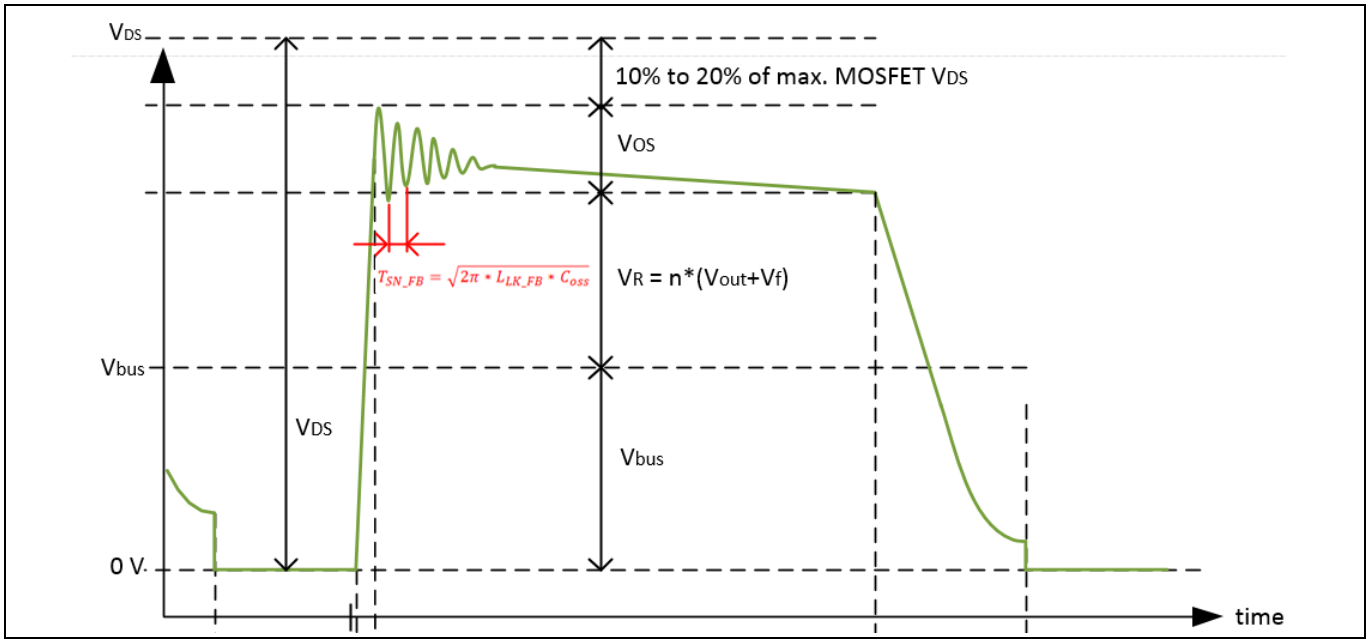



**Figure 20 MOSFET Drain-source voltage and snubber capacitor voltage**

The RCD snubber network limits the high voltage spike turning on the snubber diode once the MOSFET drain voltage exceeds a certain voltage limit and absorbing the current in the leakage inductance by. The voltage over-shoot $V_{os}$ limited by the RCD snubber is related to the power dissipation in the clamping network. Setting the voltage overshoot too low can lead to high power dissipation in the clamping circuit and thus low system power efficiency. For reasonable clamping circuit design, voltage over-shoot $V_{os}$ is typically 1~2 times the reflected output voltage.

It is typical to have a margin of 10~20% of the breakdown voltage for maximum MOSFET voltage stress. The maximum voltage stress of the MOSFET is given as:

$$V_{DS\_stress\_FB} = V_{bus\_OVP1} + V_{R\_max} + V_{OS} < 0.9 * V_{BR\_DSS\_FB}$$

So the voltage overshoot is:

$$V_{OS} < 0.9 * V_{BR\_DSS\_FB} - V_{bus\_OVP1} - V_{R\_max}$$

The peak current of the clamping network is:

$$I_{pk\_sn\_FB} = \sqrt{I_{p\_pk}^2 - \frac{C_{oss} * V_{OS}^2}{L_{LK\_FB}}}$$

The leakage inductance measured with an LCR meter tends to be larger than the actual effective leakage inductance. Moreover, the effective output capacitance of the MOSFET is difficult to measure. The best way to obtain these parameters correctly is to use the drain voltage waveform. Since $L_{LK\_FB}$ can be measured with an LCR meter, thus $C_{OSS}$ can be calculated from the measured resonant period $T_{SN\_FB}$ (as shown in the **Figure 20**) as following:

$$C_{oss} = \frac{T_{SN_{FB}}^2}{2\pi * L_{LK\_FB}}$$

The power dissipation in the clamping circuit is obtained as:

$$P_{loss\_sn\_FB} = \frac{1}{2} * f_{sw\_FB} * L_{leak\_FB} * I_{pk\_sn\_FB}^2 * \frac{V_R + V_{OS\_FB}}{V_{OS\_FB}}$$

Then the clamping circuit resistor is calculated as:

$$R_{sn\_FB} = \frac{(V_R + V_{OS})^2}{P_{loss\_sn\_FB}}$$

In order to reduce the power stress of the snubber resistor, it is recommended to separate the resistor to two parallel connected resistors. The actual drain voltage can be lower than the design due to the loss of stray resistance of inductor and capacitor. The resistor value can be adjusted after the power supply is actually built. The voltage rating of the snubber diode should be higher than the MOSFET drain-source break down voltage. It is strongly recommended to use an ultra-fast diode with 1A current rating for the snubber network. A normal diode with longer reverse recovery time could have unexpected influence on the voltage waveform of the auxiliary winding so that the primary side voltage measurement is wrong. To allow less than 40 V ripple on the clamping capacitor voltage, the clamping capacitor should be calculated as:

$$C_{sn\_FB} \geq \frac{V_R + V_{OS\_FB}}{\Delta V_{sn} * R_{sn\_FB} * f_{sw\_FB}}$$

## 2.5.5 Flyback secondary rectifier diode

The rectifier diode at the secondary side is selected mainly according to the voltage and current ratings. Because the flyback converter works either in QRM or in DCM mode, so there is no reverse recovery requirement of the diode and an ultra-fast is thus not necessary. The maximum reverse voltage of the diode is given as:

$$V_{RRM\_D\_sec} \geq 1.25 * \left(\frac{V_{bus\_OVP2}}{n} + V_{out\_OV}\right) = 235\ V$$

The maximum average forward current of the rectifier diode is given as:

$$I_{F\_D\_sec} \geq 1.5 * I_{s\_RMS\_max} = 3.1\ A$$

The forward voltage of the rectifier diode is directly related to the power efficiency. So the forward voltage should be chosen as small as possible. With an assumption of the forward voltage of 1 V, the maximum conduction loss of the diode is calculated as:

$$P_{loss\_D\_sec} = I_{out\_max} * V_{F\_D\_sec} = 1.5\ \text{W}$$

The important parameters for secondary rectifier diode which used in the 100 W driver reference design are summarized in the following table:

**Table 26 Flyback secondary rectifier diode design parameters**

| Parameter | Symbol | Value | Unit |
|---|---|---|---|
| Maximum reverse voltage | $V_{RRM\_D\_sec}$ | 300 | V |
| Average rectified forward current | $I_{F\_D\_sec}$ | 2x 10 | A |
| Forward voltage | $V_{F\_D\_sec}$ | 0.9 | V |

### 2.5.6 Flyback secondary snubber

When the primary-side MOSFET is turned on, severe voltage oscillation occurs across the secondary-side diode, as shown in **Figure 21**. This is caused by the oscillation between the diode parasitic capacitance $C_{D\_sec\_FB}$ and transformer secondary side leakage inductance $L_{leak\_sec\_FB}$. To reduce the oscillation, an RC snubber is typically used, as shown in the following figure:

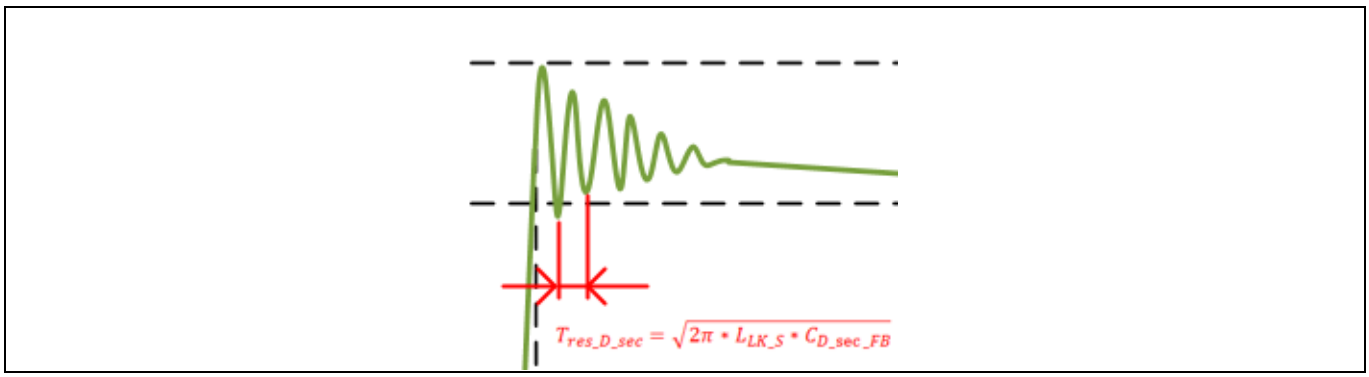



**Figure 21 Secondary rectifier diode voltage waveform**

The secondary side leakage inductance and the diode parasitic capacitance are difficult to measure with an LCR meter. The best way is to use a test capacitor across the diode. First, measure the natural resonance period $T_{res\_D\_sec}$ without to connect anything to the diode. Then, add a test capacitor across the diode $C_{test}$ such that the test resonance period $T_{res\_D\_sec\_test}$ becomes about twice its original value and measure the test resonance period. With the measured $T_{res\_D\_sec}$, $T_{res\_D\_sec\_test}$, and $C_{test}$, the resonance parameters can be calculated as:

$$C_{D\_sec\_FB} = \frac{C_{test}}{\left(\frac{T_{res\_D\_sec\_test}}{T_{res\_D\_sec}}\right)^2 - 1}$$

$$L_{leak\_sec\_FB} = \left(\frac{T_{res\_D\_sec}}{2\pi}\right)^2 * \frac{1}{C_{D\_sec\_FB}}$$

Then the snubber circuit parameters can be calculated as following:

$$R_{sn\_D\_sec} = \sqrt{\frac{L_{leak\_sec\_FB}}{C_{D\_sec\_FB}}}$$

$$C_{sn\_D\_sec} = 2.5 * C_{D\_sec\_FB}$$

If the voltage rating of the secondary rectifier diode is selected high enough to provide enough margins, then the snubber circuit can be saved for a better power efficiency.

### 2.5.7 Flyback secondary output capacitor

Output capacitance will need to be selected carefully in order to meet the LED ripple current. It represents a trade-off between LED ripple current and BOM cost that the designer has to meet. In addition, the capacitor has to be able to handle the ripple current through it. As a rule of thumb, the total output capacitors should be able to handle at least 2.5 times the max LED DC current at max temperature.

The ripple current of the output capacitor is obtained as:

$$\Delta I_{out\_cap} = \sqrt{I_{s\_RMS}^2 - I_{out}^2}$$

The ripple current should be smaller than the ripple current specification of the capacitor. The voltage ripple on the output is given by:

$$\Delta V_{out} = \frac{I_{out} * D_{max}}{C_{out} * f_{sw\_FB}} + \frac{I_{p\_pk\_FB} * V_R * R_{C_{out}}}{V_{out} + V_{F\_D\_sec}}$$

Where $R_{cout}$ is the effective series resistance (ESR) of the output capacitor.

Sometimes it is impossible to meet the ripple specification with a single output capacitor due to the high ESR of the electrolytic capacitor. Then, additional LC filter stages (post filter) can be used. When using the post filters, be careful not to place the corner frequency too low. Too low a corner frequency may make the system unstable or limit the control bandwidth. It is typical to set the corner frequency of the post filter at around 1/10~1/5 of the switching frequency.

## 2.5.8 Flyback zero-crossing detection divider

The digital controller XDPL8221 provides primary side flyback converter control of output current and output voltage. No external feedback components are necessary for the current control as the primary side regulation control loop is fully integrated. This primary side control feature is realized through the ZCD pin of XDPL8221, which has three functions:

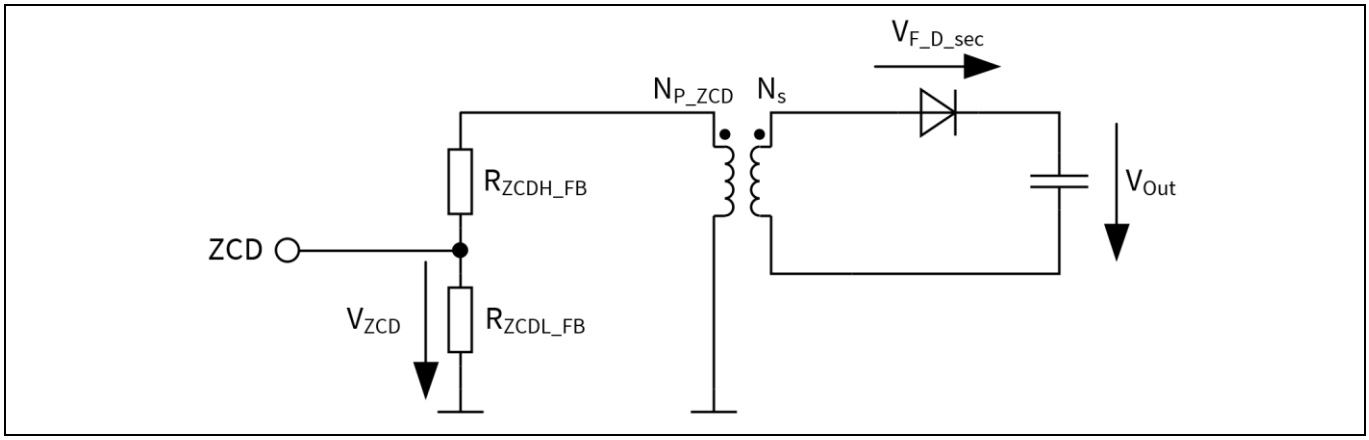



**Figure 22 Flyback zero-crossing detection divider**

- Output voltage measurement:

The output voltage is determined by measuring the reflected output voltage on the auxiliary winding of the flyback transformer. A resistor divider adapts the voltage to the operating range of the ZCD pin. The voltage measured at the ZCD pin is calculated:

$$V_{ZCD} = (V_{out} - V_{F\_D\_sec}) * \frac{N_{p\_ZCD}}{N_s} * \frac{R_{ZCDL\_FB}}{R_{ZCDH\_FB} + R_{ZCDL\_FB}}$$

The measurement range of the ZCD pin is from 0V to 2.66V. To ensure that the maximum bus voltage and output voltage can be measured at the pin, following relation must be fulfilled:

$$R_{ZCDH\_FB} > \frac{V_{bus\_OVP1} * \frac{N_{p\_ZCD}}{N_p} - V_{ZCD\_clamp} * \frac{V_{out\_OV}}{V_{ZCD\_max}} * \frac{N_{p\_ZCD}}{N_s}}{I_{ZCD\_clamp\_max}} = 30\ k\Omega$$

where

- $V_{bus\_OVP1}$ is the bus over voltage protection level 1 threshold

- $V_{out\_OV}$ is the output overvoltage threshold
- $V_{ZCD\_clamp}$ = 0.18 V (refer to the XDPL8221 datasheet)
- $V_{ZCD\_max}$ = 2.66 V is the upper measurement range (refer to the XDPL8221 datasheet)
- $I_{ZCD\_clamp\_max}$ = 3.2 mA (refer to the XDPL8221 datasheet)

In the 100 W driver reference design, $R_{ZCDH\_FB}$ = 68 KΩ is selected to have enough margin and low power loss for a better standby power consumption. Then the lower resistor of the divider should fulfill the following relation:

$$R_{ZCDL\_FB} < \frac{R_{ZCDH\_FB} * V_{ZCD\_max}}{V_{out\_OV} * \frac{N_{p\_ZCD}}{N_s} - V_{ZCD\_max}} = 4.7\ k\Omega$$

$R_{ZCDL\_FB}$ = 3.9 kΩ is selected. To ensure the output voltage measurement accuracy, it is strongly recommended that both resistors should have maximum 1% intolerance or less.

***Attention:*** ***Please note that the demagnetizing time has to be longer than 2.0 µs to ensure that the reflected output voltage can be sensed correctly at the ZCD pin.***

- Bus voltage measurement:

As already described above, the bus voltage is monitored when the flyback MOSFET is turned on. The resistor divider adapts the negative voltage to the operating range of the ZCD pin. This second measurement path is required to protect against component failures in the VS measurement path (open loop protection for the PFC stage).

- Zero-crossing detection:

Zero-crossing detection is to catch the moment, when the transformer is completely demagnetized and the secondary current decreases to zero. This is necessary for QRM and DCM. Meanwhile, it is used to realize the valley switching, which reduces the switching loss of the flyback MOSFET.

In order to filter the noise spike at the ZCD pin so that there is no switching cycle triggered unwanted, it is recommended to use a 100 pF ceramic capacitor directly near the pin. As the capacitance of such ceramic capacitors varies with temperature, a C0G/NP0 ceramic capacitor is more suitable.

*Note:* *The filter capacitor at the ZCD pin is not used to delay the MOSFET turning on to realize the valley switching. This is done in the XDPL8221 internally.*

The important parameters for designing the zero-crossing divider are summarized in the following table:

**Table 27 Zero-crossing detection divider design parameters**

| Parameter | Symbol | Value | Unit |
|---|---|---|---|
| ZCD pin voltage measurement range | $V_{ZCD}$ | 0 ~ 2.66 | V |
| Upper resistor of the ZCD divider | $R_{ZCDH\_FB}$ | 68 | kΩ |
| Lower resistor of the ZCD divider | $R_{ZCDL\_FB}$ | 3.9 | kΩ |
| Filter capacitor at the ZCD pin | $C_{ZCD}$ | 100 | pF |

## 2.5.9 Flyback current sense resistor

As the flyback converter operates in the peak current control mode, the power is transferred from the primary to the secondary side with cycle by cycle current limitation. This peak current control mode compensates the bus voltage ripple automatically which contributes to the minimization of the secondary current output variation.

The primary peak current is determined by sensing the voltage $V_{CS}$ at the CS pin which is connected via a RC-filter to the current sensing shunt resistor. The output current $I_{out}$ will then be calculated based on the output diode conduction time and the switching period.

The recommended operating voltage range at the CS pin is 0 V to slightly lower than 1.08 V. According to the calculated maximum primary peak current which calculated in the previous chapter, the shunt resistor must follow:

$$R_{cs\_FB} < \frac{1.08}{I_{p\_pk\_\max\_FB}} = 0.46\ \Omega$$

For a lower power consumption, $R_{cs\_FB}$ = 0.33 Ω is selected. To reduce the power stress of the shunt resistor, three parallel connected resistors of 1 Ω are used. For the control accuracy, resistors with tolerance less than 1% must be used. The power dissipation of each resistor is then calculated as:

$$P_{loss\_CS\_FB} = \frac{1}{2} * I_{p\_RMS}^2 * R_{cs\_FB}$$

In order to filter the voltage spike so that the peak current control is not wrongly triggered, there is a leading edge blanking time built inside the controller. Besides, an external filter is recommended as well. In the 100 W driver design, a RC-filter is used with $R_{flt\_CS\_FB}$ = 470 Ω and $C_{flt\_CS\_FB}$ = 330 pF. The capacitor should be placed directly near the CS pin.

The important parameters for designing the current sense resistor are summarized in the following table:

**Table 28 Flyback converter current sense design parameters**

| Parameter | Symbol | Value | Unit |
|---|---|---|---|
| Flyback current sense pin voltage measurement range | $V_{cs\_FB}$ | 0 to 1.2 | V |
| Flyback current sense shunt resistor | $R_{cs\_FB}$ | 1 \|\| 1 \|\| 1= 0.33 | Ω |
| Flyback current sense filter resistor | $R_{flt\_CS\_FB}$ | 470 | Ω |
| Flyback current sense filter capacitor | $C_{flt\_CS\_FB}$ | 330 | pF |

## 2.5.10 Flyback operating window

The XDPL8221 includes three different control schemes for a CC (constant current), CV (constant voltage) or LP (limited power) output. Different use cases require the controller to operate according to different operation schemes:

- In the case of typical LED strings, the forward voltage of the LED string determines the output voltage of the driver. XDPL8221 operates in CC and drives a constant output current $I_{out\_full}$ to the load. The forward voltage of the connected LED string has to be below a configurable maximum value $V_{out\_set}$.
- In the case of LED loads including a power stage (e.g. Infineon BCR linear regulators or Infineon DC/DC buck ILD2111, ILD6150, ILD1151), XDPL8221 operates in CV, ensuring a constant voltage $V_{out\_set}$ to the load. The total output current drawn by the load has to be below a configurable maximum value $I_{out\_full}$.
- In the case of a high output current set-point $I_{out\_full}$ and an overly long LED string which exceeds the configurable power limit $P_{out\_set}$, XDPL8221 operates in LP to ensure that the power limit of the driver is not exceeded. The controller reduces the output current automatically, ensuring light output without any interruption even for overly long LED strings. The forward voltage of the connected LED string has to be below a configurable maximum value $V_{out\_set}$.

For every update of the control loop, the control scheme is selected on the basis of the current operation conditions (output voltage $V_{out}$ and output current $I_{out}$) and their distance to the three limiting set-points ($V_{out\_set}$, $P_{out\_set}$ and $I_{out\_full}$):

- For CC schemes, the internal reference current $I_{out\_full}$ is weighted according to thermal management and a dimming curve to yield $I_{out\_set}$. The calculated output current $I_{out}$ is compared with the weighted reference current $I_{out\_set}$ to generate an error signal for the output current.
- For CV schemes, the sensed output voltage $V_{out}$ at the ZCD pin is compared to a reference voltage $V_{out\_set}$ to generate an error signal for the output voltage.
- For LP schemes, the output current is limited to a maximum of $I_{out\_set} = P_{out\_set} / V_{out}$.

Out of these three schemes, for each step the most critical error is selected (see Figure 23):

- If any set-point is exceeded, the largest error for power decrease is selected to bring the controller back to the desired operating point as quickly as possible.
- If the current operating conditions are below all three set-points, the smallest error for power increase is selected to avoid overshooting any set-point.

The selected error signal is fed into a compensator to control the gate driver switching parameters (i.e. duty-cycle and frequency) for the power MOSFET of the Flyback converter.

In dimming cases, the output current set-point $I_{out\_set}$ is located between $I_{out\_min}$ and $I_{out\_full}$ and varies according to the sensed PWM duty cycle $D_{DIM}$. Dimming can be visualized by moving the vertical line for the output current set-point in Figure 23 from right to left.

*Note: An operation in limited power mode can cause dimmer dead-travel until the controller enters constant current mode.*

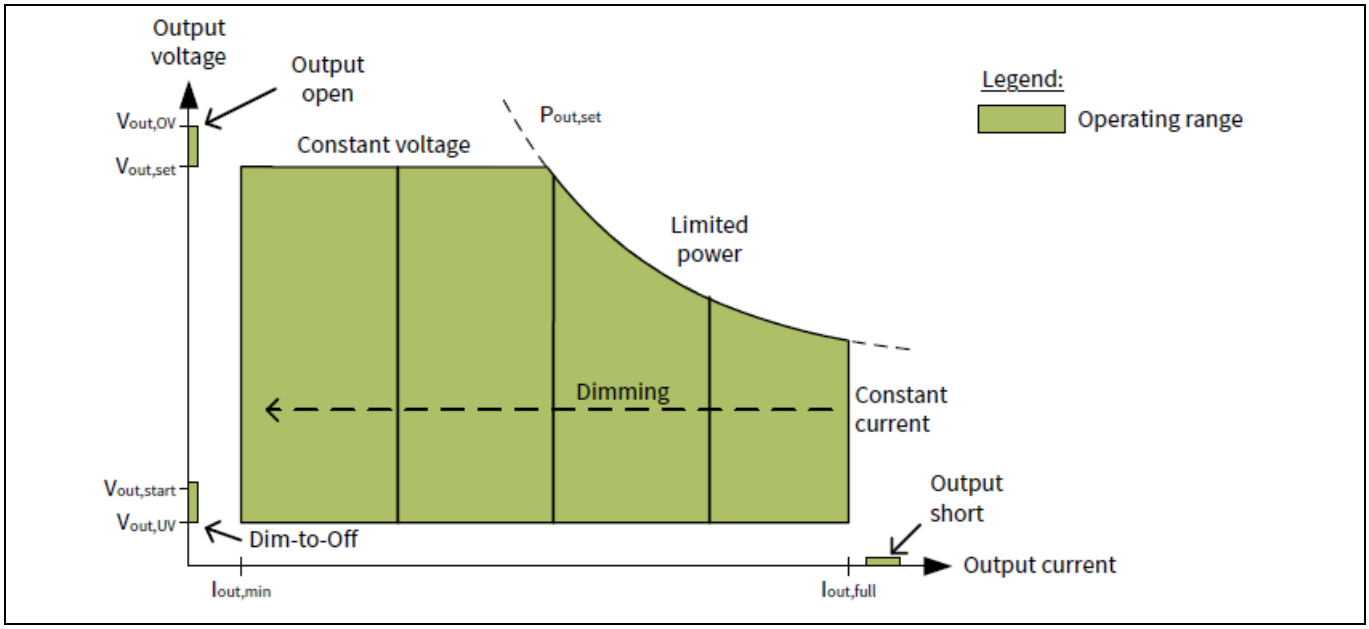



**Figure 23 Flyback operating window**

***Attention: One or more of the output control schemes can be deactivated by configuration of the set-points. Some examples are given below:***

- The LP scheme is not active for $P_{out\_set} > V_{out\_set} * I_{out\_full}$. For such a configuration, the controller will only select between a CC and CV scheme.
- The CV scheme is not active for $V_{out\_set} = V_{out\_OV}$ as the output overvoltage protection will be triggered.
- The CC scheme is not active for $I_{out\_full} = I_{out\_OC}$ as the output overcurrent protection will be triggered.

The important parameters to set up the flyback converter output are summarized in the following table:

**Table 29 Flyback converter operating window design parameters**

| Parameter | Symbol | Value | Unit |
|---|---|---|---|
| Flyback non-dimmed output current | $I_{out\_full}$ | 2500 | mA |
| Flyback output voltage set-point | $V_{out\_set}$ | 50 | V |
| Flyback output power limitation set-point | $P_{out\_set}$ | 100 | W |

## 2.5.11 Flyback multi-mode control

The control loop of XDPL8221 uses three different switching modes as shown in the following **Figure 24**. QRM1 is optimized for high efficiency at heavy loads while DCM and ABM are used in light load and dim-to-off conditions.

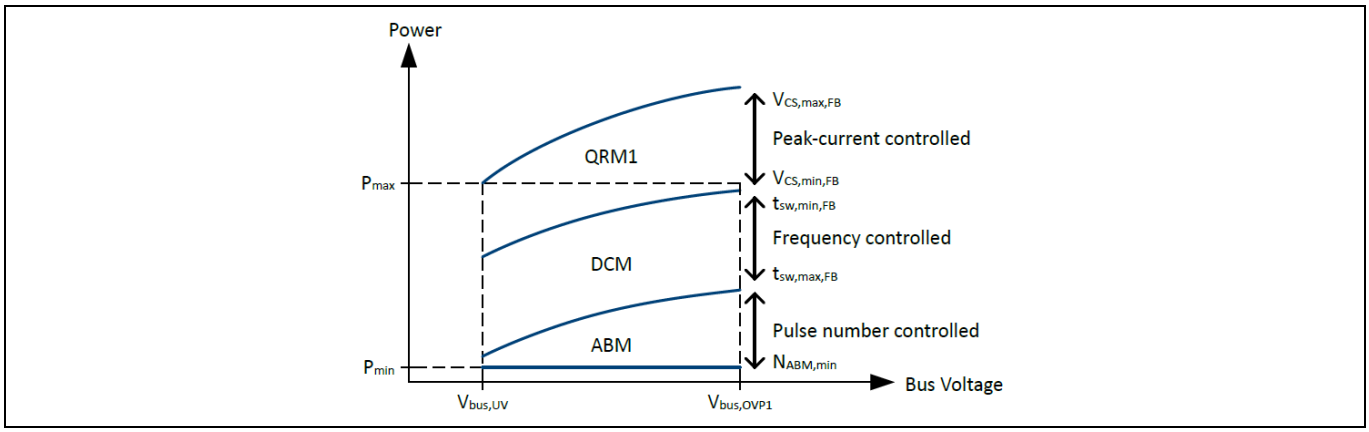



**Figure 24 Flyback multi-mode control**

- QRM1: This mode maximizes the efficiency by switching on the 1st valley of the ZCD signal. This ensures zero current switching with a minimum of switching losses. The power is controlled by regulating the primary peak current as given in the following formula:

$$P_o = \frac{1}{2} * L_{p\_FB} * I_{p\_pk}^2 * f_{sw\_FB}$$

With

$$I_{p\_pk} = \frac{V_{CS\_OCP1}}{R_{CS\_FB}}$$

$$f_{sw\_FB} = \frac{1}{\frac{L_{P\_FB} * V_{CS_{OCP1}}}{R_{CS_{FB}} * V_{bus}} * \left(1 + \frac{N_s}{N_p} * \frac{V_{bus}}{V_{out}}\right) + 0.5 * T_{osc\_FB}}$$

- DCM: This mode is used if the peak current limit reaches its minimum value $V_{CS\_min\_FB}$. To allow lower output power, the controller decreases the switching frequency $f_{sw\_FB}$. Vally switching in the DCM is not guaranteed. The output power is calculated as following:

$$P_o = \frac{1}{2} * L_{p\_FB} * I_{p\_pk\_min}^2 * f_{sw\_FB}$$

With

$$I_{p\_pk\_min} = \frac{V_{CS\_OCP1\_min}}{R_{CS\_FB}}$$

- ABM: This mode is used if $V_{CS\_OCP1}$ cannot be reduced and the switching frequency $f_{sw\_FB}$ cannot be decreased anymore. To reduce power transfer, the controller will enter the active burst mode. The output power is calculated as following:

$$P_o = \frac{1}{2} * L_{p\_FB} * I_{p\_pk\_min}^2 * N_{ABM\_FB} * f_{burst\_FB}$$

The minimum primary peak current $I_{p\_pk\_min}$ is restricted by the minimum demagnetization time $t_{demag\_min}$:

$$I_{p\_pk\_min} = t_{demag\_min} * \frac{N_p}{N_s} * \frac{V_{out\_OV}}{L_{p\_FB}} = 0.34\ A$$

And the mode change from QRM1 to DCM happens if the CS pin voltage:

$$V_{CS\_min\_FB} \le I_{p\_pk\_min} * R_{CS\_FB} = 0.11\ V$$

The minimum power in the DCM is limited by the transformer primary inductance $L_{p\_FB}$, the minimum switching frequency $f_{sw\_min\_FB}$ and the minimum primary peak current $I_{p\_pk\_min}$:

$$P_{o\_min} = \frac{1}{2} * L_{p_{FB}} * I_{p\_pk\_min}^2 * f_{sw\_min\_FB} = 0.92\ W$$

The minimum power in the ABM is limited by the transformer primary inductance $L_{p\_FB}$, the minimum primary peak current $I_{p\_pk\_min}$, the pulses number $N_{ABM\_FB}$ and the burst frequency $f_{burst\_FB}$:

$$P_{o\_min} = \frac{1}{2} * L_{P_{FB}} * I_{p\_pk\_min}^2 * \frac{N_{ABM\_FB}}{t_{burst\_FB}} = 57.8\ mW$$

The important parameters to set up the flyback converter multi-mode control scheme are summarized in the following table:

**Table 30 Flyback converter multi-mode set-up design parameters**

| Parameter | Symbol | Value | Unit |
|---|---|---|---|
| Flyback minimum primary peak current | $I_{p\_pk\_min}$ | 0.15 | A |
| Minimum demagnetization time | $t_{demag\_min}$ | 2 | µs |
| Flyback minimum CS voltage for the QR1 and DCM mode change | $V_{CS\_min\_FB}$ | 0.11 | V |
| Flyback minimum output power in the DCM | $P_{o\_min\_DCM}$ | 0.92 | W |
| Flyback minimum output power in the ABM | $P_{o\_min\_ABM}$ | 57.8 | mW |
| Number of pulse in the ABM | $N_{ABM\_FB}$ | 5 | - |
| Burst frequency in the ABM | $f_{burst\_FB}$ | 200 | Hz |

*Note: If the load drops below the minimum load of $P_{o\_min}$, the output voltage will rise up to the output overvoltage threshold $V_{out\_OV}$ and trigger the protection. An auto-restart can be used to keep the output voltage close to $V_{out\_OV}$ until the load increases again.*

## 2.5.12 Flyback start-up control

After the bus voltage reaches the threshold $V_{bus\_start\_FB}$ for the flyback converter to start-up, the controller XDPL8221 initiates a soft-start for the flyback converter to minimize the switching stress for the flyback power MOSFET and secondary rectifier diode.

As shown in the following **Figure 25**, after the start-up check, the flyback converter starts with switching frequency $f_{sw\_start\_FB}$ and the cycle-by-cycle current limit is increased in steps of $V_{CS\_step}$ with a configurable duration $t_{softstart}$ for each step. After the final limit level $V_{CS\_max\_start\_FB}$ has been reached, the output will be charged until the minimum output voltage $V_{out\_start}$ has been reached. At this condition, the Continuous Conduction Mode (CCM) as well as the output under-voltage protections are activated and the control loop takes over.

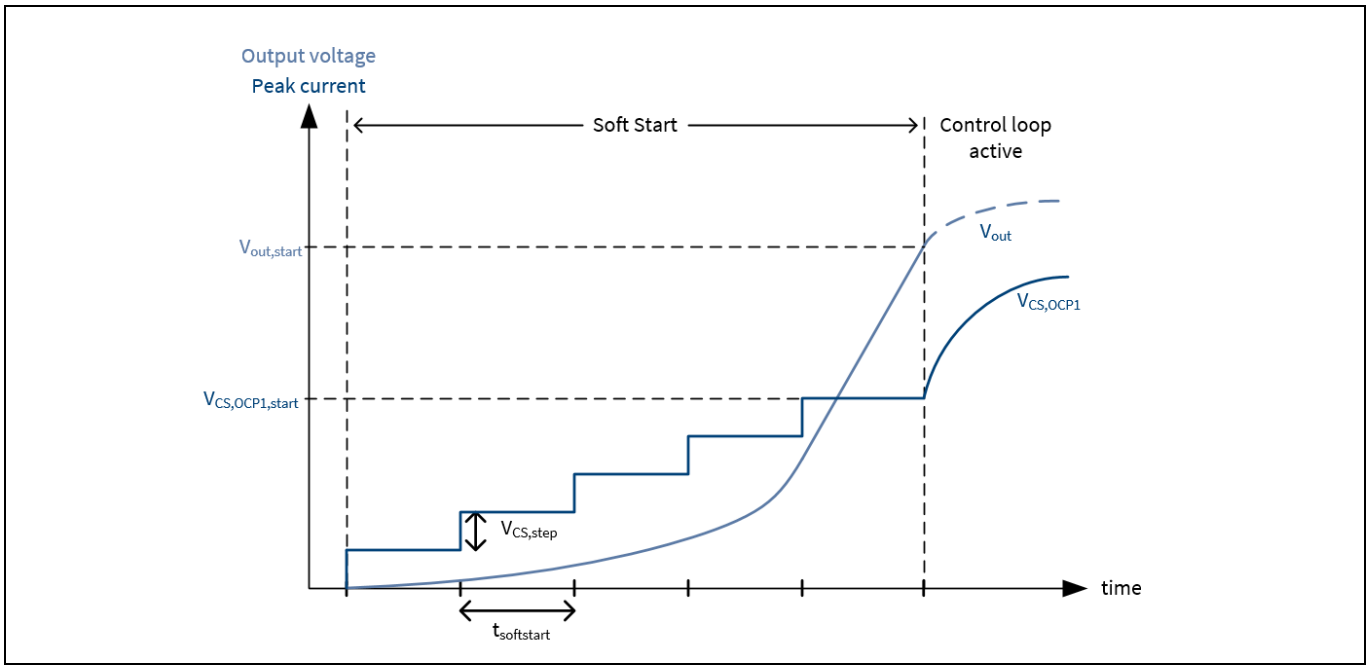



**Figure 25 Flyback start-up control**

- For CC schemes with LED strings at output: after the soft-start is finished, XDPL8221 control loop should take over with ABM and a very lower power transfer. The parameter $ABM_{init}$ should be set in CC and this prevents an incorrect output current before the PWM dimming level is detected. $V_{out\_start}$ should be set lower than the $V_{out\_min}$.
- For CV schemes with DC-DC buck converter at output: $V_{out\_start}$ should be set close to $V_{out\_set}$ so that the soft-start phase is extended to provide enough power for the buck converter power consumption. When the control loop take over after $V_{out\_start}$ is reached, the proper power transfer is required so that there is no output voltage falling back (too low power transfer) and no output voltage over-shoot (too much power transfer). The parameter $ABM_{init}$ should be set in CV.

The important parameters to set up the flyback converter start-up control are summarized in the following table:

**Table 31 Flyback converter multi-mode set-up design parameters**

| Parameter | Symbol | Value | Unit |
|---|---|---|---|
| Bus voltage threshold for the flyback stage start-up | $V_{bus\_start\_FB}$ | 460 | V |
| Flyback soft-start switching frequency | $f_{sw\_start\_FB}$ | 20 | kHz |
| Flyback soft-start peak current limit changing step | $V_{CS\_step}$ | 0.11 | V |
| Flyback peak current limit threshold to end the soft-start phase and enter output charging phase | $V_{CS\_max\_start\_FB}$ | 0.6 | V |
| Flyback soft-start time duration of each step | $t_{softstart}$ | 0.5 | ms |
| Flyback minimum output voltage for CC regulation | $V_{out\_min}$ | 16 | V |

| Parameter | Symbol | Value | Unit |
|---|---|---|---|
| Flyback output voltage threshold for control loop to take over the regulation (for CC regulation with $V_{out\_min}$ = 16 V) | $V_{out\_start}$ | 12.5 | V |
| ABM initialization optimization selection | $ABM_{init}$ | CC (default) | - |

## 2.5.13 Flyback protection features

Protections ensure the operation of the controller under restricted conditions. Protections are triggered if fault conditions are present longer than the blanking time configured for each protection. The controller will react to a triggered protection as configured. The following table defines which protections are enabled or disabled with respect to the state of the stages described in the last chapter:

**Table 32 Flyback Protection States**

| Protection | Stopped | Start-Up | Regulation |
|---|---|---|---|
| Flyback primary over-current level 2 protection | Disabled | Enabled | Enabled |
| Flyback output under-voltage protection at startup | Disabled | Enabled | Disabled |
| Flyback output under-voltage protection during operation | Disabled | Disabled | Enabled |
| Flyback output over-voltage protection | Disabled | Enabled | Enabled |
| Flyback output over-current protection | Disabled | Enabled | Enabled |
| Flyback output over-power protection | Disabled | Enabled | Enabled |
| Flyback CCM protection | Disabled | Disabled | Enabled |
| Flyback soft-start failure | Disabled | Enabled | Disabled |
| Flyback CSFB pin short to GND failure | Enabled | Disabled | Enabled |
| Flyback bus voltage plausibility check failure | Disabled | Enabled | Enabled |
| Flyback missing data failure | Disabled | Disabled | Enabled |

### 2.5.13.1 Flyback primary over-current protection

The primary side overcurrent protection implemented in hardware covers fault conditions like a short in the transformer primary winding or an open CS pin. The primary side current is compared to a configurable overcurrent protection threshold $V_{CS\_OCP2}$. If the threshold is exceeded for longer than the blanking time $t_{blank\_OCP2\_FB}$, the protection will be triggered. The flyback gate driver will be disabled at once by hardware and PFC stage is disabled, too by the firmware. After then, XDPL8221 will enter the auto-restart mode.

The important design parameters for primary over-current protection are summarized in the table below:

**Table 33 Flyback primary over-current protection design parameters**

| Parameter | Symbol | Value | Unit | Configurable |
|---|---|---|---|---|
| Flyback OCP level 2 threshold | $V_{CS\_OCP2}$ | 1.6 | V | No |
| Blanking time for flyback OCP2 | $t_{blank\_CP2\_FB}$ | 250 | ns | No |
| Reaction for flyback OCP2 | - | Auto-Restart | - | Yes |

### 2.5.13.2 Flyback output under-voltage protection

In the case of a short in the output, the output voltage may drop to a very low level. Detection of the under-voltage of the output is realized by measurement using the ZCD pin. The output voltage is compared to a configurable under-voltage protection threshold $V_{out\_UV}$. If the threshold is exceeded for longer than the blanking time $t_{blank\_out\_UV}$, the protection will be triggered. Both PFC and flyback stages are disabled and XDPL8221 will enter auto-restart mode.

Output under-voltage protection is disabled during startup. The startup threshold $V_{out\_start}$ has to be configured higher than the under-voltage threshold to allow undershoots. This occurs especially for resistive loads.

The important design parameters for output under-voltage protection are summarized in the table below:

**Table 34 Flyback Output Under-Voltage Protection Design Parameters**

| Parameter | Symbol | Value | Unit | Configurable |
|---|---|---|---|---|
| Flyback under-voltage protection threshold | $V_{out\_UV}$ | 8 | V | Yes |
| Blanking time for output under-voltage protection | $t_{blank\_out\_UV}$ | 1 | ms | Yes |
| Reaction for output under-voltage protection | - | Auto-Restart | - | Yes |

### 2.5.13.3 Flyback output over-voltage protection

In case of an open output, the output voltage may rise to a high level. The Overvoltage detection of the output is provided by measurement at the ZCD pin. The output voltage is compared to a configurable overvoltage protection threshold $V_{out\_OV}$. If the threshold is exceeded for longer than the blanking time $t_{blank\_out\_OV}$, the protection will be triggered. Both PFC and flyback stages are disabled and XDPL8221 will enter auto-restart mode.

*Note: The blanking time $t_{blank\_Vout\_OV}$ should be set to the minimum value to minimize overshoots of the output voltage above the protection threshold.*

*Note: This protection is usually triggered if the output is open or the output load drops below the minimum load $P_{min}$.*

The important design parameters for output over-voltage protection are summarized in the table below:

**Table 35 Flyback output over-voltage protection design parameters**

| Parameter | Symbol | Value | Unit | Configurable |
|---|---|---|---|---|
| Flyback over-voltage protection threshold | $V_{out\_OV}$ | 53 | V | Yes |
| Blanking time for output over-voltage protection | $t_{blank\_out\_OV}$ | 0.2 | ms | Yes |
| Reaction for output over-voltage protection | - | Auto-Restart | - | Yes |

In addition to the output over-voltage provides by the XDPL8221 from the primary side, there are also two other analog hardware protection features necessary against the output over-voltage:

- To protect the secondary output capacitors, a zener diode with a current limitation resistor will clamp the output voltage under the voltage rating of the output capacitor.
- An active bleeder at the secondary side will discharge the output capacitor continuously if the flyback converter is in the auto-restart or latch mode.

### 2.5.13.4 Flyback output over-current protection

Overcurrent detection in the output current is provided on the basis of the calculated output current. The calculated output current is compared to a configurable overcurrent protection threshold $I_{out\_OC}$. If the threshold is exceeded for longer than the blanking time $t_{blank\_out\_OC}$, the protection will be triggered. Both PFC and flyback stages are disabled and XDPL8221 will enter auto-restart mode.

**Table 36 Flyback output over-current protection design parameters**

| Parameter | Symbol | Value | Unit | Configurable |
|---|---|---|---|---|
| Flyback over-current protection threshold | $I_{out\_OC}$ | 2750 | mA | Yes |
| Blanking time for output over-voltage protection | $t_{blank\_out\_OC}$ | 1 | ms | Yes |
| Reaction for output over-voltage protection | - | Auto-Restart | - | Yes |

### 2.5.13.5 Flyback output over-power protection

Overpower detection of the output power is provided on the basis of the calculated output power. The calculated output power is compared to a configurable overpower protection threshold $P_{out\_OP}$. If the threshold is exceeded for longer than the blanking time $t_{blank\_out\_OP}$, the protection will be triggered. Both PFC and flyback stages are disabled and XDPL8221 will enter auto-restart mode.

**Table 37 Flyback output over-current protection design parameters**

| Parameter | Symbol | Value | Unit | Configurable |
|---|---|---|---|---|
| Flyback over-current protection threshold | $P_{out\_OP}$ | 105 | W | Yes |
| Blanking time for output over-voltage protection | $t_{blank\_out\_OP}$ | 1 | ms | Yes |
| Reaction for output over-voltage protection | - | Auto-Restart | - | Yes |

### 2.5.13.6 Flyback CCM protection

Continuous conduction mode (CCM) operation occurs when the magnetizing current does not decrease to zero before the next switching cycle starts. This happens usually in the soft-start phase or when the output voltage is shorted. However, when the output is over-loaded or bus voltage is too low, the inductor peak current will be very high and the demagnetizing of the flyback transformer cannot be operated completely, too. In the soft-start phase, the CCM operation is allowed for limited time but in other conditions, XDPL8221 must enter the protection mode.

The CCM operation is monitored at the flyback ZCD pin. When the ZCD signal does not come till the maximum switching period time-out happens, it will be treated as a CCM cycle. If the CCM operation happens beyond the blanking time $t_{blank\_CCM\_FB}$, both PFC and flyback stages are disabled and XDPL8221 will enter auto-restart mode.

The important design parameters for flyback CCM protection are summarized in the table below:

**Table 38 Flyback CCM protection design parameters**

| Parameter | Symbol | Value | Unit | Configurable |
|---|---|---|---|---|
| Blanking time for flyback CCM operation | $t_{blank\_CCM\_FB}$ | 1 | ms | Yes |
| Reaction flyback CCM protection | - | Auto-Restart | - | Yes |

### 2.5.13.7 Soft-start failure

When the bus voltage is very low or the output is over-loaded/shorted, the start-up time of the flyback converter is very long. In both cases, the protection is triggered and XDPL8221 will enter the auto-restart mode. The flyback soft-start time is monitored from the moment that the bus voltage reaches threshold to start flyback converter till the secondary output voltage reaches the threshold $V_{out\_start}$. If this time exceeds the defined maximum allowed flyback soft-start time $t_{start\_max\_FB}$, protection will be triggered. Both PFC and flyback stages are disabled and XDPL8221 will enter auto-restart mode.

The important design parameters for flyback soft-start failure are summarized in the table below:

**Table 39 Flyback soft-start failure design parameters**

| Parameter | Symbol | Value | Unit | Configurable |
|---|---|---|---|---|
| Voltage threshold for flyback soft-start end | $V_{out\_start}$ | 12.5 | V | Yes |
| Maximum allowed flyback soft-start time | $t_{start\_max\_FB}$ | 30 | ms | Yes |
| Reaction flyback soft-start failure | - | Auto-Restart | - | Yes |

### 2.5.13.8 Other flyback protections

XDPL8221 includes additional protections to ensure the integrity and correct flow of the firmware.

- A hardware weak pull-up protects against an open CSFB pin. The CSFB OCP2 will be triggered for an open CSFB pin.
- A firmware watchdog protects against the CSFB pin becoming shorted to GND. The protection triggers if the sampled CSFB voltage is less than 97.6 mV for longer than the blanking time of $t_{softstart}$.
- A firmware plausibility check ensures that both bus voltage measurements using the ZCD and VS pins are consistent.
- A firmware watchdog supervises correct data handling of the flyback.

## 2.6 Design the power supply for XDPL8221

The power supply for the controller XDPL8221 is provided by the capacitors connected to the $V_{cc}$ pin. It is strongly recommended to use both electrolytic capacitor and ceramic capacitor parallel connected as $V_{cc}$ capacitors. Due to its high capacitance, electrolytic capacitor is suitable as charge stores but has a bad AC coupling behavior. Ceramic capacitor in the contrary has an excellent AC decoupling effect but has a capacitance derating strongly dependent on voltage and temperature. There are three different way to charge the $V_{cc}$ capacitors for power supply of XDPL8221:

- Start-up Cell

At every cold start, after the AC or DC is applied at input, the $V_{cc}$ capacitors are charged by the start-up cell before the $V_{cc}$ reaches the on-threshold. The start-up cell is connected through the HV pin to the rectified AC or DC input. After the XDPL8221 is active, the start-up cell is switched off. The charging current is dependent on the RMS value of the input voltage. Using AC input as example, the maximum charge current through the start-up cell happens at maximum AC input:

$$I_{HV\_max} = \frac{\sqrt{2} * V_{in\_max\_rms}}{R_{HV}} = 6.52\ mA$$

And the minimum charge current through the start-up cell happens at minimum AC input:

$$I_{HV\_min} = \frac{\sqrt{2} * V_{in\_min\_rms}}{R_{HV}} = 2.83\ mA$$

- PFC auxiliary winding

When the XDPL8221 is active, the start-up cell will be switched off. After the input AC/DC detection, XDPL8221 will start PFC boost converter. The $V_{cc}$ capacitors can be then charged by the PFC auxiliary winding. Due to the slowly increased voltage difference across the PFC boost inductor in the start-up phase, the charging current is very limited at the beginning. It is recommended to use a charge pump together with a linear regulator for the power supply. The linear regulator ensures that the $V_{cc}$ is under the over-voltage threshold and the zener diode can be so selected that later when the flyback converter is active, the PFC auxiliary winding power supply can be disabled.

It is recommended to design the charge pump using PFC auxiliary winding as strong as enough. Because in the flyback soft-start phase or very light load condition, the energy comes from the flyback auxiliary winding is very limited. The bus voltage in those cases will be over set point and thus in the DCM which leads very small on time. To ensure that the voltage of $V_{cc}$ capacitors does not fall below the off threshold, the on time of PFC in the DCM should be chosen correctly.

If an average IC power consumption of 8 mA is assumed and the $V_{cc}$ must be hold higher than the off-threshold for 15ms without any power supply due to the PFC input check, the $V_{cc}$ capacitors must fulfill following requirement:

$$C_{Vcc} > \frac{I_{IC\_avg\_startup}}{V_{Vcc\_on\_min} - V_{Vcc\_off}} * 15\ ms = 9.2\ \mu F$$

- Flyback auxiliary winding

After the bus voltage is boosted to the threshold to start flyback converter, the charging of $V_{cc}$ capacitors should be taken over by the flyback auxiliary winding actually. But as the flyback stage starts with soft-start phase and the power transfer is low before the PWM dimming level is detected, it is strongly recommended to design an sufficient energy puffer from the PFC charge pump so that the Vcc won't drop below the UVLO level. In case of deep dimming condition, bleeders for the bus voltage or at secondary output could help to hold the $V_{cc}$ power supply. The flyback auxiliary winding can be designed either in forward mode or in flyback mode.

**Table 40 Design considerations for the Vcc power supply using flyback auxiliary winding**

| | Forward Mode | Flyback Mode |
|---|---|---|
| Descriptions | $V_{cc}$ capacitors are charged when the primary MOSFET turns on. | $V_{cc}$ capacitors are charged when the primary MOSFET turns off and secondary output capacitors are charged. |
| Advantages | • The winding voltage is only dependent on fixed bus voltage and thus almost constant. No Vcc regulator is required. | • In the dim-to-off condition, the flyback mode auxiliary winding can be used as bleeder which takes over part of the unwanted energy transferred to the secondary output. |

| | Forward Mode | Flyback Mode |
|---|---|---|
| | • The energy transfered in forward mode does not have influence on the accuracy of flyback primary side regulation. | |
| Disadvantages | • In the dim-to-off condition, the forward mode auxiliary winding cannot be used as bleeder which takes over part of the unwanted energy transferred to the secondary output. | • The winding voltage changes according to the forward voltage of LED, which varies due to the different connected LED type or in dimming condition. Therefore a Vcc regulator is required.<br>• The energy transfer to Vcc capacitors in the flyback mode has influence on the accuracy of flyback primary side regulation. |

With the winding turns-ratio $N_p/N_{p\_aux\_FWD}$ of 32:1 and the voltage drop 1 V of the rectifier diode, the $V_{cc}$ voltage is around 15 V. The zener diode of the linear regulator for PFC auxiliary winding power supply should be selected as 12 V so that the PFC power supply is disabled after flyback converter is active.

In the 100 W driver reference design, there are two $V_{cc}$ capacitors of 15.1 µF all together connected parallel directly to the $V_{cc}$ pin: One electrolytic capacitor of 15µF and one ceramic capacitors of 100nF. The ceramic capacitors should be placed directly near the $V_{cc}$ pin. At the start-up, the maximum time to charge these capacitors to the $V_{cc}$ on-threshold is:

$$t_{HV\_charge} = C_{Vcc} * \frac{V_{Vcc\_on\_max}}{I_{HV\_min}} = 117\ ms$$

With a start-up time 50ms of PFC and 30ms start-up time for flyback, the time-to-light can be controlled within 250ms as following calculated:

$$time_{to_{light}} = t_{HV_{charge}} + t_{startup_{PFC}} + t_{startup_{FB}} = 197\ ms$$

The important parameters for designing the power supply for XDPL8221 are summarized in the following table:

**Table 41 Power supply for XDPL8221 design parameters**

| Parameter | Symbol | Value | Unit |
|---|---|---|---|
| Minimum AC input voltage | $V_{in\_AC\_min\_rms}$ | 120 | Vrms |
| Maximum AC input voltage | $V_{in\_AC\_min\_rms}$ | 277 | Vrms |
| Maximum $V_{cc}$ on threshold | $V_{Vcc\_on\_max}$ | 22 | V |
| Minimum $V_{cc}$ on threshold | $V_{Vcc\_on\_min}$ | 20.5 | V |
| $V_{cc}$ off threshold | $V_{Vcc\_off}$ | 6 | V |
| HV current limitation resistor | $R_{HV}$ | 20x3=60 | kΩ |
| $V_{cc}$ capacitor | $C_{Vcc}$ | 15+0.1=15.1 | µF |

## 2.7 Design the bleeder

The bleeder is used to discharge the output capacitors, which has the following meanings:

- The output capacitors need to be discharged if the LED module is disconnected so that when another one with lower forward voltage connected will not get damaged.
- In the case of Dim-to-off, output bleeder helps to keep the output voltage under the LEDs forward voltage so that LED does not light.
- In the case of Dim-to-off, output bleeder works as the load for the flyback instead of LEDs so that the secondary auxiliary winding gets power supply for the dimming circuit.

There are two different bleeders which can be use:

- Passive bleeder

  Resistors can be used as passive bleeder which always discharges the output capacitors. This has the disadvantage of lower power efficiency in the light load and standby mode.
- Active Bleeder

  There are switches which switch on the passive bleeder conditionally is used as active bleeder. The passive bleeder only works if necessary which will lead to better power efficiency in the light load and standby mode.

In the XDPL8221 reference design, two kind of bleeders are designed for difference purposes:

- Passive weak bleeder

  Weak bleeder discharges the all the time in the operation. It will generate a small load even in the very light load condition which can be very important for the XDPL8221 and dimming circuit power supply. This bleeder can also be used if customers wish to have a constant output voltage when the output is open. In this case, a stronger passive bleeder is required and higher power consumption is expected.

  For designing the XDPL8221 in the constant voltage application or constant current application using UART dimming (without requirement of secondary side dimmer power supply), a weak bleeder is enough.
- Active strong bleeder

  Strong bleeder is used in the auto-restart mode or dim-to-off condition. As the power supply for the dimming circuit has to be ensured in the dim-to-off condition, strong bleeder discharges the output so that LED does not light and flyback also transfer energy for the dimming circuit. The bleeder will be controlled only when the flyback switching stops for certain time, which reduce the power consumption in the dim-to-off condition.

The active bleeder consists of three mainly parts: charge pump, two MOSFET switches and discharge resistor. As the schematic shows below in the **Figure 26**, if the flyback converter is in the normal operation, the charge pump will charge the capacitor C106 continuously and the MOSFET Q101 is on and Q100 is off. There is no discharge of the output capacitor. If the flyback converter is in the auto-restart or latch mode, capacitor C106 will be discharged so the MOSFET Q101 is off and Q100 is on. The output capacitor is discharged. The discharge resistors R103 and R104 decides the discharge current and the discharge resistor R105 for capacitor C106 decides how long after the no-switching of the flyback converter the discharge should begin.

The bleeder has a deciding meaning for the system standby power in the dim-to-off as well output open conditions.

- For CC schemes with LED Strings at output: both passive and active bleeders are needed.
- For CV schemes with DC-DC buck converter at output: no bleeder is needed normally.

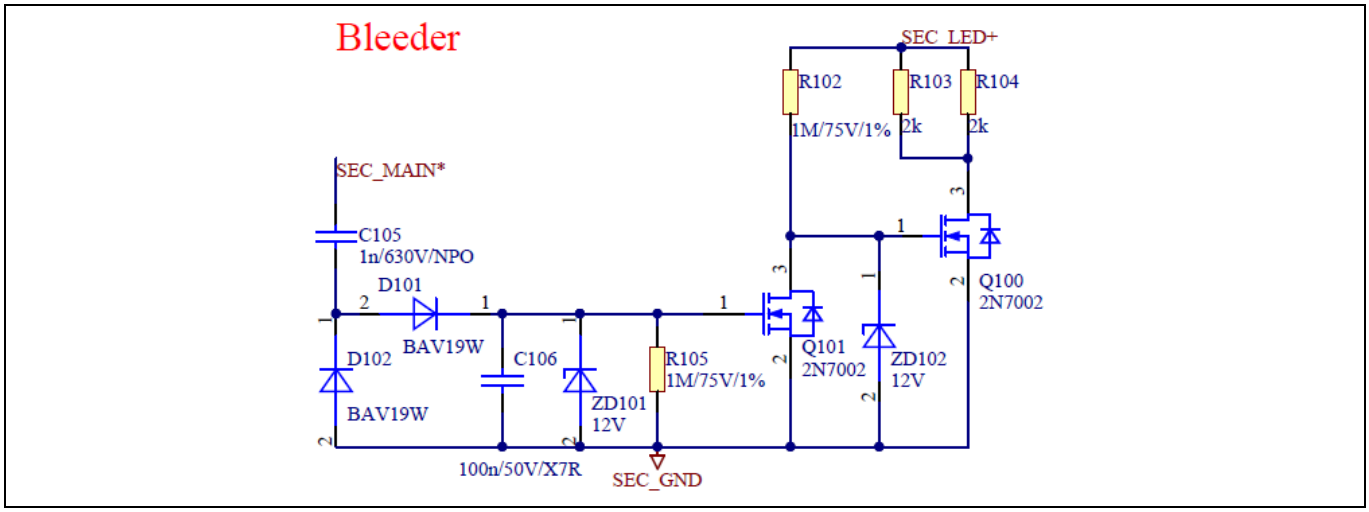



**Figure 26 Active bleeder reference design schematic**

## 2.8 Design the adaptive temperature protection

XDPL8221 offers two kinds of temperature protections:

- Internal over-temperature protection: it initiates a shut-down once the critical temperature level $T_{critical}$ is exceeded. As shown in **Figure 27**, once the internal temperature sensor exceeds $T_{critical}$, XDPL8221 will trigger internal over-temperature protection. If the controller is configured to react with auto-restart, it will only restart after the temperature drops below $T_{start}$.

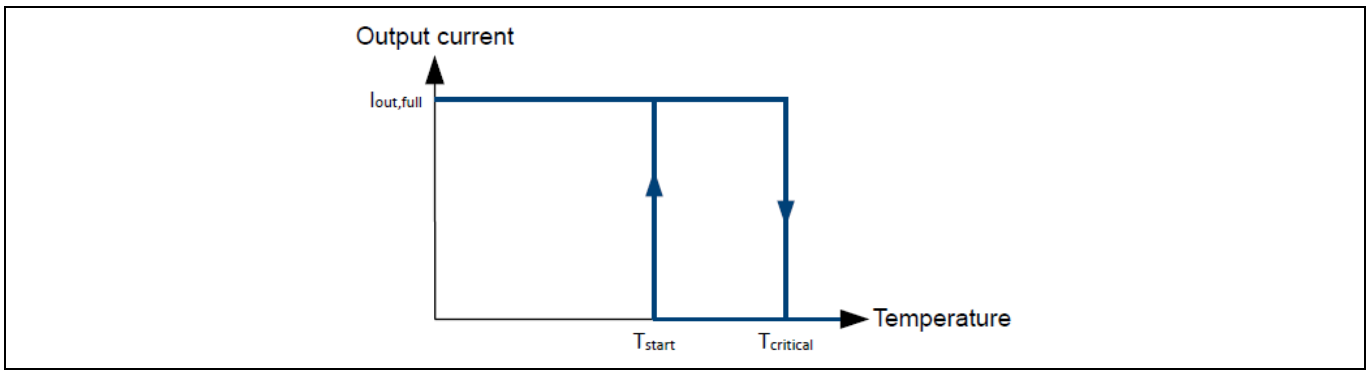



**Figure 27 Internal over-temperature protection**

- External adaptive temperature protection:

XDPL8221 provides adaptive temperature protection using external temperature sensors. This feature reduces the output current according to temperature to protect the load and driver against over-temperature. As long as the resistance of the external connected NTC is lower than the temperature threshold $R_{NTC,hot}$, the current is gradually reduced from the maximum current $I_{out,set}$, as shown in **Figure 28**. If the resistance of the NTC is higher than threshold $R_{NTC,hot}$, the output current is gradually increased again. This allows the controller to ensure operation at or below a temperature matching to $R_{NTC,hot}$.

If a reduction down to a minimum current $I_{out\_red}$ is not able to compensate for any continued increase in temperature, over-temperature protection is triggered when $T_{critical}$ is exceeded and XDPL8221 will enter auto-restart mode. After the temperature decreases to the safe level of $T_{start}$, the system will go back to the normal operation again.

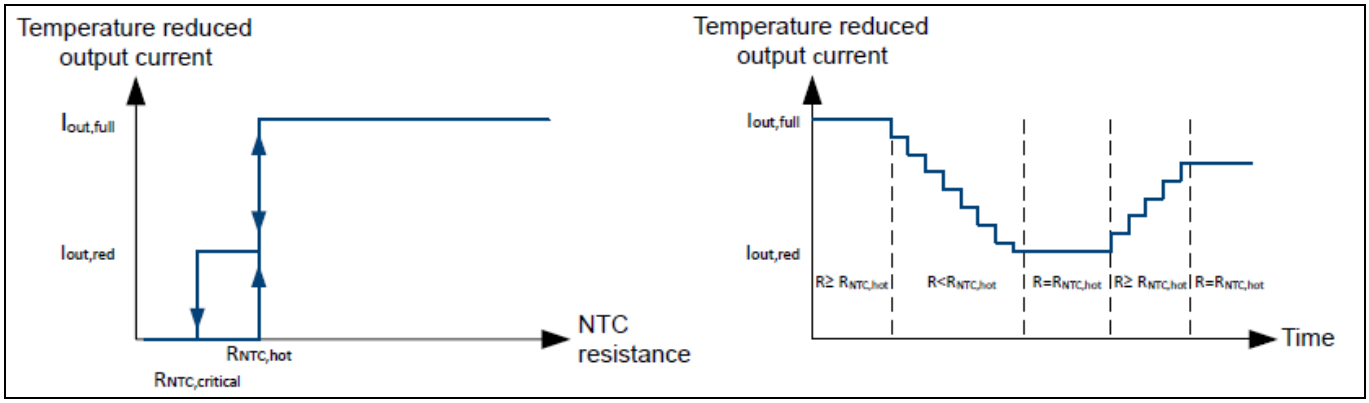



**Figure 28 Adaptive temperature protection**

*Note: Please note that the internal temperature sensor can only protect external components which have sufficient thermal coupling to XDPL8221. The external temperature sensor can be used to protect the temperature of external components (e.g. power MOSFETs or LED engine).*

If an external NTC resistor is connected at the temp pin, the temperature threshold will be converted correspondingly to the NTC resistor value.

The important parameters for designing the adaptive temperature protection for XDPL8221 are summarized in the following table:

**Table 42 Adaptive temperature protection design parameters**

| Parameter | Symbol | Value | Unit |
|---|---|---|---|
| Internal temperature threshold to trigger the internal over-temperature protection | $T_{critical}$ | 110 | °C |
| Internal temperature threshold to activate the adaptive temperature protection | $T_{start}$ | 100 | °C |
| Time step to reduce the output current in the adaptive temperature protection | $t_{step}$ | 2 | s |
| Minimum output current level in the in the adaptive temperature protection | $I_{out\_red}$ | 200 | mA |
| Current step to reduce the output current in the adaptive temperature protection | $I_{out\_step}$ | 5 | mA |
| External NTC resistor value threshold to trigger the external over-temperature protection | $R_{NTC\_critical}$ | 1657 | Ω |
| External NTC resistor value threshold to activate the adaptive temperature protection | $R_{NTC\_hot}$ | 2293 | Ω |
| Reaction internal over-temperature protection | - | Auto-Restart | configurable |
| Reaction external over-temperature protection | - | Auto-Restart | configurable |

## 2.9 Design the dimming interface

There are two dimming interface designed for the XDPL8221: PWM dimming or UART dimming.

- PWM dimming

The analog output current will be regulated continuously according to the duty cycle of the PWM dimming signal.

For PWM dimming, the PWM pin is used to sense the duty cycle of the applied PWM signal to determine the output current level. The XDPL8221 can be configured to use either a linear or a quadratic dimming curve. Either normal or inverted dimming curves can be selected.

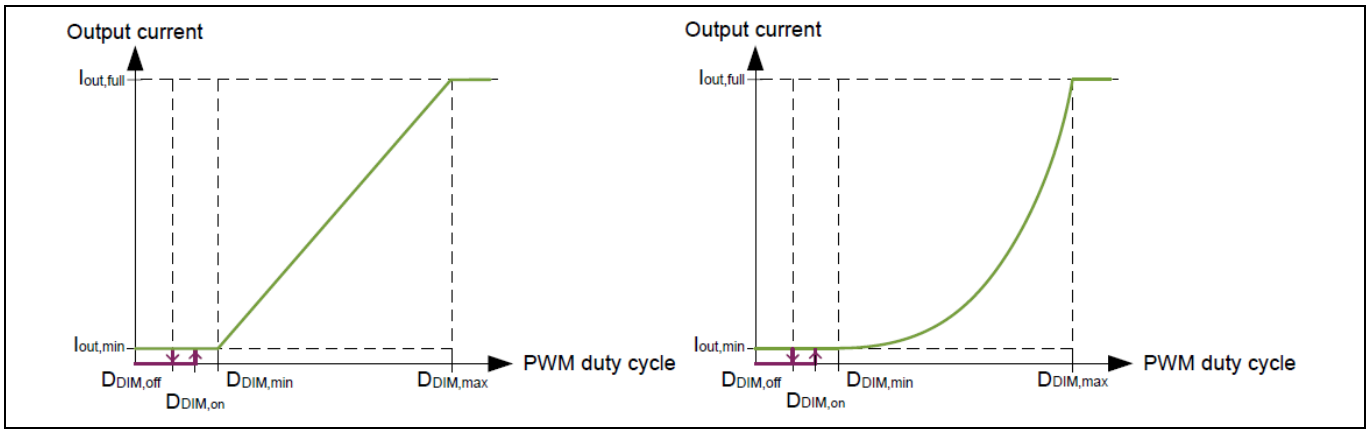



**Figure 29 Configurable dimming curves**

**Figure 29** shows the relationship of the PWM duty cycle to the output current target value. Configurable levels $D_{DIM\_min}$ and $D_{DIM\_max}$ ensure that the minimum current $I_{out\_min}$ and maximum current $I_{out\_full}$ can always be achieved, thereby making the application robust against component tolerances.
Using the optional Dim-to-Off feature, the light output can be stopped without removal of input voltage. In Dim-to-off, the controller will enter auto-restart operation to minimize power consumption. The auto-restart recharges the output voltage to a minimum output voltage of $V_{out\_start}$ to measure the PWM duty cycle. With this feature, the output voltage can be maintained in a specific range by configuration of the startup voltage $V_{out,start}$ and auto-restart time $t_{AR}$, and by dimensioning of an active or passive output bleeder. If $V_{out\_start}$ is configured to be low enough than the minimum forward voltage of the LED string, the LEDs will show no light in this state.

*Note: Either an active or passive output bleeder is required to allow the controller to maintain the output voltage if the Dim-to-Off feature is enabled. Dim-to-Off is entered if the PWM duty cycle exceeds the configurable threshold $D_{DIM,off}$ (see purple line in **Figure 29**). As soon as the duty cycle exceeds $D_{DIM\_on}$, the controller will start to continuously regulate output voltage or output current again.*

- UART dimming

The analog output current will be regulated continuously according to the percentage of the maximum output current which input through the UART command.

*Note: To ensure the correct output current in dimming condition, the right dimming interface must be selected correspondingly in the CSV file and burned as parameter. If the UART dimming is selected, the pin voltage level at PWM pin must match the 100% dimming output current according to the dimming curve direction.*

- Minimum output current

The minimum output current is decided by the minimum output power $P_{o\_min}$ and the output voltage $V_{out}$:

$$I_{out\_min} = \frac{P_{o\_min}}{V_{out}}$$

For both CV and CC schemes, the possible smallest output current happens with the highest output voltage $V_{out\_set}$ = 48 V. For LED strings with lower output voltage, the minimum output current is higher. In order to design 1% dimming for all LED strings output voltage, the minimum output power must be designed according to the lowest output voltage.

The important parameters for designing the dimming interface of XDPL8221 are summarized in the following table:

**Table 43 Dimming interface design parameters**

| Parameter | Symbol | Value | Unit |
|---|---|---|---|
| Dimming type | - | PWM/UART | |
| Dimming curve | - | Linear/Quadratic | - |
| Dimming curve direction | - | Normal/Inverted | - |
| Duty cycle threshold to enter dim-to-off state | $D_{DIM\_off}$ | 5 | % |
| Duty cycle threshold to leave dim-to-off state | $D_{DIM\_on}$ | 7 | % |
| Maximum duty cycle for the full output current | $D_{DIM\_max}$ | 95 | % |
| Minimum duty cycle for the minimum output current | $D_{DIM\_min}$ | 10 | % |
| Minimum output current | $I_{out\_min}$ | 48 | mA |

## 2.10 UART Interface

The digital controller XDPL8221 provides the UART command interface, which allows to control the operation of the LED driver as well as to read out the operating status information from the controller. In case that the communication interface must be isolated, two separated opto-coupler must be used for receiving and transmission as shown in the following **Figure 30**:

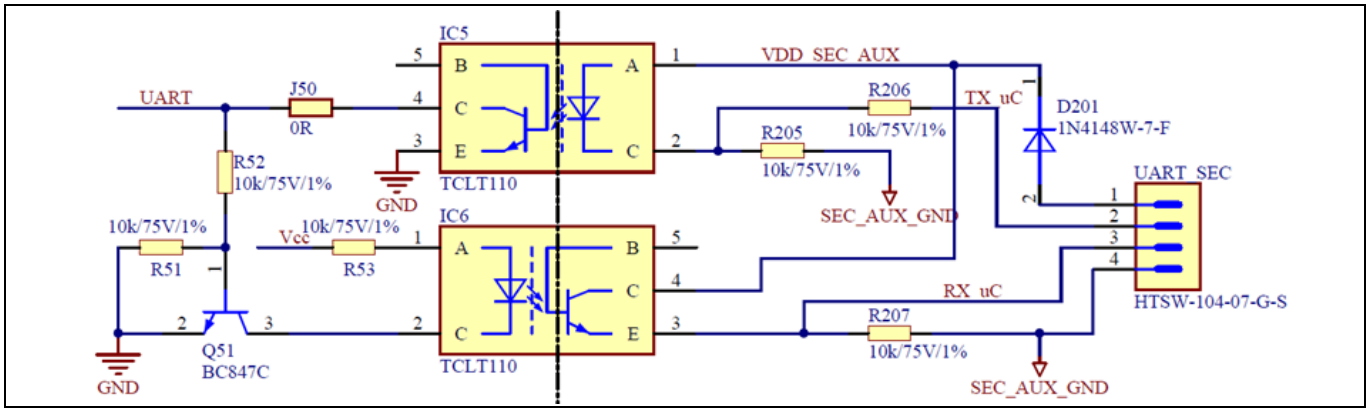



**Figure 30 Isolated UART command interface**

*Note: To ensure an error-free UART communication, a filter capacitor of max 1 nF is recommended.*

The selection of opto-coupler is related to the UART baud rate, as the XDPL8221 has a flexible UART baud rate between 9600 and 57600. Low speed opto-couplers can be used when lower UART baud rate is selected and XDPL8221 is externally power supplied by another DC source. However, expensive high speed opto-coulpers

must be used when XDPL8221 is self supplied. For more design information about XDPL8221 UART interface, please refer the application note “XDPL8221 UART Interface [4]”.

## 2.11 PCB Layout guidelines

Printed Circuit Board (PCB) layout and design are very important for switching power supplies where the voltage and current change with high dv/dt and di/dt. Good PCB layout minimizes excessive EMI and prevents the power supply from being disrupted during surge / ESD tests. AS XDPL8221 combines the PFC boost and flyback in one controller, to prevent the interference of these two stages plays also a very critical role in the PCB layout. The following guidelines are recommended for layout designs:

### 2.11.1 Star connection of grounding

A good grounding of XDPL8221 is proven to minimize the risk of mutual interference among signals:

- The electrolytic PFC bulk cap ground is taken as the system ground reference at primary side. The other power ground of PFC stage, flyback main stage, MOSFET/Diode heatsink and EMI return ground should have separated connections to this system ground reference point in a star structure with preferably thick and short traces.
- The second ground reference is the ground of the XDPL8221 $V_{CC}$ electrolytic capacitor which should be placed close to the IC. The flyback auxiliary winding ground is treated as power ground and should be connected to this second ground reference directly with a preferably thick and short trace.
- The $V_{CC}$ electrolytic capacitor ground should be connected to the PFC bulk cap ground directly with a preferably thick and short trace.
- The ground of the XDPL8221 should be first connected to the $V_{CC}$ ceramic capacitors ground and then to the $V_{CC}$ electrolytic capacitor ground with a preferably short and thick PCB track.
- All ground connections of small signals like CS, ZCD, PWM and UART around the controller XDPL8221 should be connected to the $V_{CC}$ ceramic capacitors ground with preferably short traces in a star structure.

### 2.11.2 Filtering capacitors of XDPL8221

Generally, filtering capacitors are used to suppress the high frequency noises which could cause interference or ground shifting when entering IC controller and will trigger some protections unwanted. These capacitors are usually made from ceramic and must be placed very close to the XDPL8221 and the ground of them must be connected to the IC ground as short as possible.

- $V_{CC}$ pin filter capacitor: 100 nF ceramic capacitor recommended
- PFC VS pin filter capacitor: 1 nF ceramic capacitor recommended
- Flyback ZCD pin filter capacitor: 100 pF ceramic capacitor recommended
- Flyback CS pin filter capacitor: 330 pF ceramic capacitor recommended
- PWM pin filter capacitor: 100 pF ceramic capacitor recommended
- UART pin filter capacitor: maximum 1 nF ceramic capacitor recommended at room temperature, with increased environmental temperature, the value should be decreased.
- TEMP pin filter capacitor: maximum 1 nF ceramic capacitor recommended
- An optional 100 nF high-frequency-and-high-voltage bypass capacitor is recommended to be mounted in parallel with the PFC bulk capacitor, and close to the PFC MOSFET and PFC diode, to suppress EMI.

### 2.11.3 PFC Voltage sense circuit

The design and layout of the PFC voltage sense circuit play a critical role for the PFC boost stage operation, or over-voltage protection could be triggered unwanted by wrong layout. The trace of the sensing divider must be

as short as possible and must be routed as far as possible from the PFC and flyback MOSFET. The filter capacitor of 1 nF is mandatory and must be placed directly at the pin.

### 2.11.4 Minimum current loop

Minimized power and gate current loop areas reduce the radiated EMI noise and interference to the other signal traces.

- The PFC and flyback power current flowing loop area should be minimized as small as possible.
- The gate current of PFC and flyback stage should be minimized as small as possible and if allowed, the gate current should has its own ground trace back to the XDPL8221 ground instead of using the power ground traces.

### 2.11.5 Other layout considerations

- It is suggested that the track to ***HV*** pin shall be kept away from other small signal tracks. The distance is better to be more than 3 mm.
- Keep distance of small signal tracks from MOSFET drain trace of at least 4mm.
- Any PCB track with high current should be designed as short and wide as possible to reduce the parasitic inductance like traces through the MOSFET Drain-Source and shunt resistors.
- The ground traces should be designed as wide as possible and better as area if possible. This helps also increase the immunity to noise.
- The PFC and flyback MOSFET drain tracks should be designed to areas and as large as possible if SMD packages are used. These areas are used as heat sink and spread the heat dissipated by the MOSFETs.
- An ESD protection diode is recommended to be designed for the UART pin as it may be touchable through the programming connector.

# 3 Configuration setup and procedures

As the XDPL8221 is default burned with parameters for 50 W Infineon reference board, users must configure the XDPL8221 with calculated 100 W driver hardware components and other parameters values. This is achieved by entering the hardware configuration and the application's requirements into the .dp Vision tool. Based on this data, the .dp Vision tool will automatically calculate all relevant parameters. The tool allows the user to test the ICs with the parameters and finally to burn the parameters into the ICs.

## 3.1 Design parameters

The parameters are defined with the default values in the CSV file. This is provided by Infineon and available under http://www.infineon.com/cms/en/product/promopages/digital-power to be downloaded. After opening an existing configuration CSV file, it is necessary to enter the appropriate values calculated previously. All available parameters for 100 W driver design are described in the "XDPL8221 100 W CSV File Description **[3]**".

*Note: .dpVision will check the plausibility of the parameters values which are input by the user. If any value violates the limits, the value will turn red and a warning will appear. The limits may also be dependent on other user inputs.*

## 3.2 XDPL8221 Configuration

To configure the parameters of the digital controller XDPL8221, please refer "First Steps with XDPL8221 **[5]**".

# References

[1] XDPL8221 Datasheet

[2] .dp Vision – Basic Mode User Manual

[3] XDPL8221 100 W CSV File Description

[4] XDPL8221 UART Interface

[5] First Steps with XDPL8221

[6] Power Management Selection guide:
http://www.infineon.com/powermanagement-selectionguide

# Revision history

| Document version | Date of release | Description of changes |
|---|---|---|
| 1.1 | 2019-09-28 | Modifed chapter UART communication |
| 1.0 | 2018-10-23 | First release |
| | | |

**Trademarks**
All referenced product or service names and trademarks are the property of their respective owners.

**Edition 2019-09-28**

**Published by**

**Infineon Technologies AG**

**81726 Munich, Germany**



**Do you have a question about this document?**

**Email:** erratum@infineon.com

**Document reference**
**DG_1711_PL39_1712_143020**

**IMPORTANT NOTICE**

The information contained in this application note is given as a hint for the implementation of the product only and shall in no event be regarded as a description or warranty of a certain functionality, condition or quality of the product. Before implementation of the product, the recipient of this application note must verify any function and other technical information given herein in the real application. Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind (including without limitation warranties of non-infringement of intellectual property rights of any third party) with respect to any and all information given in this application note.

The data contained in this document is exclusively intended for technically trained staff. It is the responsibility of customer's technical departments to evaluate the suitability of the product for the intended application and the completeness of the product information given in this document with respect to such application.

For further information on the product, technology delivery terms and conditions and prices please contact your nearest Infineon Technologies office (**www.infineon.com**).

**WARNINGS**

Due to technical requirements products may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies office.

Except as otherwise explicitly approved by Infineon Technologies in a written document signed by authorized representatives of Infineon Technologies, Infineon Technologies' products may not be used in any applications where a failure of the product or any consequences of the use thereof can reasonably be expected to result in personal injury.