# TEC2200-12-074xA

## AC/DC-DC CRPS Front-End Power Supply

TEC2200-12-074xA is a 2200 W Common Redundant Power Supply (CRPS) power supply that converts standard AC mains power or High Voltage DC bus voltages (HVDC) into a main output of 12 VDC for powering systems using distributed power architectures.

The power supply is hot-swappable and supports N+1 redundant architecture. The high-power density helps to improve the overall system efficiency and enhance system reliability. The full digital control facilitates remote set-up, monitoring and control.

TEC2200-12-074xA offers multiple protections including overvoltage, overtemperature, overcurrent, overpower & short circuit protection.

This power supply meets international safety standards and displays the CE-Mark for the European Low Voltage Directive (LVD).

### Key Features & Benefits

- 80 PLUS Titanium Efficiency
- Input Voltage Range 90 – 140 VAC / 180 – 264 VAC; 180 – 300 VDC
- Nominal Output Voltage 12.2 VDC
- Standby Output 12 $V_{SB}$ (2.1 A)
- Output Power up to 2200 W
- Intel Standard CRPS Form Factor
- Dimensions: 185 x 73.5 x 40 mm (7.28 x 2.89 x 1.57 in)
- High Power Density
- UL/CSA 62368-1, EN/IEC 62368-1 Certified
- Supports N+1 Redundancy, SMART_ON Redundancy, Internal ORing
- Black Box Recorder, Bootloader
- Clockwise and Counter-Clockwise Fan Rotation
- Supports Power Management Bus Communication Protocol

### Applications

- Networking Switches
- Servers & Routers
- Telecommunications



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## 1 ORDERING INFORMATION

| TEC | 2200 | - | 12 | - | 074 | x | A |
|---|---|---|---|---|---|---|---|
| **Product Family** | **Power Level** | **Dash** | **V1 Output** | **Dash** | **Width** | **Airflow** | **Input** |
| TEC Front-Ends | 2200 W | | 12 V | | 73.5 mm | N: Normal<br>R: Reverse | A: AC |

## 2 INPUT

| PARAMETER | DESCRIPTION / CONDITION | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Input Voltage Ranges* | Low Voltage AC Range (1000 W) | 90 | 100-127 | 140 | $V_{RMS}$ |
| | Low Voltage Start-up | | 85 ± 5 | | VAC |
| | Low Voltage Power Off | | 75 ± 5 | | VAC |
| | High Voltage AC Range (2200 W) | 180 | 200-240 | 264 | $V_{RMS}$ |
| | High Voltage Start-up | | 175 ± 5 | | |
| | High Voltage Power Off | | 165 ± 5 | | |
| | HVDC (240 V) | 180 | 240 | 300 | VDC |
| | Start-up | | 170 ± 5 | | VDC |
| | Power Off | | 160 ± 5 | | VDC |
| AC Line Inrush Current | | | | 50 | $A_{pk}$ |
| Input Frequency | | 47 | 50/60 | 63 | Hz |
| Power Factor | 230 VAC and 50 Hz, 10% load | 0.90 | | | |
| | 230 VAC and 50 Hz, 20% load | 0.96 | | | |
| | 230 VAC and 50 Hz, 50% load | 0.98 | | | |
| | 230 VAC and 50 Hz, 100% load | 0.99 | | | |
| Current iTHD (Total Harmonic Distortion) | 200 / 240 VAC and 50/60 Hz, ≥ 10% load | | | 20 | % |
| | 200 / 240 VAC and 50/60 Hz, > 20% & < 30 % load | | | 15 | |
| | 200 / 240 VAC and 50/60 Hz, ≥ 30 % load | | | 10 | |
| | 200 / 240 VAC and 50/60 Hz, ≥ 50% load | | | 8 | |
| | 200 / 240 VAC and 50/60 Hz, 100% load | | | 5 | |
| Efficiency | 230 VAC / 60 Hz, 10% load | 90 | | | % |
| | 230 VAC / 60 Hz, 20% load | 94 | | | % |
| | 230 VAC / 60 Hz, 50% load | 96 | | | % |
| | 230 VAC / 60 Hz, 100% load | 93 | | | % |
| Hold-up Time | @ 70% of max. loading | 6 | | | ms |
| $12V_{SB}$ Hold-up Time | @ 100% load | 70 | | | ms |
| AC Line Sag | 0 to 1/2 AC cycle (nom AC voltage ranges, 50/60 Hz)<br>No loss of function or performance. (0%-60%load) | | 95 | | % |
| | > 1 AC cycle (nom AC voltage ranges, 50/60 Hz)<br>Loss of function acceptable, self-recoverable | 30 | | | % |
| AC Line Surge | Continuous (nom AC voltage ranges, 50/60 Hz)<br>No loss of function or performance | | 10 | | % |
| | 0 to 1/2 AC cycle (mid-point of nom VAC ranges, 50/60 Hz)<br>No loss of function or performance | | 30 | | % |
| AC Line Isolation | Primary to secondary; reinforced insulation (IEC 60950) | 3000<br>4242 | | | VAC<br>VDC |

* The Brown IN/OUT Hysteresis min is 5 VAC.

1. Maximum input current at high input voltage range is measured at 200 VAC, at max load 2200 W (16 Arms)
2. AC Brown-in/out loading is 80%load; (low line & high line)



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## 3 OUTPUT

| PARAMETER | DESCRIPTION / CONDITION | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Output Voltage | Output voltage adjusted to 12.2 VDC ± 0.05 VDC @ 50% load | | 12.2 | | VDC |
| Voltage Regulation Limits | ± 6 % | +11.47 | +12.2 | +12.93 | $V_{RMS}$ |
| Max Continuous Output Power | Low line: 1000 W | | | 2200 | W |
| Output Current | @ 110 VAC<br>@ 220 VAC | 0 | | 82<br>178 | A |
| Load Regulation | | | ± 3 | | % |
| Line Regulation | | | ± 1 | | % |
| Overshoot / Undershoot | | | 5 | | % |
| Transient Load * | Δ Step Load Size, 50% of Load Max, 3300 µF | | | 0.5 | A/µs |
| Capacitive Loading | | 3300 | | 20000 | µF |
| Output Ripple & Noise | 10 Hz to 20 MHz BW | | | 150 | mVpp |
| **+12 $V_{SB}$ OUTPUT** | | | | | |
| +12 $V_{SB}$ Output Voltage | | | +12.2 | | $V_{SB}$ |
| Voltage Regulation Limits | ± 5 % | +11.59 | +12.2 | +12.81 | $V_{RMS}$ |
| +12 $V_{SB}$ Output Current | | 0 | | 2.1 | A |
| Load Regulation | | | ± 3 | | % |
| Line Regulation | | | ± 1 | | % |
| Overshoot / Undershoot | | | 5 | | % |
| Transient Load | Δ Step Load Size = 1 A, 1000 µF | | | 0.5 | A/µs |
| Capacitive Loading | | 100 | | 3100 | µF |
| Output Ripple & Noise | 10 Hz to 20 MHz BW | | | 150 | mVpp |

* For dynamic condition +12 V min loading is 1 A

### 3.1 CRPS LOAD REQUIREMENTS

| Output | Input voltage (VAC) | Min. (A) | Max. Continuous (A) | CLST Peak 20 sec duration (A) | Pmax. app Peak 10 msec duration (A) |
|---|---|---|---|---|---|
| 12V main | 200 – 240 | 0.0 | PSU rating (178 A) | Rated + 6 A | Rated + 30 A |
| 12V main | 100 – 127 | 0.0 | PSU rating (82 A) | Rated + 6 A | Rated + 30 A |
| 12Vstby [1] | 100 – 240 | 0.0 | 2.1 | 2.4 | NA |

[1] The length of time 20 sec peak power can be supported, based on thermal sensor and assertion of the SMBAlert# signal. Minimum peak power duration is 20 seconds without asserting the SMBAlert# signal at maximum operating temperature.



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## 3.2 TIMING REQUIREMENTS

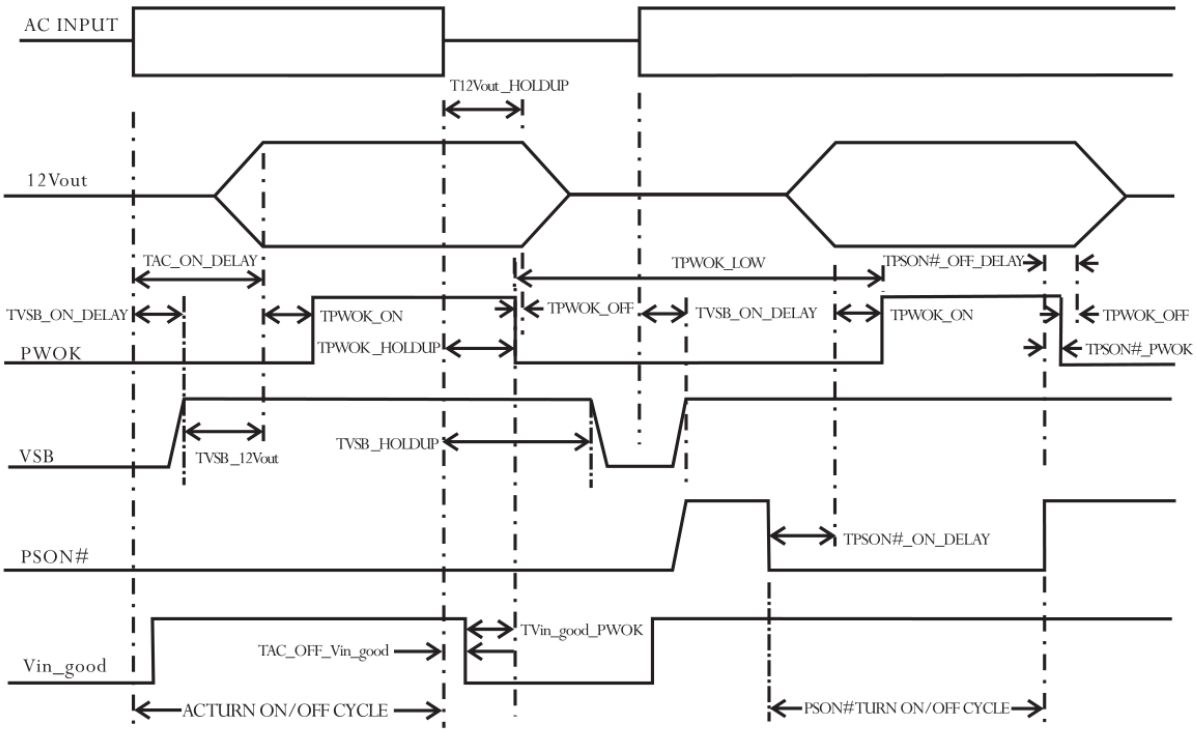


*Figure 1. Signal Timing Sequence*

**Timing Values for Signal Timing Sequence:**

| ITEM | DESCRIPTION | MIN | MAX | UNITS |
|---|---|---|---|---|
| $T_{AC_OFF_Vin_good}$ | The time interval between AC Drop to zero to Vin_good signal gets asserted. | | 4 | ms |
| $T_{Vin_good_PWOK}$ | Vin_good shall be get asserted 1ms prior to PWOK during ac loss event. | 1 | | ms |
| $T_{VSB_RISE}$ | Standby voltage rise time for VSB. | 1 | 25 | ms |
| $T_{VSB_ON_DELAY}$ | Delay from AC being applied to 12VSB being within regulation. | | 1500 | ms |
| $T_{12Vout_RISE}$ | Output voltage rises time for $12V_{OUT.}$ | 1 | 70 | ms |
| $T_{AC_ON_DELAY}$ | Delay from AC being applied to $12V_{OUT}$ output voltage being within regulation. | | 3000 | ms |
| $T_{12Vout_HOLDUP}$ | Time 12VOUT output voltage stays within regulation after loss of AC at 70% load condition. | 6 | | ms |
| $T_{PWOK_HOLDUP}$ | Delay from loss of AC to desertion of PWOK at 70% load condition. | 5 | | ms |
| $T_{PSON\#_ON_DLEAY}$ | Delay from PSON# active to output voltages within regulation limits. | 5 | 400 | ms |
| $T_{PSON\#_PWOK}$ | Delay from PSON# deactivate to PWOK being deserted. | | 5 | ms |
| $T_{PWOK_ON}$ | Delay from output voltages within regulation limits to PWOK asserted at turn on. | 100 | 500 | ms |
| $T_{PWOK_OFF}$ | Delay from PWOK de-asserted to +12V dropping out of regulation limits. | 1 | | ms |
| $T_{PWOK_LOW}$ | Duration of PWOK being in the deserted state during an off/on cycle using AC or the PSON# signal. | 100 | | ms |
| $T_{VSB_12Vout}$ | Delay from 12 VSB being in regulation to O/Ps being in regulation at AC turn on. | 50 | 2000 | ms |
| $T_{VSB_HOLDUP}$ | Time the +12VSB output voltage stays within regulation after loss of AC. | 70 | | ms |



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# 4 PROTECTION

Protection circuits inside the power supply cause only the power supply's main outputs to shutdown. If the power supply latches off due to a protection circuit tripping, an AC cycle OFF for 15 sec and a PSON# cycle HIGH for 1 sec are able to reset the power supply.

## 4.1 OVER CURRENT PROTECTION (OCP)

The power supply shall have current limit to prevent the outputs from exceeding the values shown in table below. If the current limits are exceeded the power supply shall shutdown and latch off. The latch will be cleared by toggling the PSON# signal or by an AC power interruption. The power supply shall not be damaged from repeated power cycling in this condition. 12VSB will be auto-recovered after removing OCP limit.

| | | THRESHOLDS | | TIMING | |
|---|---|---|---|---|---|
| PARAMETER | DESCRIPTION | MIN | MAX | MIN | MAX |
| OCP | Slow over current protection (shutdown and latch after MIN/MAX timing) | Rating + 10 A | Rating + 18 A | 20 ms | 200 ms |
| OCW | Slow over current warning (SMBAlert#) | Rating + 6 A | Rating + 10 A | 10 ms | 15 ms |
| OCPstby | Stby over current protection (shutdown, hiccup mode) | 2.5 A | 4.0 A | 1 ms | 100 ms |

## 4.2 OVER VOLTAGE PROTECTION (OVP)

The power supply over voltage protection will be locally sensed. The power supply will shutdown and latch off after an over voltage condition occurs. This latch will be cleared by toggling the PSON# signal or by an AC power interruption. The values are measured at the output of the power supply's connectors. The voltage should never exceed the maximum levels when measured at the power connectors of the power supply connector during any single point of fail. The voltage should never trip any lower than the minimum levels when measured at the power connector. 12 $V_{SB}$ will be auto-recovered after removing OVP limit.

| PARAMETER | DESCRIPTION / CONDITION | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Over Voltage Protection (OVP) | +12 V Output | 13.3 | 14 | 14.5 | V |
| | +12 $V_{SB}$ Output | 13.3 | 14 | 14.5 | V |

## 4.3 OVER TEMPERATURE PROTECTION (OTP)

The power supply will be protected against over temperature conditions caused by loss of fan cooling or excessive ambient temperature. In an OTP condition the PSU will shutdown. When the power supply temperature drops to within specified limits, the power supply will restore power automatically, while the 12 $V_{SB}$ remains always on. The OTP circuit must have built in margin such that the power supply will not oscillate on and off due to temperature recovering condition. The OTP trip level shall have a minimum of 5°C of ambient temperature margin.

## 4.4 SHORT CIRCUIT PROTECTION (SCP)

The power supply shuts down and latches off for shorting the main outputs. 12 $V_{SB}$ is capable of being shorted indefinitely. The latch will be cleared by toggling the PSON# signal or by an AC power interruption. The power supply should not be damaged from repeated power cycling in this condition. 12 $V_{SB}$ will be auto-recovered after removing SCP limit.

## 4.5 OVER POWER PROTECTION (OPP)

The power supply shall support over power protection (OPP) level low enough to protect the power supply running in this mode for repeated 1msec durations at a 1% duty cycle. The power supply shall be stable operating at any load point from rated power up to the OPP point.

CRPS-185 Load Requirement: OPP Threshold = (Imax + 49 A) +/-50 W
SMBAlert# shall always assert ahead of the OPP threshold being exceeded



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### 4.6 CLOSED LOOP SYSTEM THROTTLING (CLST)

The power supply will always assert the SMBAlert# signal whenever temperature-monitored component in the power supply reaches a warning threshold. Upon reduction of the load within 2msec after the SMBAlert# signal is asserted if the load is reduced to less than the power supply rating; the power supply will continue to operate and not shutdown.

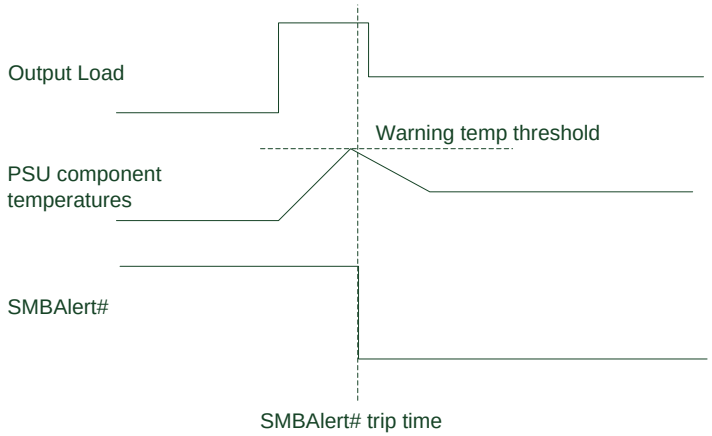


*Figure 2. CLST Timing Requirements*

### 4.7 SMART RIDE-THROUGH (SmaRT)

The power supply will assert the SMBAlert# signal < 4 msec after AC input voltage is lost to 0 VAC.

## 5 CONTROL

The following sections define the input and output signals from the power supply. Signals that can be defined as low true use the following convention: Signal# = low true.

### 5.1 DEVICE ADDRESS LOCATION (B19: A0; B20: A1)

Address Bit 0: A 10 kΩ pull-up resistor pulled to internal +3.3 V in the PSU.
Address Bit 1: A 10 kΩ pull-up resistor pulled to internal +3.3 V in the PSU.

| LOCATIONS | PSU#1 | PSU#2 |
|---|---|---|
| PBD addressA1/A0 | 0/0 | 0/1 |
| Power supply FRU device | A0h | A2h |
| Power supply PSMI device | B0h | B2h |
| Signal type | 10 kohm pull up resistor from +3.3 Vdd device. | |
| A1 or A0 = low | A1 or A0 address bit = 0 | |
| A1 or A0 = high | A1 or A0 address bit = 1 | |
| | MIN | MAX |
| Logic level low voltage | 0 V | 0.4 V |
| Logic level high voltage | 2.4 V | 3.46 V |

### 5.2 I2C BUS (S6: SCL; S5: SDA)

Each module shall provide SCL/SDA bus for EEPROM read/write of system. It's pull up from +3.3Vdd device by a 10K ohm resistor. System should have 1k~2k ohm pull high resistor on the SCL/SDA bus. SCL/SDA pin should be link together and closer. The SCL/SDA bus total capacitance must lower 100pF from system and PDB. The max I2C bus speed is 100 kHz and the mcu of PSU is slave device in I2C bus. The time interval of I2C command is 1ms.



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## 5.3 SMBAlert# INDICATE (Pin A22: SMBAlert#)

This is an active low signal and indicates that the power supply is experiencing a problem that the user should investigate. This shall be asserted due to Critical events or Warning events. The signal shall activate in the case of critical component temperature reached a warning threshold, general failure, over-current, over-voltage, under-voltage, failed fan. This signal may also indicate the power supply is reaching its end of life or is operating in an environment exceeding the specified limits.

This signal is to be asserted in parallel with LED turning solid Amber or blink Amber.

| SIGNAL TYPE (ACTIVE LOW) | OPEN COLLECTOR / DRAIN OUTPUT FROM POWER SUPPLY. PULL-UP TO 3.3 VSB LOCATED IN SYSTEM. | |
|---|---|---|
| Alert# = High | OK | |
| Alert# = Low | Power Alert to system | |
| | MIN | MAX |
| Logic level low voltage, Isink = 4 mA | 0 V | 0.4 V |
| Logic level high voltage, Isink = 50 uA | | 3.46 V |
| Sink current, Alert# = low | | 4 mA |
| Sink current, Alert# = high | | 50 µA |

## 5.4 PSON# INPUT SIGNAL (PIN: A21: PSON#)

The PSON# signal is required to remotely turn on/off the power supply. PSON# is an active low signal that turns on the +12V power rail. When this signal is not pulled low by the system, or left open, the outputs (except the +12VSB) turn off. This signal is pulled to a standby voltage by a pull-up resistor internal to the power supply.

| SIGNAL TYPE | ACCEPTS AN OPEN COLLECTOR/DRAIN INPUT FROM THE SYSTEM. PULL-UP TO 3.3VSB LOCATED IN POWER SUPPLY. | |
|---|---|---|
| PSON# = Low | ON | |
| PSON# = High or Open | OFF | |
| | MIN | MAX |
| Logic level low (power supply ON) | 0 V | 1.0 V |
| Logic level high (power supply OFF) | 2.0 V | 3.46 V |
| Source current, $V_{PSON\#}$ = low | | 4 mA |
| Power off delay: $T_{PSON\#_OFF_DELAY}$ | | 5 ms |
| Power up delay: $T_{PSON\#_ON_DELAY}$ | 5 ms | 400 ms |
| PWOK delay: $T_{PSON\#_PWOK}$ | | 5 ms |

## 5.5 PWOK OUTPUT SIGNAL (PIN A25: PWOK)

PWOK is a power OK signal and will be pulled HIGH by the power supply to indicate that all the outputs are within the regulation limits of the power supply. When any output voltage falls below regulation limits or when AC power has been removed for a sufficiently long time so that power supply operation is no longer guaranteed, PWOK will be de-asserted to a LOW state. See Table: for a representation of the timing characteristics of PWOK. The start of the PWOK delay time shall be inhibited as long as any power supply output is in current limit.

| SIGNAL TYPE | OPEN COLLECTOR/DRAIN OUTPUT FROM POWER SUPPLY. PULL-UP TO 3.3VSB LOCATED IN THE POWER SUPPLY. | |
|---|---|---|
| PWOK = High | Power OK | |
| PWOK = Low | Power Not OK | |
| | MIN | MAX |
| Logic level low voltage, Isink = 400 uA | 0 V | 0.4 V |
| Logic level high voltage, Isource = 200 uA | 2.4 V | 3.46 V |
| Sink current, PWOK = low | | 400 µA |
| Source current, PWOK = high | | 2 mA |
| PWOK delay: Tpwok_on | 100 ms | 500 ms |
| PWOK rise and fall time | | 100 µs |



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## 5.6 SMART_ON CONTROL (PIN B22: ENABLE BY SYSTEM)

Before enabling SMART_ON function, make sure pin B22 (SMART_ON) on output golden finger of each PSU is connected together.

## 5.7 PRESENT# (Pin B24)

This signal is an active low type signal and is connected to the power supply's output ground internally. The mating pin of this signal in system side should have a pull-up resistor which limit the max. current 4mA to go through from this signal pin to the power supply. A Low state on this signal indicates the PSU is physically presents.

## 5.8 Vin_good (Pin B25)

This signal is an output to indicate AC power is existence and is within operation range. It should act from high to low level within 2ms only for Vin drops out to zero and input voltage brown-out events. The 4ms timing is defined as Vin=0 to Vin_Good signal low level.

| SIGNAL TYPE | PULL-UP 2kohm TO INTERNAL 3.3V LOCATED IN POWER SUPPLY. | |
|---|---|---|
| Vin_good = High | Input voltage is in operating range | |
| Vin_good = Low | Input voltage is out of operating range | |
| | MIN | MAX |
| Logic level low, Isink = 4 mA | 0 V | 0.4 V |
| Logic level high, Isource = 50 µA | 2.0 V | 3.46 V |
| Sink current, Vin_good = low | | 4 mA |
| Source current, Vin_good = high | | 50 µA |
| Vin_good rise and fall time | | 400 µs |



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# 6 FRU REQUIREMENTS

## 6.1 OVERVIEW

The Power Management Bus features included in this specification are requirements for AC/DC golden box power supply for use in server systems. This specification is based on the Power Management Bus specifications parts I and II, revision 1.2.

## 6.2 RELATED DOCUMENTS

Power Management Bus Power System Management Protocol Specification Part I – General Requirements, Transport and Electrical Interface; Revision 1.2.

Power Management Bus Power System Management Protocol Specification Part II – Command Language; Revision 1.2. SMBus 2.0.

## 6.3 HARDWARE CONNECTING

The device in the power supply shall be compatible with both SMBus 2.0 'high power' specification for I2C Vdd based power and drive (for Vdd = 3.3 V). This bus shall operate at 3.3 V.
The circuits inside the power supply shall derive their power from the standby output. For redundant power supplies the device(s) shall be powered from the system side of the or'ing device. The Power Management Bus device shall be on whenever AC power is applied to the power supply or a parallel redundant power supply in the system. Only weak pull-up resistors shall be on SCL or SDA inside the power supply. The main pull-up resistors are provided by the system and may be connected to 3.3 Vsb. For the system design, the main pull-ups shall be located external to the power supply and derive their power from the standby rail.

## 6.4 DATA SPEED

The POWER MANAGEMENT BUS device in the power supply shall operate at the full 100 kbps SMBus speed and avoid using clock stretching that can slow down the bus. For example, the power supply can clock stretch while parsing a command or a power supply servicing multiple internal interrupts or NACK may require some use of clock stretching.
The Power Management Bus device shall support SMBus cumulative clock low extend time (Tlow:sext) if < 25msec. This requires the device to extend the clock time no more than 25msec between START and STOP for any given message.

## 6.5 BUS ERROR

The Power Management Bus device shall support SMBus clock-low timeout (Ttimeout). This capability requires the device to abort any transaction and drop off the bus if it detects the clock being held low for >25ms and be able to respond to new transactions 10ms later.
The device must recognize SMBus START and STOP conditions on ANY clock interval. (These are requirements of the SMBus specifications but are often missed in first-time hardware designs.) The device must not hang due to 'runt clocks', 'runt data', or other out-of-spec bus timing. This is defined as signals, logic-level glitches, setup, or hold times that are shorter than the minimums specified by the SMBus specification. The device is not required to operate normally but must return to normal operation once 'in spec' clock and data timing is again received. Note if the device 'misses' a clock from the master due to noise or other bus errors, the device must continue to accept 'in spec' clocks and re-synch with the master on the next START or STOP condition.

## 6.6 FRU DATA FORMAT

For identification of the power supply an internal 256x8 bit EEPROM with Power Management Bus interface is used. The information in the EEPROM follows the IPMI (Platform Management FRU Information Storage Definition) guidelines Document Revision 1.1 from November 15, 1999.



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### 6.7 COMMUNICATION ADDRESS

Four pins will be allocated for the FRU and Power Management Bus information on the Power Supply connector. One pin is the serial clock (SCL). The second pin is used for serial data (SDA). Two pins are for address lines

A0-A1 to indicate to the power supply's EEPROM and MCU. which position the power supply is located in the system. The SCL and SDA signals are pulled up by system, the address lines are also pulled up by system.

| A1 LOGICAL VOLTAGE | A0 LOGICAL VOLTAGE | PSU ADDRESS | FRU ADDRESS |
|---|---|---|---|
| 0 | 0 | 0xB0 | 0xA0 |
| 0 | 1 | 0xB2 | 0xA2 |
| 1 | 0 | 0xB4 | 0xA4 |
| 1 | 1 | 0xB6 | 0xA6 |

## 7 POWER MANAGEMENT BUS

### 7.1 POWER MANAGEMENT BUS COMMAND TABLE

The following table shows mandatory Power Management Bus commands to be supported by the PSU.

| COMMAND CODE | COMMAND NAME | SMBUS TRANSACTION TYPE: | | NUMBER OF DATA BYTES | COMMENT |
|---|---|---|---|---|---|
| | | Writing Data | Reading Data | | |
| 00h | PAGE | Write Byte | Read Byte | 1 | |
| 01h | OPERATION | Write Byte | Read Byte | 1 | 0x80 ON;<br>0x00 OFF<br>Default: 0x80 |
| 02h | ON_OFF_CONFIG | Write Byte | Read Byte | 1 | 0x1D |
| 03h | CLEAR_FAULTS | Send Byte | N/A | 0 | |
| 05h | PAGE_PLUS_WRITE | Block Write | N/A | Variable | |
| 06h | PAGE_PLUS_READ | N/A | Block Write – Block Read | Variable | |
| 19h | CAPABILITY | N/A | Read Byte | 1 | 0xB0 |
| 1Ah | QUERY | N/A | Block Write – Block Read | 1 | |
| 1Bh | SMBALERT_MASK | Write Word | Block Write – Block Read | 2 | |
| 20h | VOUT_MODE | | Read Byte | 1 | 0x17 (n=-9) |
| 21h | VOUT_COMMAND | Write Word | Read Word | 2 | |
| 30h | COEFFICIENTS | N/A | Block Write – Block Read | 5 | Use for Ein/Eout |
| 31h | POUT_MAX | N/A | Read Word | 2 | |
| 3Ah | FAN_CONFIG_1_2 | Write Byte | Read Byte | 1 | Default is Duty |
| 3Bh | FAN_COMMAND_1 | Write Word | Read Word | 2 | |
| 4Ah | IOUT_OC_WARN_LIMIT | | Read Word | 2 | |
| 51h | OT_WARN_LIMIT | | Read Word | 2 | |
| 5Dh | IIN_OC_WARN_LIMIT | | Read Word | 2 | |
| 6Ah | POUT_OP_WARN_LIMIT | | Read Word | 2 | |
| 6Bh | PIN_OP_WARN_LIMIT | | Read Word | 2 | |
| 78h | STATUS_BYTE | Write Byte | Read Byte | 1 | |
| Bit 6 | OFF | | | | |
| Bit 5 | VOUT_OV_FAULT | | | | |
| Bit 4 | IOUT_OC | | | | |
| Bit 3 | VIN_UV | | | | |
| Bit 2 | TEMPERATURE | | | | |
| Bit 1 | CML | | | | |
| Bit 0 | NON OF THE ABOVE | | | | |
| 79h | STATUS_WORD | Write Word | Read Word | 2 | |
| Bit 7(H) | VOUT | | | | |



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| | | | | | |
|---|---|---|---|---|---|
| Bit 6 | IOUT/POUT | | | | |
| Bit 5 | INPUT | | | | |
| Bit 3 | POWER_GOOD# | | | | |
| Bit 2 | FANS | | | | |
| Bit 6(L) | OFF | | | | |
| Bit 5 | VOUT_OV_FAULT | | | | |
| Bit 4 | IOUT_OC_FAULT | | | | |
| Bit 3 | VIN_UV_FAULT | | | | |
| Bit 2 | TEMPERATURE | | | | |
| Bit 1 | CML | | | | |
| Bit 0 | NON OF THE ABOVE | | | | |
| 7Ah | STATUS_VOUT | Write Byte | Read Byte | 1 | |
| Bit 7 | VOUT_OV_FAULT | | | | |
| Bit 4 | VOUT_UV_FAULT | | | | |
| 7Bh | STATUS_IOUT | Write Byte | Read Byte | 1 | |
| Bit 7 | Iout OC fault | | | | |
| Bit 5 | Iout OC warning | | | | |
| Bit 1 | Pout OP fault | | | | |
| Bit 0 | Pout OP warning | | | | |
| 7Ch | STATUS_INPUT | Write Byte | Read Byte | 1 | |
| Bit 5 | Vin UV warning | | | | |
| Bit 4 | Vin UV fault | | | | |
| Bit 3 | Unit off for insufficient input | | | | |
| Bit 1 | Iin over current warning | | | | |
| Bit 0 | Pin over power warning | | | | |
| 7Dh | STATUS_TEMPERATURE | Write Byte | Read Byte | 1 | |
| Bit 7 | OT fault | | | | |
| Bit 6 | OT warning | | | | |
| 7Eh | STATUS_CML | Write Byte | Read Byte | 1 | |
| Bit 7 | Invalid COMMAND | | | | |
| Bit 6 | Invalid DATA | | | | |
| Bit 5 | PEC Failed | | | | |
| 81h | STATUS_FANS_1_2 | Write Byte | Read Byte | 1 | |
| Bit 7 | Fan 1 fault | | | | |
| Bit 5 | Fan 1 warning | | | | |
| Bit 3 | Fan1 speed overridden | | | | |
| 86h | READ_EIN | N/A | Block Read | 6 | DIRECT Data Format |
| 87h | READ_EOUT | N/A | Block Read | 6 | DIRECT Data Format |
| 88h | READ_VIN | N/A | Read Word | 2 | Linear |
| 89h | READ_IIN | N/A | Read Word | 2 | Linear |
| 8Bh | READ_VOUT | N/A | Read Word | 2 | Linear16 |
| 8Ch | READ_IOUT | N/A | Read Word | 2 | Linear |
| 8Dh | READ_TEMPERATURE_1 | N/A | Read Word | 2 | Ambient |
| 8Eh | READ_TEMPERATURE_2 | N/A | Read Word | 2 | SR Hotspot |
| 8Fh | READ_TEMPERATURE_3 | N/A | Read Word | 2 | PFC Hotspot |
| 90h | READ_FAN_SPEED_1 | N/A | Read Word | 2 | In RPM |
| 96h | READ_POUT | N/A | Read Word | 2 | Linear |
| 97h | READ_PIN | N/A | Read Word | 2 | Linear |
| 98h | PMBUS_REVISION | N/A | Read Byte | 1 | 1.2 |
| 99h | MFR_ID | N/A | Block Read | Variable (3) | "bel" |
| 9Ah | MFR_MODEL | N/A | Block Read | Variable (16) | "TEC2200-12-074NA" |
| | | | | | "TEC2200-12-074RA" |
| 9Bh | MFR_REVISION | N/A | Block Read | Variable (3) | "VXX" |



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| | | | | | |
|---|---|---|---|---|---|
| 9Ch | MFR_LOCATION | N/A | Block Read | Variable (8) | "DONGGUAN" |
| 9Dh | MFR_DATE | N/A | Block Read | Variable (8) | "YYYYMMDD" |
| 9Eh | MFR_SERIAL | N/A | Block Read | Variable (19) | Serial Number |
| 9Fh | APP_PROFILE_SUPPORT | N/A | Block Read | Variable (2) | PMBus 1.2 |
| A0h | MFR_VIN_MIN | N/A | Read Word | 2 | 90V |
| A1h | MFR_VIN_MAX | N/A | Read Word | 2 | 264V |
| A2h | MFR_IIN_MAX | N/A | Read Word | 2 | |
| A3h | MFR_PIN_MAX | N/A | Read Word | 2 | |
| A4h | MFR_VOUT_MIN | N/A | Read Word | 2 | 11.47V |
| A5h | MFR_VOUT_MAX | N/A | Read Word | 2 | 12.93V |
| A6h | MFR_IOUT_MAX | N/A | Read Word | 2 | |
| A7h | MFR_POUT_MAX | N/A | Read Word | 2 | |
| A8h | MFR_TAMBIENT_MAX | N/A | Read Word | 2 | |
| A9h | MFR_TAMBIENT_MIN | N/A | Read Word | 2 | |
| AAh | MFR_EFFICIENCY_LL | N/A | Block Read | 14 | At 20%/50%/100% |
| ABh | MFR_EFFICIENCY_HL | N/A | Block Read | 14 | At 20%/50%/100% |
| C0h | MFR_MAX_TEMP_1 | N/A | Read Word | 2 | |
| C1h | MFR_MAX_TEMP_2 | N/A | Read Word | 2 | |
| C2h | MFR_MAX_TEMP_3 | N/A | Read Word | 2 | |
| D0h | MFR_SMART_ON_ REDUNDANCY_CONFIG | Write Byte | Read Byte | 1 | |
| D4h | MFR_HW_COMPATIBILITY | N/A | Read Word | 2 | |
| D5h | MFR_FWUPLOAD_CAPABILITY | N/A | Read Byte | 1 | |
| D6h | MFR_FWUPLOAD_MODE | Write Byte | Read Byte | 1 | |
| D7h | MFR_FWUPLOAD | Block Write | N/A | | |
| D8h | MFR_FWUPLOAD_STATUS | N/A | Read Word | 21 | |
| D9h | MFR_FW_REVISION | N/A | Block Read | 3 | |
| DCh | MFR_BLACK_BOX | N/A | Block Read | 237 | |
| DDh | MFR_REAL_TIME | Block Write | Block Read | 4 | |
| DEh | MFR_SYSTEM_BLACK_BOX | Block Write | Block Read | 40 | |
| DFh | MFR_BLACKBOX_CONFIG | Write Byte | Read Byte | 1 | |
| E0h | MFR_CLEAR_BLACKBOX | Send Byte | N/A | 1 | |

*Table 1. Supported Power Management Bus Command*

**Note:** Write protocol must include PEC (Packet Error Checking).



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## 7.2 STATUS COMMANDS

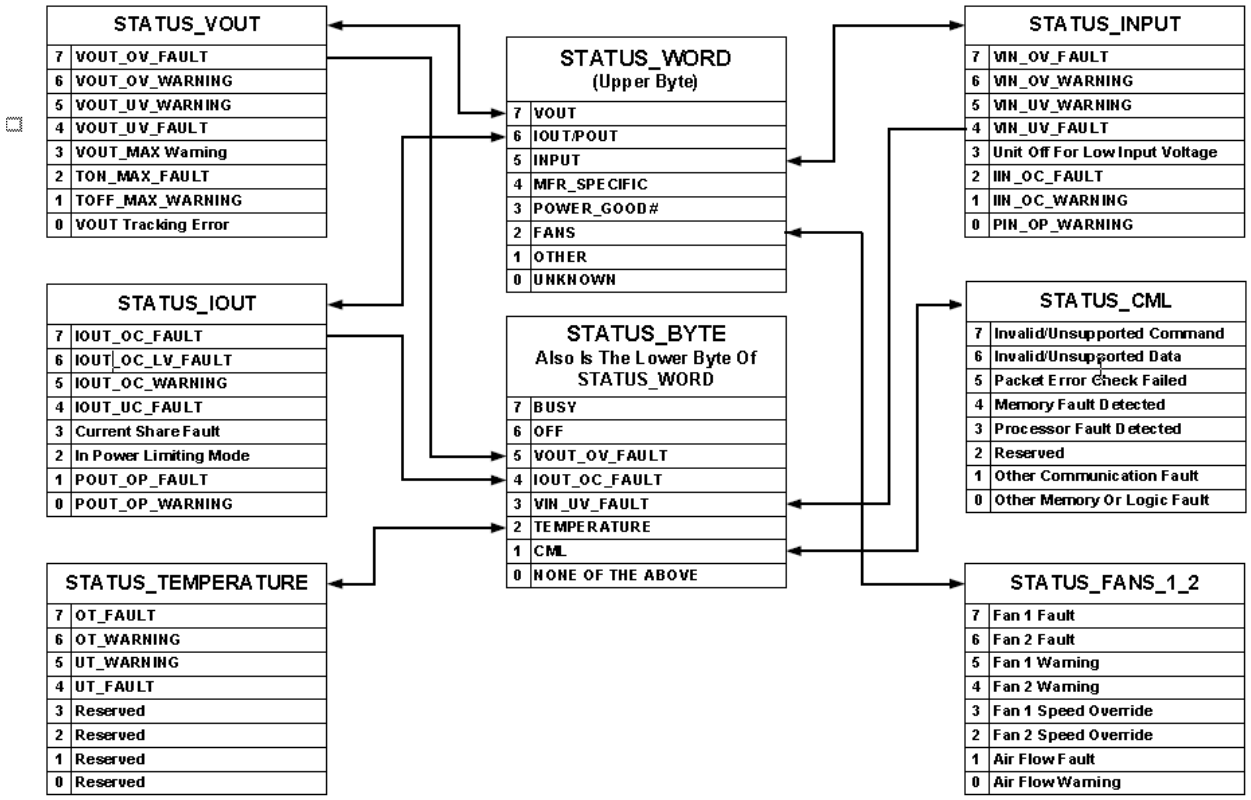


*Figure 3. Summary of The Status Registers*

The following Power Management Bus STATUS commands shall be supported. All STATUS commands stated in Table Supporting PAGE instances shall support the PAGE_PLUS_WRITE and PAGE_PLUS_READ commands since they are used by both the BMC and ME. The BMC and ME refer to the two instances of the commands accessed via the PAGE_PLUS_WRITE and PAGE_ PLUS_READ commands. The status bits shall assert whenever the event driving the status bit is present. Once a bit is asserted it shall stay asserted until cleared

The STATUS commands that are supported with the PAGE_PLUS_READ and PAGE_PLUS_W RITE commands shall still support direct access of the base STATUS_XXX commands using the read word, write word, read byte, and write byte protocols.

STATUS_FAN_1_2 command is only accessed by the system BMC. It uses the standard read byte protocol to read status and write byte protocol to clear bits.

The STATUS events are also used to control the SMBAlert# signal. The new SMBALERT_MASK command is used to define which status event controls the SMBAlert# signal. Default values for these mask bits are shown in the table below.



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| POWER MANAGEMENT BUS COMMAND | BIT LOCATION | PSU STATE WHEN BIT IS ASSERTED ('1') | INSTANCES NO PAGE'ING2 PAGE 00H = BMC PAGE 01H = ME | SMBALERT_MASK DEFAULTS FOR EACH OF THE THREE INSTANCES (NO PAGE, PAGE 00H, PAGE 01H) 0 = CAUSES ASSERTION OF SMBAlert# 1 = DOES NOT CAUSE ASSERTION OF SMBAlert# |
|---|---|---|---|---|
| STATUS_WORD | | | No PAGE, 00h, 01h | |
| OFF | 6 (lower) | OFF | | NA |
| IOUT_OC_FAULT | 4 (lower) | Refer to STATUS_IOUT | | NA |
| VIN_UV_FAULT | 3 (lower) | Refer to STATUS_INPUT | | NA |
| TEMPERATURE | 2 (lower) | Refer to STATUS_TEMPERATURE | | NA |
| CML | 1 (lower) | ON | | NA |
| VOUT | 7 (upper) | Refer to STATUS_VOUT | | NA |
| IOUT/POUT | 6 (upper) | Refer to STATUS_IOUT | | NA |
| INPUT | 5 (upper) | Refer to STATUS_INPUT | | NA |
| FANS | 2 (upper) | Refer to STATUS_FANS | | NA |
| STATUS_VOUT | | | No PAGE'ing | |
| VOUT_OV_FAULT | 7 | OFF | | 1, 1, 1 |
| VOUT_UV_FAULT | 4 | OFF | | 1, 1, 1 |
| STATUS_IOUT | | | No PAGE'ing, 00h,01h | |
| IOUT_OC_FAULT | 7 | OFF | | 1, 1, 1 |
| IOUT_OC_WARNING | 5 | ON | | 1, 1, 0 |
| POUT_OP_FAULT | 1 | OFF | | 1, 1, 1 |
| POUT_OP_WARNING | 0 | ON | | 1, 1, 1 |
| STATUS_INPUT | | | No PAGE'ing, 00h,01h | |
| VIN_UV_WARNING | 5 | ON | | 1, 1, 1 |
| VIN_UV_FAULT | 4 | OFF | | 1, 1, 0 |
| Unit off for low input voltage | 3 | OFF | | 1, 1, 1 |
| IIN_OC_WARNING | 1 | ON | | 1, 1, 1 |
| PIN_OP_WARNING | 0 | ON | | 1, 1, 1 |
| STATUS_TEMPERATURE | | | No PAGE'ing, 00h,01h | |
| OT_FAULT | 7 | OFF | | 1, 1, 1 |
| OT_WARNING | 6 | ON | | 1, 1, 0 |
| STATUS_FANS_1_2 | | | No PAGE'ing | |
| Fan 1 fault | 7 | OFF | | 1, 1, 1 |
| Fan 1 warning | 5 | ON | | 1, 1, 1 |

*Table 2. Power Management Bus STATUS Commands Summary*

1. The Vin Fault bit in STATUS_INPUT shall get asserted if the input power has dropped below the PSU's operating range for any duration of time; even if the PSU continues to operate normally through a momentary input dropout event.
2. 'No PAGE' is the standard STATUS_ commands accessed directly without using the PAGE_PLUS commands.
3. All fans in the PSU shall be OR'ed into a single fan status bit for fault and warning conditions.



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## 7.3 POWER MANAGEMENT BUS TEMPERATURE READ COMMANDS

The following temperature read commands as documented by the Power Management Bus specification Part II version 1.2 should be supported.
READ_TEMPERATURE_1(8Dh), should provide the PSU inlet temperature.
READ_TEMPERATURE_2(8Eh), should provide the temperature of the SR heat sink in the PSU.
READ_TEMPERATURE_3(8Fh), should provide the temperature of the PFC heat sink in the PSU.

## 7.4 PAGE (00h)

Setting a PAGE value of FFh is used to clear all status bits in all PAGEs with the CLEAR_FAULT command.

## 7.5 OPERATION (01h)

The OPERTION command is used to configure the operational state of the converter, in conjunction with input from the CONTROL pin. The OPERATION command is used to turn the Power Management Bus device output on and off.
Bit [7] controls whether the Power Management Bus device output is on or off.
If Bit [7] is cleared (equals 0) then the output is off. If Bit [7] is set (equals 1), then the output is on.

## 7.6 ON_OFF_CONFIG (02h)

The ON_OFF_CONFIG command configures the combination of CONTROL pin input and serial bus commands needed to turn the unit on and off. This includes how the unit responds when power is applied.
The default response for any Power Management Bus device is specified by the device manufacturer. The default value is 0x1D.

X = don't care
HW = turn-on/off by control pin
HI = control pin active high turn-on power
LO = control pin active low turn-on power
SW = turn-on/off by operation command

| SETTING TYPE | BIT 7~5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 | DATA VALUE | DESCRIPTION | SUPPORTED |
|---|---|---|---|---|---|---|---|---|---|
| 1 | 0 | 0 | X | X | X | 1 | 0x01 | If AC ok, turn-on | YES |
| 2 | 0 | 1 | 0 | 1 | 0 | 1 | 0x15 | HW + LO | YES |
| 3 | 0 | 1 | 1 | 0 | X | 1 | 0x19 | SW | YES |
| 4 | 0 | 1 | 1 | 1 | 0 | 1 | 0x1D | HW + LO + SW | YES |

*Table 3. ON_OFF_CONFIG Data Byte*


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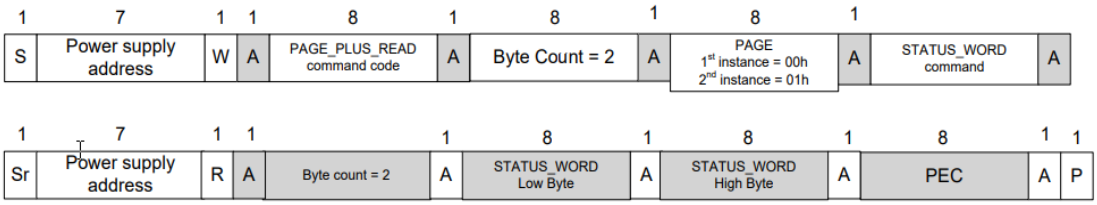
## 7.7 CLEAR_FAULTS COMMAND (03h)

The CLEAR_FAULTS command is used to clear any fault bits that have been set. This command clears all bits in all status registers simultaneously. At the same time, the device negates (clears, releases) its SMBAlert# signal output if the device is asserting the SMBAlert# signal.

## 7.8 PAGE_PLUS_WRITE / PAGE_PLUS_READ COMMANDS (05h/06h)

The new PAGE_PLUS_WRITE and PAGE_PLUS_READ commands are used with the STATUS_WORD, STATUS_INPUT, STATUS_TEMPERATURE, STATUS_IOUT, STATUS_VOUT, and STATUS_CML to create two instances of the same command. Each instance is set by the same events but cleared by their own master in the system. The instances at PAGE 00h are controlled by the system BMC and the instances at PAGE 01h are controlled by the system ME. Below are the protocols used to read and clear the STATUS_ commands using the PAGE_PLUS_WRITE and PAGE_PLUS_READ commands.

Reading STATUS_WORD
Block Write – Block Read Process Call with PEC




Reading STATUS_TEMPERATURE, STATUS_IOUT, STATUS_INPUT, STATUS_CML
Block Write – Block Read Process Call with PEC

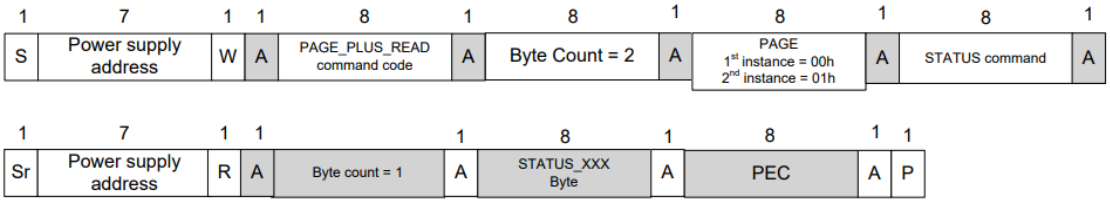



*Figure 4. Reading STATUS commands with PAGE_PLUS_READ*

Clearing STATUS commands (write '1' to clear a bit) STATUS_TEMPERATURE, STATUS_IOUT, STATUS_INPUT, STATUS_CML
Block Write with PEC

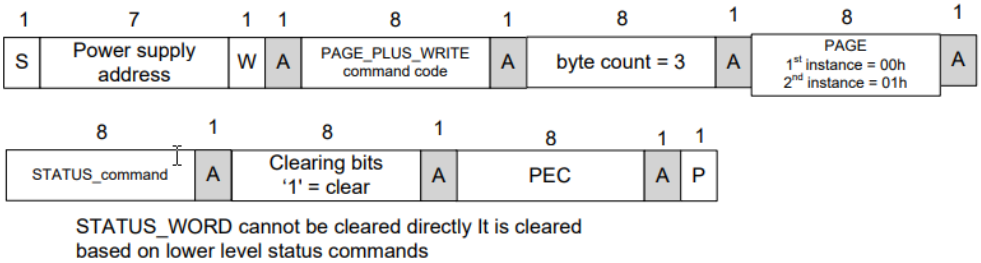



*Figure 5. Clearing STATUS commands using PAGE_PLUS_WRITE*



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## 7.9 CAPABILITY (19h)

This command provides a way for a host system to determine some key capabilities of a Power Management Bus device. There is one data byte formatted as shown in table below. This command is read only.

| BITS | DESCRIPTION | VALUE | MEANING |
|---|---|---|---|
| 7 | Packet Error Checking | 0 | Packet Error Checking not supported |
| | | 1 | Packet Error Checking is supported |
| 6:5 | Maximum Bus Speed | 00 | Maximum supported bus speed is 100 kHz |
| | | 01 | Maximum supported bus speed is 400 kHz |
| | | 10 | Reserved |
| | | 11 | Reserved |
| 4 | SMBAlert# | 0 | The device does not have a SMBAlert# pin and does not support the SMBus Alert Response protocol |
| | | 1 | The device does have a SMBAlert# pin and does support the SMBus Alert Response protocol |
| 3:0 | Reserved | X | Reserved |

*Table 4. CAPABILITY COMMAND Data Byte Format*

## 7.10 QUERY (1Ah)

The QUERY command is used to ask a Power Management Bus device if it supports a given command, and if so, what data formats it supports for that command. This command uses the Block Write-Block Read Process Call described in the SMBus specification.

| BITS | VALUE | MEANING |
|---|---|---|
| 7 | 1 | Command is supported |
| | 0 | Command is not supported |
| 6 | 1 | Command is supported for write |
| | 0 | Command is not supported for write |
| 5 | 1 | Command is supported for read |
| | 0 | Command is not supported for read |
| 4:2 | 000 | Linear Data Format used |
| | 001 | 16 bit signed number |
| | 010 | Reserved |
| | 011 | Direct Mode Format used |
| | 100 | 8 bit unsigned number |
| | 101 | VID Mode Format used |
| | 110 | Manufacturer specific format used |
| | 111 | Command does not return numeric data. This is also used for commands that return blocks of data. |
| 1:0 | XX | Reserved for future use |

*Table 5. QUERY Command Returned Data Byte Format*

If bit [7] is zero, then the rest of the bits are “don’t care”.



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## 7.11 SMBALERT_MASK (1Bh)

This allows the system to mask events from asserting the SMBAlert# signal and to read back this information from the PSU. SMBALERT_MASK command can be used with any of the supported STATUS events. The events are masked from asserting SMBAlert# by writing a '1' to the associated STATUS bits. The SMBALERT_MASK command is used in conjunction with the PAGE_PLUS command and STATUS_ commands. It is not supported for masking the Non-PAGE'd STATUS_ commands. Below are the protocols.

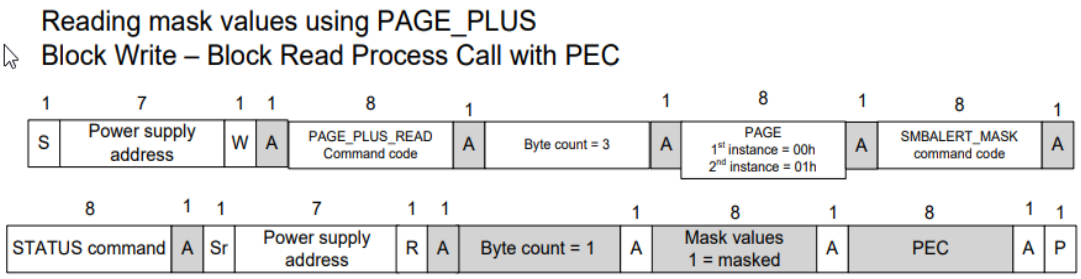


*Figure 6. PAGE_PLUS_READ command.*

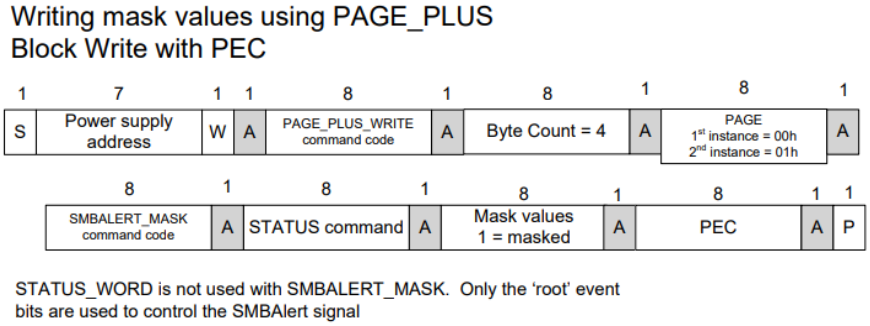


*Figure 7. PAGE_PLUS_WRITE command.*

## 7.12 COEFFICIENT (30h)

The power supply shall support the Power Management Bus COEFFICIENT command. The system shall use this to read the values of m, b, and R used to determine READ_EIN and READ_EOUT accumulated power values.

| COMMAND | COEFFICIENTS SUPPORT | M | B | R |
|---|---|---|---|---|
| READ_EIN | Yes | 01h | 00h | 00h |
| READ_EOUT | Yes | 01h | 00h | 00h |

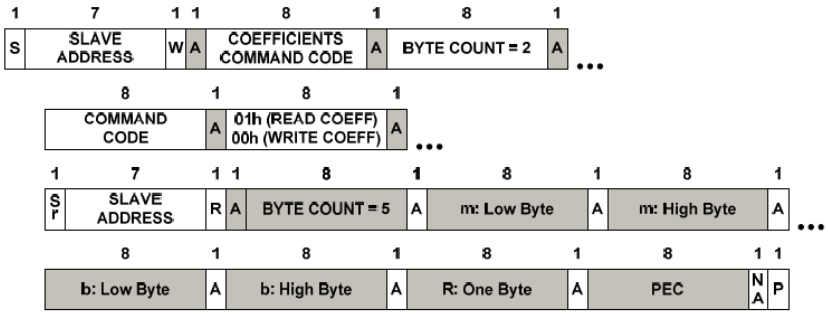


*Figure 8. Retrieving Coefficients Using PEC*



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## 7.13 FAN_CONFIG_1_2 (3Ah)

The FAN_CONFIG_1_2 command is used to define the presence of a fan and the method it is controlled (by duty cycle or RPM).

The first of the configuration tells the Power Management Bus device whether or not a fan associated with position 1 (or 2) is installed. Any combination of fan installation is permitted.

The second part of the configuration tells the device whether the fan speed commands are in RPM or PWM duty cycle (in percent). These settings do not have to be the same for Fan 1 and Fan 2.

The third part of the configuration data tells the Power Management Bus device the number of tachometer pulses per revolution each fan provides. This information is needed for commanding and reporting fan speed in RPM. Two bits are provided for each fan. These settings do not have to be the same for Fan 1 and Fan 2. The binary values of these bits map to pulses per revolution as follows:

- 00b = 1 pulse per revolution,
- 01b = 2 pulses per revolution,
- 10b = 3 pulses per revolution,
- 11b = 4 pulses per revolution.

This command has one data byte formatted as follows:

| BITS | VALUE | MEANING |
|---|---|---|
| 7 | 1 | Fan in position 1 |
| 6 | 0 | Fan 1 commanded in Duty Cycle |
| | 1 | Fan 1 commanded in RPM |
| 5:4 | 00b-11b | Fan 1 Tachometer Pulses Per Revolution |
| 3 | 0 | No fan in position 2 |
| 2 | Not used | |
| 1:0 | Not used | |

*Table 6. FAN_CONFIG_1_2 Command*

## 7.14 FAN_COMMAND_1 (3Bh)

The system may increase the power supplies fan speed through using the FAN_COMMAND_1 command. This command can only increase the power supplies fan speed; it cannot decrease the PSU fan speed below what the PSU minimum speed of the thermal requirement.

The default control mode of fan is duty (0-100).

## 7.15 READ_FAN_SPEED_1 (90h)

The system will read the fan speed by using the READ_FAN_SPEED_1 command. This data shall return the fan speed in the Power Management Bus linear format.

## 7.16 POWER MANAGEMENT BUS_REVISION (98h)

This is a correction to the table in the Power Management Bus part II specification regarding the POWER MANAGEMENT BUS_REVISION command.

| BITS [7:4] | PART I REVISION | BITS [3:0] | PART II REVISION |
|---|---|---|---|
| 0000 | 1.0 | 0000 | 1.0 |
| 0001 | 1.1 | 0001 | 1.1 |
| 0010 | 1.2 | 0010 | 1.2 |
| 0011 | 1.3 | 0011 | 1.3 |

*Table 7. POWER MANAGEMENT BUS_REVISION Command*



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## 7.17 MFR-EFFIENCY_LL (AAh)

The MFR_EFFICIENCY_LL command sets or retrieves information about the efficiency of the device while operating at a low line condition. Not including the PEC byte, if used, and the byte count byte, there are fourteen data bytes as described below. The efficiency is specified at one input voltage and three data points consisting of output power and the efficiency at that output power. The three power ratings are typically referred as low, medium and high output power and are transmitted in that order. For example, the low, medium and high output power might correspond to 20%, 50% and 100% of the rated output power. The exact values of the output power are specified is left to the Power Management Bus device manufacturer. Each value (voltage, power or efficiency) is transmitted as two bytes in linear format.

| BYTE NUMBER | BYTE ORDER | DESCRIPTION |
|---|---|---|
| 0 | Low Byte | The input voltage, in volts, at which the low line efficiency data is applicable. Note that byte 0 is the first data byte transmitted as part of the block transfer. |
| 1 | High Byte | |
| 2 | Low Byte | Power, in watts, at which the low power efficiency is specified |
| 3 | High Byte | |
| 4 | Low Byte | The efficiency, in percent, at the specified low power. |
| 5 | High Byte | |
| 6 | Low Byte | Power, in watts, at which the medium power efficiency is specified |
| 7 | High Byte | |
| 8 | Low Byte | The efficiency, in percent, at the specified medium power. |
| 9 | High Byte | |
| 10 | Low Byte | Power, in watts, at which the high power efficiency is specified |
| 11 | High Byte | |
| 12 | Low Byte | The efficiency, in percentage, at the specified high power. Note that byte 13 is the last data byte transmitted as part of the block transfer. |
| 13 | High Byte | |

*Table 8. MFR_EFFICIENCY_LL*

## 7.18 MFR-EFFIENCY_HL (ABh)

The MFR_EFFICIENCY_HL command sets or retrieves information about the efficiency of the device while operating at a high line condition. Not including the PEC byte, if used, and the byte count byte, there are fourteen data bytes as described below. The efficiency is specified at one input voltage and three data points consisting of output power and the efficiency at that output power. The three power ratings are typically referred as low, medium and high output power and are transmitted in that order. For example, the low, medium and high output power might correspond to 20%, 50% and 100% of the rated output power. The exact values of the output power is specified is left to the Power Management Bus device manufacturer. Each value (voltage, power or efficiency) is transmitted as two bytes in linear format.

| BYTE NUMBER | BYTE ORDER | DESCRIPTION |
|---|---|---|
| 0 | Low Byte | The input voltage, in volts, at which the high line efficiency data is applicable. Note that byte 0 is the first data byte transmitted as part of the block transfer. |
| 1 | High Byte | |
| 2 | Low Byte | Power, in watts, at which the low power efficiency is specified |
| 3 | High Byte | |
| 4 | Low Byte | The efficiency, in percent, at the specified low power. |
| 5 | High Byte | |
| 6 | Low Byte | Power in watts, at which the medium power efficiency is specified |
| 7 | High Byte | |
| 8 | Low Byte | The efficiency, in percent, at the specified medium power. |
| 9 | High Byte | |
| 10 | Low Byte | Power, in watts, at which the high-power efficiency is specified |
| 11 | High Byte | |
| 12 | Low Byte | The efficiency, in percentage, at the specified high power. Note that byte 13 is the last data byte transmitted as part of the block transfer. |
| 13 | High Byte | |

*Table 9. MFR_EFFICIENCY_HL*



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## 7.19 READ EIN (86h)

The new READ_EIN command is used to allow the system to apply its own input power filtering. This will allow the system to get faster input power data while preventing aliasing. The command returns an accumulated power value and an associated sample count of number of accumulated power values. This allows the system to calculate its own average power value each time the system polls the PSU.

| | MIN | MAX | DESCRIPTION |
|---|---|---|---|
| Format | Power Management Bus Direct format m = 01h, R = 00h, b = 00h | | Power Management Bus data format; refer to Power Management Bus specification for details. |
| Psample averaging period | 4 AC cycles | | Period instantaneous input power is averaged over to calculate Psample. |
| READ_EIN update period | 80/66.7ms (50/60Hz) | | Period at which the power accumulator and sample counter are updated |
| Range of System polling period | 1 sec | 100 ms | The PSU shall be polled over this range of rates while testing accuracy. |

**IMPORTANT:**
The PSU READ_EIN update period MUST always be less than the system polling period. To make sure the PSU is compatible with all possible system polling periods; the PSU must update the READ_EIN power accumulator and sample counter at a period less than 100msec (required period is 4 AC cycles 80/67msec).

*Table 10. READ_EIN Requirements Summary*

## 7.20 READ EOUT (87h)

The new READ_EOUT command is used to allow the system to apply its own output power filtering. This will allow the system to get faster output power data while preventing aliasing. The command returns an accumulated power value and an associated sample count of number of accumulated power values. This allows the system to calculate its own average power value each time the system polls the PSU.

| | MIN | MAX | DESCRIPTION |
|---|---|---|---|
| Format | Power Management Bus Direct format m = 01h, R = 00h, b = 00h | | Power Management Bus data format; refer to Power Management Bus specification for details. |
| Psample averaging period | Nominal 50 ms | | Period instantaneous input power is averaged over to calculate Psample. |
| Sampling period | Nominal 50 ms | | Period at which the power accumulator and sample counter are updated |
| System polling rate | 1 sample /s | 10 samples /s | The PSU shall be polled over this range of rates while testing accuracy. |

*Table 11. READ_EOUT Requirements Summary*



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## 7.21 READ_EIN & READ_EOUT FORMATS

The READ_EIN and READ_EOUT commands shall use the Power Management Bus direct format to report an accumulated power value and the sample count. The Power Management Bus coefficients m, R, and b shall be fixed values and the PSU shall report these values using the Power Management Bus COEFFICIENT command. The coefficient m shall be set to 01h, coefficient R shall be set to 00h, and coefficient b shall be set to 00h.

READ_EIN and READ_EOUT shall use the SMBus Block Read with PEC protocol in the below format.

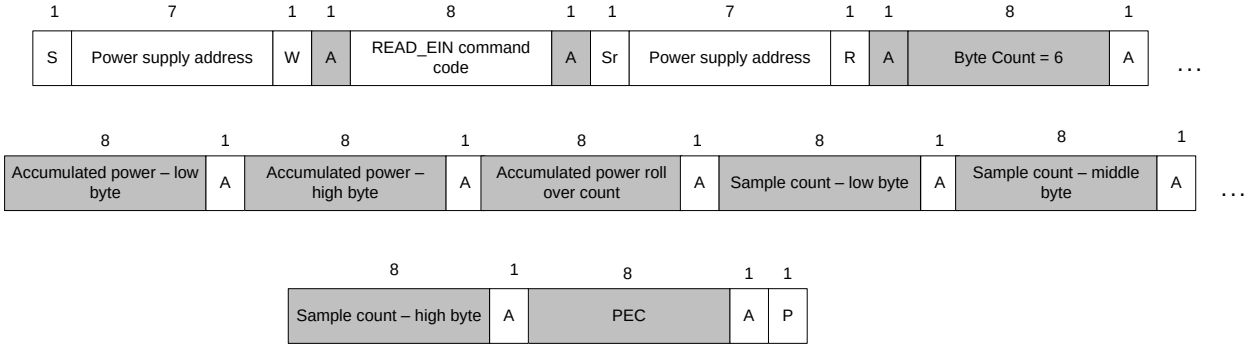


*Figure 9. READ_EIN Command*

The accumulated power data shall be the sum of input power values averaged over 4 AC cycles (or over 50ms for READ_EOUT). The value shall automatically roll-over when the 15 bit maximum value is reached ( > 7FFFh). The sample count should increment 1 for each accumulated power value. The system shall calculate average power by dividing the accumulated power value by the sample count. The system must sample READ_EIN and READ_EOUT faster than the roll-over period to get an accurate power calculation. Below is a block diagram depicting the accumulator function in the PSU.

IMPORTANT NOTE:

When the PSU responds to the system requesting READ_EIN or READ_EOUT data; the data in the sample count must always alignment with the number of samples accumulated in the power accumulator. To achieve this power accumulator, power rollover counter, and sample counter shall be loaded into a READ_EIN and READ_EOUT register at the same time.

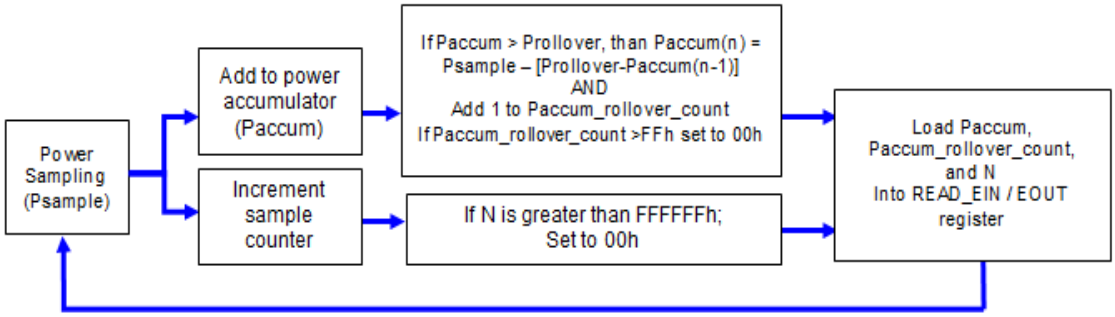


*Figure 10. READ_EIN PSU Functional Diagram*

| VALUE | DESCRIPRION |
|---|---|
| Psample: | The sampled power value in linear or direct format |
| Paccum: | 2 bytes in Power Management Bus linear or direct format. The accumulated power values made up of Psample(0) + Psample(1) + … + Psample(n) |
| N: | 3 byte unsigned integer value. The number of accumulated power values summed in Paccum |
| Prollover: | The max value of Paccum before a rollover will occur |
| Paccum_rollover_count: | 1 byte unsigned integer counting the number of times Paccum rolls over. Once this reaches FFh; it will automatically get reset to 00h |



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## 7.22 POWER SUPPLY ACCURACY

The following Power Management Bus commands shall be supported for the purpose of monitoring current, voltage, and power. All sensors shall continue providing real time data as long as the Power Management Bus device is powered. This means in standby mode the main output(s) of the PSU shall be zero amps and zero volts. Sensors shall meet requirements at nominal input voltage; maximum deviation for the ambient temperature is +/- 4°C.

| | 10%~20% of Max. Load | 20%~50% of Max. Load | 50%~100% of Max. Load |
|---|---|---|---|
| **Pin/Ein** | ±10 W or ±5% | ±3% | ±3% |
| **Iin** | ±0.08 A or ±5% | ±3% | ±3% |
| **Iout** | ±1A or ±5% | ±3% | ±3% |
| **Pout/Eout** | ±5% or ±10 W | ±3% | ±3% |
| **Vout** | ±3% | ±3% | ±3% |
| **Vin** | ±3% | ±3% | ±3% |

*Table 12. Power Management Bus Accuracy for AC-DC Models*

Note.1:

The spec is based on input voltage 115 VAC, 230 VAC and 240 VDC measurement, the Max. output may be different between low and high line, the load definition where is taken Max. value.

Note.2:

In 240 VDC application, no matter the input polarity is positive or negative, the PSU could operate normally, but Accuracy shall be measured when positive polarity on Neutral. If customer may apply positive polarity on either one, please inform bel early.

Note.3:

For light load reporting requirement, in the normal redundant application, PSU shall report below value to system once the below condition is set, which is not included the PSU that in SMART_ON redundant mode and set as slave. For system power calculation requirement, the reporting performance shall make sure the Pin > Pout situation,

Note.4:

The accuracy of AMB temperature is defined as the temperature around the temperature sensor inside of PSU, thereby this accuracy performance shall measure the closest point on the inlet chassis to internal temperature sensor.



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## 7.23 LINEAR DATA FORMAT

The Linear Data Format is typically used for commanding and reporting the parameters such as (but not only) the following:

- Output Current,
- Input Voltage,
- Input Current,
- Operating Temperatures,
- Time (durations), and Energy Storage Capacitor Voltage.

The Linear Data Format is a two byte value with:

- An 11 bit, two's complement mantissa and,
- A 5 bit, two's complement exponent (scaling factor),

The format of the two data bytes is illustrated in Figure as show below.

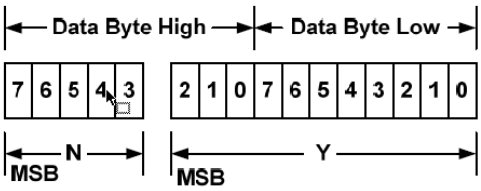


*Figure 11. Linear Data Format Data Bytes*

The relation between $Y$, $N$ and the "real world" value is:
$X = Y \cdot 2^N$

Where, as described above:
$X$ is the "real world" value;
$Y$ is an 11 bit, two's complement integer; and
$N$ is a 5 bit, two's complement integer.

Devices that use the linear format must accept and be able to process any value of $N$.



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## 7.24 VOUT_MODE (20h)

The data byte for the VOUT_MODE command is one byte that consists of a three bit Mode and a five bit exponent. The three bit Mode shall be set to indicate the LINEAR mode for output voltage related commands. The five bit Exponent shall be set to indicate the value of the five bit two's complement exponent for the mantissa delivered as the data bytes for an output voltage related command.

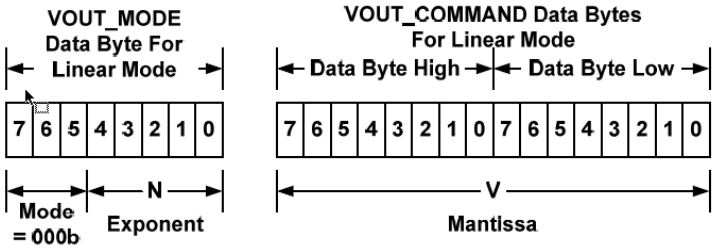


*Figure 12. Linear Format Data Bytes*

The voltage, in volts, is calculated from the equation Voltage = $V \cdot 2^N$, where:

- V is a 16 bit unsigned binary integer
- N is a 5 bit two's complement binary integer

Sending the VOUT_MODE command with the address set for writing is not supported. If the system sends a VOUT_MODE command for a write, the power supply shall reject the command, and set the Invalid/Unsupported Data bit in the STATUS_CML register.



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# 8 SMART_ON REDUNDANCY

## 8.1 OVERVIEW

Below is a block diagram showing the SMART_ON Redundancy architecture. When the power subsystem is in SMART_ON Redundant mode; only the needed power supply to support the best power delivery efficiency are ON. Any additional power supplies; including the redundant power supply, is in SMART_ON Standby state.

Each power supply has an additional signal that is dedicated to supporting SMART_ON Redundancy; SMART_ON_BUS. This signal is a common bus between all power supplies in the system. SMART_ON_BUS is asserted (pulled low) when there is a fault in any power supply OR the power supplies output voltage falls below the Vfault threshold. Asserting the SMART_ON_BUS signal causes all power supplies in SMART_ON Standby state to power ON.

Enabling power supplies to maintain best efficiency is achieved by looking at the Load Share bus voltage and comparing it to a programmed voltage level via a Power Management Bus command.

Whenever there is no SMART_ON Redundant active power supply on the SMART_ON Redundancy bus driving a HIGH level on the bus all power supplies are ON no matter their defined SMART_ON Redundant roll (active or SMART_ON Standby). This guarantees that incorrect programming of the SMART_ON Redundancy states of the power supply will never cause the power subsystem to shut down or become over loaded. The default state of the power subsystem is all power supplies ON. There needs to be at least one power supply in SMART_ON Redundant Active state or Standard Redundant state to allow the SMART_ON Standby state power supplies to go into SMART_ON Standby state.

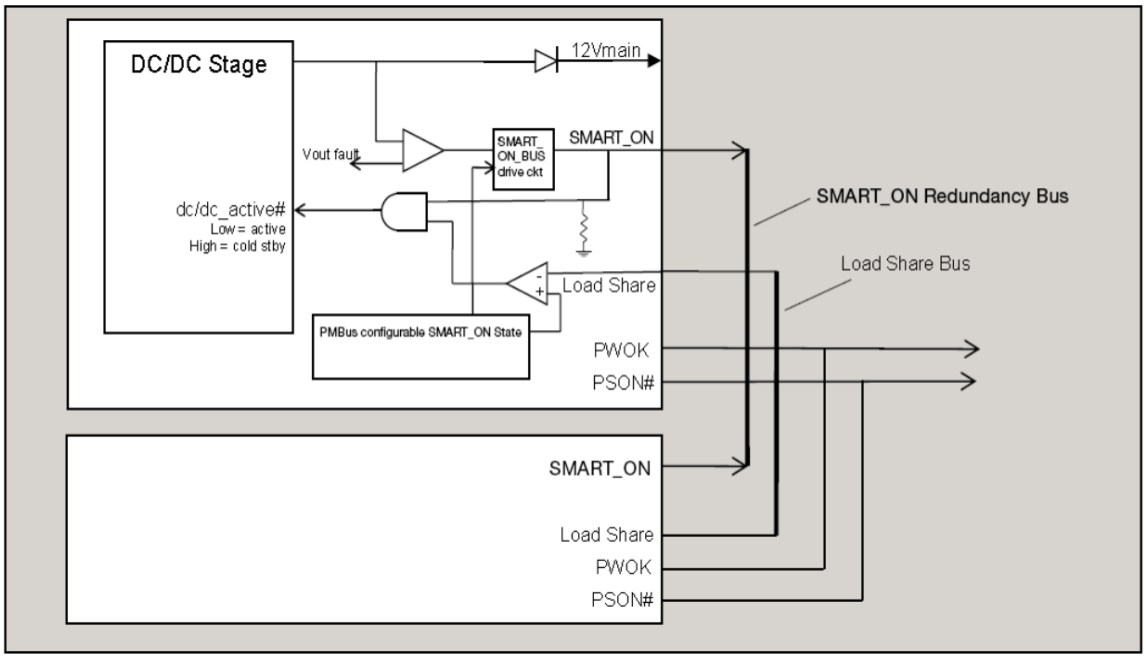


*Figure 13. SMART_ON Redundancy 1+1 Functional Block Diagram*

| SMART_ON_BUS | LOAD SHARE | DC/DC_ACTIVE# | SMART_ON STANDBY POWER SUPPLY STATE(S) |
|---|---|---|---|
| High | < $V_{SMART_ON}$ | High | SMART_ON Standby |
| Low | < $V_{SMART_ON}$ | Low | Active |
| High | > $V_{SMART_ON}$ | Low | Active |
| Low | > $V_{SMART_ON}$ | Low | Active |

*Table 13. Logic Matrix for SMART_ON Standby Power Supplies*



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## 8.2 POWERING ON SMART_ON STANDBY SUPPLIES TO MAINTAIN BEST EFFICIENCY

Power supplies in SMART_ON Standby state shall monitor the shared voltage level of the load share signal to sense when it needs to power on. Depending upon which position (1, 2, or 3) the system defines that power supply to be in the SMART_ON standby configuration; will slightly change the load share threshold that the power supply shall power on at.

| | Enable Threshold for $V_{SMART_ON_EN}$ | Disable Threshold for $V_{SMART_ON_DIS}$ | SMART_ON_BUS De-asserted / Asserted States |
|---|---|---|---|
| Standard Redundancy | N/A; Ignore dc/dc_ active# signal; power supply is always ON | | OK = Tri-state<br>Fault = Low |
| SMART_ON Redundant Active | NA; Ignore dc/dc_ active# signal; power supply is always ON | | OK = High<br>Fault = Low |
| SMART_ON Standby 1 (02h) | 3.2 V (40% of max) | 90% x (3.2V x 1/2) = 1.44 V | OK = Tri-state<br>Fault = Low |
| SMART_ON Standby 2 (03h) | 5.0 V (62% of max) | 90% x (5.0V x 2/3) = 3.01 V | OK = Tri-state<br>Fault = Low |
| SMART_ON Standby 3 (04h) | 6.7 V (84% of max) | 90% x (6.7V x 3/4) = 4.52 V | OK = Tri-state<br>Fault = Low |

*Table 14. Example Load Share Threshold for Activating Supplies*

Notes:
Maximum load share voltage = 8.0 V at 100% of rated output power
These are example load share bus threshold; for any power supply these shall be customized to maintain the best efficiency curve that specific model.

## 8.3 POWERING ON SMART_ON STANDBY SUPPLIES DURING A FAULT OR OVER CURRENT CONDITION

When an active power supply asserts its SMART_ON_BUS signal (pulling it low), all parallel power supplies in SMART_ON standby mode shall power on within 100µsec.

## 8.4 SMART_ON REDUNDANCY SMBUS COMMANDS

The Power Management Bus manufacturer specific command MFR_SPECIFIC_00 is used to configure the operating state of the power supply related to SMART_ON redundancy. We will call the command SMART_ON_Redundancy_Config (D0h). Below is the definition of the values used with the Read-Write Byte SMBus protocol with PEC.

| VALUE | STATE | DESCRIPTION |
|---|---|---|
| 00h | Standard Redundancy (default power on state) | Turns the power supply ON into standard redundant load sharing more. The power supply's SMART_ON_BUS signal shall be in Tri-state but still pull the bus low if a fault occurs to activate any power supplies still in SMART_ON Standby state. |
| 01h | SMART_ON Redundant Active | Defines this power supply to be the one that is always ON in a SMART_ON redundancy configuration. |
| 02h | SMART_ON Standby 1 [1] | Defines the power supply that is first to turn on in a SMART_ON redundant configuration as the load increases. |
| 03h | SMART_ON Standby 2 [1] | Defines the power supply that is second to turn on in a SMART_ON redundant configuration as the load increases. |
| 04h | SMART_ON Standby 3 [1] | Defines the power supply that is third to turn on in a SMART_ON redundant configuration as the load increases. |
| 05h | Always Standby [1] | Defines this power supply to be always in SMART_ON redundant configuration no matter what the load condition. |

[1] When the SMART_ON_BUS transitions from a high to a low state; each PSU programmed to be in SMART_ON Standby state shall be put into Standard Redundancy mode (SMART_ON_redundancy_Config = 00h). For the power supplies to enter SMART_ON Redundancy mode the system must re-program the power supplies using the SMART_ON_Redundancy_Config command.

*Table 15. SMART_ON_Redundancy_Config (D0h)*

## 8.5 SMART_ON REDUNDANT SIGNALS

There is an additional signal defined supporting SMART_ON Redundancy. This is connected to a bus shared between the power supplies; the SMART_ON_BUS.



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# 9 BLACK BOX

## 9.1 BLACK BOX FUNCTION DESCRIPTION

This specification defines the requirements for power supplies with Power Management Bus capability to store Power Management Bus and other data into non-volatile memory inside the power supply. The data shall be saved to non-volatile memory upon a critical failure that caused the power supply to shutdown. The data can be accessed via the Power Management Bus interface by applying power to the 12Vstby pins. No AC power need to be applied to the power supply.

## 9.2 WHEN IS DATA SAVED TO THE BLACK BOX?

Data is saved to the Black Box for the following fault events:

- General fault
- Over voltage on output
- Over current on output
- Loss of AC input
- Input voltage fault
- Fan failure
- Over temperature

## 9.3 BLACK BOX EVENTS

There are two types of data saved in the black box:

1) System Tracking Data.
2) Power supply event data.

System tracking data is saved to the Black Box whenever the system powers ON or when a power supply is added to the system.

## 9.4 BLACK BOX PROCESS

- System writes system tracking data to the power supply RAM at power ON.
- System writes the real time clock data to the PSU RAM once every ~5 minutes.
- Power supply tracks number of PSON# and AC power cycles in EEPROM.
- Power supply tracks ON time in EEPROM
- Power supply loads warning and fault event counter data from EEPROM into RAM
- Upon a warning event; the PSU shall increment the associated counter in RAM.
- Upon and fault event the PSU shall increment the associated counter in RAM
- Upon a fault event that causes the PSU to shut down all event data in the PSU's RAM is saved to event data location N in the power supply's EEPROM. This data includes the real time clock, number of AC & PSON# power cycles, PSU ON time, warning event counters and fault event counters.

## 9.5 RELATED COMMAND OF BLACK BOX

The following command set will be used for Black Box function via the Host System. The commands and protocol used by the Host System and shall be implemented by the microcontroller are defined by this document.

| COMMAND CODE | COMMAND NAME | SMBUS TRANSACTION TYPE | NUMBER OF DATA BYTES | REMARK |
|---|---|---|---|---|
| DCh | MFR_BLACK_BOX | Read only (7) | 237 | Read the data of the Black box. |
| DDh | MFR_REAL_TIME | Read/Write (6/7) | 4 | Read/Write the data of MFR real time. |
| DEh | MFR_SYSTEM_BLACK_BOX | Read/Write (6/7) | 40 | Read/Write the data of MFR system black box. |
| DFh | MFR_BLACKBOX_CONFIG | Read/Write (2/3) | 1 | Read/Write the data of MFR black box configure. |
| E0h | MFR_CLEAR_BLACKBOX | Write only (1) | 1 | Send one byte to clear all data of black box. |



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### 1) Command Name: MFR_BLACKBOX

Format: Read Block with PEC (237 bytes)

**Code: DCh**

| | ITEM | NUMBER OF BYTES | DESCRIPTION |
|---|---|---|---|
| System Tracking Data | System top assembly number | 10 | The system will write its Intel part number for the system top assembly to the power supply when it is powered ON. This is 9 ASCII characters. |
| | System serial number | 10 | The system shall write the system serial number to the power supply when it is powered ON. This includes the serial number and date code. |
| | Motherboard assembly number | 10 | The system will write the motherboard Intel part number for the assembly to the power supply when it is powered ON. This is 9 ASCII characters. |
| | Motherboard serial number | 10 | The system shall write the motherboard's serial number to the power supply when it is powered ON. This includes the serial number and date code. |
| | Present total PSU ON time | 3 | Total on time of the power supply with PSON# asserted in minutes. LSB = 1 minute. |
| | Present number of AC power cycles | 2 | Total number of times the power supply powered OFF then back ON due to loss of AC power. This is only counted when the power supply's PSON# signal is asserted. This counter shall stay at FFFFh once the max is reached. |
| | Present number of PSON# power cycles | 2 | Total number of times the power supply is powered OFF then back ON due to the PSON# signal de-asserting. This is only counted when AC power is present to the power supply. This counter shall stay at FFFFh once the max is reached. |
| Power supply event data (N) | | 38 | Most recent occurrence of saved black box data |
| Time Stamp | | | The power supply shall track these time and power cycle counters in RAM. When a black box event occurs, the data is saved into the Black Box. |
| | Power supply total power on time | 3 | Total on time of the power supply in minutes. LSB = 1 minute. |
| | Real Time Clock Data from System (reserved for future use) | 4 | This time stamp does not need to be generated by the power supply. The system rights a real time clock value periodically to the power supply using the MFR_REAL_TIME command. Format is based on IPMI 2.0. Time is an unsigned 32-bit value representing the local time as the number of seconds from 00:00:00, January 1, 1970. This format is sufficient to maintain time stamping with 1-second resolution past the year 2100. This is based on a long-standing UNIX-based standard for time keeping, which represents time as the number of seconds from 00:00:00, January 1, 1970 GMT. Similar time formats are used in ANSI C. |
| | Number of AC power cycles | 2 | Number of times the power supply powered OFF then back ON due to loss of AC power at the time of the event. This is only counted when the power supply's PSON# signal is asserted. |
| | Number of PSON# power cycles | 2 | Number of times the power supply is powered OFF then back ON due to the PSON# signal de-asserting at the time of the event. This is only counted when AC power is present to the power supply. |
| Power Management Bus | | | The power supply shall save these Power Management Bus values into the Black Box when a black box event occurs. Fast events may be missed due to the filtering effects of the Power Management Bus sensors. |
| | STATUS_WORD | 2 | |
| | STATUS_IOUT | 1 | |
| | STATUS_INPUT | 1 | |
| | STATUS_TEMPERTATURE | 1 | |
| | STATUS_FAN_1_2 | 1 | |
| | READ_VIN | 2 | |
| | READ_IIN | 2 | |
| | READ_IOUT | 2 | |
| | READ_TEMPERATURE_1 | 2 | |



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| | | | |
|---|---|---|---|
| | READ_TEMPERATURE_2 | 2 | |
| | READ_FAN_SPEED_1 | 2 | |
| | READ_PIN | 2 | |
| | READ_VOUT | 2 | |
| Event Counters | | | The power supply shall track the total number for each of the following events. These values shall be saved to the black box when a black box event occurs. Once a value has reached 15, it shall stay at 15 and not reset. |
| | AC shutdown due to under voltage on input | Lower ½ | The power supply shall save a count of these critical events to non-volatile memory each time they occur. The counters will increment each time the associated STATUS bit is asserted. |
| | Thermal shutdown | Upper ½ | |
| | Over current or over power shutdown on output | Lower ½ | |
| | General failure shutdown | Upper ½ | |
| | Fan failure shutdown | Lower ½ | |
| | Shutdown due to over voltage on output | Upper ½ | |
| | Input voltage warning; no shutdown | Lower ½ | The power supply shall save into RAM a count of these warning events. Events are count only at the initial assertion of the event/bit. If the event persists without clearing the bit the counter will not be incremented. When the power supply shuts down it shall save these warning event counters to non-volatile memory. The counters will increment each time the associated STATUS bit is asserted. |
| | Thermal warning; no shutdown | Upper ½ | |
| | Output current power warning; no shutdown | Lower ½ | |
| | Fan slow warning; no shutdown | Upper ½ | |
| Power supply event data (N-1) | | 38 | |
| Power supply event data (N-2) | | 38 | |
| Power supply event data (N-3) | | 38 | |
| Power supply event data (N-4) | | 38 | |

### 2) Name: MFR_REAL_TIME_BLACK_BOX

Format: Write/Read Block with PEC (4 bytes)

**Code: DDh**

The system shall use this command to periodically write the real time clock data to the power supply.

Format is based on IPMI 2.0. Time is an unsigned 32-bit value representing the local time as the number of seconds from 00:00:00, January 1, 1970. This format is sufficient to maintain time stamping with 1-second resolution past the year 2100. This is based on a long standing UNIX-based standard for time keeping, which represents time as the number of seconds from 00:00:00, January 1, 1970 GMT. Similar time formats are used in ANSIC.

### 3) Name: MFR_SYSTEM_BLACK_BOX

Format: Write/Read Block with PEC (40 bytes). Low byte first.

**Code: DEh**

The system uses this command to write the following data to the PSU.

| Item | Bytes | |
|---|---|---|
| System top assembly number | 1-10 | Low bytes |
| System serial number | 11-20 | |
| Motherboard assembly number | 21-30 | |
| Motherboard serial number | 31-40 | High bytes |



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### 4) Name: MFR_BLACKBOX_CONFIG

Format: Read/Write Byte with PEC

**Code: DFh**

| BIT | VALUE | DESCRIPTION |
|---|---|---|
| 0 | 0 = disable black box function<br>1 = enable black box function | Writing a 1 enables the power supply with black box function. Writing a 0 disables the power supply black box function.<br>The state of MFR_BLACKBOX_CONFIG shall be saved in non-volatile memory so that it is not lost during power cycling.<br>Intel shall receive the power supply with the black box function enabled; bit 0 = '1'. |
| 1-7 | | Reserved |

### 5) Name: MFR_CLEAR_BLACKBOX

Format: Send Byte with PEC

**Code: E0h**

The MFR_CLEAR_BLACKBOX command is used to clear all black box records simultaneously.

This command is write only. There is no data byte for this command.

## 9.6 HARDWARE REQUIREMENTS

The SMBus interface shall be used to access the Black Box data. It may be accessed when the power supply is ON or in standby mode. It also may be accessed when no AC power is applied, and power is only applied at the standby output pins by an external source (12Vstby).



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# 10 BOOTLOADER

## 10.1 FUNCTION DESCRIPTION

This specification defines the common architecture for in-system power supply firmware updates. It is required that the FW in the main microcontroller on the secondary side of the power supply must be able to be updated in the system using the In-System Firmware Update feature while in the ON state (i.e. with AC power present and PSON# asserted). It is desired that any other microcontroller in the power supply also be able to be updated with this same process (example: primary side microcontroller); however, this is not a requirement at this time.

## 10.2 FW IMAGE MAPPING

The power supply firmware image shall be made up of two parts; 1) Boot loader; 2) Main program. The system shall contain a backup of the power supply image in its BMC whenever updating the FW to the power supply.

**1) Boot Loader:**
This is the part of the power supply firmware that is never updated by the system. The power supply shall always be able to recover and power ON into the boot loader mode no matter the state of the power supply's main program. This code shall support the In-System FW update code and basic power supply functions to power ON/OFF, fan cooling, and protections (UV, OV, OC).

**2) Main Program:**
This is the fully functional power supply program space. There is no requirement to keep a backup image of this code in the power supply since a copy of the power support FW image shall always for kept in the system's BMC.

## 10.3 POWER SUPPLY OPERATING MODE DURING AND AFTER FIRMWARE UPDATE

**1) Firmware update mode in ON state with no power cycle needed:**
Power supply may be able to support FW upload in the ON state. The new FW will take effect once it is taken out of FW upload load.

**2）Bad image after firmware update:**
The power supply must always be able to power on in the boot loader mode with minimal operating capabilities even if the FW image sent to the power supply is bad or corrupt. If in this mode the power supply must be able to still enter the FW upload mode to upload a proper FW image to the PSU.



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## 10.4 TEC2200-12-074NA FIRMWARE IMAGE HEADER

| | | |
|---|---|---|
| Byte 1 | CRC Low Byte | Supplier internal use area 10 bytes |
| Byte 2 | CRC High Byte | |
| Byte 3 | Image Offset Low Byte | |
| Byte 4 | Image Offset High Byte | |
| Byte 5 | Image Size Low Byte | |
| Byte 6 | Image Size High Byte | |
| Byte 7 | Image Sector ID Low Byte | |
| Byte 8 | Image Sector ID High Byte | |
| Byte 9 | Image Update Key Low Byte | |
| Byte 10 | Image Update Key High Byte | |
| Byte 11 | T | Model Name 12 bytes |
| Byte 12 | E | |
| Byte 13 | C | |
| Byte 14 | 2 | |
| Byte 15 | 2 | |
| Byte 16 | 0 | |
| Byte 17 | 0 | |
| Byte 18 | - | |
| Byte 19 | 1 | |
| Byte 20 | 2 | |
| Byte 21 | N | |
| Byte 22 | A | |
| Byte 23 | Not used, for future use | Not used, for future use |
| Byte 24 | FW_MAJOR (Bit 7: down revision control bit, Bit 0-6: Major version). | Firmware Revision 3 bytes; in binary format |
| Byte 25 | FW_MINOR_PRIMARY (not used by system) | |
| Byte 26 | FW_MINOR_SECONDARY | |
| Byte 27 | HW_REVISION_FIRST | Hardware Compatible Revision 2 bytes |
| Byte 28 | HW_REVISION_SECOND | |
| Byte 29 | BLOCK SIZE Low Byte | |
| Byte 30 | BLOCK SIZE High Byte | |
| Byte 31 | Write Time Low Byte | |
| Byte 32 | Write Time High Byte | |



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## 10.5 TEC2200-12-074RA FIRMWARE IMAGE HEADER

| | | |
|---|---|---|
| Byte 1 | CRC Low Byte | Supplier internal use area 10 bytes |
| Byte 2 | CRC High Byte | |
| Byte 3 | Image Offset Low Byte | |
| Byte 4 | Image Offset High Byte | |
| Byte 5 | Image Size Low Byte | |
| Byte 6 | Image Size High Byte | |
| Byte 7 | Image Sector ID Low Byte | |
| Byte 8 | Image Sector ID High Byte | |
| Byte 9 | Image Update Key Low Byte | |
| Byte 10 | Image Update Key High Byte | |
| Byte 11 | T | Model Name 12 bytes |
| Byte 12 | E | |
| Byte 13 | C | |
| Byte 14 | 2 | |
| Byte 15 | 2 | |
| Byte 16 | 0 | |
| Byte 17 | 0 | |
| Byte 18 | - | |
| Byte 19 | 1 | |
| Byte 20 | 2 | |
| Byte 21 | R | |
| Byte 22 | A | |
| Byte 23 | Not used, for future use | Not used, for future use |
| Byte 24 | FW_MAJOR (Bit 7: down revision control bit, Bit 0-6: Major version). | Firmware Revision 3 bytes; in binary format |
| Byte 25 | FW_MINOR_PRIMARY (not used by system) | |
| Byte 26 | FW_MINOR_SECONDARY | |
| Byte 27 | HW_REVISION_FIRST | Hardware Compatible Revision 2 bytes |
| Byte 28 | HW_REVISION_SECOND | |
| Byte 29 | BLOCK SIZE Low Byte | |
| Byte 30 | BLOCK SIZE High Byte | |
| Byte 31 | Write Time Low Byte | |
| Byte 32 | Write Time High Byte | |



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## 10.6 FIRMWARE UPDATE PROCESS

**IMPORTANT!**

- PSU may be in standby mode or ON mode during FW update process
- If the FW update process is interrupted at any point during the process; the PSU must always be able to return to the boot loader code.
- The PSU must always check that the application program is not corrupted before starting to run from the application program
- During the FW upload process the PSU must always respond to any communication on the bus; acknowledging its address and the supporting commands without holding the bus. For unsupported boot loader commands the PSU may respond with Not Acknowledge or 00h.
- BMC must configure correct addresses into ME at BMC startup to avoid bad PSU address config if AC power is lost or BMC is reset while the PSU update is in progress

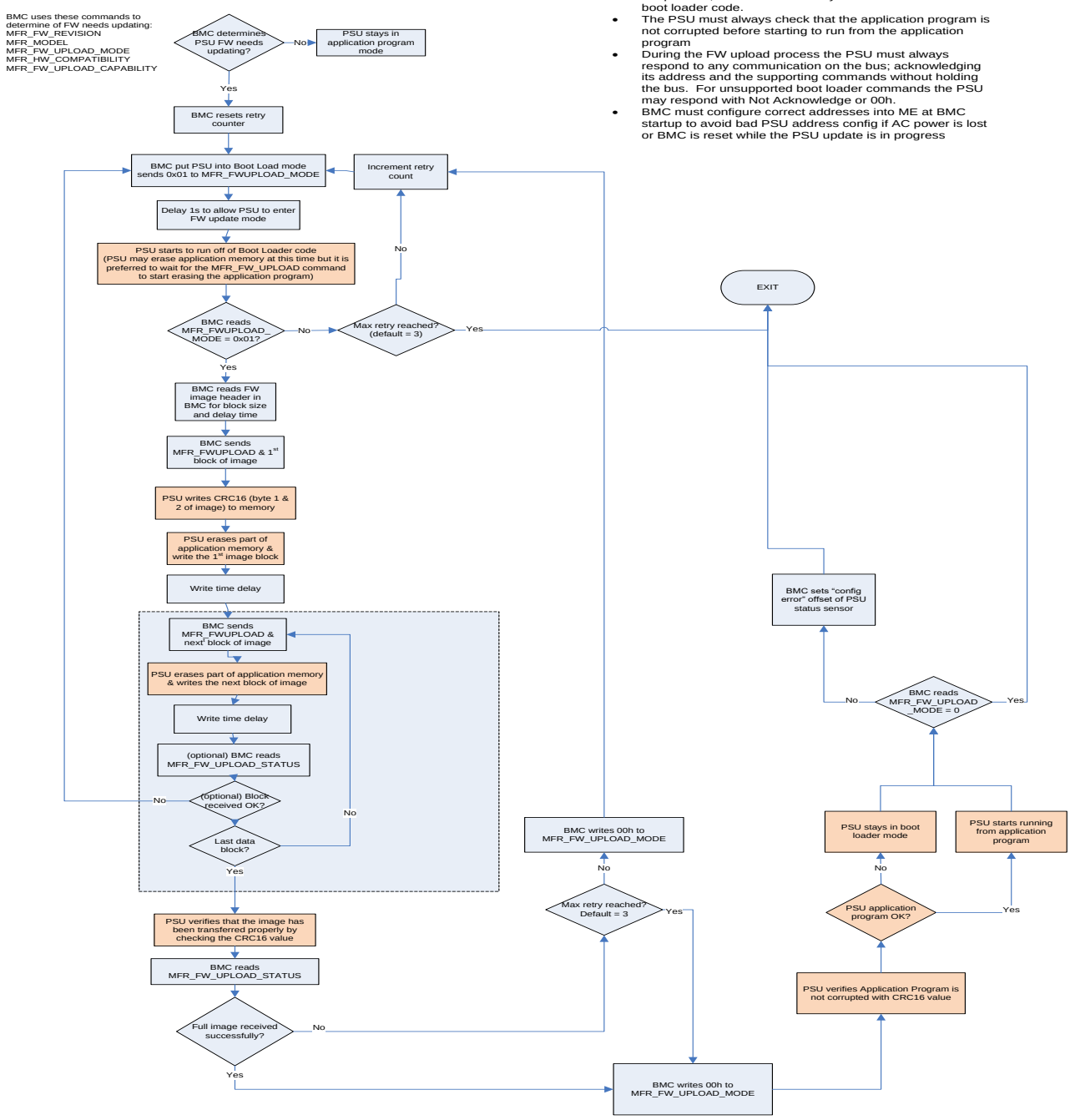


*Figure 14. PSU Upload Process*



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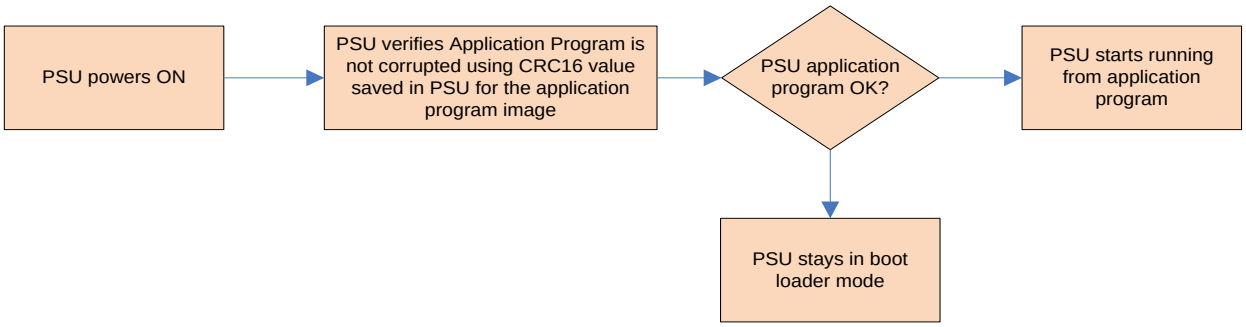


*Figure 15. PSU flow during powering ON*



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## 10.7 RELATED COMMAND OF BOOTLOADER

### 1) Name: MFR_HW_COMPATIBILITY

Format: Read Word

**Code: D4h**

| BYTES | VALUE | DESCRIPTION |
|---|---|---|
| low | ASCI code for first letter/number of the PSU HW compatibility. | This is a COMPATIBILITY value used to tell if there are any changes in the FW that create an incompatibility with the FW. This value only changes when the PSU HW is changed creating an incompatibility with older versions of FW. |
| high | ASCI code for second letter/number of the PSU HW compatibility. | |

### 2) Name: MFR_FWUPLOAD_CAPABILITY

Format: Read Byte

**Code: D5h**

The system can read the power supply's FW upload mode capability using this command. For any given power supply; more than one FW upload mode may be supported. The supported FW upload mode(s) must support updating all available FW in the power supply.

| BIT | VALUE | DESCRIPTION |
|---|---|---|
| 0 (for future use) | 1 = PSU support FW uploading in standby mode only | For future use |
| 1 (for future use) | 1 = PSU supports FW uploading in ON state; but all the new FW will not take effect until a power cycle with PSON#. | For future use |
| 2 | 1 = PSU supports FW uploading in the ON state and no power cycle needed | Method used for updating the application program in the power supply |
| 3-7 | Reserved | |

### 3) Name: MFR_FWUPLOAD_MODE

Format: Read/Write Byte

**Code: D6h**

| BIT | VALUE | DESCRIPTION |
|---|---|---|
| 0 | 0 = exit firmware upload mode<br>1 = firmware upload mode | Writing a 1 puts the power supply into firmware upload mode and gets it ready to receive the 1st image block via the MFR_FW_UPLOAD command. The system can use this command at any time to restart sending the FW image.<br>Writing a 0 puts the power supply back into normal operating mode.<br>Writing a 1 restarts<br>This command will put the PSU into standby mode if the PSU supports FW update in standby mode only.<br>If the power supply image passed to the PSU is corrupt the power supply shall stay in firmware upload mode even if the system requested the PSU to exit the FW upload mode. |
| 1-7 | | Reserved |

### 4) Name: MFR_FWUPLOAD

Format: Block Write (block = size as defined by the image header)

**Code: D7h**

| BYTES | VALUE | DESCRIPTION |
|---|---|---|
| Block size defined in header | Image header & image data | Command used to send each block of the FW image.<br>Header should follow the format described in section 13.4.<br>The image shall contain block sequencing numbers to make sure the PSU puts the right data blocks into the right memory space on the PSU MCU. |



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### 5) Name: MFR_FWUPLOAD_STATUS

Format: Read Word

**Code: D8h**

At any time during or after the firmware image upload the system can read this command to determine status of the firmware upload process.
Reset: all bits get reset to '0' when the power supply enters FW upload mode.

| BIT | DESCRIPTION |
|---|---|
| 0 | 1 = Full image received successfully |
| 1 | 1 = Full image not received yet. The PSU will keep this bit asserted until the full image is received by the PSU. |
| 2 | 1 = Full image received but image is bad or corrupt. Power supply can power ON, but only in 'safe mode' with minimal operating capability. |
| 3 (for future use) | 1 = Full image received but image is bad or corrupt. Power supply can power ON and support full features. |
| 4 | 1 = FW image not supported by PSU. If the PSU receives the image header and determines that the PSU HW does not support the image being sent by the system; it shall not accept the image and it shall assert this bit. |
| 5 – 15 | Reserved |

### 6) Name: MFR_FW_REVISION

Format: Block Read, 3 bytes

**Code: D9h**

| BYTE | VALUE | DESCRIPTION |
|---|---|---|
| 0 | 0 - 255 | Minor revision; secondary |
| 1 | 0 - 255 | Minor revision; primary |
| 2 | 0 - 255 | Bit 7:<br>1→ Down grading of PSU FW has to be avoided. System BMC can elect to ignore this bit if needed but recommended to follow.<br>0 → No restriction in downgrading the PSU FW. BMC can update the PSU FW to be in sync with its known version.<br>Bit 0-6: Major revision |

### 7) MFR_MODEL (existing Power Management Bus command)

**Code: 9Ah**

Maximum of 16 byte value; ending in terminator character.

### 8) MFR_REVISION (existing Power Management Bus command)

**Code: 9Bh**



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# 11 ELECTROMAGNETIC COMPATIBILITY

## 11.1 IMMUNITY

The power supply complies with the limits defined in EN 55024.

| PARAMETER | DESCRIPTION / CONDITION | CRITERION |
|---|---|---|
| Electrostatic Discharge | IEC / EN 61000-4-2 | B |
| Radiated Immunity | IEC / EN 61000-4-3 | A |
| Fast Transient / Burst | IEC / EN 61000-4-4 | B |
| Surge Immunity | IEC / EN 61000-4-5 (2 kV line to ground and 1 kV line to line) | A |
| Conducted Susceptibility | IEC / EN 61000-4-6 | |
| Power Frequency Magnetic Immunity | IEC / EN 61000-4-8 | |
| Voltage Dips and Interruptions | IEC / EN 61000-4-11 | |

## 11.2 EMISSION

| PARAMETER | DESCRIPTION / CONDITION | CRITERION |
|---|---|---|
| Conducted & Radiated Emissions | EN 55032 / CISPR 32 | Class A<br>6 dB margin |
| Power Harmonics | EN 61000-3-2 | Class A |
| Voltage Fluctuation and Flicker | EN 61000-3-3 | Class A |
| Acoustic Noise | Variable speed fan(s) incorporated, measured accord. to ECMA 74 and reported according to ISO 9296. | TBD dBA |

# 12 SAFETY / APPROVALS

| PARAMETER | DESCRIPTION / CONDITION | STATUS |
|---|---|---|
| Agency Approvals | • UL / CSA 62368-1 (USA / Canada)<br>• EN / IEC 62368-1 (Europe / International)<br>• CB Certificate & Report, IEC 62368-1 (Report includes all country national deviations)<br>• CE – Low Voltage Directive 2006/95/EC (Europe)<br>• Nordics – EMKO-TSE (74-SEC) 207/94<br>• GB4943.1 – CNCA Certification (China) | |
| Leakage Current | Max. 3.5 mA at 264 VAC, 60 Hz | |

# 13 ENVIRONMENTAL

| PARAMETER | DESCRIPTION / CONDITION | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| Ambient Temperature | Operating | TEC2200-12-074NA | 0 | | +50 | °C |
| | | TEC2200-12-074RA | 0 | | +50 | |
| | Non-Operating | | -40 | | +70 | |
| Humidity | Operating, relative (non-condensing) | | 5 | | 85 | % |
| | Non-Operating, relative (non-condensing) | | 5 | | 95 | |
| Altitude | Operating | | 0 | | 5 000 | ft |
| | Non-Operating | | 0 | | 15 200 | ft |
| Mechanical Shock (non-operating) | 50 G Trapezoidal Wave, Velocity change = 170 in. / sec | | | | | |
| Vibration (non-operating) sinusoidal | 1.5G, pk-pk, 10 Hz-500 Hz–10 Hz, 0.5 octave/min; 2 sweeps per axis | | | | | |
| Vibration (non-operating) random | 2 Grms, 10 Hz-500 Hz, 60 mins per axis | | | | | |
| Thermal Shock (non-operating) | 50 cycles, 30°C /min. ≧ transition time ≧ 15°C /min | | -40 | | +70 | °C |
| Audible Noise | @ 100% rated DC load and inlet $T_A$ = 25°C | | | | 70 | dB |



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## 14 RELIABILITY

| PARAMETER | DESCRIPTION / CONDITION | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Mean time between failures (MTBF) | $T_A$ = 25°C, 100% load, according Telcordia SR-332 | 200 000 | | | h |

## 15 MECHANICAL

| PARAMETER | DESCRIPTION / CONDITION | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Dimensions (W x H x L) | | | 73.5 x 40.0 x 185 | | mm |
| | | | 2.89 x 1.57 x 7.28 | | in |
| Weight | | | 740 | | g |

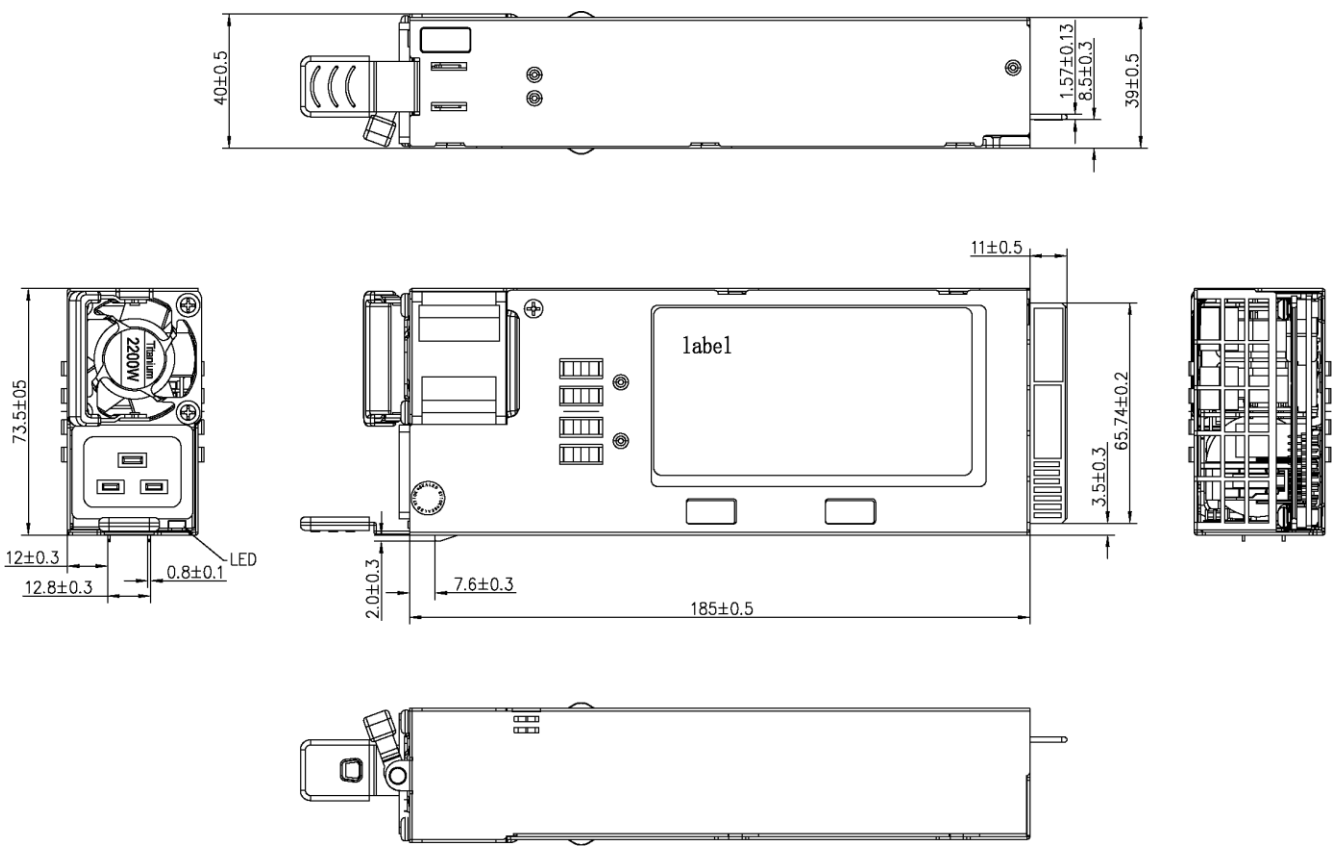


*Figure 16. Mechanical Drawing*



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## 15.1 AIRFLOW DIRECTION

The normal airflow direction (NA) is from the card edge connector side to the AC inlet side of the power supply.
The reverse airflow direction (RA) flows from the AC inlet side of the power supply to the card edge connector side.

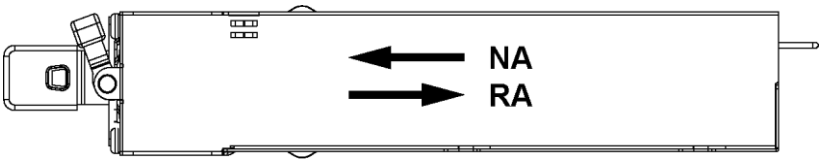


*Figure 17. Airflow Direction*

## 15.2 HANDLE RETENTION

The power supply has a handle to assist extraction. The module can be inserted and extracted without the assistance of tools.
The power supply has a latch which retains the power supply into the system and prevents the power supply from being inserted or extracted from the system when the AC power cord is pulled into the power supply.
The handle protects the operator from any burn hazard using the Customer Corporation Industrial designed plastic handle.

## 15.3 LED MARKING AND IDENTIFICATION

The power supply has a single bi-colored LED (green & amber) for indication of the power supply status.

| POWER SUPPLY CONDITION | LED STATE |
|---|---|
| Output ON and OK | GREEN |
| No AC power to all power supplies | OFF |
| AC present / Only 12VSB on (PS off) or PS in SMART_ON state | 1 Hz Blink GREEN |
| AC cord unplugged or AC power lost; with a second power supply in parallel still with AC input power. | AMBER |
| Power supply warning events where the power supply continues to operate; high temp, high power, high current, slow fan. | 1 Hz Blink Amber |
| Power supply critical event causing a shutdown; failure, OCP, OVP, Short circuit, Over temperature, Fan Fail | AMBER |
| Power supply FW updating | 2 Hz Blink GREEN |



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# 16 CONNECTORS

## 16.1 AC INLET CONNECTOR

The AC input connector is an IEC 320 C-20 power inlet. This inlet is rated for 16 A / 250 VAC.

## 16.2 DC OUTPUT CONNECTOR PIN LOCATIONS

The power supply shall use a card edge output connection for power and signal that is compatible with a 2x25 Power Card Edge connector (equivalent to 2x25 pin configuration of the Oupiin power card connector 9305-4P12S14B7SAA01)

| PIN-OUT | DEFINITION | PIN-OUT | DEFINITION |
|---|---|---|---|
| A1-9 | GND | B1-9 | GND |
| A10-18 | +12V | B10-18 | +12V |
| A19 | Power Management Bus SDA | B19 | A0 (SMBus address) |
| A20 | Power Management Bus SCL | B20 | A1 (SMBus address) |
| A21 | PSON# | B21 | +12VSB |
| A22 | SMBAlert# | B22 | SMART_ON |
| A23 | Return Sense | B23 | +12V Load Share Bus |
| A24 | +12V Remote Sense | B24 | PRESENT# |
| A25 | PWOK | B25 | Vin_good |

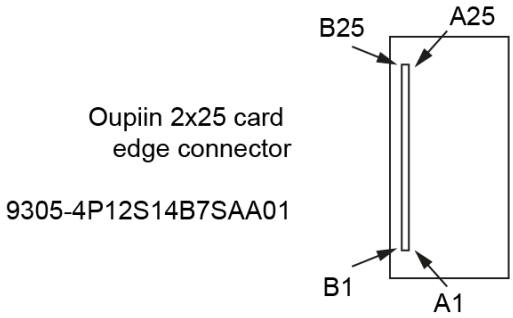


*Figure 18. Back DC output golden finger port*



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