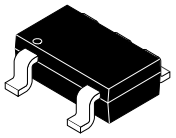
Schottky Barrier Diode

30 V, 1 A, Low I_R

SBE807



CPH5
CASE 318BC

Features

- Low Switching Noise
- Low Reverse Current (V_R = 16 V, I_R Max=15 μA)
- This Device is Pb−Free and Halide Free

Applications

- High Frequency Rectification (Switching Regulators, Converters, and Choppers)

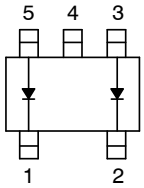
Specifications

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Parameter	Symbol	Conditions	Ratings	Unit
Repetitive Peak Reverse Voltage	V_{RRM}	−	30	V
Nonrepetitive Peak Reverse Surge Voltage	V_{RSM}	−	35	V
Average Output Current	I_O	−	1.0	A
Surge Forward Current	I_{FSM}	50 Hz sine wave, 1 cycle	10	A
Junction Temperature	T_j	−	− 55 to +125	°C
Storage Temperature	T_{stg}	−	− 55 to +125	°C

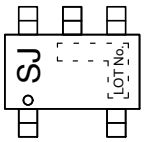
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

ELECTRICAL CONNECTION



1: Cathode
2: Cathode
3: Anode
4: No Contact
5: Anode

MARKING DIAGRAM



SJ = Specific Device Code

ORDERING INFORMATION

Device	Package	Shipping†
SBE807−TL−W	CPH−5 (Pb-Free and Halogen Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS (Ta = 25°C)

Parameter	Symbol	Conditions	Ratings			Unit
			Min	Typ	Max	
Reverse Voltage	V_R	I_R = 0.2 mA	30	–	–	V
Forward Voltage	V_F1	I_F = 0.7 A	–	0.45	0.50	V
	V_F2	I_F = 1.0 A	–	0.48	0.53	V
Reverse Current	I_R	V_R = 16 V	–	–	15	μA
Interterminal Capacitance	C	V_R = 10 V, f = 1 MHz	–	27	–	pF
Reverse Recovery Time	t_{rr}	I_F = I_R = 100 mA, See specified Test Circuit.	–	–	10	ns
Thermal Resistance	$Rth_{(j-a)}$	When mounted on ceramic substrate (900 $mm^2 \times 0.8$ mm)	–	111	–	°C/W

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

t_{rr} Test Circuit

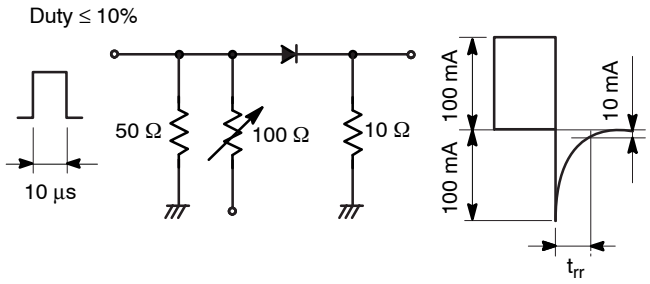


Figure 1. t_{rr} Test Circuit

TYPICAL CHARACTERISTICS

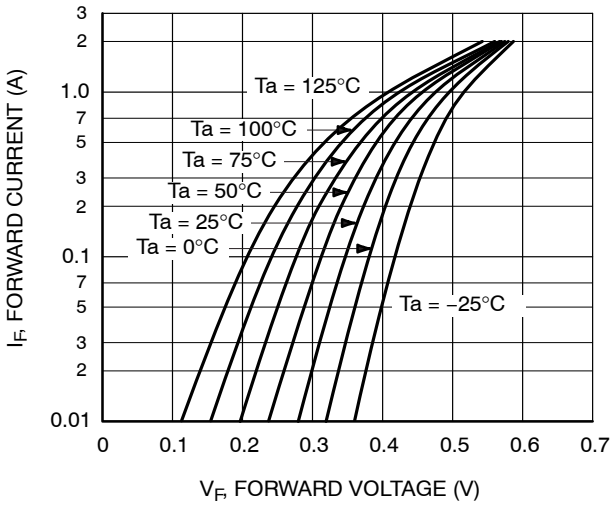


Figure 3. I_F – V_F

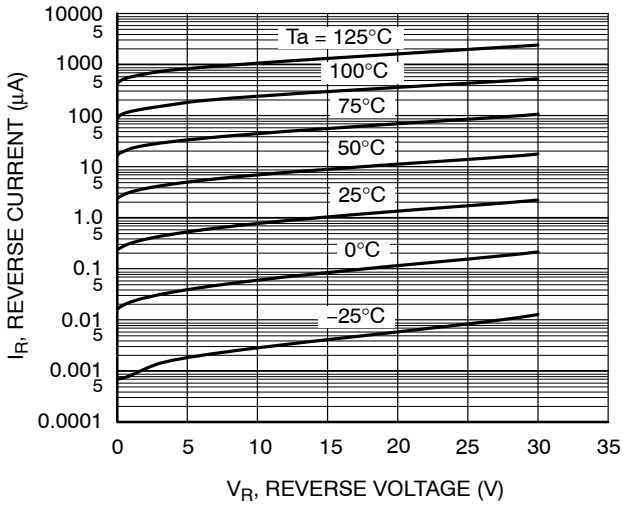


Figure 4. I_R – V_R

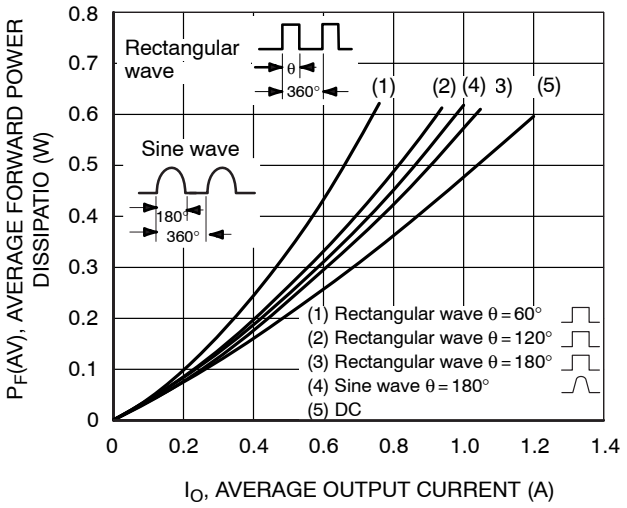


Figure 5. $P_F(AV)$ – I_O

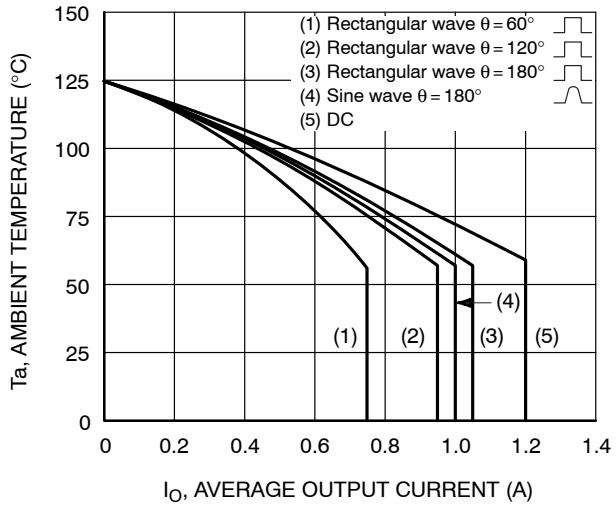


Figure 7. Ta – I_O

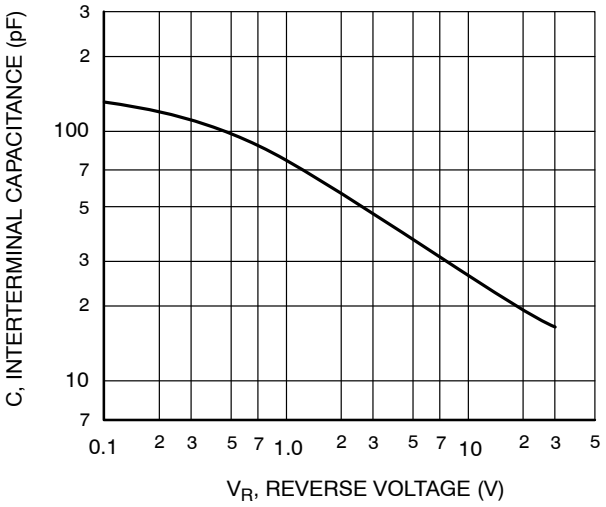


Figure 6. C – V_R

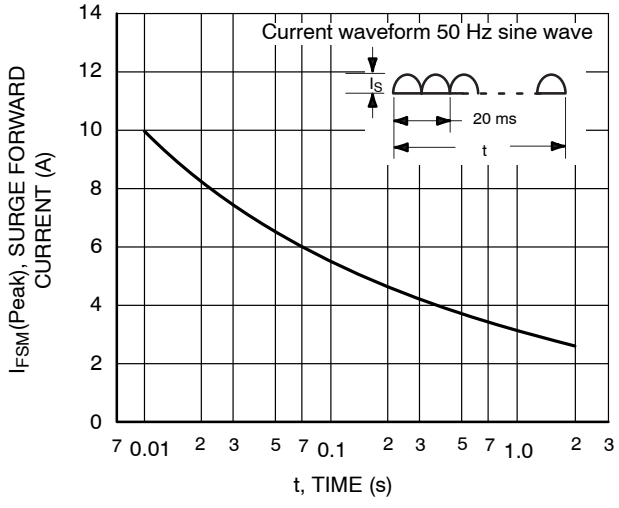
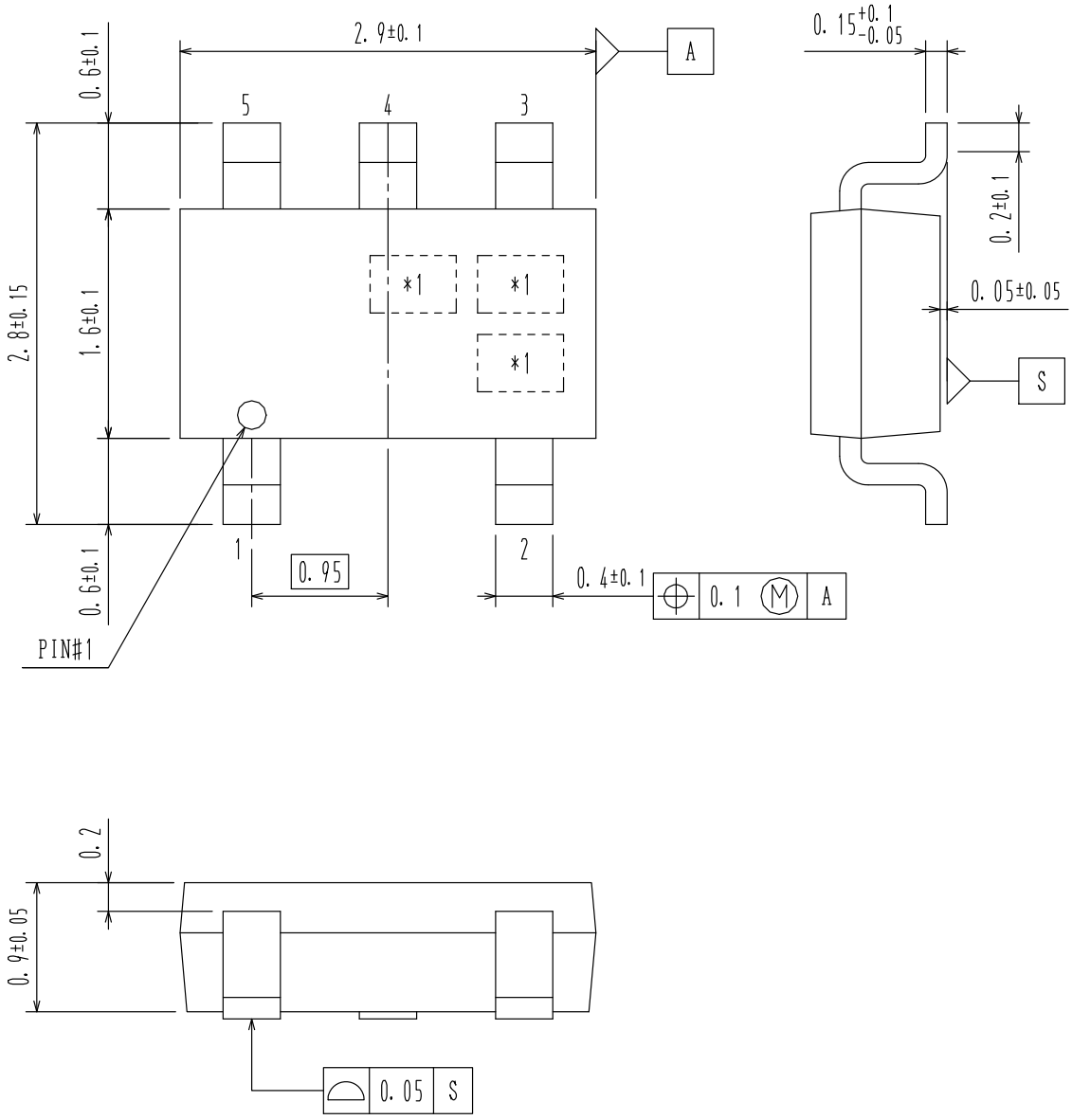


Figure 2. I_{FSM} – t

CPH5
CASE 318BC
ISSUE O

DATE 30 NOV 2011



DOCUMENT NUMBER:	**98AON65439E**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	**CPH5**	**PAGE 1 OF 1**

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support
For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales

◊