N-Channel Power MOSFET

30V, 108A, 4.5mΩ

FEATURES

- Low $R_{DS(ON)}$ to minimize conductive losses
- Low gate charge for fast power switching
- 100% UIS and R_g tested
- Compliant to RoHS directive 2011/65/EU and in accordance to WEEE 2002/96/EC
- Halogen-free according to IEC 61249-2-21

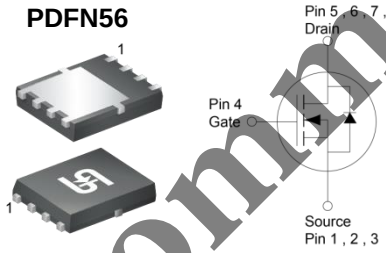
KEY PERFORMANCE PARAMETERS			
PARAMETER		**VALUE**	**UNIT**
V_{DS}		30	V
$R_{DS(on)}$ (max)	V_{GS} = 10V	4.5	mΩ
	V_{GS} = 4.5V	6.3	
Q_g		9	nC

APPLICATIONS

- DC-DC Converters
- Battery Power Management
- ORing FET/Load Switching

Pb-Free RoHS COMPLIANT HALOGEN FREE

PDFN56



Note: MSL 1 (Moisture Sensitivity Level) per J-STD-020

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)				
PARAMETER		**SYMBOL**	**LIMIT**	**UNIT**
Drain-Source Voltage		V_{DS}	30	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current (Note 1)	T_C = 25°C	I_D	108	A
	T_A = 25°C		18	
Pulsed Drain Current		I_{DM}	432	A
Single Pulse Avalanche Current (Note 2)		I_{AS}	26	A
Single Pulse Avalanche Energy (Note 2)		E_{AS}	104	mJ
Total Power Dissipation	T_C = 25°C	P_D	89	W
	T_C = 125°C		17.8	
Total Power Dissipation	T_A = 25°C	P_D	2.6	W
	T_A = 125°C		0.5	
Operating Junction and Storage Temperature Range		T_J, T_{STG}	- 55 to +150	°C

THERMAL PERFORMANCE			
PARAMETER	**SYMBOL**	**LIMIT**	**UNIT**
Junction to Case Thermal Resistance	$R_{\Theta JC}$	1.4	°C/W
Junction to Ambient Thermal Resistance	$R_{\Theta JA}$	48	°C/W

Thermal Performance Note: $R_{\Theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistances. The case-thermal reference is defined at the solder mounting surface of the drain pins. $R_{\Theta JA}$ is guaranteed by design while $R_{\Theta CA}$ is determined by the user's board design.

ELECTRICAL SPECIFICATIONS (T_A = 25°C unless otherwise noted)						
PARAMETER	**CONDITIONS**	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNIT**
Static						
Drain-Source Breakdown Voltage	V_{GS} = 0V, I_D = 250μA	BV_{DSS}	30	--	--	V
Gate Threshold Voltage	V_{GS} = V_{DS}, I_D = 250μA	$V_{GS(TH)}$	1.2	2	2.5	V
Gate-Source Leakage Current	V_{GS} = ±20V, V_{DS} = 0V	I_{GSS}	--	--	±100	nA
Drain-Source Leakage Current	V_{GS} = 0V, V_{DS} = 30V	I_{DSS}	--	--	1	μA
	V_{GS} = 0V, V_{DS} = 30V T_J = 125°C		--	--	100	
Drain-Source On-State Resistance (Note 3)	V_{GS} = 10V, I_D = 18A	$R_{DS(on)}$	--	3.6	4.5	mΩ
	V_{GS} = 4.5V, I_D = 18A		--	5.5	6.3	
Forward Transconductance (Note 3)	V_{DS} = 5V, I_D = 18A	g_{fs}	--	47	--	S
Dynamic (Note 4)						
Total Gate Charge	V_{GS} = 10V, V_{DS} = 15V, I_D = 18A	Q_g	--	19	--	nC
Total Gate Charge	V_{GS} = 4.5V, V_{DS} = 15V, I_D = 18A	Q_g	--	9	--	
Gate-Source Charge		Q_{gs}	--	4	--	
Gate-Drain Charge		Q_{gd}	--	3.7	--	
Input Capacitance	V_{GS} = 0V, V_{DS} = 15V f = 1.0MHz	C_{iss}	--	1194	--	pF
Output Capacitance		C_{oss}	--	421	--	
Reverse Transfer Capacitance		C_{rss}	--	97	--	
Gate Resistance	f = 1.0MHz	R_g	0.4	1.2	2.4	Ω
Switching (Note 4)						
Turn-On Delay Time	V_{GS} = 10V, V_{DS} = 15V, I_D = 18A, R_G = 2Ω,	$t_{d(on)}$	--	5.4	--	ns
Turn-On Rise Time		t_r	--	2.2	--	
Turn-Off Delay Time		$t_{d(off)}$	--	12.6	--	
Turn-Off Fall Time		t_f	--	2	--	
Source-Drain Diode						
Forward Voltage (Note 3)	V_{GS} = 0V, I_S = 18A	V_{SD}	--	--	1.2	V
Reverse Recovery Time	I_S = 18A , dI/dt = 100A/μs	t_{rr}	--	23	--	ns
Reverse Recovery Charge		Q_{rr}	--	17	--	nC

Notes:

1. Silicon limited current only.
2. L = 0.3mH, V_{GS} = 10V, V_{DD} = 50V, R_G = 25Ω, I_{AS} = 26A, Starting T_J = 25°C
3. Pulse test: Pulse Width ≤ 300μs, duty cycle ≤ 2%.
4. Switching time is essentially independent of operating temperature.

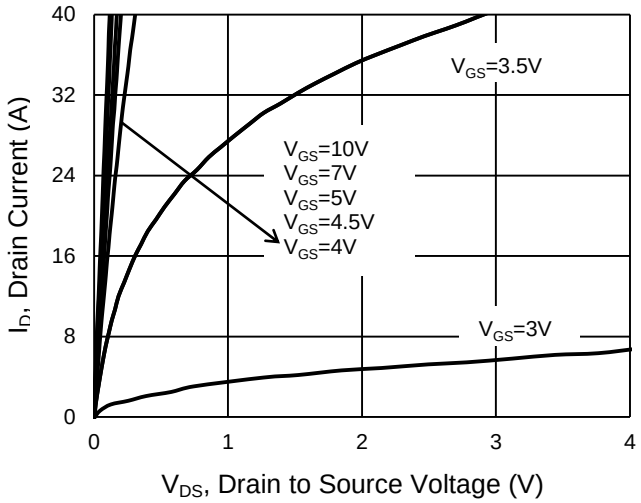
ORDERING INFORMATION

PART NO.	PACKAGE	PACKING
TSM045NA03CR RLG	PDFN56	2,500pcs / 13” Reel

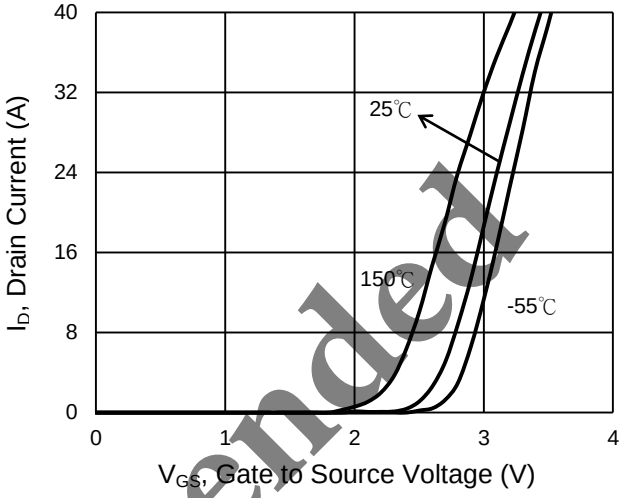
CHARACTERISTICS CURVES

(T_A = 25°C unless otherwise noted)

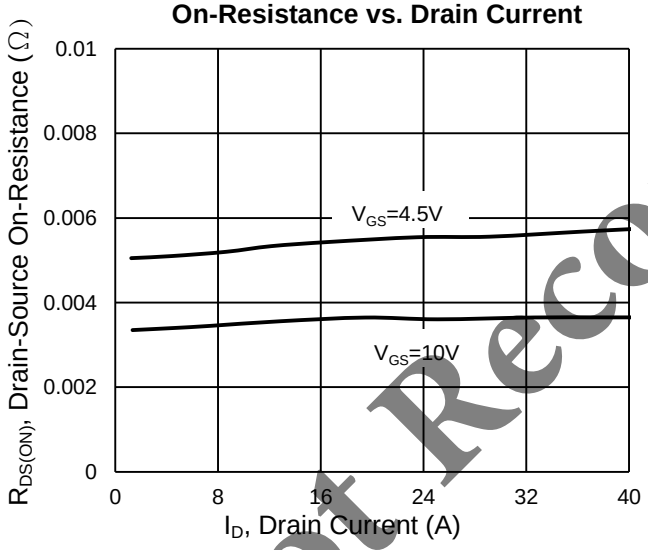
Output Characteristics



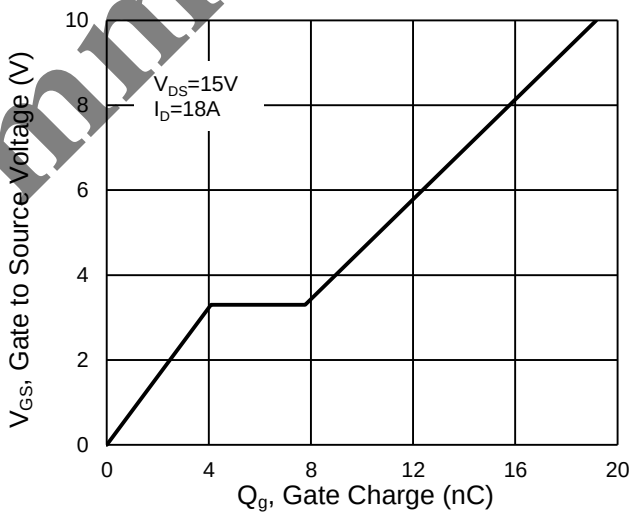
Transfer Characteristics



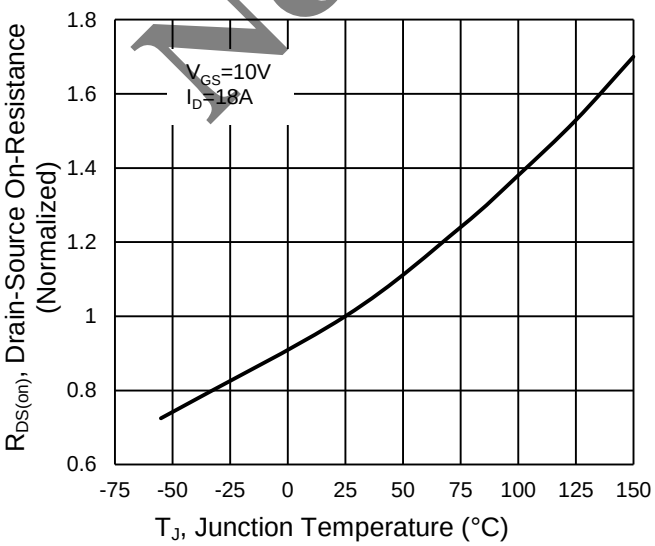
On-Resistance vs. Drain Current



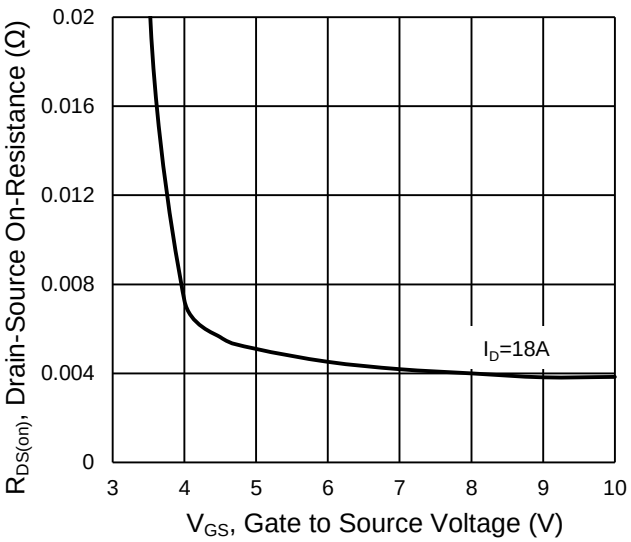
Gate-Source Voltage vs. Gate Charge



On-Resistance vs. Junction Temperature



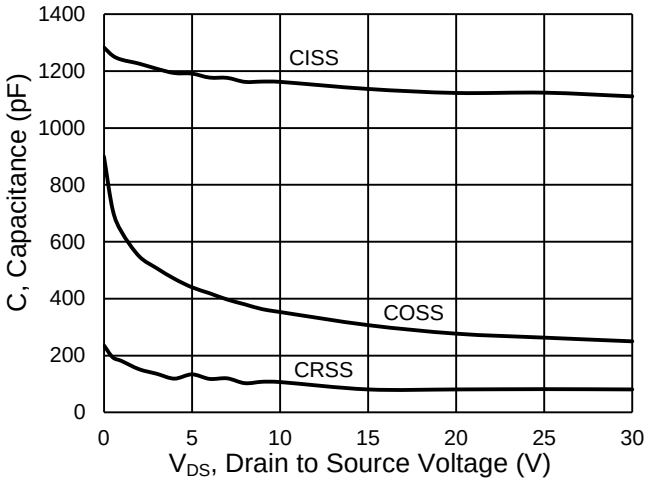
On-Resistance vs. Gate-Source Voltage



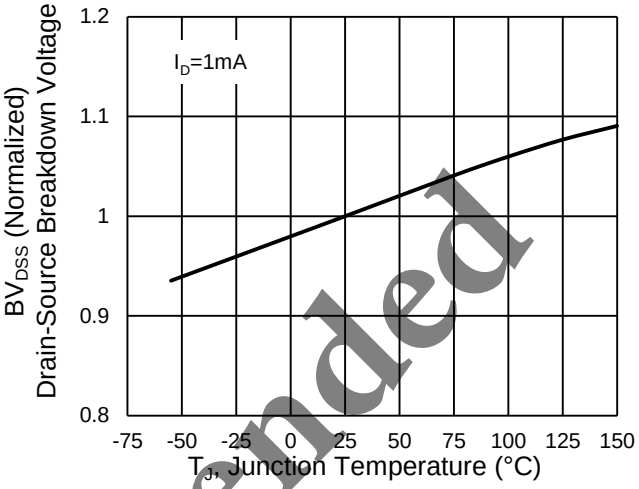
CHARACTERISTICS CURVES

(T_A = 25°C unless otherwise noted)

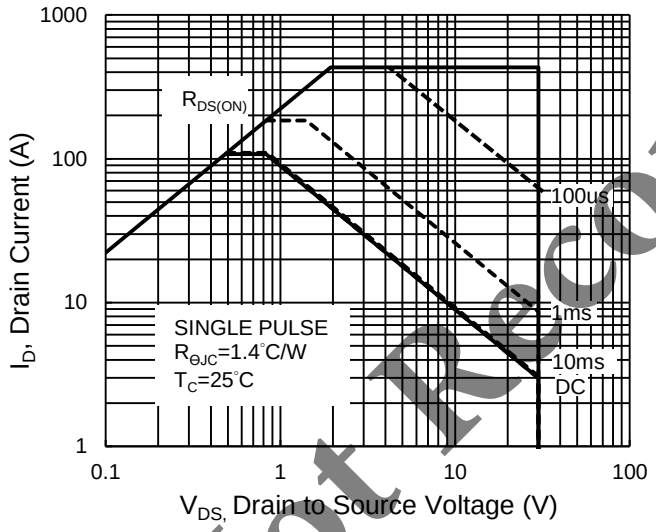
Capacitance vs. Drain-Source Voltage



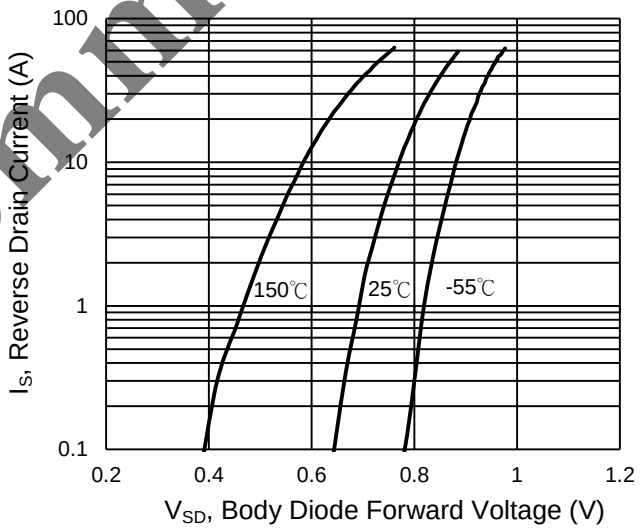
BV_{DSS} vs. Junction Temperature



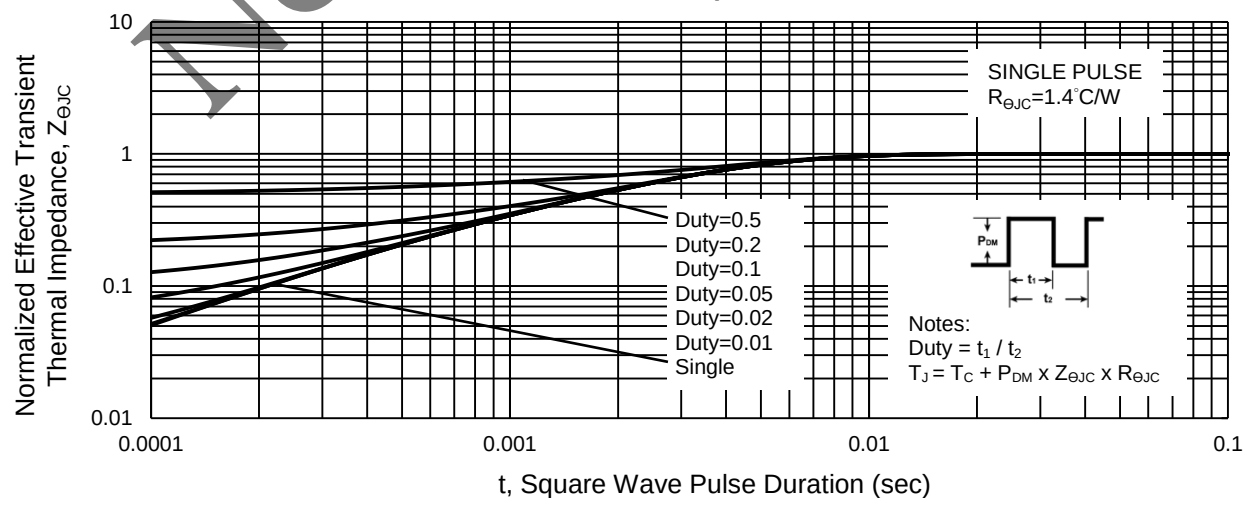
Maximum Safe Operating Area, Junction-to-Case



Source-Drain Diode Forward Current vs. Voltage

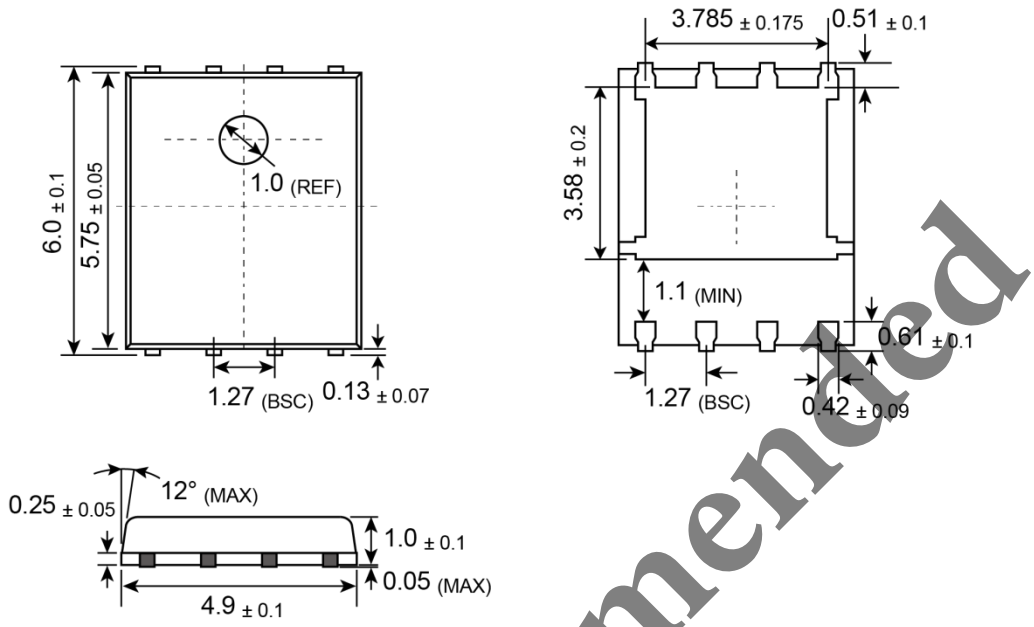


Normalized Thermal Transient Impedance, Junction-to-Case

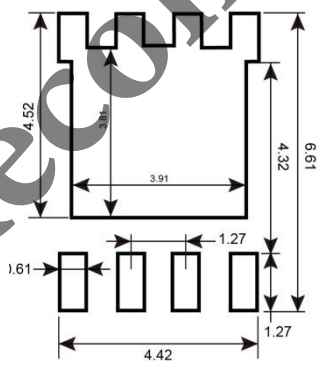


PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)

PDFN56



SUGGESTED PAD LAYOUT (Unit: Millimeters)



MARKING DIAGRAM

G = Halogen Free
Y = Year Code
WW = Week Code (01~52)
F = Factory Code

Notice

Specifications of the products displayed herein are subject to change without notice. TSC or anyone on its behalf, assumes no responsibility or liability for any errors or inaccuracies.

Information contained herein is intended to provide a product description only. No license, express or implied, to any intellectual property rights is granted by this document. Except as provided in TSC's terms and conditions of sale for such products, TSC assumes no liability whatsoever, and disclaims any express or implied warranty, relating to sale and/or use of TSC products including liability or warranties relating to fitness for a particular purpose, merchantability, or infringement of any patent, copyright, or other intellectual property right.

The products shown herein are not designed for use in medical, life-saving, or life-sustaining applications. Customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify TSC for any damages resulting from such improper use or sale.