READ2304G

High Drivability & High Slew Rate, Input Output Full Range, CMOS Dual Operational Amplifier

V_{IO}≤±6mV, SR = 8V/μs , GBW=6MHz

DESCRIPTION

The READ2304G is input and output full range dual CMOS Operational Amplifier realizing high drivability and high slew rate. This IC can be used in minimum operating supply voltage from 2.5V, and in wide ambient temperature range from -40°C to +105°C.

Available in ultra-small 8 pins TSSOP and MSOP packages.

FEATURES

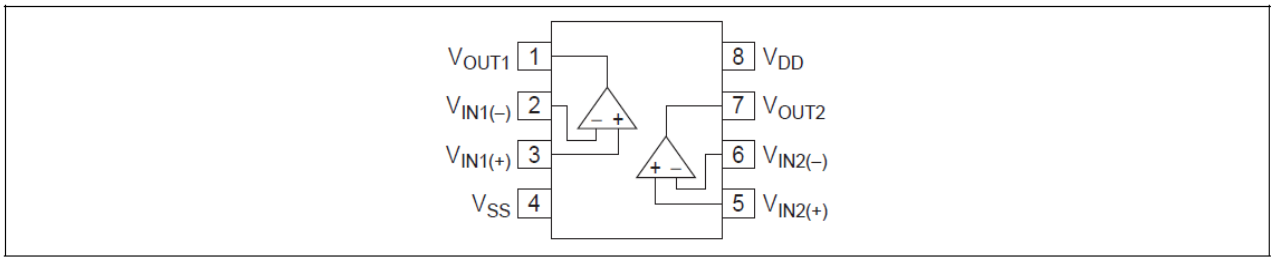
- Low voltage single supply operation — V_{DD} = 2.5V to 5.5V
- Low input offset voltage — V_{IO} ≤ ±6.0mV
- Low input bias current — I_B ≤ (1pA)
- Wide output voltage range — V_{OUT} : V_{SS}+0.1V to V_{DD}-0.1V(@I_O=5mA)
- Supply current (per channel) — I_{DD} = 0.75mA Typ.
- High slew rate — SR = 8V/μs Typ.

( ) reference value of design

ORDERING INFORMATION

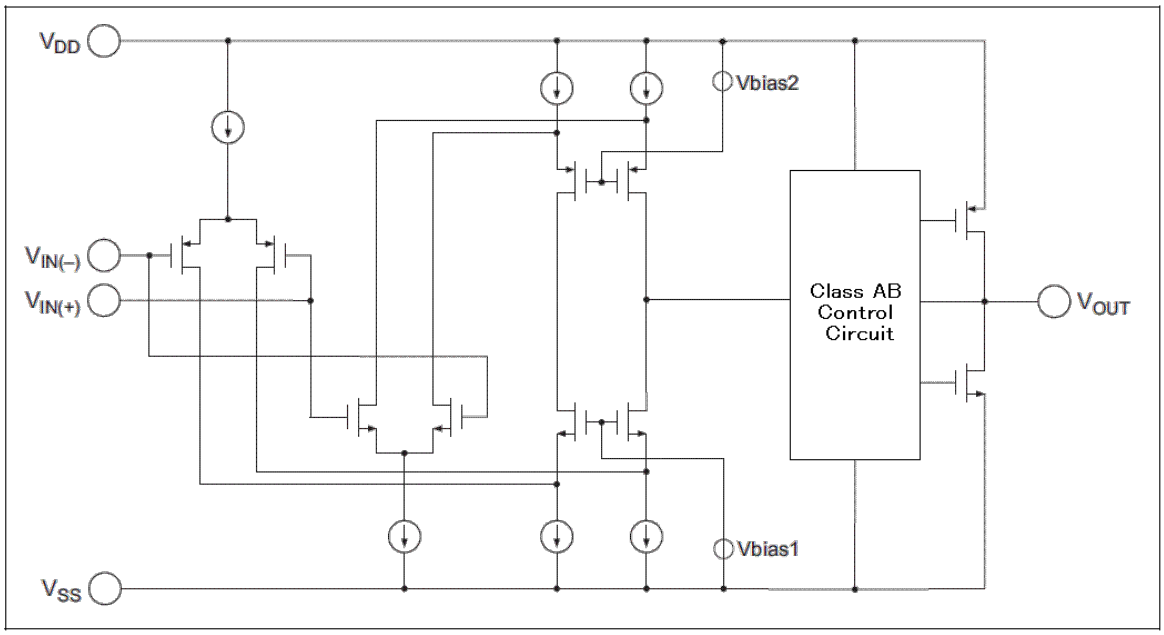
Order Name	Product type quality level	Package
READ2304GSP#GC0	High slew rate with Normal quality level	8-pin plastic TSSOP (5.72 mm (225))
READ2304GSN#GC0	High slew rate with Normal quality level	8-pin plastic MSOP (2.80 × 2.95 mm)

Pin Arrangement (Top View)



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Equivalent Circuit (per one channel)



ABSOLUTE MAXIMUM RATINGS

<T_A = 25 °C >

Items	Symbol	Ratings	Unit
Supply voltage Note.1	V_{DD}	-0.3 to +6.5	V
Differential input voltage	V_{ID}	$-V_{DD}$ to $+V_{DD}$	V
Input voltage Note.2	V_I	-0.3 to V_{DD} +0.3	V
Maximum output current	I_O	20	mA
Power dissipation Note.3	P_T	440	mW
Junction temperature	T_j	+150	°C
Operating temp. range	T_A	-40 to +105	°C
Storage temp. range	T_{stg}	-55 to +150	°C

【Note】 **1.** Please take note that reverse connection of a power supply may cause destruction.

2. Stresses above these ratings may cause permanent damage such as characteristics degradation or. destruction. Please do not exceed voltage below of GND - 0.3V as it is bottom limit. In addition, operation amplifier is operated as normal when input voltage for electrical characteristics is in common mode input voltage range.

3. The value is measured under mounted on a glass epoxy base board (size 100mm×100mm, 1mm thickness, copper foiled surface base board area with 15% solid pattern).
Note that restrictions will be made to the following conditions for each product, and the derating ratio depending on the operating ambient temperature.

READ2304GSP: Derate at -5.5 mW/°C when T_A > 69 °C

(Junction − ambient thermal resistance $R_{th(J-A)}$ = 183°C/W)

READ2304GSN: Derate at -4.8 mW/°C when T_A > 58 °C

(Junction − ambient thermal resistance $R_{th(J-A)}$ = 208°C/W)

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ELECTRICAL CHARACTERISTICS

< V_{DD}=5V, T_A=25 °C >

Items	Symbol	MIN.	TYP.	MAX.	Unit	Test Condition
Supply voltage	V_{DD} - V_{SS}	2.5		5.5	V	
Input offset voltage	V_{IO}			±6.0	mV	
Input offset current	I_{IO}			(1)	pA	
Input bias current	I_B			(1)	pA	
Output high voltage	V_{OH}	V_{DD} - 0.2			V	I_L = 10mA
Output low voltage	V_{OL}			V_{SS} + 0.2	V	I_L = 10mA
Voltage gain	A_V	60	90		dB	R_L ≥ 100kΩ
Channel supply current	I_{DD}/ch		0.75	1.5	mA	R_L = ∞, I_O = 0
Common mode rejection ratio	CMRR	60	80		dB	
Supply voltage rejection ratio	SVRR	60	80		dB	
Common mode input voltage range	V_{ICM}	V_{SS}		V_{DD}	V	
Gain bandwidth product	GBW		6		MHz	C_L = 20pF
Slew rate	SR		8		V/μs	C_L = 20pF

( ) reference value of design

【Notes】

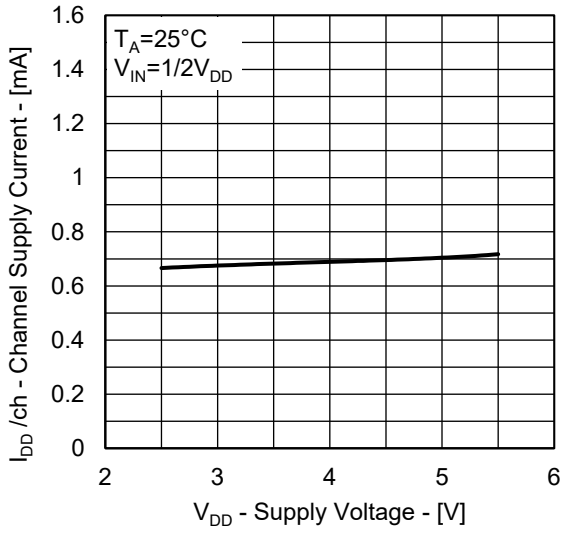
Output terminal : The over-current protection feature is not built in the output terminal of this product. Therefore, please insert resistance to output port.

Input offset voltage : The amplifier circuit of the first block of operational amplifier. A circuit suitable for operation near GND, and a circuit suitable for operation near +power supply. In case of input voltage of overlap point output port has a minute voltage shift or distortion.

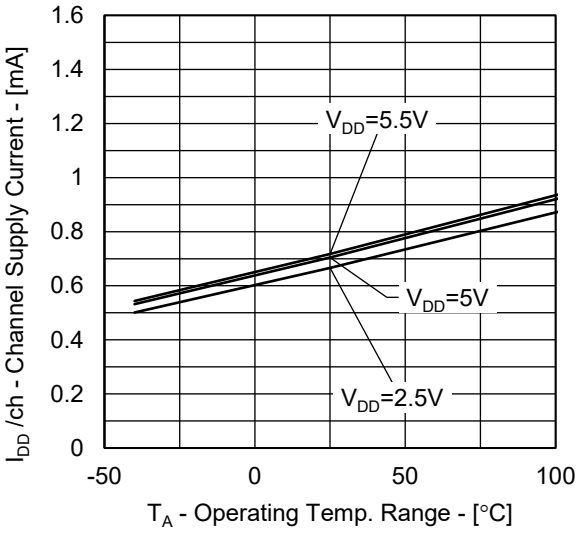
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ELECTRICAL CHARACTERISTICS

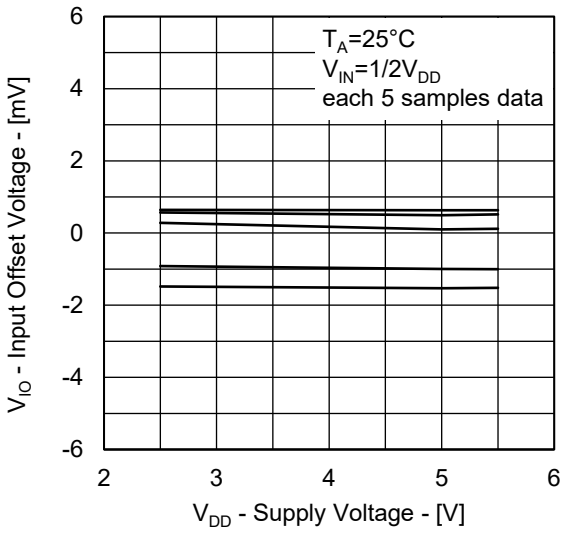
I_{DD} /ch vs. V_{DD}



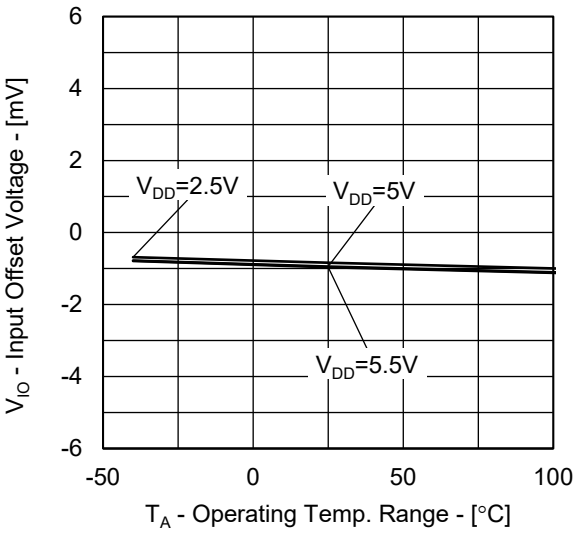
I_{DD} /ch vs. T_A



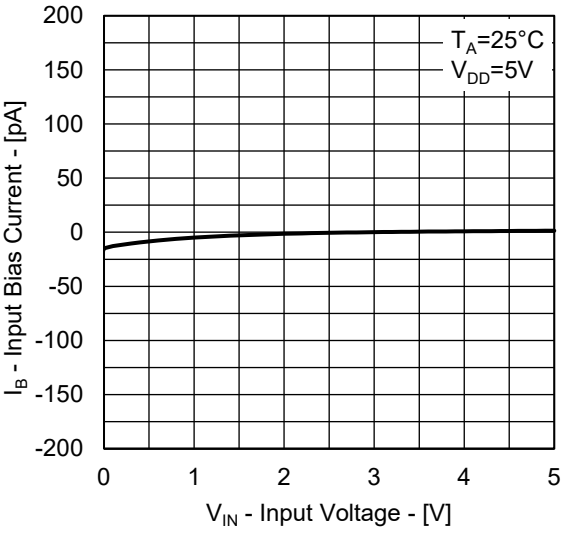
V_{IO} vs. V_{DD}



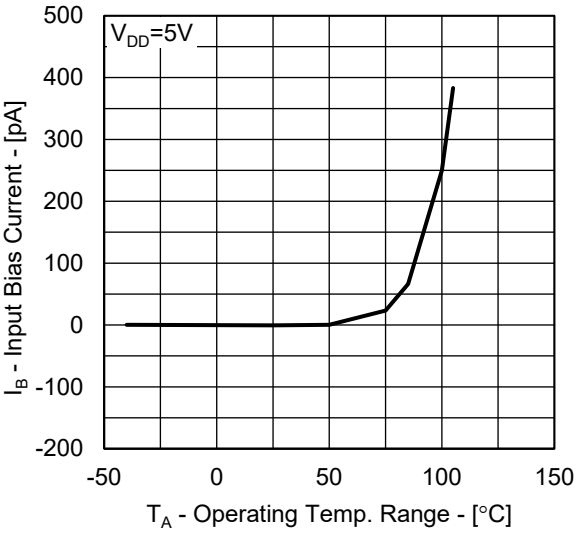
V_{IO} vs. T_A



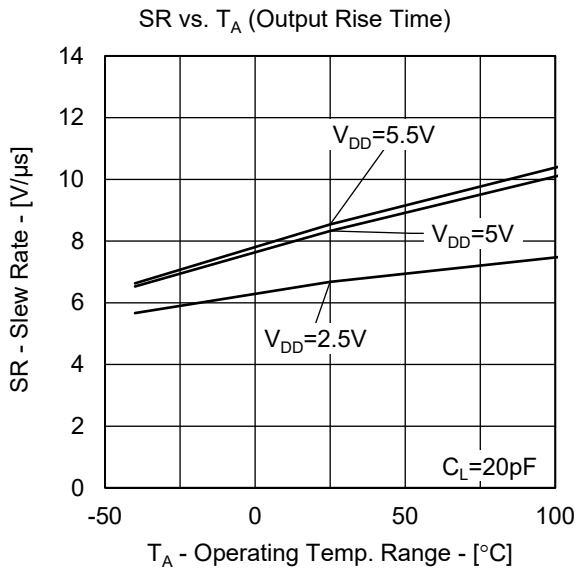
I_B vs. V_{IN}

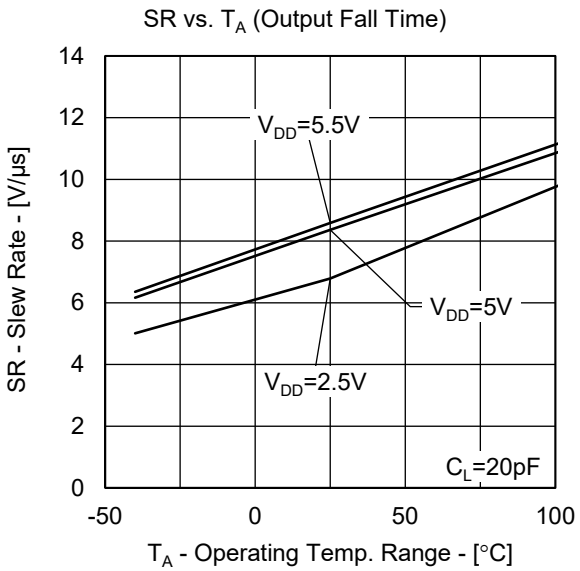


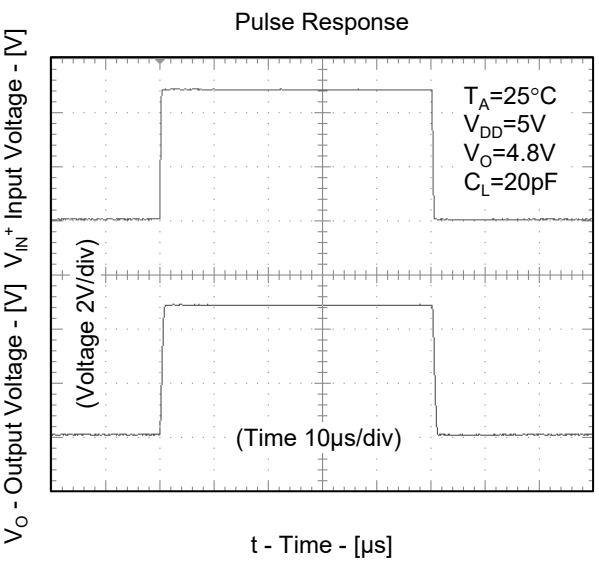
I_B vs. T_A

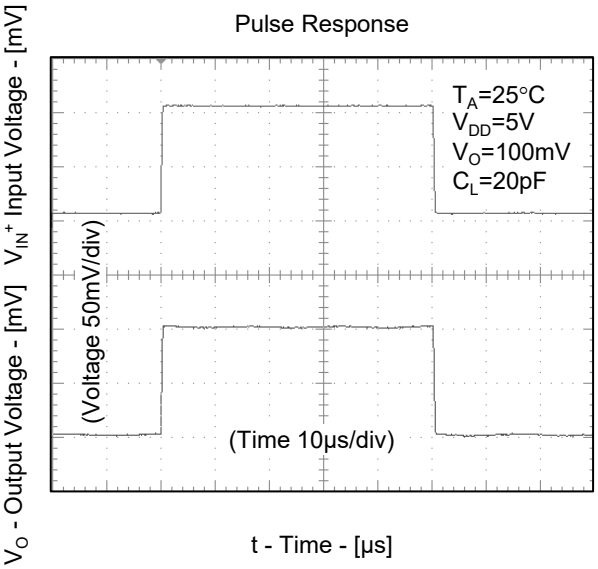


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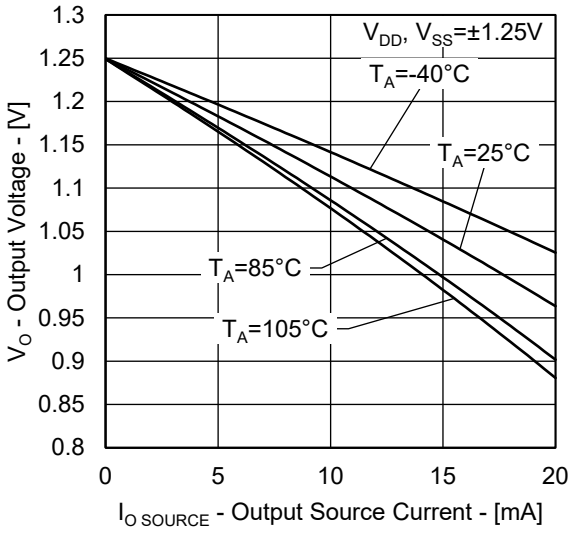




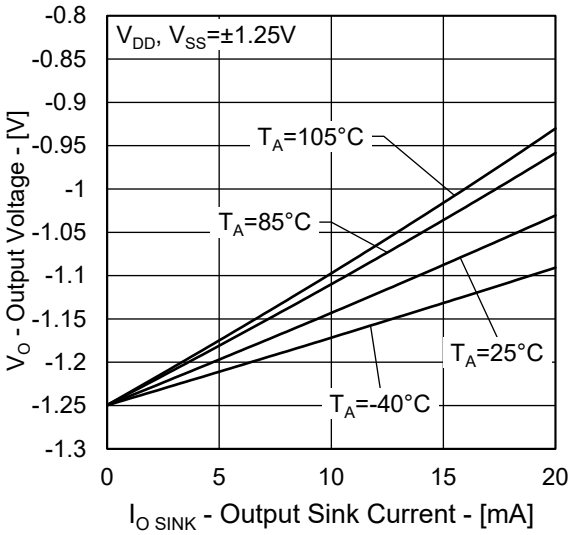


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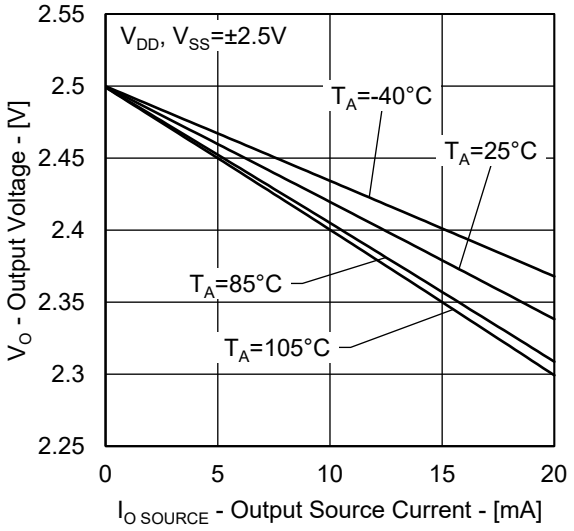
V_O vs. $I_{O\ SOURCE}$



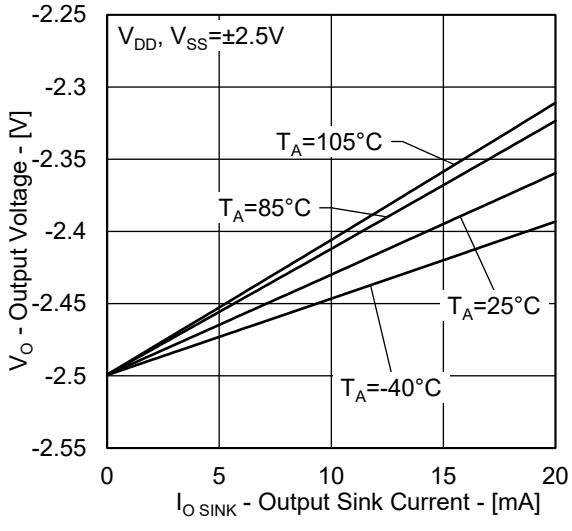
V_O vs. $I_{O\ SINK}$



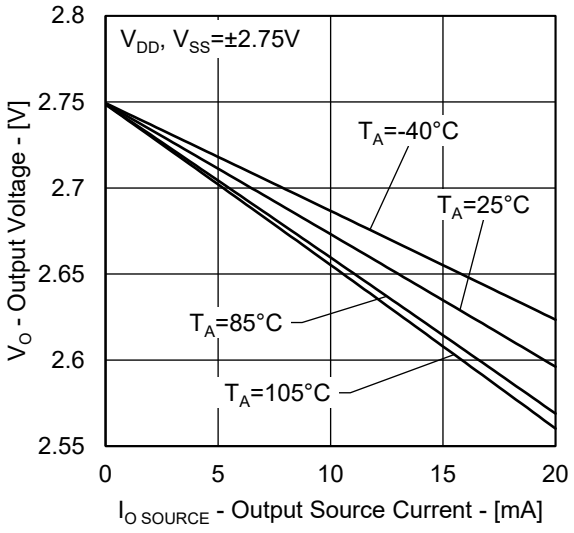
V_O vs. $I_{O\ SOURCE}$



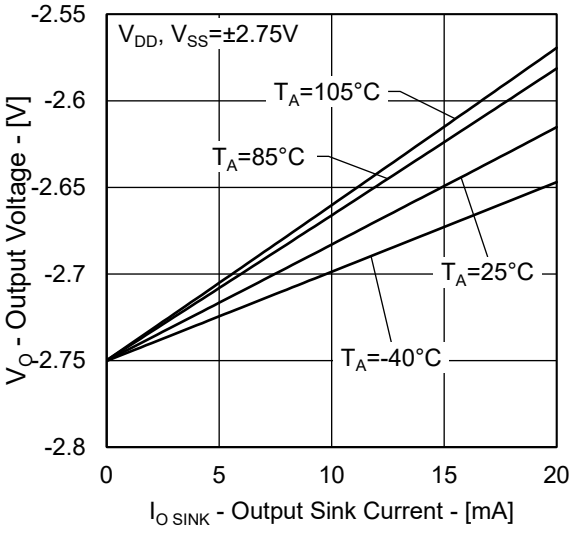
V_O vs. $I_{O\ SINK}$



V_O vs. $I_{O\ SOURCE}$

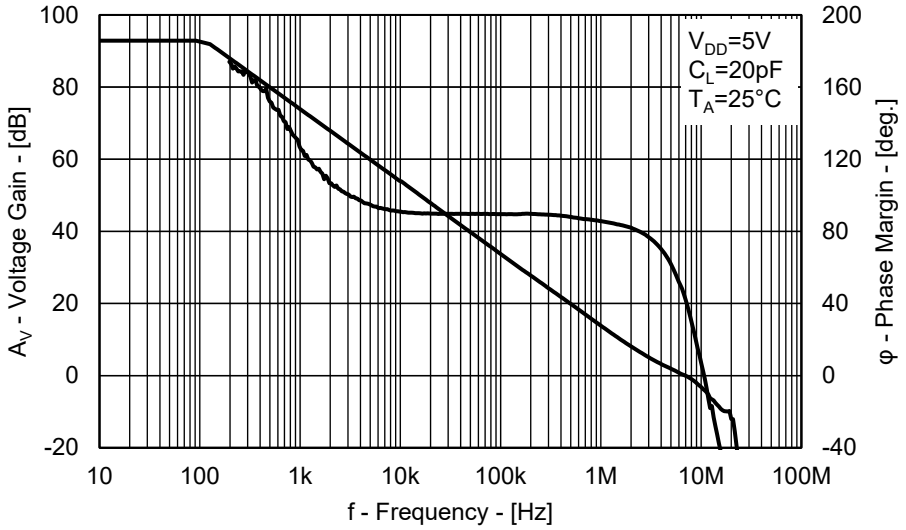


V_O vs. $I_{O\ SINK}$

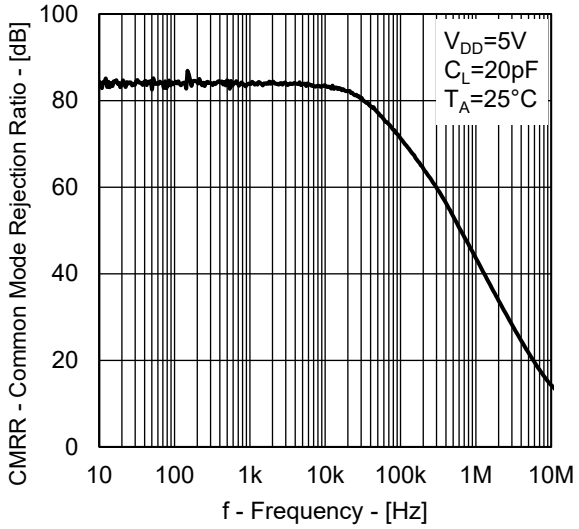


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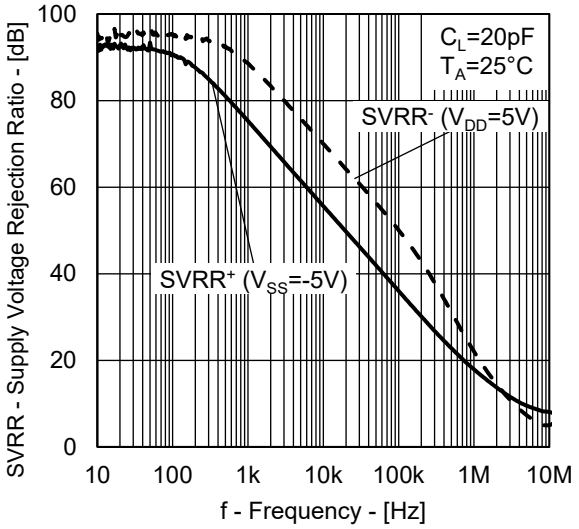
A_V, φ vs. f



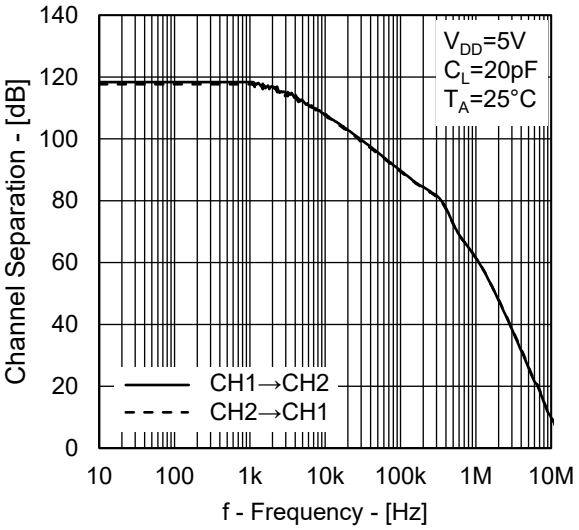
CMRR vs. f



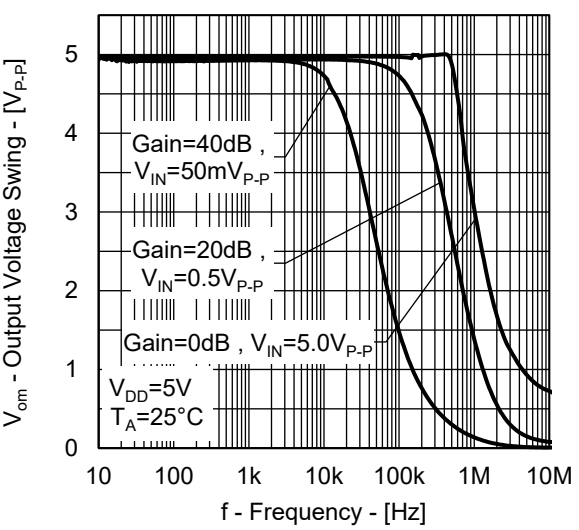
SVRR vs. f



Channel Separation vs. f



V_{om} vs. f

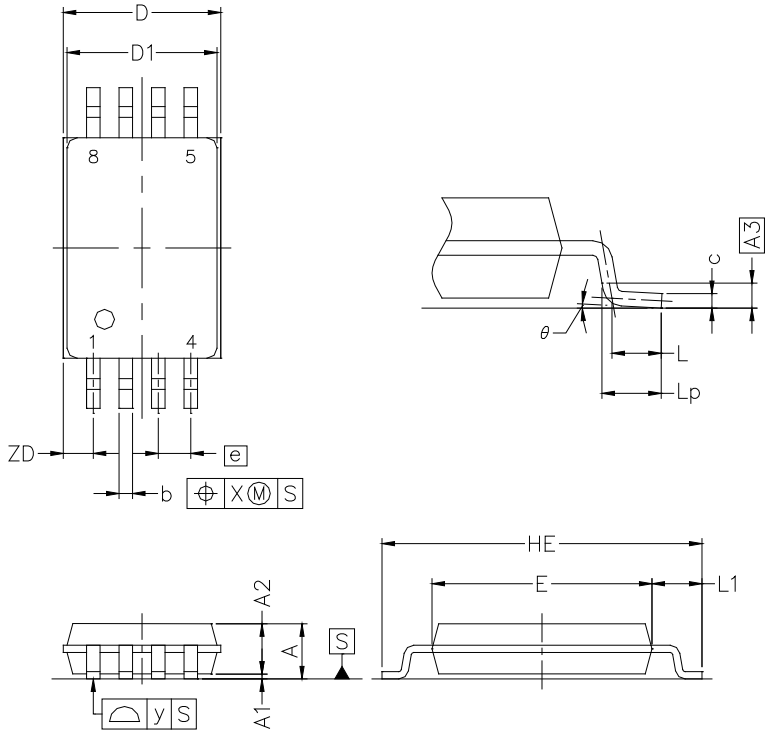


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PACKAGE DRAWINGS

8-PIN PLASTIC TSSOP

JEITA Package code	RENESAS code	Previous code	MASS(TYP.) [g]
P-TSSOP8-0225-0.65	PTSP0008JD-A	P8GR-65-9LG	—



(Unit : mm)

NOTE

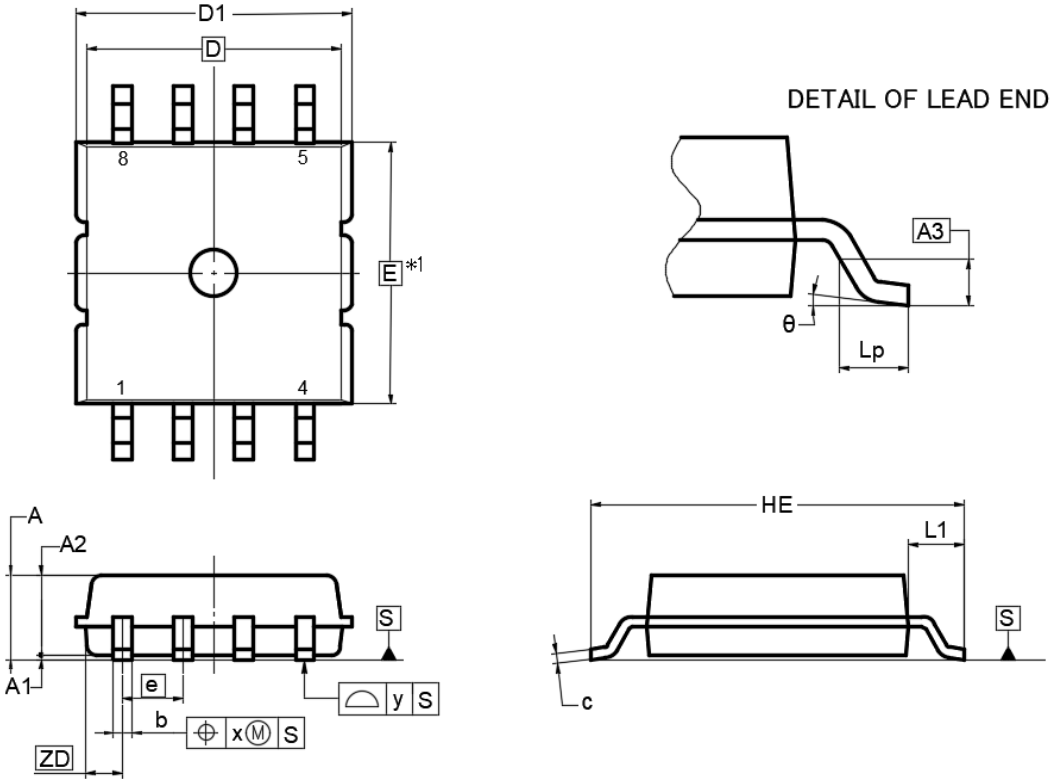
Each lead centerline is located within 0.10 mm of its true position at maximum material condition.

ITEM	MILLIMETERS
D	3.15 ±0.15
D1	3.00 ±0.10
E	4.40 ±0.10
HE	6.40 ±0.20
A	1.20 MAX.
A1	0.10 ±0.05
A2	1.00 ±0.05
A3	0.25
b	0.24 +0.06 -0.05
c	0.145 ±0.055
L	0.5
Lp	0.60 ±0.15
L1	1.00 ±0.20
θ	3° +5° -3°
e	0.65
x	0.10
y	0.10
ZD	0.60

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8-PIN PLASTIC MSOP

JEITA Package Code	RENESAS Code	MASS (TYP.) [g]
P-VSSOP8-2.75×2.8-0.65	PVSP0008JA-A	0.02[g]



NOTE)
1.DIMENSIONS"*1"
DO NOT INCLUDE MOLD FLASH.

2.EACH LEAD CENTERLINE IS LOCATED WITHIN 0.10 MM OF ITS TRUE POSITION AT MAXIMUM MATERIAL CONDITION.

(UNIT:mm)

ITEM	DIMENSIONS
D	2.75
D1	2.95±0.20
E	2.80
HE	4.00±0.30
e	0.65
b	$0.20^{+0.10}_{-0.05}$
A	1.00MAX
A1	0.05±0.05
A2	0.85±0.10
A3	0.25
L1	0.60±0.20
c	$0.13^{+0.10}_{-0.05}$
Lp	0.37±0.12
x	0.10
y	0.10
θ	7±7°
ZD	0.50

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(Rev.5.0-1 October 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
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