USB PD DUAL-ROLE POWER (DRP) CONTROLLER WITH I2C INTERFACE

Description

The AP53782 is a highly integrated USB Type-C® PD3.1 Dual-Role Power (DRP) controller to support Extended Power Range (EPR)/ Adjustable Voltage Supply (AVS) up to 28V and Standard Power Range (SPR)/Programmable Power Supply (PPS) up to 21V.

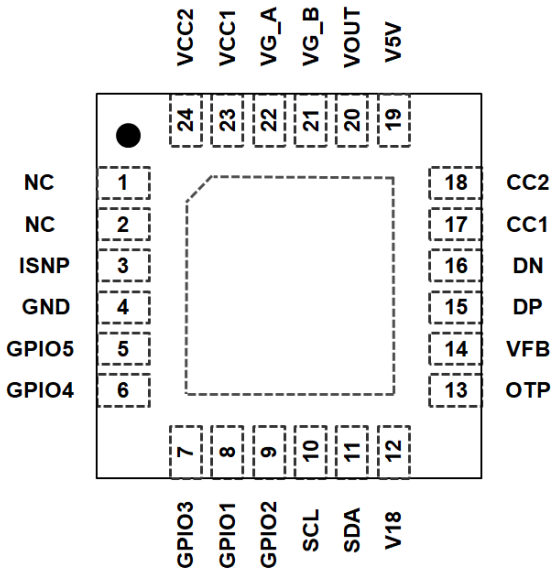
The AP53782 is targeting for operating with external MCU through the I2C Interface pins (SCL, SDA) and interrupt mechanism. With the I2C registers and commands defined by AP53782, the host MCU could control the AP53782 to act as a sink controller to get desired Request Data Object (RDO) from a PD3.1 compliant source adapter, or to play as a source PD controller to provide Power Data Object (PDO) capability to supply a Type-C connector-equipped device (TCD). The AP53782 could consume as low as 50μA to meet requirement of equipped battery-power devices during the power down mode.

The AP53782 supports the QC2.0/3.0 functions and dead battery during the sink role and provides both I2C control and VFB feedback for the external DC/DC controller during the power negotiation. Meanwhile, the host MCU could further inquire about the status of various I2C registers for intended applications. The AP53782 integrates Rp/Rd termination resistors and switches for DRP control. It operates from 3.6V up to 28V with low-side current sense topology.

Based on high-voltage process, the AP53782 offers short-protection between CC1/CC2 (CCx) pins to adjacent high-voltage pin up to 34V. The smart built-in firmware of the AP53782 offers comprehensive safety protection schemes, including overvoltage protection (OVP), undervoltage protection (UVP), overcurrent protection (OCP), and moisture detection for the USB connector.

Pin Assignments

(Top View)



W-QFN4040-24 (Type A1)

Features

- USB PD3.1 v1.8 Certified with TID: 11689
- Support Autonomous DRP Control
- Support EPR/AVS up to 28V with 100mV/Step
- Support SPR/PPS up to 21V with 20mV/Step and 50mA/Step
- Support Power-Down Consumption as Low as 50μA
- Support Status Register for System Monitor and Control
- Support I2C Commands for PDO and RDO Selections
- Support I2C Commands for External MCU to Monitor and Control
- Support QC2.0/3.0 Sink and Source Controls
- Support Dual Gate Drivers for VBUS nMOS Switches
- Support VFB Feedback Through Current DAC for External DC/DC
- Operating Voltage 3.6V to 28V with Low-Side Current Sense
- Support Dead-Battery Mode
- Support VBUS and VOUT Discharge Paths
- Support OVP/UVP/OCP with Auto Restart
- Support Moisture Detection for the USB Connector
- VBUS Short Protection on CC1/CC2 Pins up to 34V
- VBUS Short Protection on DP/DN Pins up to 24V
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/104/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please contact us or your local Diodes representative. https://www.diodes.com/quality/product-definitions/**

Applications

- Power banks
- Power tools
- Wireless speakers
- E-bikes
- POS terminals
- Portable displays

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

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Typical Applications Circuit

The AP53782 acts as a USB PD DRP controller after the power-on initialization. The AP53782 alternates periodically the Type-C CCx pin connections between the pulldown resistance, Rd, and pullup resistance, Rp. After the negotiation, the AP53782 will decide if it serves as Type-C source or sink controller.

The AP53782 is targeting for operating with host MCU via the I2C Interface pins (SCL, SDA) and interrupt mechanism. With the I2C registers and commands defined by AP53782, the host MCU could control the AP53782 to play as a sink controller to get desired RDO from a PD3.1 compliant source adapter, or to play as a source PD controller to provide PDO capability to supply a TCD device. The AP53782 could consume as low as 50μA to meet the requirement of equipped battery-power devices during the power-down mode.

As shown in Figure 1 below, the AP53782 provides multi-master I2C communication for the host MCU and other I2C based components, where the AP53782 not only acts as an I2C master to control an external bi-directional DC/DC controller, but also simultaneously acts as I2C slave device to receive the control signals from the host MCU. The AP53782 provides 2 gate drivers for the external VBUS nMOS switch control of single-direction or bi-direction DC/DC controller. Besides, it supports VFB control for DC/DC controller during the power profile negotiation.

Meanwhile, the AP53782 supports QC2.0/3.0 functions and dead battery operation during the sink role. In addition, the AP53782 operates from 4.5V up to 28V with 5mΩ low-side current sense topology. The discharge paths for VBUS are built in the AP53782 chip.

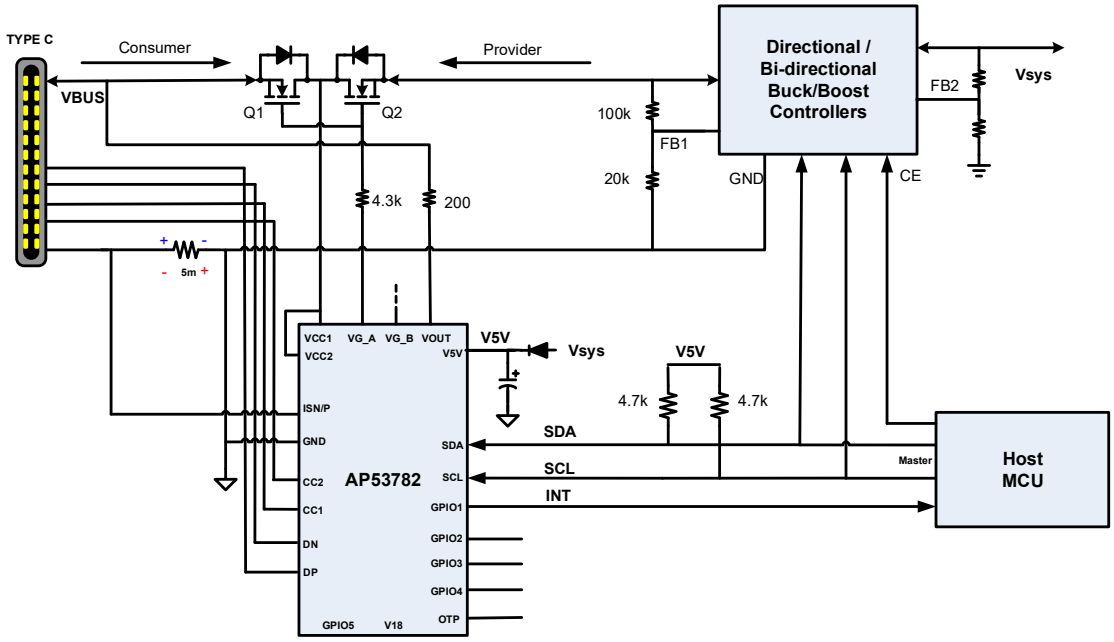


Figure 1. The AP53782 can support multi-master I2C communication topology, where AP53782 acts as the I2C master to control the DC/DC controller and simultaneously acts as the I2C slave to receive control signals from the host MCU.

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Pin Descriptions

Pin No.	Pin Name	Type (Note 4)	Pin Function
1	NC	—	No Connection
2	NC	—	No Connection
3	ISNP	AI	Current Sense Node
4	GND	GND	Chip Ground Pin
5	GPIO5	DIO	General-Purpose Input/Output Pin or Constant Current Source Output
6	GPIO4	DIO	General-Purpose Input/Output Pin or Constant Current Source Output
7	GPIO3	DIO	General-Purpose Input /Output Pin or Constant Current Source Output
8	GPIO1	DIO	General-Purpose Input/Output Pin or UART
9	GPIO2	DIO	General-Purpose Input/Output Pin or UART
10	SCL	DIO	Clock pin of I2C bus or UART, need to be pulled up externally.
11	SDA	DIO	Data pin of I2C bus or UART, need to be pulled up externally.
12	V18	DP	LDO Output Pin. Needs to connect a decoupling capacitor (10nF) to GND. This LDO is just to supply internal digital circuit. This pin cannot drive external load.
13	OTP	AIO	100μA Current Source Output for NTC Connected to Ground. This NTC is used to monitor temperature variation.
14	VFB	AI	Analog Voltage Feedback Input for External PWM Controller
15	DP	AIO	DP of Type-C Connector
16	DN	AIO	DN of Type-C Connector
17	CC1	AIO	Configuration Channel 1 (CC1) of Type C
18	CC2	AIO	Configuration Channel 2 (CC2) of Type C
19	V5V	AP	Output of the Internal LDO with VCC as Input. A 1μF cap is required to connect this pin to GND. When VCC is off, V5V pin could be an alternative power path for the AP53782 when provided a 5V external power.
20	VOUT	AHV	VOUT Terminal. It is used to detect output voltage and provides a discharge path with connecting an external 200Ω resistor in series.
21	VG_B	AHV	High-Voltage Gate Driver_B for External nMOS VBUS Switch
22	VG_A	AHV	High-Voltage Gate Driver_A for External nMOS VBUS Switch
23	VCC1	AHV	Chip power supply input when VBUS is active. The power will enter the chip through the body diode of VBUS nMOS switch.
24	VCC2	AHV	Voltage Detection Input and Discharge Path
—	EPAD	GND	Exposed pad is suggested to connect to GND pin.

Note: 4. AHV – Analog High Voltage pin.
AP – Power for Analog Circuit and Analog I/O pins, 5.0V operation.
AI – Analog Input pin.
DP – Power for Digital Circuit operation.
AIO – Analog Input/Output pin with 5.0V operation. However, DP/DN & CC1/CC2 pins are 3.3V operation.
DI – Digital Input pin. All are 5.0V operation.
DO – Digital Output pin. All are 5.0V operation.
DIO – Digital Input/Output pin. All are 5.0V operation.

Table 1. The pin descriptions of AP53782 PD3.1 DRP controller

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Functional Block Diagram

The AP53782 block diagram is shown in Figure 2 below, where the external host MCU is used for the operation of this DRP controller. Both source and sink roles support USB PD3.1 and QC protocols.

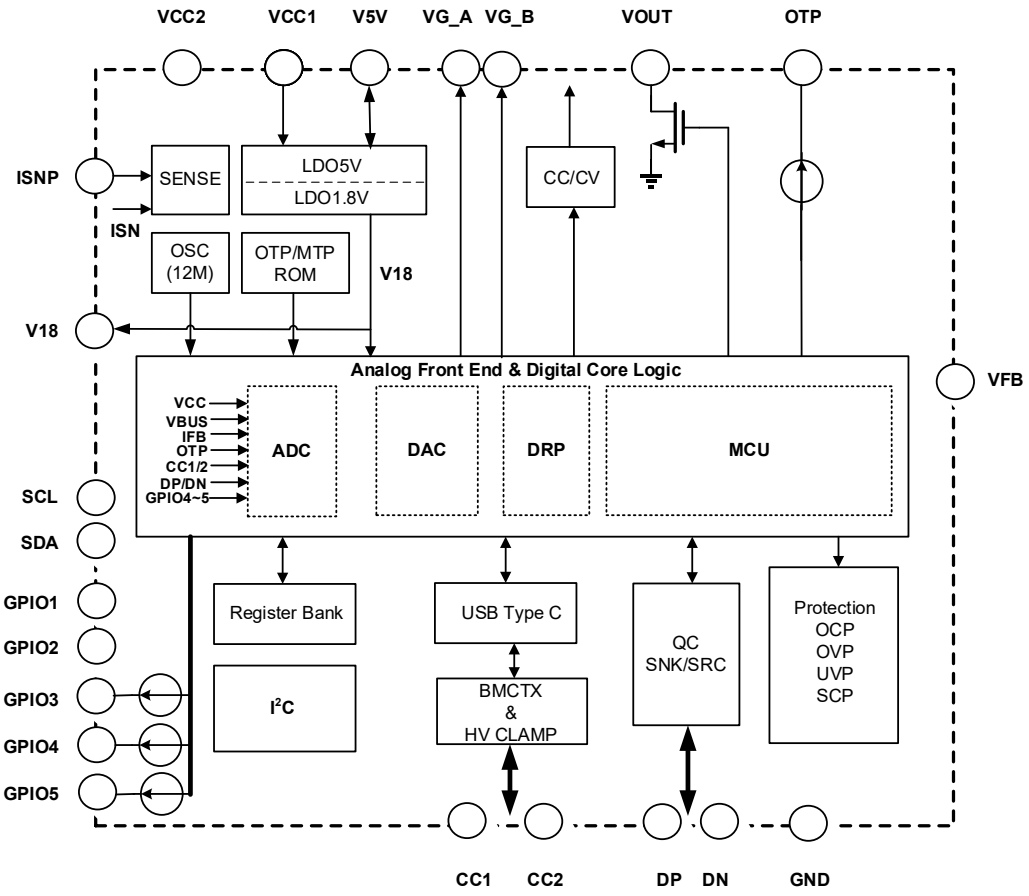


Figure 2. The AP53782 block diagram is shown as above.

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Absolute Maximum Ratings (Note 5)

Symbol	Parameter	Rating	Unit
V_{VCC1}, V_{VCC2}	Input Voltage at VCC1, VCC2 Pins	-0.3 to 34	V
V_{VFB}	Input Voltage at VFB Pin	-0.3 to 7	V
V_{VOUT}, V_{VG_A}, V_{VG_B}	Input Voltage at VOUT, VG_A, VG_B Pins	-0.3 to 38	V
—	Voltage from VG_A, VG_B to VCC2 Pin	-38 to 7	V
V_{V5V}	Input Voltage at V5V Pin	-0.3 to 7	V
V_{V18}, V_{ISNP}	Input Voltage at V18, ISNP Pins	-0.3 to 2	V
V_{CC1}, V_{CC2}	Input Voltage at CC1, CC2 Pins	-0.3 to 31	V
V_{DP}, V_{DN}	Input Voltage at DP, DN Pins	-0.3 to 24	V
V_{SCL}, V_{SDA}	Input Voltage at SCL, SDA Pins	-0.3 to 7	V
V_{GPIO1} to V_{GPIO5}, V_{OTP}	Input Voltage at GPIO1 to GPIO5, OTP Pins	-0.3 to 7	V
T_J	Operating Junction Temperature	-40 to +150	°C
T_{STG}	Storage Temperature	-65 to +150	°C
T_{LEAD}	Lead Temperature (Soldering, 10s)	+300	°C
ESD	Human Body Model	2	kV
ESD	Charged Device Model	750	V

Note: 5. Stresses greater than those listed under *Absolute Maximum Ratings* can cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to *Absolute Maximum Ratings* for extended periods can affect device reliability.

Package Thermal Information (Note 6)

Symbol	Parameter	Value	Unit
$R_{\theta JA}$	Junction-to-Ambient Thermal Resistance	29.6	°C/W
$R_{\theta JC(top)}$	Junction-to-Case (Top) Thermal Resistance	20.6	°C/W
$R_{\theta JB}$	Junction-to-Board Thermal Resistance	11.2	°C/W
Ψ_{JT}	Junction-to-Top Characterization Parameter	0.4	°C/W
Ψ_{JB}	Junction-to-Board Characterization Parameter	11.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-Case (Bottom) Thermal Resistance	6.0	°C/W

Note: 6. Test condition: device mounted on FR-4 substrate PC board, 2oz copper, with the minimum footprint.

Recommended Operating Conditions

Symbol	Parameter	Min	Max	Unit
V_{VCC1}, V_{VCC2}	Power Supply Voltage VCC1, VCC2 Pins	3.6	31	V
V_{V5V}	Input Voltage at V5V Pin	3	5.5	V
V_{VFB}	Input Voltage at VFB Pin	0	5	V
V_{V18}	Input Voltage at V18 Pin	0	2	V
V_{SDA}, V_{SCL}	Input Voltage at SDA, SCL Pins	0	5.5	V
V_{GPIO1} to V_{GPIO5}	Input Voltage at GPIO1 to GPIO5 Pins	0	5.5	V
V_{DP}, V_{DN}	Input Voltage at DP, DN Pins	0	3.7	V
V_{OTP}	Input Voltage at OTP Pin	0	5.5	V
T_A	Operating Ambient Temperature	-40	+85	°C
T_J	Operating Junction Temperature	-40	+125	°C

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Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Power Supply Section (Note 7)						
V_{VCC1}	VCC1 Operating Voltage	—	2.5	3	3.5	V
V_{VCC1_HYS}	VCC1 Hysteresis	—	—	0.3	—	V
I_{VCC1}	VCC1 Operating Current	—	—	2.5	6	mA
I_{VCC1_SLEEP}	VCC1 Input Current in Sleep Mode	CC1/2 detach	—	550	700	μA
$I_{VCC1_SLEEP_DRP}$	VCC1 Input Current in Sleep Mode under DRP Toggling Without Connection	—	—	30	50	μA
V_{VBUS_DB}	VBUS Voltage for Dead-Battery Mode	—	3.5	—	—	V
V5V Output						
V_{V5V}	V5V Output Voltage	—	4.4	5	5.4	V
I_{V5VOCP}	V5V Output Current Capability	—	—	30	—	mA
V_{VDRV_DO}	V5V Output Dropout	I_{VDRV} = 40mA	—	100	—	mV
Constant Voltage (CV) Control						
V_{VBUS_CV5}	VBUS Voltage for 5V CV Control	—	4.85	5	5.15	V
V_{VBUS_LSB}	VBUS Step per LSB	—	—	10	—	mV
V_{VBUS_Range}	VBUS Range	—	3.6	—	28	V
ΔVBUS%	VBUS Regulation Accuracy	VBUS = 3.6V to 28V	97	—	103	%
V_{CABLE}	Cable Compensation (Notes 8, 10)	VBUS = 3.6V to 28V	—	30	—	mV/A
Constant Current (CC) Control						
I_{CC_Range}	CC Range	—	1	—	5	A
CC_{1A3A}	Current Sense and CC Loop Correction	R_{SENS} = 5mΩ I_L = 1A to 3A	-150	—	150	mA
CC_{3A5A}	Current Sense and CC Loop Correction	R_{SENS} = 5mΩ I_L = 3A to 5A	-5	—	5	%
t_{CC}	CC Load Transient Current Settling Time	—	—	—	250	ms
t_{CCCV}	CC to CV Transient Voltage Settling Time	—	—	—	270	ms
SR_{IL}	Max Load Slew Rate for IL Changes (Note 10)	—	-150	—	150	mA/μs
Protection Function						
V_{OVP5V_SNK}	5V VBUS OVP @Sink	(Note 9)	6.3	7	7.7	V
V_{OVP9V_SNK}	9V VBUS OVP @Sink	(Notes 9, 10)	—	11	—	V
V_{OVP15V_SNK}	15V VBUS OVP @Sink	(Notes 9, 10)	—	17	—	V
V_{OVP20V_SNK}	20V VBUS OVP @Sink	(Notes 9, 10)	—	22	—	V
V_{OVP28V_SNK}	28V VBUS OVP @Sink	(Notes 9, 10)	—	30	—	V
$t_{DEBOUNCE_OVP_SNK}$	OVP Debounce Time @Sink	(Note 11)	—	30	—	ms
V_{OVP5V_SRC}	5V VBUS OVP @Source	(Note 9)	5.5	6	6.6	V
V_{OVP9V_SRC}	9V VBUS OVP @Source	(Notes 9, 10)	—	10.8	—	V
V_{OVP15V_SRC}	15V VBUS OVP @Source	(Notes 9, 10)	—	18	—	V
V_{OVP20V_SRC}	20V VBUS OVP @Source	(Notes 9, 10)	—	24	—	V
V_{OVP28V_SRC}	28V VBUS OVP @Source	(Notes 9, 10)	—	30.8	—	V
$t_{DEBOUNCE_OVP_SRC}$	OVP Debounce Time @Source	(Note 11)	—	3	—	ms

Notes:
7. There are 2 power suppliers for chip: VCC1 pin and V5V(IN) pin, as shown in Figure 3 and Figure 4.
8. Cable compensation voltage can be adjusted by setting from 0 to N*V_{CABLE}, by setting where N is from 0 to 7.
9. OVP: 120%*PDO @Source, 110%*PDO @Source > 28V, 2V+RDO @Sink.
   UVP: 80%*PDO @Source, 80%*RDO @Sink.
   OCP: 110%*IPDO and 110%*IRDO
10. Guaranteed by design.
11. OVP blanking time during V_O transition from high output voltage to low output voltage, such as 9V to 5V, or 20V to 5V.

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Electrical Characteristics (continued) (@T_A = +25°C, unless otherwise specified.)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Protection Function (continued)						
V_{UVP5V_SNK}	5V VBUS UVP @Sink	(Note 9)	3.5	4	4.5	V
V_{UVP9V_SNK}	9V VBUS UVP @Sink	(Notes 9, 10)	—	7.2	—	V
V_{UVP15V_SNK}	15V VBUS UVP @Sink	(Notes 9, 10)	—	12	—	V
V_{UVP20V_SNK}	20V VBUS UVP @Sink	(Notes 9, 10)	—	16	—	V
V_{UVP28V_SNK}	28V VBUS UVP @Sink	(Notes 9, 10)	—	22.4	—	V
$t_{DEBOUNCE_UVP_SNK}$	UVP Debounce Time @Sink	—	—	30	—	ms
V_{UVP5V_SRC}	5V VBUS UVP @Source	(Note 9)	3.5	4	4.5	V
V_{UVP9V_SRC}	9V VBUS UVP @Source	(Notes 9, 10)	—	7.2	—	V
V_{UVP15V_SRC}	15V VBUS UVP @Source	(Notes 9, 10)	—	12	—	V
V_{UVP20V_SRC}	20V VBUS UVP @Source	(Notes 9, 10)	—	16	—	V
V_{UVP28V_SRC}	28V VBUS UVP @Source	(Notes 9, 10)	—	22.4	—	V
$V_{UVP5V_SRC_QC}$	5V VBUS UVP @Source (QC)	(Note 9)	3.5	4	4.5	V
$V_{UVP9V_SRC_QC}$	9V VBUS UVP @Source (QC)	(Notes 9, 10)	3.5	4	4.5	V
$V_{UVP12V_SRC_QC}$	15V VBUS UVP @Source (QC)	(Notes 9, 10)	3.5	4	4.5	V
$t_{DEBOUNCE_UVP_SRC}$	UVP Debounce Time @Source	—	—	30	—	ms
OCP_{1A}	Overcurrent Protection (110%)	—	0.95	1.1	1.25	A
OCP_{3A}	Overcurrent Protection (110%)	—	3.15	3.3	3.45	A
OCP_{5A}	Overcurrent Protection (110%)	—	5.25	5.5	5.75	A
t_{OCP}	OCP Deglitch Time	—	—	30	—	ms
t_{SCP}	SCP Debounce Time @Source	—	—	4	—	ms
$t_{RESTART_INTERVAL_SCP}$	SCP Recovery Time @Source	—	—	0.8	—	s
T_{OTP}	Internal OTP Temperature	—	—	+130	—	°C
$T_{OTP-HYS}$	Internal OTP Temperature Hysteresis	—	—	+30	—	°C
CC1/CC2 (CCx) Pin Section						
V_{OH_CCX}	Pull High Voltage of CCx	—	3.0	3.3	3.6	V
I_{Rp_80}	CCx Pullup Current as SRC – Default	R_D = 5.1kΩ	—	80	—	μA
I_{Rp_180}	CCx Pullup Current as SRC – 1.5 A	R_D = 5.1kΩ	—	180	—	μA
I_{Rp_330}	CCx Pullup Current as SRC – 3.0 A	R_D = 5.1kΩ	303.6	330	356.4	μA
V_{ATH_80}	Attach Detection of CCx – Default	R_D = 5.1kΩ	—	0.408	—	V
V_{ATH_180}	Attach Detection of CCx – 1.5A Mode	R_D = 5.1kΩ	—	0.918	—	V
V_{ATH_330}	Attach Detection of CCx – 3.0A Mode	R_D = 5.1kΩ	1.30	1.68	1.98	V
V_{CCx_OVP}	CCx Overvoltage Protection	—	5.2	5.6	6.1	V
V_{RdCCX_80}	Source = 80μ for Dead Battery	—	0.78	0.93	1.08	V
V_{RdCCX_180}	Source = 180μ for Dead Battery	—	0.9	1.057	1.2	V
V_{RdCCX_330}	Source = 330μ for Dead Battery	—	1.02	1.178	1.32	V
t_{SLEEP}	Enter Sleep Mode Time after Cable Detached	—	—	3	—	s

Notes: 9. OVP: 120%*PDO @Source, 110%*PDO @Source > 28V, 2V+RDO @Sink.
UVP: 80%*PDO @Source, 80%*RDO @Sink.
OCP: 110%*IPDO and 110%*IRDO
10. Guaranteed by design.

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Electrical Characteristics (continued) (@T_A = +25°C, unless otherwise specified.)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
USB PD Transceiver						
V_{OH_TxDC}	Output High of CCx for BMC Tx	(Note 10)	1.05	1.125	1.2	V
V_{OL_TxDC}	Output Low of CCx for BMC Tx	(Note 10)	—	—	0.075	V
V_{IH_RX}	Noise Margin for BMC Rx	(Note 10)	0.25	—	0.85	V
V_{TH_RX}	Vth of BMC_RX	(Note 10)	—	0.55	—	V
t_{R_Tx}	Rising Time of CCx for BMC Tx	(Note 10)	300	—	—	ns
t_{F_Tx}	Falling Time of CCx for BMC Tx	(Note 10)	300	—	—	ns
DP/DN and QC Section (Source+Sink)						
$V_{OVP_DP/DN}$	DP/DN Line OVP Threshold	—	4.2	4.5	4.8	V
V_{DP/DN_APP}	DP/DN Apple Mode 2.7V Output	—	2.48	2.68	2.88	V
V_{DP/DN_0P6V}	DP/DN DCP 0.6V Output Voltage	Source Current 250μA	—	0.6	—	V
R_{DP/DN_DWN20k}	DP/DN 20k Pulldown Resistor	—	16	20	24	kΩ
$R_{DP/DN_DWN900k}$	DP/DN 900k Pulldown Resistor	—	700	900	1200	kΩ
R_{DP/DN_short}	DPDN Short Resistor	—	5	20	40	Ω
R_{DN_IMP}	Impedance Check at DN	—	175	275	505	Ω
$V_{OH_DP/DN}$	Output High Voltage of DP/DN	Source Current 2mA	2.9	3.1	3.6	V
$V_{OL_DP/DN}$	Output Low Voltage of DP/DN	Sink Current 2mA	—	—	200	mV
VCONN Capability						
V_{CONN_DROP}	V_{CONN_DROP} Voltage (V5V-V_{CONN})	Source Current 20mA	—	600	—	mV
DRP Section						
I_{DRPNC}	DRP Current Consumption While Toggling Without Connection	—	—	30	—	μA
t_{DRP}	DRP t_{Rp} + t_{Rd} Cycle Time	—	—	80	—	ms
D_{Rp}	Duty of Rp During a DRP Cycle	—	—	50	—	%
Gate Drivers for VG_A and VG_B						
$V_{VG_A_SO}$	VG_A Gate to Source Overdrive	V_{VBUS} = 5V	3	—	—	V
$I_{_SRC}$	Driving Capability	V_{GS} = 2.5V	—	10	—	μA
t_{ON}	Turn-On Time	V_{GS} = 3.5V & C_{load} = 10nF	—	6.5	—	ms
VBUS and VOUT Discharge Current						
I_{DISCHG_VBUS}	Discharge Current for VBUS Pin	V_{VBUS} = 5V	—	150	—	mA
I_{DISCHG_VOUT}	Discharge Current for VOUT Pin	V_{VOUT} = 5V	—	90	—	mA

Note: 10. Guaranteed by design.

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Electrical Characteristics (continued) (@T_A = +25°C, unless otherwise specified.)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
ADC Section						
N_{ADC}	Resolution	(Note 10)	—	8	—	bit
V_{VREF_ADC}	Reference Voltage of ADC	—	2.026	2.046	2.066	V
DNL_{ADC}	DNL	(Note 10)	—	4	—	LSB
INL_{ADC}	INL	(Note 10)	—	2	—	LSB
FS_{ADC}	ADC Sampling Frequency	(Note 10)	—	66	—	kHz
I2C Interfaces						
V_{IH}	Input High Threshold of SCL/SDA	—	1.4	—	—	V
V_{IL}	Input Low Threshold of SCL/SDA	—	—	—	0.4	V
$I_{SINK_SCL/SDA}$	SCL/SDA Pin Sink Current	—	—	4	—	mA
GPIO and OTP Pins						
V_{IH}	Input High Threshold Voltage of GPIO	—	1.4	—	—	V
V_{IL}	Input Low Threshold Voltage of GPIO	—	—	—	0.4	V
V_{OH}	Output High Level Voltage of GPIO	Source Current 4mA	4.3	—	—	V
V_{OL}	Output Low Level Voltage of GPIO	Sink Current 4mA	—	—	300	mV
$I_{GPIO4\sim5}$	GPIOs Used as Current Source	—	—	20	—	μA
I_{OTP}	OTP Current Source Capability	(Note 10)	—	100	—	μA

Note: 10. Guaranteed by design.

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Functional Overview

AP53782 Overview

The AP53782 is a highly integrated USB Type-C DRP port controller that complies with the latest USB PD3.1 standards and is targeted at power bank applications that need an external MCU to handle the desired sink RDO and source PDO data via the I2C interface.

The AP53782 includes a USB Type-C CC logic and PD transceiver, DRP operation and power control, constant current and constant voltage (CC/CV) loops, power protections for sink and source, I2C interface for RDO and PDO selection, and an embedded 8-bit 1T 8051 compatible MCU to handle protocol handshake. It is designed to support Extended Power Range (EPR)/Adjustable Voltage Supply (AVS) up to 28V and Standard Power Range (SPR)/Programmable Power Supply (PPS) up to 21V.

Chip Power Overview

The AP53782 that uses a typical DC/DC controller for power bank application is illustrated in Figure 3. It is powered from either V5V pin from Vsys, or VCC1 pin from VBUS.

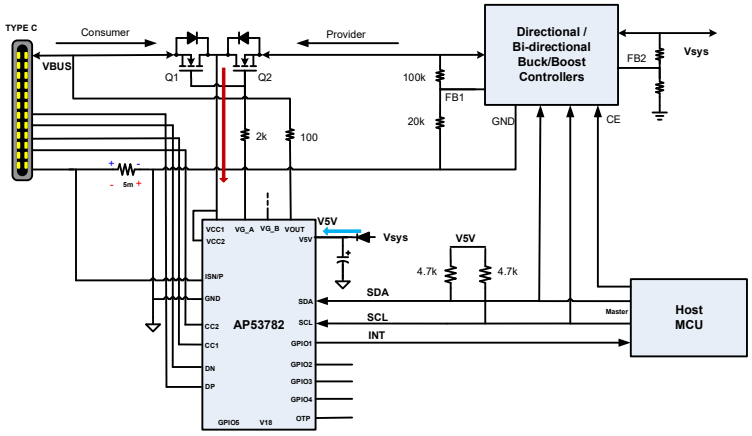


Figure 3. The AP53782 chip power is coming from system injection: Vsys, or VCC1 connection from VBUS

When no cable attachment happened, the VBUS is not active to provide power to the AP53782. The TCD system can be initialized by feeding AP53782 power from V5V pin via connecting Vsys with a suitable DC power supply. The Vsys will enter the internal V5V power path through an external diode, providing operation of the AP53782 other than the high voltage area and the external circuitry connected to V5V. At the same time, the TCD device is waiting for cable attachment.

As soon as the cable is attached, the AP53782 DRP role will make it act as a consumer or provider. No matter which role it will act, the gate driver is turned on by enabling VCC2, and there is a power supplied from the Q1 or Q2 VBUS switch to drive the VCC1 pin, as the red color direction shown in Figure 3. The VCC1 will enable the high voltage analog block, the V5V LDO to power the internal 5V circuitry. The extra LDOs also step the voltage down from 5V to 3.3V and 1.8V to provide the digital core circuitry and the I/O bonding pads. For system stability, both V5V and 1.8V pads are connected to do external decoupling. The AP53782 power supply plan is shown in Figure 4.

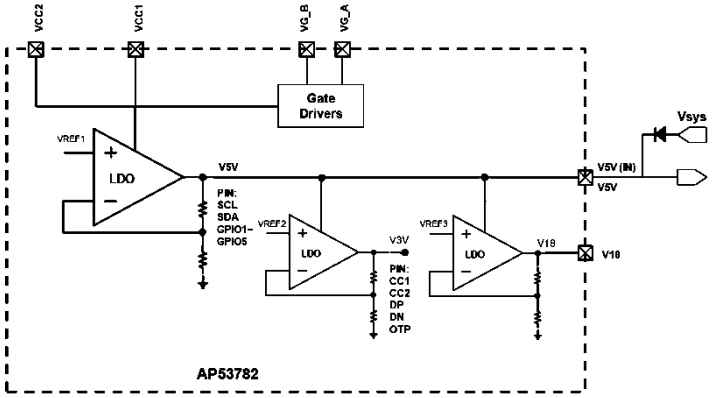


Figure 4. The AP53782 chip power plan

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Functional Overview (continued)

Dead-Battery Mode

When neither V5V nor VCC1 can provide chip power, the AP53782 enters the dead-battery mode by presenting a Rd resistance on its respective CCx pin. Once an active Type-C device is attached to this AP53782, the Rd resistance will allow the AP53782 to act as a sink device and enable a 5V output on the VBUS if the plugged-in device is a Type-C source or DRP controller. The 5V power supply will go through the body diode of the nMOS Q1 switch and feed into VCC1 pin to power on the AP53782 and the output node connected to V5V pin, as shown in Figure 5.

The AP53782 then enters the power-on initialization sequence by setting up its internal registers and receiving the RDO and PDO configuration parameters by the host MCU via I2C commands.

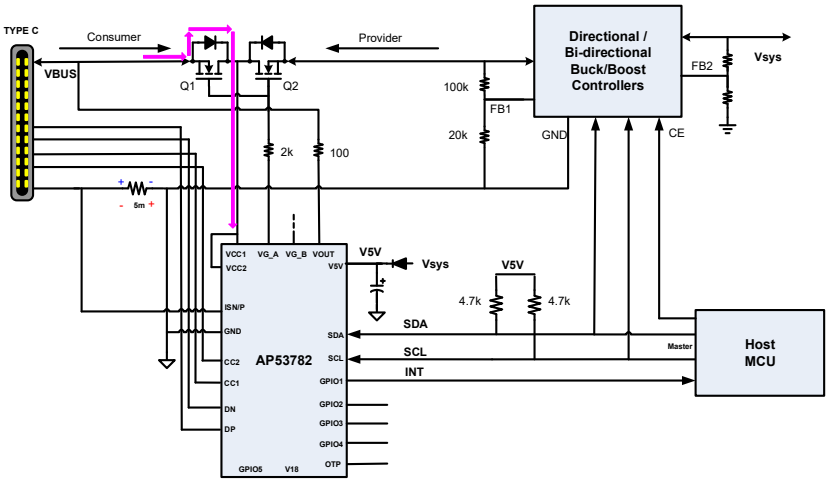


Figure 5. The Power path in dead-battery mode

Type-C Configuration Channel (CC) Logic

The CC1/CC2 (CCx) logic block includes all termination resistors (Rp and Rd), control switches, cable detection and connection logic. Rp and Rd resistors are required to implement cable detection, plug flip detection, and USB source/sink role establishing as required by the USB Type-C spec. As shown in Figure 6, the AP53782-based device communicates with the cable and another USB Type-C and PD device at the opposite end. The two CCx pins on the connector are used to implement a configuration process to establish and manage the source-to-sink connection.

The CCx pin voltage amplitude will depend on the resistor dividing effect of source Rp, sink Rd, and e-Marker Ra during the cable insertion. The AP53782 can then decide if the cable is attached, detached, or e-Marker embedded by detecting the CCx voltage. At the same time, the CCx voltage is used to configure which side serves as Type-C source or sink, and if Type-C cable is flipped or not.

After the source to sink connection is built up, the V_{CONN} switche is turned on by source to feed power to the cable through unconnected CC pin, and then the data path from source to sink is accomplished. Meanwhile, the VBUS switch is turned on to provide 5V from source to VBUS, and its current capability is assigned by the pullup resistor or current source on its CC pin.

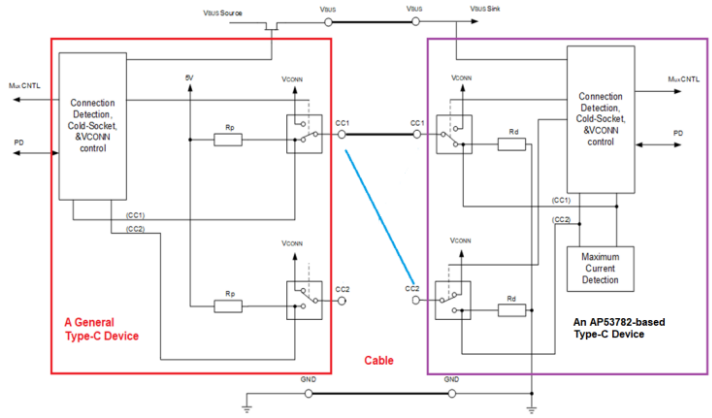


Figure 6. The AP53782-based Type-C PD device connects with another Type-C/PD device at the opposite end of the cable.

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Functional Overview (continued)

DRP Operation

The AP53782 plays as a USB PD DRP controller after the cable is plugged in. It toggles periodically the Type-C CCx pin connections between the pulldown resistance, Rd, and pullup resistance, Rp, as shown in Figure 7. When the AP53782 detects an Rd connected externally to CCx pin, it will act as a power provider and its PDO data are assigned by the host MCU via the I2C commands. If the AP53782 detects a Rp connected externally to CCx pin, it will play as a power consumer and its RDO data are assigned by the host MCU via the I2C commands. The Rp+Rd toggle period is fixed at 80ms, and 50% duty for Rp and Rd respectively. Here, the Rp resistors are implemented as current sources, I_{Rp}.

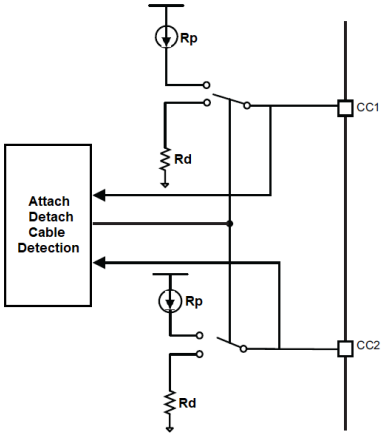


Figure 7. The AP53782 toggles CCx pin connections between Rp and Rd during the DRP handshake.

USB PD Physical Layer

The USB PD physical layer includes a USB Type-C baseband transceiver, physical-layer logic, and buffers for PD message handling, as shown in Figure 8. This transceiver performs the bi-phase Mark Coding (BMC), the 4b/5b encoding and decoding functions as well as integrating the analog front-end circuit. The BMC signal is output on the same pin (CC1 or CC2, aligned with the flip of the reversible USB Type-C cable) that is DC biased due to the cable attach mechanism. The transmitter driver overdrives the CC DC bias while transmitting but returns to a Hi-Z state, allowing the DC voltage to return to the CC level when it is not transmitting. All the communication is half-duplex, and the physical layer should implement collision avoidance to minimize communication errors on the configuration channel.

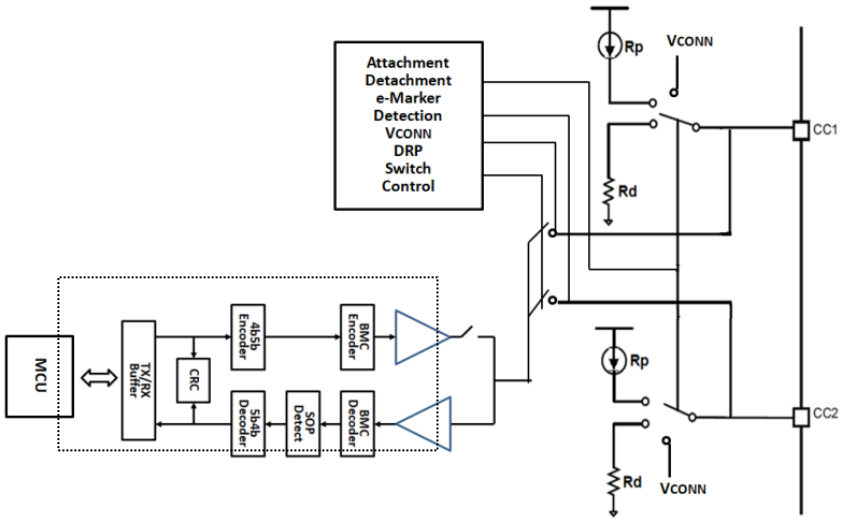


Figure 8. The USB PD uses BMC signaling and CC pin to communicate with another USB PD device.

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Functional Overview (continued)

VBUS Voltage Regulation and VFB Feedback

The AP53782 includes constant voltage (CV) loop for VBUS voltage regulation. Once the AP53782 acts as a source role, it will generate the PDO voltage to provide the attached device after the protocol handshake.

It uses a current DAC to sink or source the corresponding current directly from the external DC/DC feedback circuit according to requested PDO voltage, as shown in Figure 9 below. Due to the negative feedback loop, the current flowing through R1 is changed to keep VFB staying constant, and the VBUS is transitioned to a new level.

The current DAC in VFB pin has a LSB of 0.1 μA. That means if the feedback R1/R2 network of the external DC/DC is 100KΩ/20KΩ, then the VBUS voltage change resolution is 10 mV per step. It is recommended to choose R1/R2 resistors within 1% accuracy for a better matching in VBUS voltage.

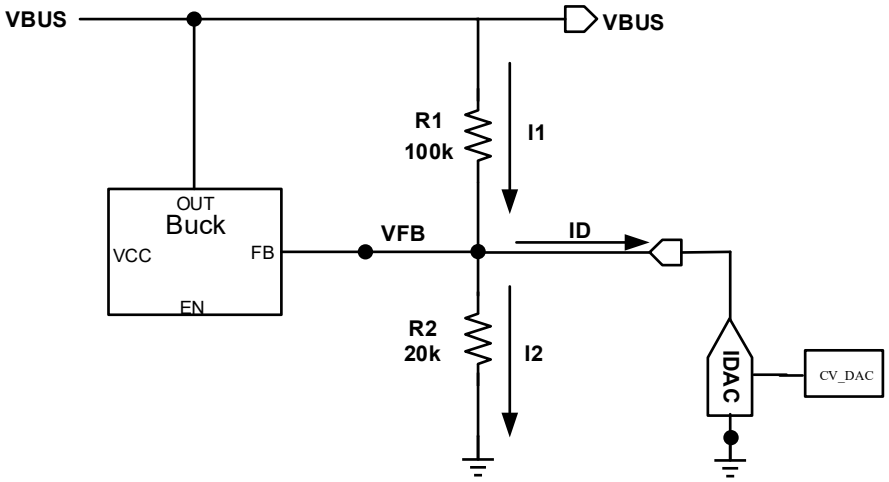


Figure 9. The current DAC is used to sink or source a current from the external DC/DC feedback network.

Constant Current Loop

The AP53782 provides a constant current (CC) loop to provide the PD PPS function and other kinds of protocol which uses CC function. The CC loop, as shown in Figure 10 below, is implemented by sensing the low side IR drop on Rsense resistor and monitoring the internal OCP flag at the same time. If the output current is high enough to make the IR drop larger than the predetermined output current limit set by DAC, the OCP flag is enabled. Once the flag is high, the output voltage will be reduced to keep the output current at constant.

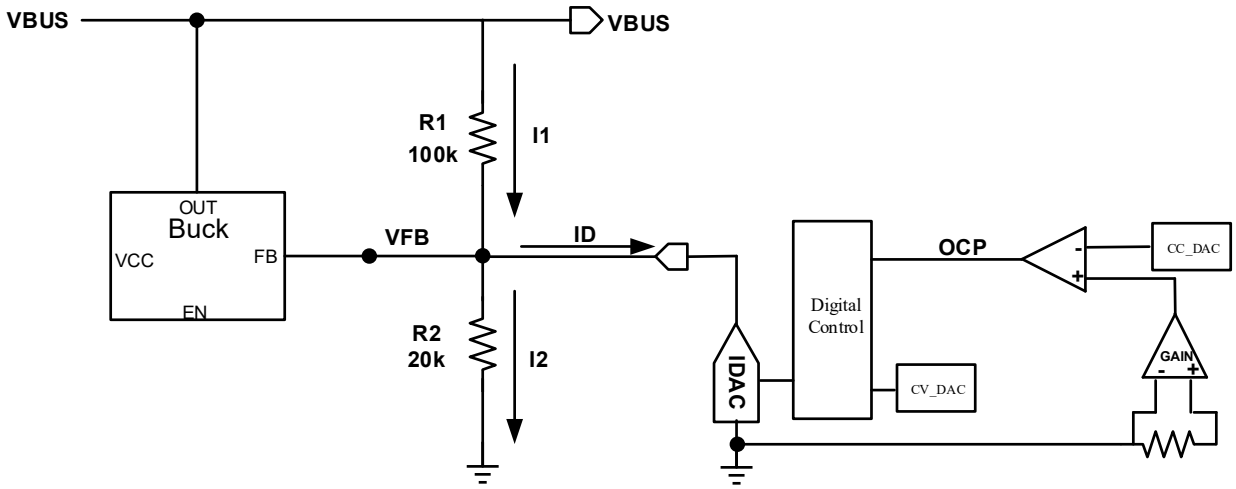


Figure 10. The constant current loop in AP53782

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Functional Overview (continued)

Power Protection in Source and Sink Modes

The AP53782 supports OVP/UVP/OCP power protection functions for source provider path and sink consumer path. The AP53782 provides two high-voltage gate drivers to drive external low-cost high-side nMOS switches for VBUS power on/off control. A 4.3kΩ resistance is suggested to connect the high-voltage gate drivers to the external nMOS gates. Figure 11 shows the consumer and provider paths for AP53782-based system.

The OVP threshold is set at 120% of contracted PDO, 110% of contracted PDO (≥ 28V) @ source and 2V+ RDO @sink. Once the VBUS voltage is higher than OVP threshold, the corresponding VBUS MOS is turned off and an internal discharge path from VBUS node to ground is turned on to reduce the overvoltage duration.

The UVP threshold is set at 80% of contracted PDO and RDO output. Once the VBUS voltage drops to UVP threshold, the corresponding VBUS MOS is turned off to avoid the abnormal operation of the electrical appliances.

The AP53782 integrates a low-side current sense amplifier that is capable of detecting current levels ranging from 100mA up to 6A across a 5mΩ external resistor. The OCP threshold is set at 110% of PDO and RDO maximum load. Once the VBUS output current is higher than OCP threshold, the AP53782 will shut down VBUS output. If AP53782 acts as a source, a “Hard Reset” command will be sent to the sink device at the same time. Based on high-voltage process, the AP53782 offers VBUS short protection for CCx pins up to 34V.

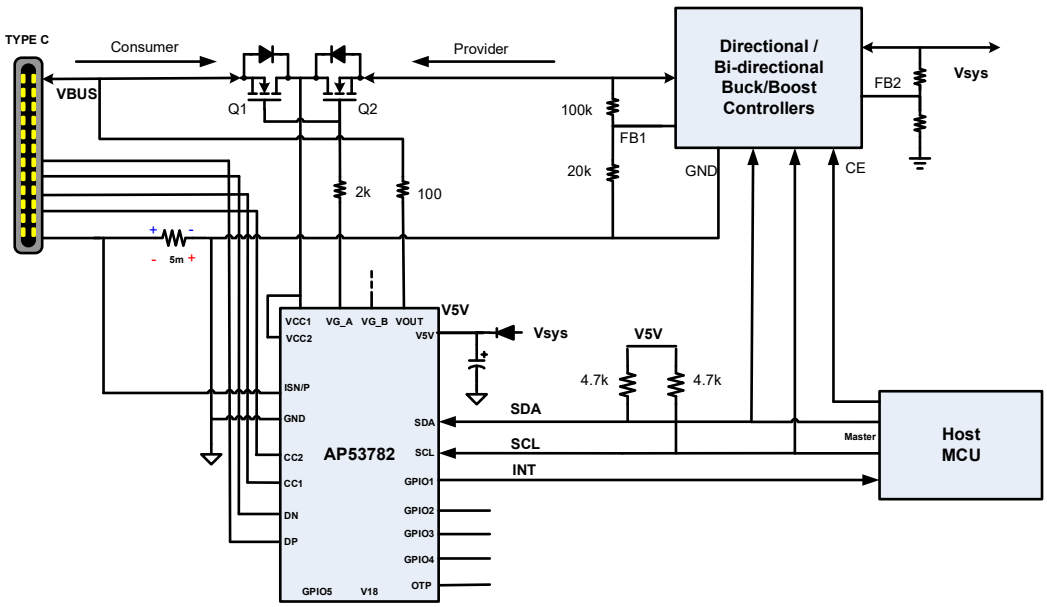


Figure 11. The consumer and provider paths for the AP53782-based system.

VBUS and VOUT Discharge Path

To meet the timing requirements of the USB PD specification, the AP53782 supports VBUS discharge paths to speed up the voltage decreasing speed of power path, where VCC2 and VOUT pins are respectively connected to an internal MOSFET and discharge resistor. Through the firmware control, the discharge paths act as a bleeder to help discharge the energy stored in the output capacitor. With this mechanism, VBUS can be regulated to 5V upon the detachment of a connected device, or to a lower desired output voltage level upon a request from the protocol handshake result, such as RDO and PDO voltage transition, and power protection. One 200Ω resistor between VBUS node and AP53782 VOUT pin is required.

ADC Converter

The AP53782 supports an internal successive approximation ADC. The input to the ADC is an analog multiplex that connects multiple inputs from various voltage and current sources in the chip. The proper signal could be digitized at the predetermined time and controlled by the firmware. The ADC output is available to be read and used by the embedded MCU. Through the data processing and appropriate algorithm, the AP53782 can make a precise management of the DRP controller.

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Functional Overview (continued)

QC Sink Support

The AP53782 not only provides QC source side but also provides the QC sink side for protocol communication handshake. The High Voltage Dedicated Charging Port (HVDCP) Detection Flow for QC sink support is shown in Figure 12 below.

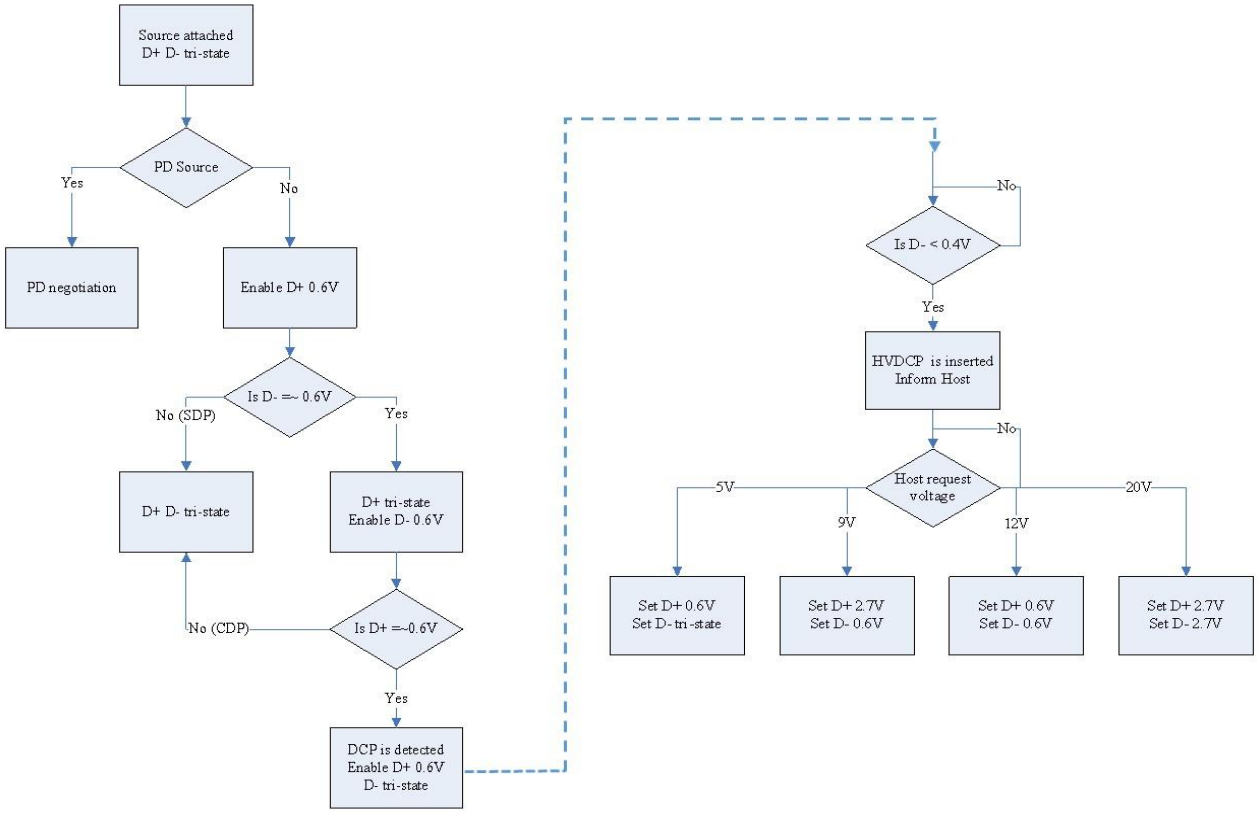


Figure 12. The AP53782 provides HVDCP detection flow for QC sink support.

I2C Interface and Control

The AP53782 provides an I2C interface with multi-master communication. The I2C interface consists of SCL and SDA pins, and some dedicated GPIO pin or I2C register polling for interrupt control. It delivers I2C commands to control the external DC/DC controller. At the same time, the AP53782 acts as I2C slave device to receive the I2C commands from the same interface delivered by the host MCU for system control.

Other than the RDO and PDO selections, the operating mode of the PD controller is readable, and user can check it and putting a suitable control accordingly by properly using of CC flip polarity, sink mode, or different types of source modes through the I2C commands. Also, if the PD is coming from a source provider, its source VID and PID information are available from I2C commands.

I2C Command Format

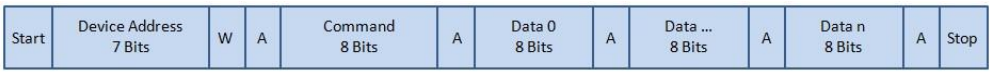
The AP53782 provides some I2C slave commands for the controlling from the host MCU. The I2C slave address is assigned as 0x44.

All commands begin with a Start bit and end with a Stop bit. A Start condition is defined as a HIGH to LOW transition of the SDA while SCL is HIGH. A Stop condition is defined as a LOW to HIGH transition of the SDA while SCL is HIGH. After the Start condition, a slave address is sent. This address is 7 bits long followed by an eighth bit which is a data R/W bit - a 'LOW' indicates a data write (W), a 'HIGH' indicates a data read (R). The Start and Stop conditions are always generated by the I2C master, the host MCU of the TCD. A data transfer is always terminated by a Stop condition generated by the master. However, if a master still wishes to communicate on the bus, it can generate a repeated Start condition (Restart) and address another slave without first generating a Stop condition. Each byte has to be followed by an acknowledge bit (A). The acknowledge-related clock pulse is generated by the master. Examples of an I2C write and read sequence are shown in Figure 13, where W, R, A, NA represent Write (LOW), Read (HIGH), Acknowledge (SDA LOW), and NOT Acknowledge (SDA HIGH), respectively.

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Functional Overview (continued)

I2C Write Operation:



I2C Read Operation:

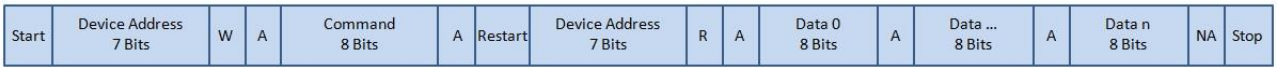


Figure 13. The I2C write and read command sequences.

The memory representation of multi-byte data types on the AP53782 is Little Endian byte order. The least significant byte (the "little end") of the data is placed at the byte of the lowest address. For example, if the integer is stored as 4 bytes, then a variable X with value of 0x12345678 will be stored as Figure 14 below:

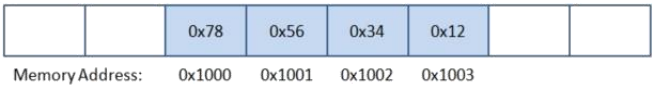


Figure 14. The Little-Endian Byte order is used in the AP53782.

Interrupt Signal

AP53782 supports a level-triggered interrupt signal through GPIO1 pin to the host MCU. The I2C command MASK (0x01) defines enable or disable of each interruptible event as shown in Table 2 below. The interrupt initialization is required before use. When the defined interruptible event happens, the default output of GPIO1 is high. AP53782 sets the GPIO1 pin output to level Low if the relevant event of the MASK register is enabled. After STATUS is read, the GPIO1 output is back to high.

MASK	Bit	Attribute	Pwr-on	Description
OTP	7	RW	0b	1: OTP status mask
OVP	6	RW	0b	1: OVP status mask
UVP	5	RW	0b	1: UVP status mask
OCP	4	RW	0b	1: OCP status mask
—	3	RW	0b	—
—	2	RW	0b	—
GPIO	1	RW	0b	1: GPIO status update mask
OPMODE_STS	0	RW	0b	1: OPMODE status update mask

Table 2. The MASK register defines enable or disable of each interruptible event.

PD Sink Voltage Select

VSEL command (0x02) is an 8-bit register and is used to control PD sink request voltage as shown in Table 3 as below for AP53782DKZ-13-FA01.

VSEL	Bit	Attribute	Pwr-on	Description
VSEL	7:0	RW	5Ah	Request voltage, LSB 100mV

Table 3. The VSEL command is used to control PD sink request voltage.

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Functional Overview (continued)

Sink Current Select

ISEL command (0x03) is an 8-bit register and is used to control PD sink request current as shown in Table 4 below.

ISEL	Bit	Attribute	Pwr-on	Description
ISEL	7:0	RW	28h	Requested current, LSB 50mA

Table 4. The ISEL command is used to control PD sink request current.

QC Sink Select

QCSEL command (0x04) is an 8-bit register and is used to select QC2 or QC3 sink and control QC sink request voltage from QC source as shown in Table 5 below.

QCSEL	Bit	Attribute	Pwr-on	Description
QCMODE	7	RW	0b	0: select QC2.0 mode 1: select QC3.0 mode
—	6	RW	0b	Reserved
QC3VOL	5:2	RW	0000b	Select QC3.0 voltage, 200mV/code When QCMODE = 1 QC3 request voltage = QCSEL[5:0]
QCVOL	1:0	RW	00b	Select QC voltage When QCMODE = 0, QCMODE = 1 0: 5V 0mV 1: 9V 200mV 2: 12V 400mV 3: Reserved 800mV

Table 5. The QCSEL command is used to control QC sink.

PDO Select

PDOSEL command (0x05) is an 8-bit register and is used to select source power 25W, 30W, 33W, 45W and 65W as shown in Table 6 below for AP53782DKZ-13-FA01.

Detailed PDO table shown in Table 19.

PDOSEL	Bit	Attribute	Pwr-on	Description
Reserved	7:3	RW	000000b	—
PWR_SEL	2:0	RW	011b	PDO power profile select 000b: 25W 001b: 30W 010b: 33W 011b: 45W 100b ~111b: 65W

Table 6. The PDOSEL command is used to select source power.

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Functional Overview (continued)

GPIO Control

GPIO command (0x06) is an 8-bit register and is used to control GPIO as shown in Table 7 below.

GPIOCTL	Bit	Attribute	Pwr-on	Description
—	7	RW	0b	—
GPIO4_IO	6	RW	0b	GPIO4 Input / Output select 0: Output, 1: Input
GPIO3_IO	5	RW	0b	GPIO3 Input / Output select 0: Output, 1: Input
GPIO2_IO	4	RW	0b	GPIO2 Input / Output select 0: Output, 1: Input
—	3	RW	0b	—
GPIO4_OUT	2	RW	0b	GPIO4 output 0: low, 1: high If GPIO4 is set to input, this bit is no meaning.
GPIO3_OUT	1	RW	0b	GPIO3 output 0: low, 1: high If GPIO3 is set to input, this bit is no meaning.
GPIO2_OUT	0	RW	0b	GPIO2 output 0: low, 1: high If GPIO2 is set to input, this bit is no meaning.

Table 7. The GPIO command is used to control GPIO pins.

Overtemperature Protection (OTP)

An NTC thermistor is used to measure the temperature of potential hot spot on the board. NTC can be connected to a constant current source of 100μA at OTP pin. As the temperature changes NTC resistance changes, with the AP53782 internal ADC, OTP pin voltage is measured.

The I2C command OTPTHR (0x07) register, as shown in Table 8 below, is used to set OTP threshold, and is 0Bh by default. If voltage on OTP pin is below the OTPTHR value after the de-bouncing time, the OTP is triggered, and STATUS Bit [7] is set to High. The associated output enable MOS switch will be turned off. While the voltage is over OTPTHR, AP53782 will recover TYPE-C detection.

OTPTHR	Bit	Attribute	Pwr-On	Description
OTPTHR	7:0	RW	0Bh	OTP threshold, Unit: 8mV The temperature threshold triggers the OTP function.

Table 8. The I2C command OTPTHR is used to set OTP threshold.

System Control

SYSCTL (0x08) is an 8-bit register and is used to control VBUS MOS through GPIO5 pin in Sink mode. If USB communications are capable, set USB communications bit.

SYSCTL	Bit	Attribute	Pwr-on	Description
—	7	RW	0b	—
—	6	RW	0b	—
—	5	RW	0b	—
—	4	RW	0b	—
DRSWAP	3	RW	0b	0: Accept DR_Swap 1: Reject DR_Swap
USB_COM	2	RW	0b	1: Set USB communications bit.
SINK_MOS	1:0	RW	00b	00: Auto 01: MOS enable 10: MOS disable 11: Reserved

Table 9. The SYSCTL is used to control system behavior.

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Functional Overview (continued)

Status

STATUS command (0x10) is an 8-bit register and is used to store AP53782 status as shown in Table 10 below.

STATUS	Bit	Attribute	Pwr-on	Description
OTP	7	RC	0b	OTP status
OVP	6	RC	0b	OVP status
UVP	5	RC	0b	UVP status
OCP	4	RC	0b	OCP status
—	3	RC	0b	Reserved
—	2	RC	0b	Reserved
GPIO	1	RC	0b	GPIO status update
OPMODE_STS	0	RC	0b	OPMODE update

Table 10. The STATUS command is used to monitor AP53782 status.

System Status and Operating Mode Inquiry

Host MCU can read PD operating modes through I2C command OPMODE (0x20), as shown in Table 11 below, where Type-C information and power role are provided.

OPMODE	Bit	Attribute	Pwr-On	Description
CCFLP	7	RO	0b	0: CC1 connected to CC line 1: CC2 connected to CC line
PWRMOD	6	RO	0b	0: Sink mode 1: Source mode
TYPEC	5	RO	0b	0: Detached. 1: Attached
DATAROLE	4	RO	0b	0: UFP 1: DFP
MISMATCH	3	RO	0b	1: Mismatch in Sink mode.
QCMOD	2	RO	0b	1: QC source connected
PDMOD	1	RO	0b	1: PD source connected
LGCYMOD	0	RO	0b	1: Legacy source connected (non-PD)

Table 11. The OPMODE command is used to monitor operation status.

GPIO Status

GPIO Status command (0x21) is an 8-bit register, provides status of GPIO 2, GPIO3 and GPIO4 in real time.

GPIOSTS	Bit	Attribute	Pwr-on	Description
—	7	RO	0b	Reserved
—	6	RO	0b	Reserved
—	5	RO	0b	Reserved
—	4	RO	0b	Reserved
—	3	RO	0b	Reserved
GPIO4	2	RO	0b	GPIO4 status
GPIO3	1	RO	0b	GPIO3 status
GPIO2	0	RO	0b	GPIO2 status

Table 12. The GPIOSTS command provides GPIO 2 to 4 status.

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Functional Overview (continued)

VID (Note 12)

I2C command VID (0x22) register, as shown in Table 13 below, VID of PD partner is stored here. If PD partner does not respond to Discover ID, the field remains default value (0000h).

VID	Bit	Attribute	Pwr-on	Description
VID	15:0	RO	0000h	The USB Vendor ID of PD partner is obtained from the ID Header VDO of Discover Identity Command response.

Table 13. The VID command provides VID of PD partner.

PID (Note 12)

I2C command PID (0x23) register, as shown in Table 14 below, PID of PD partner is stored here. If PD partner does not respond to Discover ID, the field remains default value (0000h).

PID	Bit	Attribute	Pwr-on	Description
PID	15:0	RO	0000h	The USB Product ID of PD partner is obtained from the ID Header VDO of Discover Identity Command response.

Table 14. The PID command provides PID of PD partner.

VBUS_VLU

I2C command VBUS_VLU (0x24) register, as shown in Table 15 below, the command provides VBUS voltage in real time.

VBUS_VLU	Bit	Attribute	Pwr-on	Description
VBUS_VLU	7:0	RO	00h	VBUS voltage in 100mV

Table 15. The VBUS_VLU command provides VBUS voltage.

CUR_VLU

The I2C command CUR_VLU (0x25) register, as shown in Table 16 below, the command provides current on VBUS in real time.

CUR_VLU	Bit	Attribute	Pwr-on	Description
CUR_VLU	7:0	RO	00h	VBUS current in 40mA

Table 16. The VBUS_VLU command provides current value.

TMP_VLU

The I2C command TMP_VLU (0x26) register, as shown in Table 17 below, the command provides voltage on OTP pin in real time.

TMP_VLU	Bit	Attribute	Pwr-on	Description
TMP_VLU	7:0	RO	00h	OTP pin voltage in 8mV

Table 17. The TMP_VLU command provides OTP voltage.

Note: 12. Only supported by customized FW.

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Functional Description (continued)

I2C Slave Command Summary

The slave commands provided for the host MCU are summarized in Table 18.

Register	Command	Length	Pwr-on	Attribute	Description
MASK	0x01	1	00h	RW	Interrupt enable mask
VSEL	0x02	1	5Ah	RW	PD request voltage, LSB 100mV
ISEL	0x03	1	28h	RW	PD requested current, LSB 50mA
QCSEL	0x04	1	00h	RW	QC request type and voltage
PDOSEL	0x05	1	03h	RW	PD source power profile select
GPIOCTL	0x06	1	00h	RW	Set GPIO 2 to 4
OTPTHR	0x07	1	0Bh	RW	OTP threshold. Unit: voltage in 8mV.
SYSCTL	0x08	1	00h	RW	System control
STATUS	0x10	1	00h	RC	AP53782 status
OPMODE	0x20	1	00h	RO	Operation mode
GPIOSTS	0x21	1	00h	RO	GPIO 2 to 4 status
VID	0x22	2	0000h	RO	Vendor ID of partner, obtained from Discover Identity Command response (Note 12)
PID	0x23	2	0000h	RO	Product ID of partner, obtained from Discover Identity Command response (Note 12)
VBUS_VLU	0x24	1	00h	RO	VBUS voltage in 100mV
CUR_VLU	0x25	1	00h	RO	VBUS current in 40mA
TMP_VLU	0x26	1	00h	RO	OTP pin voltage in 8mV

Attribute Convention

RW: Readable / Writable

RO: Read-Only

RC: Read-Clear

Table 18. The I2C commands provided in AP53782 PD3.1 DRP controller are illustrated.

PDO_SEL		Power Data Object				
25W	Fixed PDO	5V/3A	9V/2.78A	12V/2.08A	—	—
	PPS	—	5V~11V/2.75A	—	—	—
30W	Fixed PDO	5V/3A	9V/3A	12V/2.5A	15V/2A	20V/1.5A
	PPS	—	5V~11V/3A	—	5V~16V/2A	—
33W	Fixed PDO	5V/3A	9V/3A	12V/2.75A	15V/2.2A	20V/1.65A
	PPS	—	5V~11V/3A	—	5V~16V/2.2A	—
45W	Fixed PDO	5V/3A	9V/3A	12V/3A	15V/3A	20V/2.25A
	PPS	—	5V~11V/5A	—	5V~16V/3A	—
65W	Fixed PDO	5V/3A	9V/3A	12V/3A	15V/3A	20V/3.25A
	PPS	—	5V~11V/5A	—	—	5V~21V/3.25A

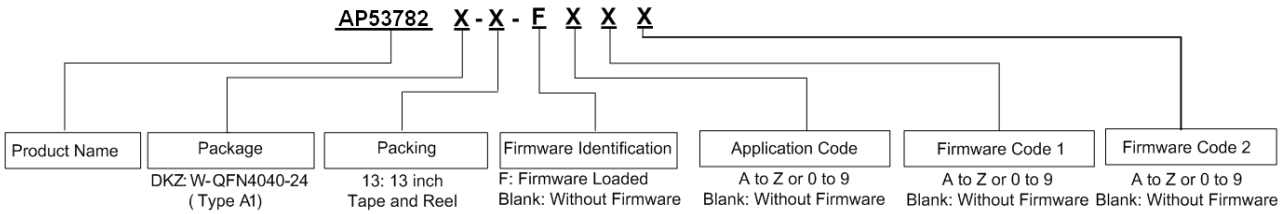
Table 19. AP53782DKZ-13-FA01 PDO table by PDOSEL

Note: 12. Only supported by customized FW.

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Ordering Information



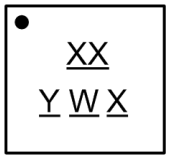
Orderable Part Number (Note 13)	Package (Note 14)	Firmware Inside	Packing	
			Qty.	Carrier
AP53782DKZ-13-FA01	W-QFN4040-24 (Type A1)	Standard Firmware (Function as Described in Datasheet)	3000	13” Tape & Reel
AP53782DKZ-13-FXXX		Customized Firmware		

Notes: 13. It is recommended to order Standard Firmware device based on functions described in the datasheet. For without firmware and customized options, please contact us or your local Diodes representative.
14. For packaging details, go to our website at https://www.diodes.com/design/support/packaging/diodes-packaging/.

Marking Information

W-QFN4040-24 (Type A1)

(Top View)



XX : Identification Code
Y : Year : 0 to 9 (ex: 6 = 2026)
W : Week : A to Z: week 1 to 26;
a to z: week 27 to 52; z represents week 52 and 53
X : Internal Code

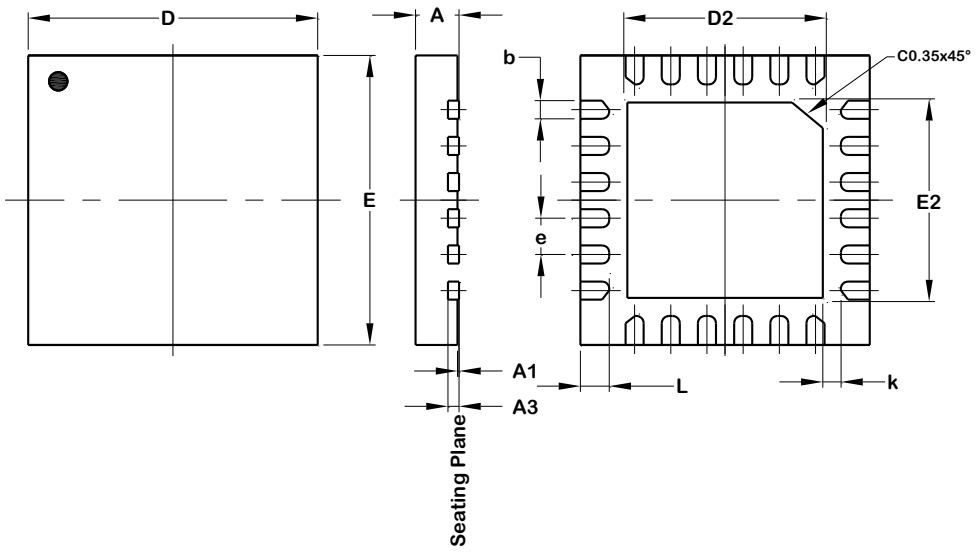
Orderable Part Number	Package	Identification Code
AP53782DKZ-13-FA01	W-QFN4040-24 (Type A1)	AZ
AP53782DKZ-13-FXXX		

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Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

W-QFN4040-24 (Type A1)

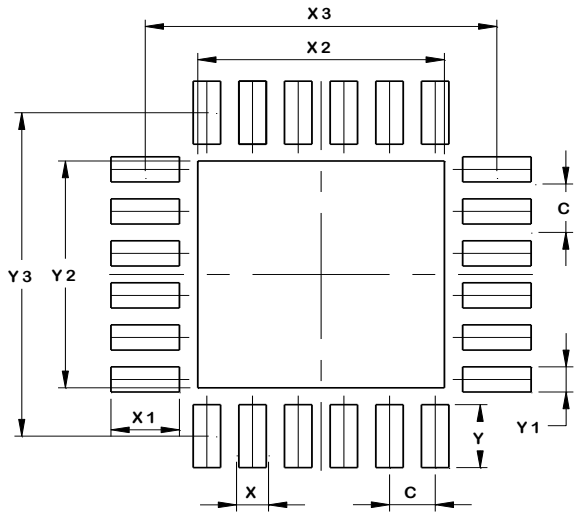


W-QFN4040-24 (Type A1)			
Dim	**Min**	**Max**	**Typ**
A	0.70	0.80	0.75
A1	0.00	0.05	0.02
A3	0.203 REF		
b	0.18	0.30	0.25
D	4.00 BSC		
D2	2.65	2.75	2.70
E	4.00 BSC		
E2	2.65	2.75	2.70
e	0.50 BSC		
k	0.20	--	--
L	0.35	0.45	0.40
All Dimensions in mm			

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

W-QFN4040-24 (Type A1)



Dimensions	Value (in mm)
C	0.500
X	0.300
X1	0.750
X2	2.700
X3	3.850
Y	0.750
Y1	0.300
Y2	2.700
Y3	3.850

Mechanical Data

- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish—Matte Tin Plated Leads, solderable per J-STD-202 e3
- Weight: 0.041 grams (Approximate)

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