DATEL®
INNOVATION and EXCELLENCE

DATIS007

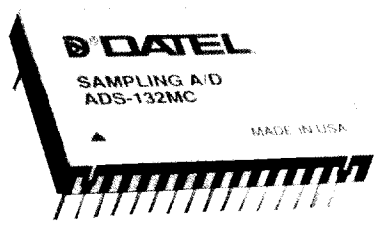
ADS-132

12–Bit, 2.0 MHz, Low–Power Sampling A/D Converter

DATIS007

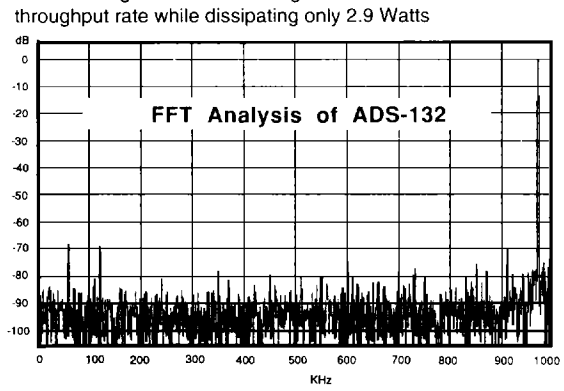
FEATURES

- 12-Bit resolution
- Internal sample hold
- 2.0 MHz minimum throughput
- Functionally complete
- Small 32-pin DIP
- Low-power, 2.9 Watts
- Three-state output buffers
- Samples up to Nyquist

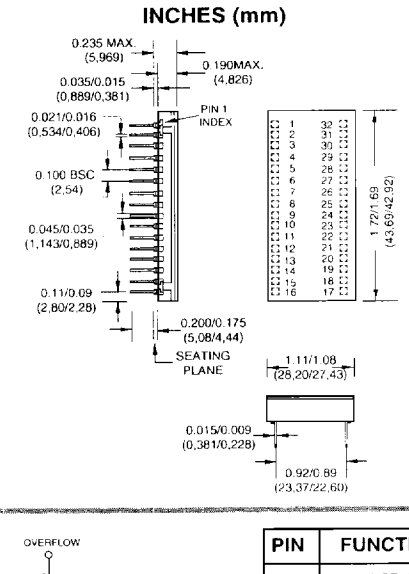


GENERAL DESCRIPTION

DATEL's ADS-132 is a 12–bit, functionally complete, sampling A/D converter that is packaged in a small 32–pin DIP The ADS–132 digitizes sinusoidal signals at a 2.0 MHz minimum throughput rate while dissipating only 2.9 Watts



MECHANICAL DIMENSIONS INCHES (mm)



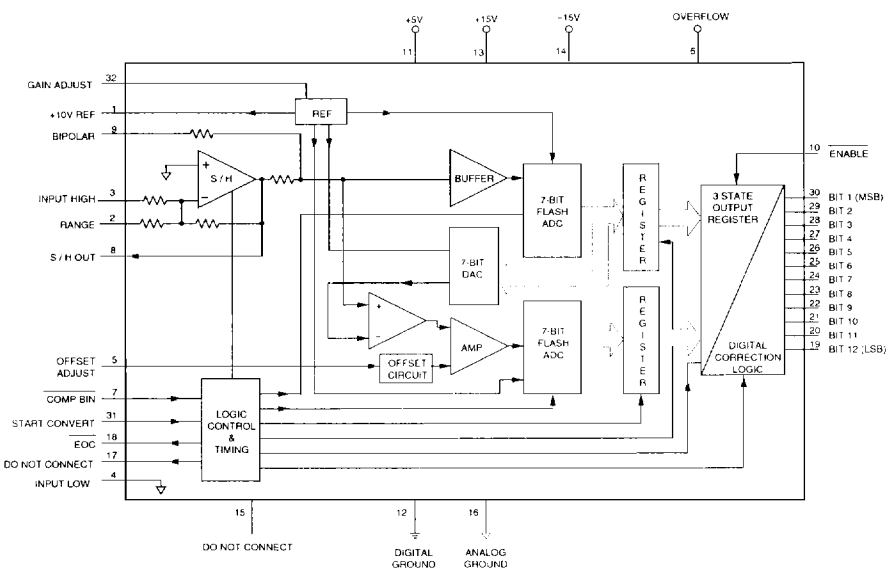


Figure 1. ADS-132 Simplified Bock Diagram

PIN	FUNCTION
1	+10V REF. OUT
2	RANGE
3	INPUT HIGH
4	INPUT LOW
5	OFFSET ADJUST
6	OVERFLOW
7	COMP. BIN
8	S/H OUT
9	BIPOLAR
10	ENABLE (1 – 12)
11	+5
12	DIGITAL GROUND
13	+15V
14	–15V
15	DO NOT CONNECT
16	ANALOG GROUND
17	DO NOT CONNECT
18	EOC
19	BIT 12 OUT (LSB)
20	BIT 11 OUT
21	BIT 10 OUT
22	BIT 9 OUT
23	BIT 8 OUT
24	BIT 7 OUT
25	BIT 6 OUT
26	BIT 5 OUT
27	BIT 4 OUT
28	BIT 3 OUT
29	BIT 2 OUT
30	BIT 1 OUT (MSB)
31	START CONVERT
32	GAIN ADJUST

ABSOLUTE MAXIMUM RATINGS

PARAMETERS	LIMITS	UNITS
+15V Supply (Pin 13)	0 to +18	Volts dc
–15V Supply (Pin 14)	0 to –18	Volts dc
+5V Supply (Pin 11)	–0.5 to +7.0	Volts dc
Digital Inputs		
(Pins 7, 10, 31)	–0.3 to V_{DD} +0.3	Volts dc
Analog Input (Pin 3)	–15 to +15	Volts dc
Lead Temp. (10 Sec.)	300 max	°C
Thermal Resistance		
@ J-C	2.7	°C/W
@ CA	11.2	°C/W

FUNCTIONAL SPECIFICATIONS

Apply over the operating temperature range and at ±15V dc and ±5V dc unless otherwise specified.

ANALOG INPUTS	MIN.	TYP.	MAX.	UNITS
Input Voltage Range				
ADS-132 (see Table 1 also)	—	0 to –5	—	Volts dc
	—	0 to –10	—	Volts dc
	—	0 to +10	—	Volts dc
	—	±5	—	Volts dc
	—	±10	—	Volts dc
Input Impedance				
Input Ranges:				
(0 to –10, +10, ±10)	800	1000	—	Ohms
(0 to –5, ±5V)	400	500	—	Ohms
Input Capacitance	—	2	—	pf
DIGITAL INPUTS				
Logic Levels				
Logic "1"	2.0	—	—	Volts dc
Logic "0"	—	—	0.5	Volts dc
Logic Loading "1"	—	—	5.0	µA
Logic Loading "0"	—	—	–600	µA
PERFORMANCE				
Integral Non-Linearity				
@ f_{IN} = 1 MHz				
0 to +70 °C	—	—	±1	LSB
–55 to +125 °C	—	—	±2	LSB
Differential Non-Linearity				
@ f_{IN} = 1 MHz				
0 to +70 °C	—	—	±3/4	LSB
–55 to +125 °C	—	—	±1.5	LSB
FS Absolute Accuracy †				
0 to +70 °C	—	±0.1	±0.32	%FSR
–55 to +125 °C	—	±0.2	±0.5	%FSR
Unipolar Zero Error †				
0 to +70 °C	—	±0.05	±0.25	%FSR
–55 to +125 °C	—	±0.18	±0.37	%FSR
Bipolar Zero Error †				
0 to +70 °C	—	±0.05	±0.25	%FSR
–55 to +125 °C	—	±0.18	±0.37	%FSR
Bipolar Offset Error †				
0 to +70 °C	—	±0.1	±0.38	%FSR
–55 to +125 °C	—	±0.53	±0.73	%FSR
Gain Error †				
0 to +70 °C	—	±0.1	±0.38	%FSR
–55 to +125 °C	—	±0.53	±0.73	%FSR
No Missing Codes (12 Bits)	Over the Operating Temp. Range			

† See Technical Note 1

OUTPUTS	MIN.	TYP.	MAX.	UNITS
Resolution	12 Bits			
Output Coding	Straight binary/offset binary Complementary binary/Complementary offset binary			
Logic Levels				
Logic "1"	2.4	—	—	Volts dc
Logic "0"	—	—	0.4	Volts dc
Logic Loading "1"	—	—	–160	µA
Logic Loading "0"	—	—	4.8	mA
Internal Reference Voltage				
+25 °C	+9.98	+10.0	+10.02	Volts dc
Drift	—	±5	±30	ppm/ °C
External Current	—	—	2	mA
DYNAMIC PERFORMANCE				
Conversion Rate, 12-Bits	2	—	—	MHz
Total Harm. Distort. (–0.5 dB)				
DC to 100 kHz	—	–80	–72	FS, –dB
100 kHz to 500 kHz	—	–75	–68	FS, –dB
500 kHz to 1 MHz	—	–71	–67	FS, –dB
Signal to Noise Ratio				
(w/o distort., –0.5 dB)				
DC to 100 kHz	70	72	—	FS, –dB
100 kHz to 500 kHz	68	70	—	FS, –dB
500 kHz to 1 MHz	66	68	—	FS, –dB
Signal to Noise Ratio ①				
(and distort., –0.5 dB)				
DC to 100 kHz	68	70	—	FS, –dB
100 kHz to 500 kHz	66	68	—	FS, –dB
500 kHz to 1 MHz	65	67	—	FS, –dB
Spurious Free Dynamic ②				
Range (–0.5 dB)				
DC to 100 kHz	—	–81	–73	FS, –dB
100 kHz to 500 kHz	—	–76	–69	FS, –dB
500 kHz to 1 MHz	—	–72	–68	FS, –dB
Two-Tone Intermodulation				
Distort. (f_{IN} = 490 kHz, 480 kHz, FS = 2 MHz, –0.5 dB)	—	–70	–67	FS, –dB
Input Bandwidth				
Small Signal (–20 dB input)	16	—	—	MHz
Large Signal (–3 dB input)	8	—	—	MHz
Slew Rate	—	300	—	V / µSec.
Aperture Delay Time	—	6	—	nSec.
Feedthrough Rejection	—	–74	—	dB
Overvoltage Recovery Time	—	—	1,000	nSec.
S/H Acquisition Time				
to 0.01% FS (10V step)	—	160	200	nSec.
S/H Acquisition Time				
to 0.1% FS (10V step)	—	100	170	nSec.
POWER REQUIREMENTS				
Power Supply Range				
+15V dc Supply	+14.25	+15.0	+15.75	Volts dc
–15V dc Supply	–14.25	–15.0	–15.75	Volts dc
+5V dc Supply	+4.75	+5.0	+5.25	Volts dc
Power Supply Current				
+15V dc Supply	—	+75	+82	mA
–15V dc Supply	—	–60	–75	mA
+5V dc Supply ③	—	+155	+200	mA
Power Dissipation	—	2.9	3.2	Watts
Power Supply Rejection	—	—	0.01	%FSR/%V
PHYSICAL/ENVIRONMENT				
Operating Temperature Range				
-MC (case)	0	—	+70	°C
-MM (case)	–55	—	+125	°C
Storage Temperature Range	–65	—	+150	°C
Package Type	32-pin DIP			
Weight	0.42 ounces (12 grams)			

① Effective bits is equal to:

$$\frac{(\text{SNR + Distortion}) - 1.76 + \left[20 \log \frac{\text{Full Scale Amplitude}}{\text{Actual Input Amplitude}}\right]}{6.02}$$

② Spurious Free Dynamic Range (SFDR); same specifications for In-Band Harmonics.
③ +5V power usage at 1 TTL logic loading per data output bit.

Specifications subject to change without notice.

TECHNICAL NOTES

1. Use external potentiometers to remove system errors or the small initial errors to zero. Use a 20K trimming potentiometer for gain adjustment with the wiper tied to pin 32 (ground pin 32 for operation without adjustments.) Use a 20K trimming potentiometer with the wiper tied to pin 5 for zero/offset adjustment (leave pin 5 open for operation without adjustment.) See Figure 3.

2. Always connect the analog and digital grounds to a ground plane beneath the converter for best performance. The analog and digital grounds are not connected internally.

3. Bypass the analog and digital supplies and the +10V reference (pin 1) to ground with a 4.7 µF, 25V tantalum electrolytic capacitor in parallel with a 0.1 µF ceramic capacitor. Bypass the +10V reference (pin 1) to ANALOG GROUND (pin 16)

4. To enable the three-state outputs, connect $\overline{\text{ENABLE}}$ (pin 10) to a logic "0" (low). To disable, connect pin 10 to a logic "1" (high).

5. The ADS-132 is in the sample mode when the internal S/$\overline{\text{H}}$ CONTROL pin is high (power-up state). The START CONVERT pulse should occur at a time delay equal to the desired acquisition time minus the 10 ns delay from START CONVERT high to S/$\overline{\text{H}}$ CONTROL low. This assures the sample-hold has the minimum required acquisition time for the particular application mode.

6. Upon going into the hold mode there will be a 85 ns maximum delay before $\overline{\text{EOC}}$ goes high and the A/D conversion begins. This consists of the remaining 50 ns of the START CONVERT (10 ns is part of the acquisition time) and a 20 ns maximum delay from START CONVERT low to $\overline{\text{EOC}}$ high. The hold mode settling time requirement is met during this time.

7. Figure 2 shows the relationship between the various input signals. The timing shown applies over the operating temperature range and over the operating power supply range. These times are guaranteed by design.

8. Re-initiating the START CONVERT (pin 16) while $\overline{\text{EOC}}$ is a logic "1" (high) results in a new conversion sequence. Subsequent data will then be valid after the minimum acquisition time is observed.

CALIBRATION PROCEDURE

1. Connect the converter per Figure 3, Table 1, and Table 4 for the appropriate full-scale range (FSR). Apply a pulse of 60 nanoseconds minimum to the START CONVERT input (pin 31) at a rate 500 kHz. This rate reduces flicker if using LED's on the outputs for calibration purposes.

2. Zero Adjustments
   Apply a precision voltage reference source between the amplifier's analog input and ground. Adjust the output of the reference source per Table 2. For unipolar, adjust the zero trimming potentiometer so that the output code flickers equally between 0000 0000 0000 and 0000 0000 0001 (straight binary) or between 1111 1111 1111 and 1111 1111 1110 (complementary binary).

   For bipolar operation, adjust the trimpot until the code flickers equally between the 1000 0000 0000 and 1000 0000 0001 (offset binary) or between 0111 1111 1111 and 0111 1111 1110 (complementary offset binary).

3. Full-Scale Adjustment
   Set the output of the voltage reference used in step 2 to the value shown in Table 2. Adjust the gain trimming potentiometer until the ouput code flickers equally between 1111 1111 1110 and 1111 1111 1111 (offset binary) or between 0000 0000 0001 and 0000 0000 0000 (complementary offset binary)

4. To confirm proper operation of the device, vary the precision reference voltage source to obtain the output coding listed in Table 3.

Table 1. ADS-132 Input Range Selection

INPUT RANGE	INPUT PIN	TIE TOGETHER
0 to -5V dc	Pin 3	Pins 8 and 9; pins 2 and 3
0 to -10V dc	Pin 3	Pins 8 and 9
0 to +5V dc	Pin 3	Pins 8 and Pin 9; pin 2 to a -5 volt Reference
0 to +10V dc	Pin 3	Pins 8 and 9, pin 2 to an EXT. -10V Reference *
±5V dc	Pin 3	Pins 1 and 9, pins 2 and 3
±10V dc	Pin 3	Pins 1 and 9

* EXT. -10V REF. may be referenced to pin 1, INT. +10V REF.

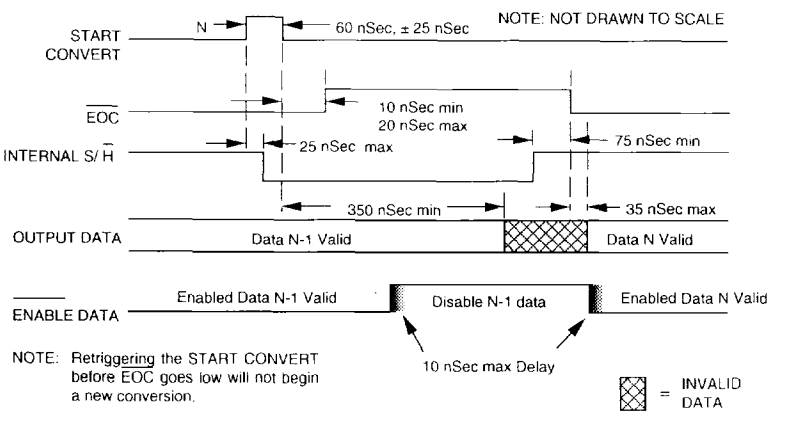


Figure 2. ADS-132 Timing Diagram

Table 3. Output Coding

					STRAIGHT BIN.	COMP. BINARY				
UNIPOLAR SCALE	INPUT RANGES, V dc				OUTPUT CODING				INPUT RANGES		BIPOLAR SCALE
	0 to +5V	0 to +10V	0 to –5V	0 to –10V	MSB	LSB	MSB	LSB	±5V dc	±10V dc	
+FS – 1 LSB	+4.998V	+9.9976V	–4.998V	–9.9976V	1111	1111 1111	0000	0000 0000	+4.9976V	+9.9951V	+FSB – 1 LSB
7/8 FS	+4.375V	+8.7500V	–4.375V	–8.7500V	1110	0000 0000	0001	1111 1111	+3.7500V	+7.5000V	+3/4 FS
3/4 FS	+3.750V	+7.5000V	–3.750V	–7.5000V	1100	0000 0000	0011	1111 1111	+2.5000V	+5.0000V	+1/2 FS
1/2 FS	+2.500V	+5.0000V	–2.500V	–5.0000V	1000	0000 0000	0111	1111 1111	0.0000V	0.0000V	0
1/4 FS	+1.250V	+2.5000V	–1.250V	–2.5000V	0100	0000 0000	1011	1111 1111	–2.5000V	–5.0000V	–1/2 FS
1/8 FS	+0.625V	+1.2500V	–0.625V	–1.2500V	0010	0000 0000	1101	1111 1111	–3.7500V	–7.5000V	–3/4 FS
1/LSB	+0.0012V	+0.0024V	0.0012V	–0.0024V	0000	0000 0001	1111	1111 1110	–4.9976V	–9.9951V	–FS + 1 LSB
0	0.0000V	0.0000V	0.0000V	0.0000V	0000	0000 0000	1111	1111 1111	–5.0000V	–10.000V	–FS
					OFFSET BINARY	COMP. OFF. BIN.					

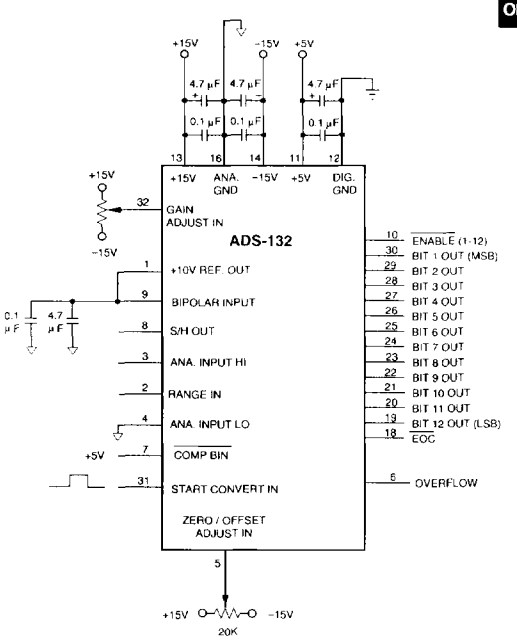


Figure 3. Typical ADS–132 Connection Drawing

Table 2. ADS–132 Zero and Gain Adjust

FSR	ZERO ADJUST +1/2 LSB	GAIN ADJUST +FS –1 1/2 LSB
0 to –5V dc	–0.61 mV	–4.9982V dc
0 to –10V dc	–1.22 mV	–9.9963V dc
0 to +5V dc	+0.61 mV	+4.9982V dc
0 to +10V dc	+1.22 mV	+9.9963V dc
±5V dc	+1.22 mV dc	+4.9963V dc
±10V dc	+2.44 mV dc	+9.9927V dc

Table 4. $\overline{\text{COMP BIN}}$ (Pin 7) Connection

INPUT RANGE	BINARY	COMPLEMENTARY BINARY
	Pin 7 Logic State *	
0 to +5V	Low	High
0 to +10V	Low	High
0 to –5V	High	Low
0 to –10V	High	Low
±5V	Low	High
±10V	Low	High

* For logic state low, connect to +5V. For logic state high, leave open.

ORDERING INFORMATION

MODEL	OPERATING TEMP. RANGE
ADS-132MC	0 °C to +70 °C
ADS-132MM	–55 °C to +125 °C
ADS-132/883	–55 °C to +125 °C
ADS-EVAL1	Evaluation Board (w/o ADS-132)

Receptacle for PC board mounting can be ordered through Amp. Inc., PN 3-331272-8 (Component lead socket), 24 required.

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