XC6133 Series

Delay capacitor adjustable voltage detectors with sense pin isolation

ETR02030-003a

■GENERAL DESCRIPTION

The XC6133 series are ultra-small delay capacitor adjustable type voltage detectors that have high accuracy and sense pin isolation. High accuracy and a low supply current are achieved by means of a CMOS process, a highly accurate reference power supply, and laser trimming technology.

The sense pin is isolated from the power input pin to enable monitoring of the voltage of another power supply. Output can be maintained in the detection state even if the voltage of the power supply that is monitored drops to 0V. The sense pin is also suitable for detecting high voltages, and the detection and release voltage can be set as desired using external resistors.

An internal delay circuit is also provided. By connecting a capacitor to the Cd/MRB pin, any release delay time and detect delay time can be set, and the pin can also be used as a manual reset pin.

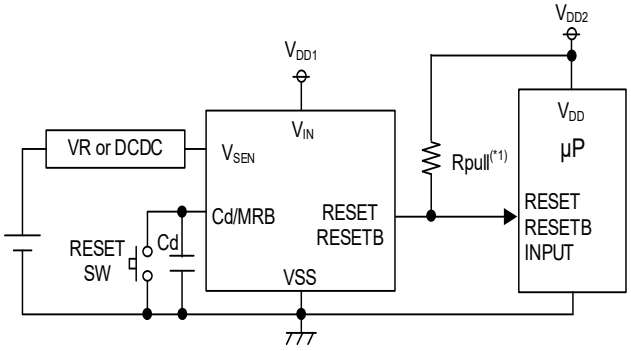
■APPLICATIONS

- ●Microcontroller reset and malfunction monitoring
- ●Battery voltage monitoring
- ●System power-on reset
- ●Power failure detection

■FEATURES

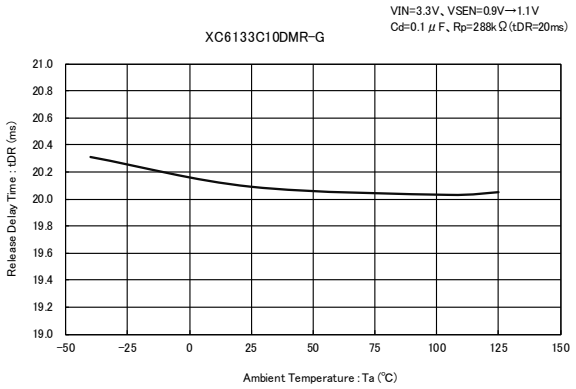
Operating Ambient Temperature	: -40℃ ~ 125℃
Operating voltage range	: 1.6V ~ 6.0V
Detect voltage range	: 1.0V ~ 5.0V
Detect voltage accuracy (Ta=25℃)	: ±18mV(V_{DF}＜1.5V) : ±1.2%(1.5V≦V_{DF}≦3.0V) : ±1.5%(3.1V≦V_{DF}≦5.0V)
Detect voltage accuracy (Ta=-40～125℃)	: ±36mV(V_{DF}＜1.5V) : ±2.7%(1.5V≦V_{DF}≦3.0V) : ±3.0%(3.1V≦V_{DF}≦5.0V)
Temperature Characteristics	: ±50ppm/℃(TYP.)
Hysteresis width	: V_{DF}×5.0%(TYP.)
Low supply current	: 1.28μA(TYP.) V_{IN}=1.6V(At detection) : 1.65μA(TYP.) V_{IN}=6.0V(At release)
Manual reset function	: Yes (For details, refer to FUNCTION CHART)
Output type	: CMOS or Nch open drain
Output logic	: H level or L level at detection
Delay capacitance pin	: Release delay / detection delay can be set in 5 time ratio options (For details, refer to Selection Guide).
Packages	: USP-6C,SOT-26
Environmentally friendly	: EU RoHS compliant, Pb free

■TYPICAL APPLICATION CIRCUIT



(*1.Unused for the CMOS output products)

■TYPICAL PERFORMANCE CHARACTERISTICS



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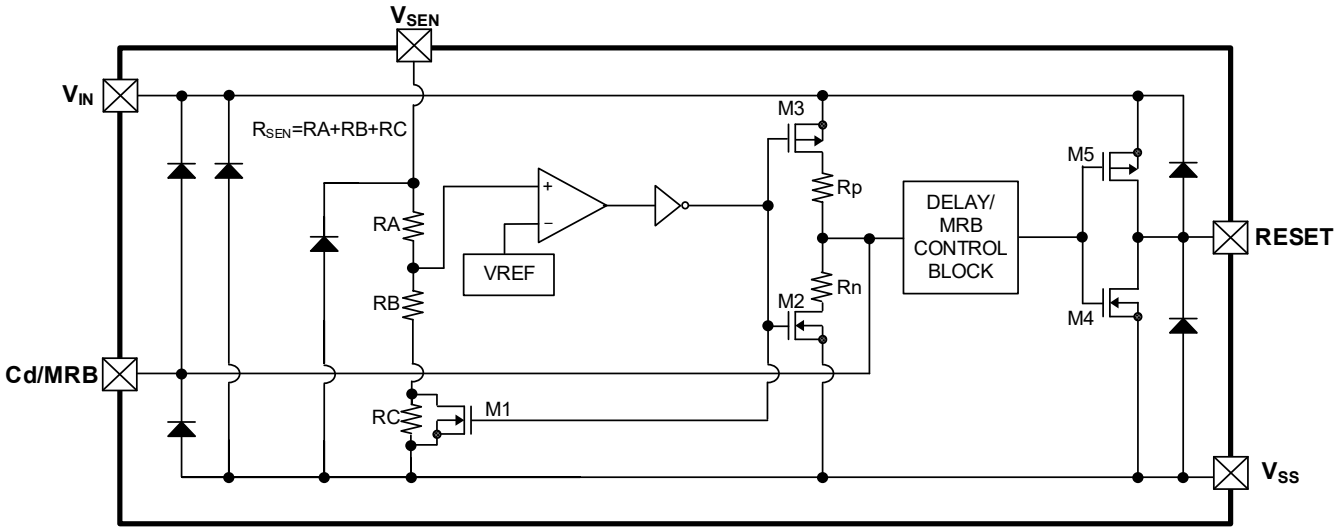
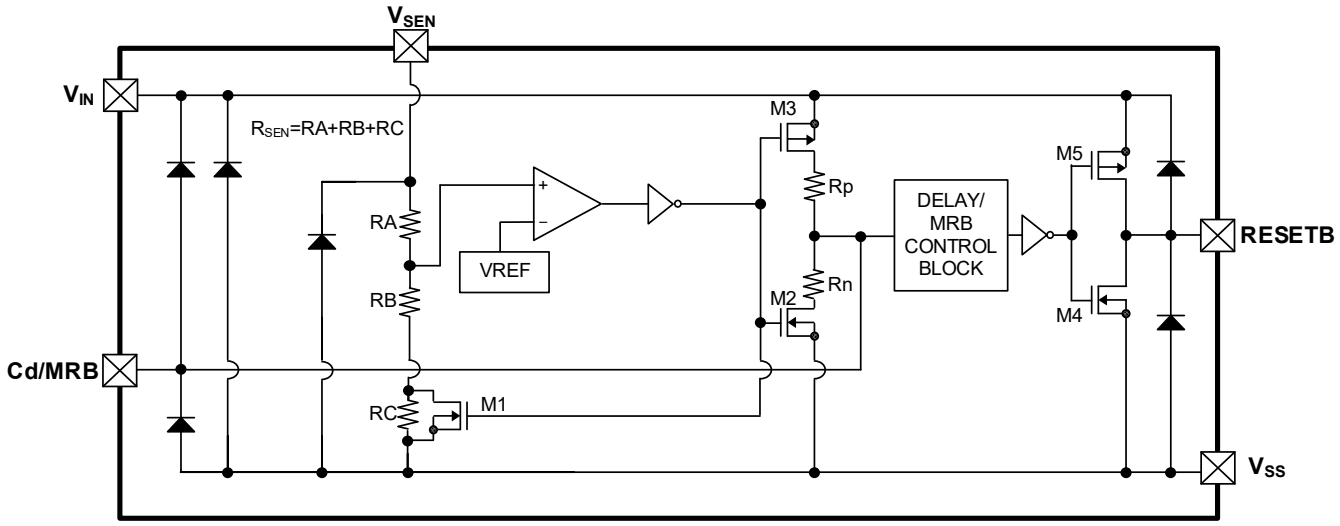
■BLOCK DIAGRAMS

(1)XC6133C Series A/B/C/D/L type (RESET OUTPUT: CMOS/Active High)



* Diodes inside the circuit are an ESD protection diode and a parasitic diode.

(2)XC6133C Series E/F/H/K/M type (RESETB OUTPUT: CMOS/Active Low)



* Diodes inside the circuit are an ESD protection diode and a parasitic diode.

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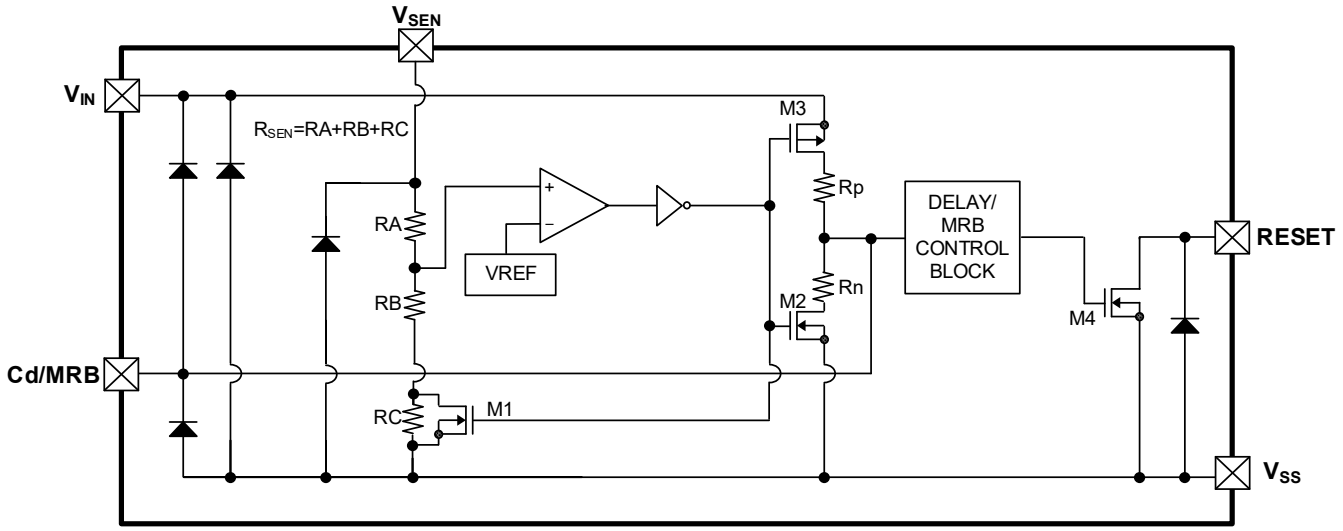
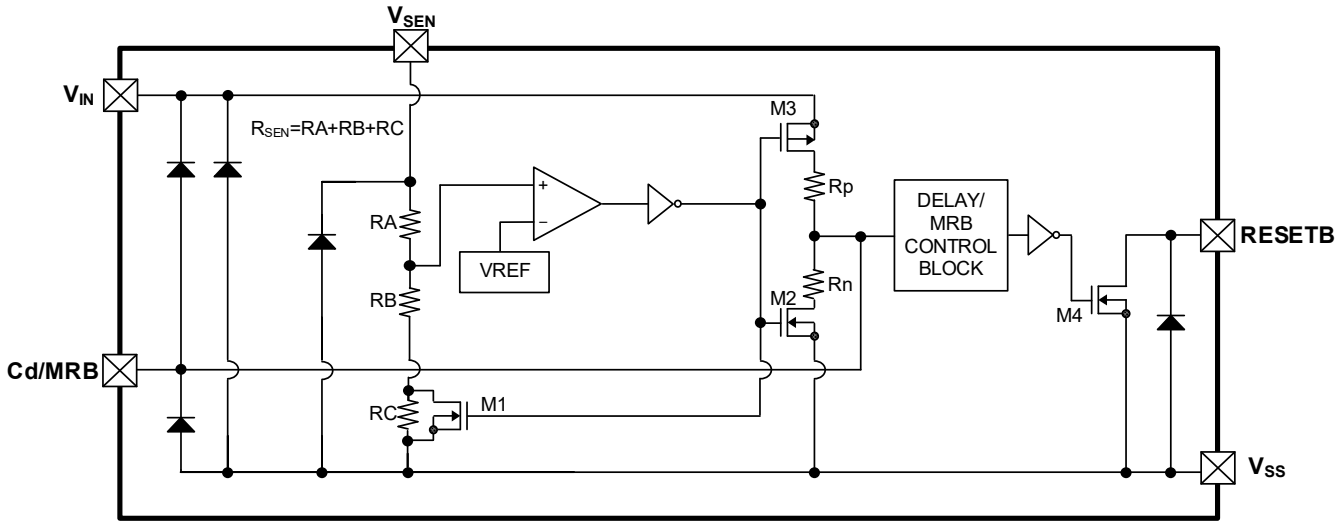
■BLOCK DIAGRAMS (Continued)

(3)XC6133N Series A/B/C/D/L type (RESET OUTPUT: Nch open drain/Active High)



* Diodes inside the circuit are an ESD protection diode and a parasitic diode.

(4)XC6133N Series E/F/H/K/M type (RESETB OUTPUT: Nch open drain/Active Low)



* Diodes inside the circuit are an ESD protection diode and a parasitic diode.

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■PRODUCT CLASSIFICATION

●Ordering Information

XC6133①②③④⑤⑥-⑦(*1)

DESIGNATOR	ITEM	SYMBOL	DESCRIPTION
①	Output Configuration	C	CMOS output
		N	Nch open drain output
②③	Detect Voltage	10 ~ 50	e.g. 1.0V → ②=1, ③=0
④	TYPE	A ~ M	Refer to Selection Guide
⑤⑥-⑦(*1)	Packages (Order Unit)	MR-G	SOT-26 (3,000pcs/Reel)
		ER-G	USP-6C (3,000pcs/Reel)

(*1) The "-G" suffix denotes Halogen and Antimony free as well as being fully EU RoHS compliant.

●Selection Guide

TYPE	RESET/RESETB OUTPUT	DELAY(Rp:Rn)		HYSTERESIS
A	Active High(*2)	1:0	144kΩ:0Ω	5.0%(TYP)
B	↑	1:0.125	144kΩ:18kΩ	↑
C	↑	1:1	144kΩ:144kΩ	↑
D	↑	2:1	288kΩ:144kΩ	↑
L	↑	0.076:1	11kΩ:144kΩ	↑
E	Active Low(*2)	1:0	144kΩ:0Ω	↑
F	↑	1:0.125	144kΩ:18kΩ	↑
H	↑	1:1	144kΩ:144kΩ	↑
K	↑	2:1	288kΩ:144kΩ	↑
M	↑	0.076 : 1	11kΩ : 144kΩ	↑

(*2) "Active High" is H level when detection occurs, and "Active Low" is L level when detection occurs.

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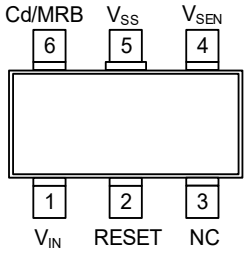
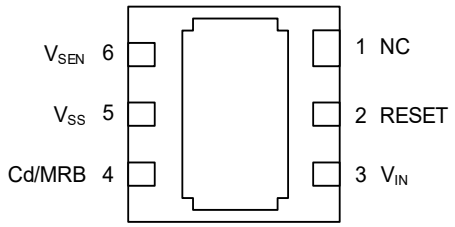
■PIN CONFIGURATION

●A/B/C/D/L type

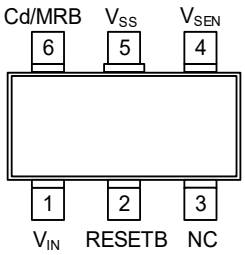


SOT-26
(TOP VIEW)

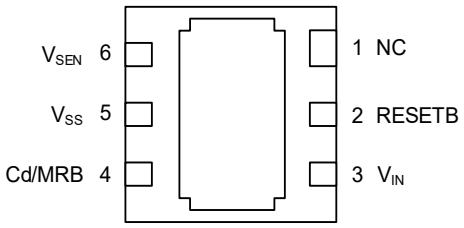


USP-6C
(BOTTOM VIEW)

●E/F/H/K/M type



SOT-26
(TOP VIEW)



USP-6C
(BOTTOM VIEW)

*The dissipation pad for the USP-6C package should be solder-plated in reference mount pattern and metal masking so as to enhance mounting strength and heat release. If the pad needs to be connected to other pins, it should be connected to V_{SS} (No. 5) pin.

■PIN ASSIGNMENT

PIN NUMBER		PIN NAME	FUNCTION
SOT-26	USP-6C		
1	3	V_{IN}	Power Input
2	2	RESETB	Reset Output (Active Low)(*1)
		RESET	Reset Output (Active High)(*1)
3	1	NC	No Connection
4	6	V_{SEN}	Voltage Sense
5	5	V_{SS}	Ground
6	4	Cd/MRB	Adjustable Pin for Delay Time/ Manual Reset

(*1) Refer to the ④ in Ordering Information table.

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■FUNCTION CHART

PIN NAME	SIGNAL	STATUS
Cd/MRB	L	Forced Reset
	H	For details, refer to " Function Chart "
	OPEN	Normal Operation

●Function Chart 1.6V≦V_{IN}≦6.0V

V_{SEN}	$V_{Cd/MRB}$	Transition of V_{RESET} Condition	Transition of V_{RESETB} Condition
		TYPE:A/B/C/D/L	TYPE:E/F/H/K/M
V_{SEN}≧V_{DF}+V_{HYS}	$V_{Cd/MRB}$≦V_{MRL}	Reset (High Level)(*2)	Reset (Low Level)(*1)
	$V_{Cd/MRB}$≧V_{MRH}	Release (Low Level)(*1)	Release (High Level)(*2)
V_{SEN}≦V_{DF}	$V_{Cd/MRB}$≦V_{MRL}	Reset (High Level)(*2)	Reset (Low Level)(*1)
	$V_{Cd/MRB}$≧V_{MRH}	Undefined(*3)	Undefined(*3)

(*1) CMOS output: V_{IN} × 0.1 or less, N-ch open drain output, pull-up voltage × 0.1 or less.
(*2) CMOS output: V_{IN} × 0.9 or higher, N-ch open drain output, pull-up voltage × 0.9 or higher.
(*3) For details, refer to page 16＜Manual reset function＞.

■ABSOLUTE MAXIMUM RATINGS

Ta=25℃

PARAMETER		SYMBOL		RATINGS	UNITS
Input Voltage		V_{IN}		-0.3 ~ 7.0	V
V_{SEN} Pin Voltage		V_{SEN}		-0.3 ~ 7.0	V
Cd/MRB Pin Voltage		$V_{Cd/MRB}$		-0.3 ~ V_{IN}+0.3 or 7.0(*1)	V
Output Voltage	XC6133C(*2)	V_{RESETB}	V_{RESET}	-0.3 ~ V_{IN}+0.3 or 7.0(*1)	V
	XC6133N(*3)			-0.3 ~ 7.0	V
Cd/MRB Pin Current		$I_{Cd/MRB}$		±5.0	mA
Output Current	XC6133C(*2)	I_{RBOUT}	I_{ROUT}	±50	mA
	XC6133N(*3)			+50	mA
Power Dissipation	SOT-26	Pd		250	mW
				600 (40mm x 40mm Standard board) (*4)	
	USP-6C			100	
				1250 (JESD51-7 board) (*4)	
Operating Ambient Temperature		Topr		-40 ~ 125	℃
Storage Temperature		Tstg		-55 ~ 125	℃

* All voltages are described based on the V_{SS}.
(*1) The maximum value should be either V_{IN}+0.3V or +7.0V in the lowest.
(*2) CMOS Output
(*3) N-ch Open Drain Output
(*4) The power dissipation figure shown is PCB mounted and is for reference only.
The mounting condition is please refer to PACKAGING INFORMATION.

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■ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	Ta=25℃			-40℃≦Ta≦125℃(*5)			UNITS	CIRCUIT
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.		
Operating Voltage	V_{IN}		1.6		6.0	1.6		6.0	V	①
V_{SEN} Input Voltage	V_{SEN}		0		6.0	0		6.0	V	
Detect Voltage	V_{DF}	$V_{DF(T)}$(*1)=1.0V～1.4V	$V_{DF(T)}$ -18mV	$V_{DF(T)}$	$V_{DF(T)}$ +18mV	$V_{DF(T)}$ -36mV	$V_{DF(T)}$	$V_{DF(T)}$ +36mV	V	
		$V_{DF(T)}$(*1)=1.5V～3.0V	$V_{DF(T)}$ ×0.988	$V_{DF(T)}$	$V_{DF(T)}$ ×1.012	$V_{DF(T)}$ ×0.973	$V_{DF(T)}$	$V_{DF(T)}$ ×1.027		
		$V_{DF(T)}$(*1)=3.1V～5.0V	$V_{DF(T)}$ ×0.985	$V_{DF(T)}$	$V_{DF(T)}$ ×1.015	$V_{DF(T)}$ ×0.970	$V_{DF(T)}$	$V_{DF(T)}$ ×1.030	V	
Temperature Characteristics	ΔV_{DF}/ (ΔTopr・V_{DF})	-40℃≦Topr≦125℃	-	±50	-	-	±50	-	ppm/℃	
Hysteresis Width	V_{HYS}		V_{DF} ×0.03	V_{DF} ×0.05	V_{DF} ×0.07	V_{DF} ×0.02	V_{DF} ×0.05	V_{DF} ×0.08	V	
Supply Current 1	I_{ss1}	V_{SEN}=V_{DF}×0.9V, V_{IN}=1.6V	-	1.28	2.65	-	1.28	3.92	μA	②
		V_{SEN}=V_{DF}×0.9V, V_{IN}=6.0V	-	1.36	2.80	-	1.36	4.22		
Supply Current 2	I_{ss2}	V_{SEN}=V_{DF}×1.1V, V_{IN}=1.6V	-	1.32	2.75	-	1.32	4.26		
		V_{SEN}=V_{DF}×1.1V, V_{IN}=6.0V	-	1.65	3.25	-	1.65	4.97		
SENSE Resistance	R_{SEN}	V_{IN}=6.0V,V_{SEN}=6.0V	E-1(*2)		-	E-2(*2)		-	MΩ	③
Release Delay Resistance (TYPE:A/B/C/E/F/H)	Rp	V_{IN}=6.0V,V_{SEN}=6.0V, $V_{Cd/MRB}$=0V	130	144	158	122	144	166	kΩ	④
Release Delay Resistance (TYPE:D/K)		V_{IN}=6.0V,V_{SEN}=6.0V, $V_{Cd/MRB}$=0V	259	288	317	245	288	331		
Release Delay Resistance (TYPE:L/M)		V_{IN}=6.0V,V_{SEN}=6.0V, $V_{Cd/MRB}$=0V	8.3	11	18.4	7.6	11	20.0		
Detect Delay Resistance (TYPE:C/D/H/K/L/M)	Rn	V_{IN}=6.0V,V_{SEN}=0V, $V_{Cd/MRB}$=6.0V	130	144	158	122	144	166		
Detect Delay Resistance (TYPE:B/F)		V_{IN}=6.0V,V_{SEN}=0V, $V_{Cd/MRB}$=6.0V	16.8	18	19.1	16.2	18	19.8		
Release Delay Time(*3)	t_{DR0}	V_{IN}=6.0V, V_{SEN}=V_{DF}×0.9V→ V_{DF}×1.1V	-	20	102	-	20	136	μs	⑤
Detect Delay Time(*4)	t_{DF0}	V_{IN}=6.0V, V_{SEN}=V_{DF}×1.1V→ V_{DF}×0.9V	-	20	82	-	20	116		

Unless otherwise specified in measurement conditions, Cd/MRB pin is open.
(*1) $V_{DF(T)}$:Nominal detect voltage
(*2) For V_{IN} conditions, refer to SPEC TABLE (p.10).
(*3) RESETB product: Time from when the V_{SEN} pin voltage reaches the release voltage until the reset output pin reaches 5.4V(V_{IN}×90%).
RESET product: Time from when the V_{SEN} pin voltage reaches the release voltage until the reset output pin reaches 0.6V(V_{IN}×10%)
Release voltage(V_{DR})=Detect voltage(V_{DF})+Hysteresis width(V_{HYS}).
(*4) RESETB product: Time from when the V_{SEN} pin voltage reaches the detect voltage until the reset output pin reaches 0.6V (V_{IN}×10%).
RESET product: Time from when the V_{SEN} pin voltage reaches the detect voltage until the reset output pin reaches 5.4V (V_{IN}×90%).
(*5) The ambient temperature range (-40℃≦Ta≦125℃) is a design Value.

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■ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	Ta=25℃			-40℃≦Ta≦125℃(*7)			UNITS	CIRCUIT
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.		
RESETB Output Current	I_{RBOUTN}	$V_{SEN}=V_{DF}\times0.9V$, Nch. $V_{RESETB}=0.3V$							mA	⑥
		$V_{IN}=1.6V$	1.9	3.4	-	0.7	3.4	-		
		$V_{IN}=2.0V$	4.2	6.0	-	2.0	6.0	-		
		$V_{IN}=3.0V$	8.6	10.5	-	4.3	10.5	-		
		$V_{IN}=4.0V$	12.7	14.1	-	6.2	14.1	-		
		$V_{IN}=5.0V$	15.6	17.0	-	7.3	17.0	-		
		$V_{IN}=6.0V$	17.8	19.2	-	8.1	19.2	-		
	I_{RBOUTP}	$V_{SEN}=V_{DF}\times1.1V$, Pch. $V_{RESETB}=V_{IN}$-0.3V								
		$V_{IN}=1.6V$	-	-1.2	-0.7	-	-1.2	-0.48		
		$V_{IN}=3.0V$	-	-3.0	-2.5	-	-3.0	-1.1		
		$V_{IN}=6.0V$	-	-4.9	-4.4	-	-4.9	-2.5		
RESET Output Current	I_{ROUTN}	$V_{SEN}=V_{DF}\times1.1V$, Nch. $V_{RESET}=0.3V$							mA	
		$V_{IN}=1.6V$	1.9	3.4	-	0.7	3.4	-		
		$V_{IN}=2.0V$	4.2	6.0	-	2.0	6.0	-		
		$V_{IN}=3.0V$	8.6	10.5	-	4.3	10.5	-		
		$V_{IN}=4.0V$	12.7	14.1	-	6.2	14.1	-		
		$V_{IN}=5.0V$	15.6	17.0	-	7.3	17.0	-		
		$V_{IN}=6.0V$	17.8	19.2	-	8.1	19.2	-		
	I_{ROUTP}	$V_{SEN}=V_{DF}\times0.9V$, Pch. $V_{RESET}=V_{IN}$-0.3V								
		$V_{IN}=1.6V$	-	-1.2	-0.7	-	-1.2	-0.48		
		$V_{IN}=3.0V$	-	-3.0	-2.5	-	-3.0	-1.1		
		$V_{IN}=6.0V$	-	-4.9	-4.4	-	-4.9	-2.5		
RESETB Output Leakage Current	I_{LEAKN}(*6)	$V_{IN}=6.0V$,$V_{SEN}=6.0V$, Nch. $V_{RESETB}=6.0V$	-	0.01	0.1	-	0.01	1.0	μA	
	I_{LEAKP}	$V_{IN}=6.0V$,$V_{SEN}=0V$, Pch. $V_{RESETB}=0V$	-	-0.01	-	-	-0.01	-		
RESET Output Leakage Current	I_{LEAKN}(*6)	$V_{IN}=6.0V$,$V_{SEN}=0V$, Nch. $V_{RESET}=6.0V$	-	0.01	0.1	-	0.01	1.0		
	I_{LEAKP}	$V_{IN}=6.0V$,$V_{SEN}=6.0V$, Pch. $V_{RESET}=0V$	-	-0.01	-	-	-0.01	-		

Unless otherwise specified in measurement conditions, Cd/MRB pin is open.
(*6) Max. value is for XC6133N (Nch open drain).
(*7) The ambient temperature range (-40℃≦Ta≦125℃) is a design Value.

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■ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	Ta=25℃			-40℃≦Ta≦125℃(*11)			UNITS	CIRCUIT
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.		
Cd Pin Sink Current (TYPE:A/E)	I_{Cd}	V_{IN}=1.6V, $V_{Cd/MRB}$=0.5V, V_{SEN}=0V	0.92	1.2		0.66	1.2		mA	⑦
Cd Pin Threshold Voltage(Release)	V_{TCd1}	V_{IN}:1.6V～6.0V, V_{SEN}=0V→V_{DF}×1.1V	V_{IN}×0.46	V_{IN}×0.5	V_{IN}×0.54	V_{IN}×0.46	V_{IN}×0.5	V_{IN}×0.54	V	⑧
Cd Pin Threshold Voltage(Detect)	V_{TCd2}	V_{IN}:1.6V～6.0V, V_{SEN}=V_{DF}×1.1V→0V								
MRB High Level Voltage	V_{MRH}	V_{IN}:1.6V～6.0V, V_{SEN}=V_{DF}×1.1V	V_{IN}×0.55		V_{IN}	V_{IN}×0.55		V_{IN}	V	⑨
MRB Low Level Voltage	V_{MRL}	V_{IN}:1.6V～6.0V, V_{SEN}=V_{DF}×1.1V	0		V_{IN}×0.18	0		V_{IN}×0.18	V	
MRB Minimum Pulse Width	t_{MRIN}(*8)	V_{IN}:Refer to V-1(*10), V_{SEN}=V_{DF}×1.1V, Apply pulse from V_{DF}×1.1V to 0V to the MRB pin.	5.0	-	-	5.0	-	-	μs	⑩
	t_{MRIN}(*9)		32.0			32.0				

Unless otherwise specified in measurement conditions, Cd/MRB pin is open.

(*8) Specification is guaranteed for types A/B/C/D/L/E/F/H/K/M of the CMOS output product and types E/F/H/K/M of the Nch open drain product.

(*9) Specification is guaranteed for types A/B/C/D/L of the Nch open drain output product.

(*10) For V_{IN} conditions, refer to SPEC TABLE (p.10).

(*11) The ambient temperature range (-40℃≦Ta≦125℃) is a design Value.

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■ELECTRICAL CHARACTERISTICS (SPEC TABLE)

Table of Characteristics by Voltage Setting

NOMINAL DETECT VOLTAGE(V)	E-1(Ta=25℃) SENSE Resistance(MΩ)		E-2(-40℃≦Ta≦125℃) SENSE Resistance(MΩ)		V-1 INPUT VOLTAGE (V)
$V_{DF(T)}$	MIN.	TYP.	MIN.	TYP.	
1.0	4.2	13.5	3.5	13.5	1.6
1.1	4.9	14.9	4.0	14.9	↑
1.2	5.5	16.3	4.5	16.3	↑
1.3	6.1	17.7	4.9	17.7	↑
1.4	6.7	19.1	5.4	19.1	↑
1.5	7.4	20.5	5.8	20.5	V_{DF}×1.1
1.6	8.0	21.8	6.3	21.8	↑
1.7	8.6	23.3	6.7	23.3	↑
1.8	9.2	24.7	7.2	24.7	↑
1.9	9.9	26.0	7.6	26.0	↑
2.0	10.5	27.5	8.1	27.5	↑
2.1	11.1	28.9	8.6	28.9	↑
2.2	18.0	38.3	12.1	38.3	↑
2.3	17.8	37.6	11.9	37.6	↑
2.4	17.5	37.0	11.8	37.0	↑
2.5	17.3	36.5	11.7	36.5	↑
2.6	17.1	36.0	11.5	36.0	↑
2.7	17.0	35.6	11.4	35.6	↑
2.8	16.8	35.2	11.3	35.2	↑
2.9	16.7	34.9	11.2	34.9	↑
3.0	16.5	34.5	11.1	34.5	↑
3.1	16.4	34.2	11.0	34.2	↑
3.2	16.3	34.0	11.0	34.0	↑
3.3	16.2	33.7	10.9	33.7	↑
3.4	16.1	33.5	10.8	33.5	↑
3.5	16.0	33.2	10.8	33.2	↑
3.6	15.9	33.0	10.7	33.0	↑
3.7	15.8	32.8	10.7	32.8	↑
3.8	15.7	32.6	10.6	32.6	↑
3.9	15.7	32.5	10.6	32.5	↑
4.0	15.6	32.3	10.5	32.3	↑
4.1	15.6	32.2	10.5	32.2	↑
4.2	15.5	32.0	10.5	32.0	↑
4.3	15.4	31.9	10.4	31.9	↑
4.4	15.4	31.8	10.4	31.8	↑
4.5	15.3	31.7	10.3	31.7	↑
4.6	15.3	31.5	10.3	31.5	↑
4.7	15.2	31.4	10.3	31.4	↑
4.8	15.2	31.3	10.2	31.3	↑
4.9	15.1	31.2	10.2	31.2	↑
5.0	15.1	30.1	10.2	30.1	↑

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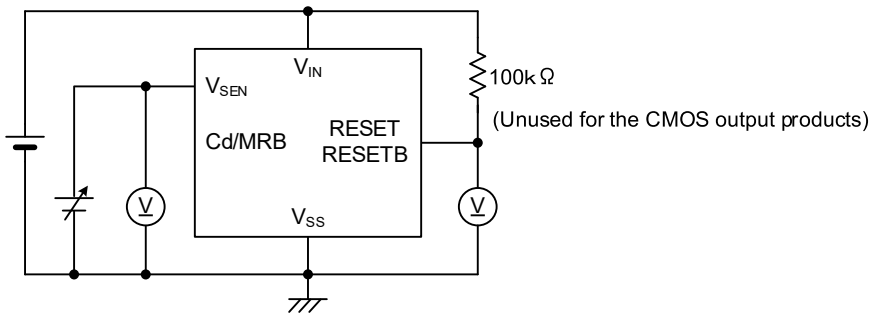
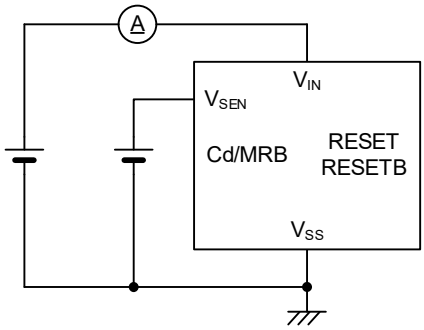
■TEST CIRCUITS

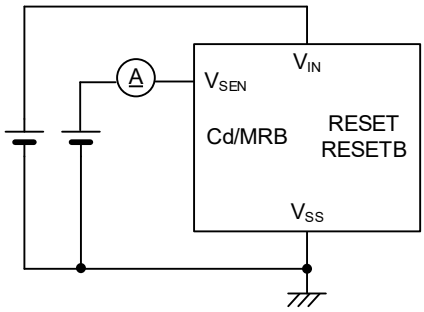
CIRCUIT①



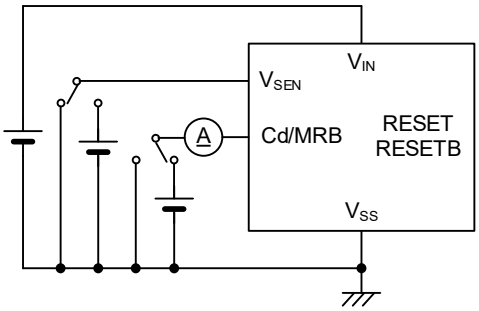
CIRCUIT②



CIRCUIT③



CIRCUIT④



*"RESET" is A/B/C/D/L type, and "RESETB" is E/F/H/K/M type.

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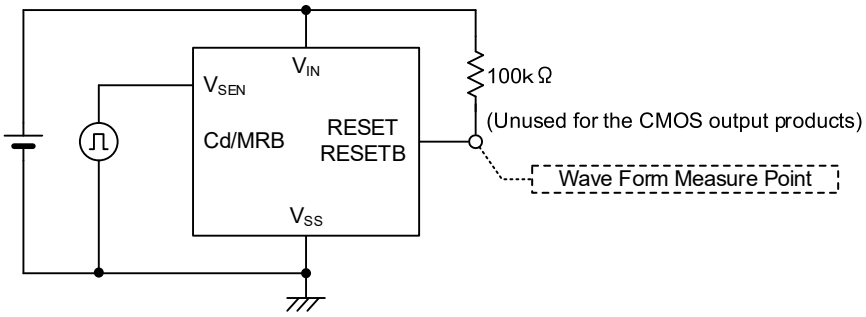
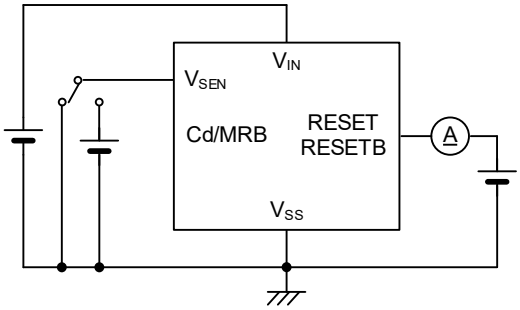
■TEST CIRCUITS (Continued)

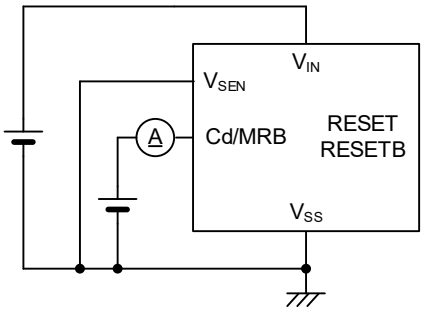
CIRCUIT⑤



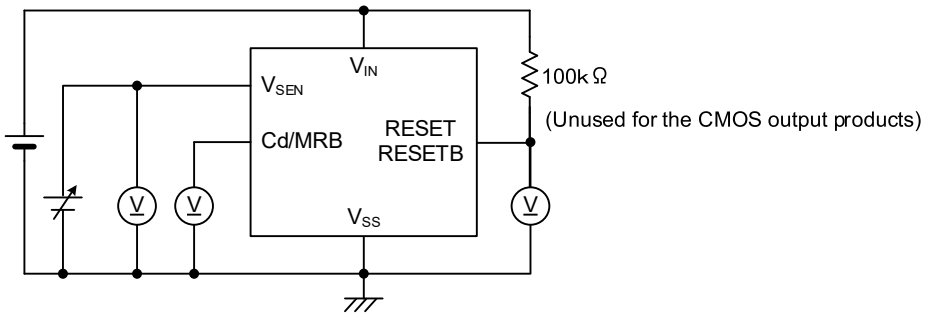
CIRCUIT⑥



CIRCUIT⑦



CIRCUIT⑧



*"RESET" is A/B/C/D/L type, and "RESETB" is E/F/H/K/M type.

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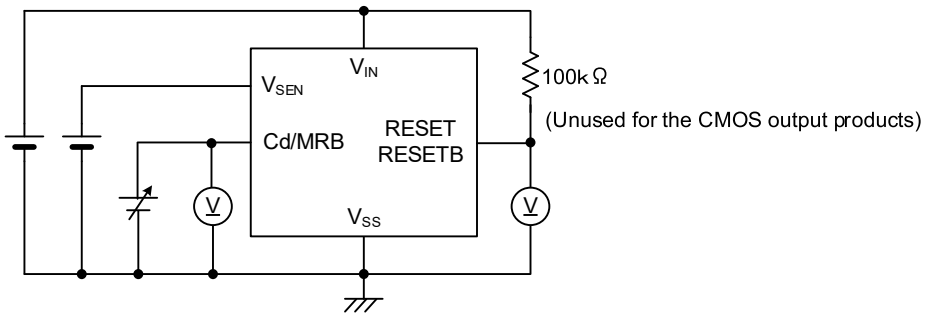
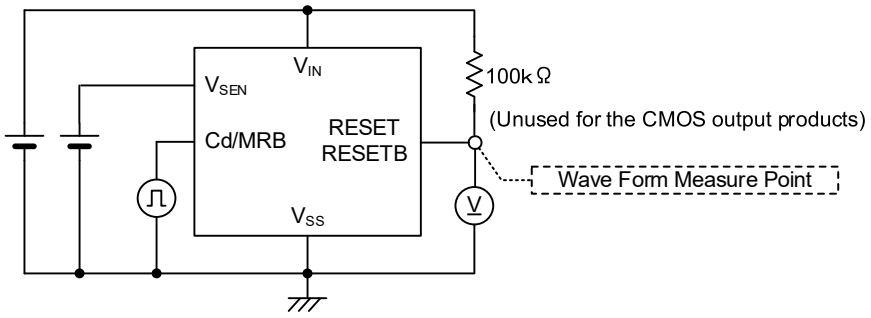
■TEST CIRCUITS (Continued)

CIRCUIT⑨



CIRCUIT⑩



*“RESET” is A/B/C/D/L type, and “RESETB” is E/F/H/K/M type.

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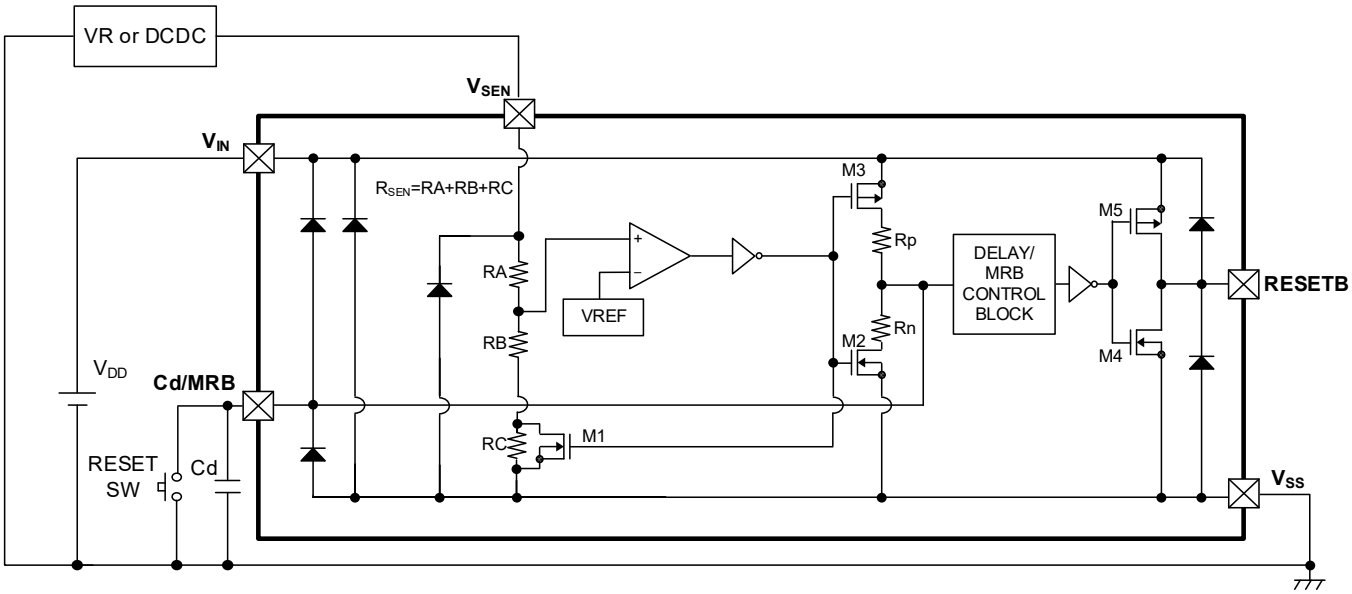
■OPERATIONAL DESCRIPTION

<Basic Operation>

Fig. 1 shows a typical block diagram. Fig. 2 shows the timing chart of Fig. 1.



* The XC6133N series (N-ch open drain output) requires a resistor to pull up the output.

Fig. 1: Typical block diagram (Active Low product)

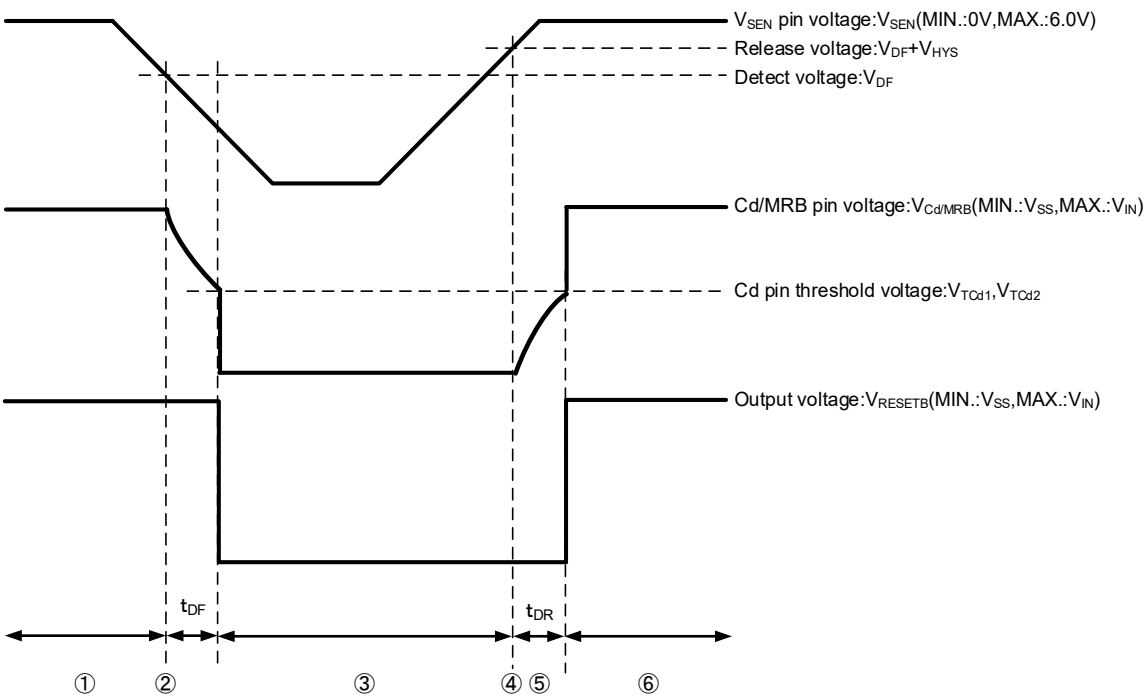


Fig. 2: Timing chart of Fig. 1(V_{IN}=6.0V, Active Low)

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■OPERATIONAL DESCRIPTION (Continued)

①In the initial state, a voltage that is sufficiently high (MAX.: 6.0V) with respect to the release voltage is applied to the V_{SEN} pin, and the delay capacitance Cd is charged up to the power input pin voltage.
The V_{SEN} pin voltage starts to fall, and during the time until it reaches the detect voltage ($V_{SEN}>V_{DF}$), V_{RESETB} is High level ($=V_{IN}$).

Note: If the pull-up resistor is connected to a power supply other than the power input pin V_{IN} when using the Nch open drain output (XC6133N), High level will be the voltage of the power supply to which the pull-up resistor is connected.

②The V_{SEN} pin voltage continues to drop, and when it reaches the detect voltage ($V_{SEN}=V_{DF}$), the Nch transistor for delay capacitance discharge turns ON, and discharge of the delay capacitance Cd starts through the delay resistor Rn.
The time from $V_{SEN}=V_{DF}$ until V_{RESETB} reaches Low level is the detect delay time t_{DF} (the detect time when the capacitor is not connected to the Cd/MRB pin is t_{DF0}).The delay capacitance Cd is discharged through the delay resistor Rn when it is above the threshold voltage of V_{TCD2}. When it is below the threshold voltage of V_{TCD2}, the delay capacitance Cd is discharged faster through the internal built-in low impedance switch.

③During the time that the V_{SEN} pin voltage is below the detect voltage V_{DF}, the delay capacitance Cd discharges to ground level.
The V_{SEN} pin starts rising again, and during the time until it reaches the release voltage ($V_{SEN}<V_{DF}+V_{HYS}$), V_{RESETB} holds Low level.

④The V_{SEN} pin voltage continues to rise, and when it reaches the release voltage ($V_{DF}+V_{HYS}$), the Nch transistor for delay capacitance discharge turns OFF, and charging of the delay capacitance Cd through the delay resistor Rp starts.
The delay capacitance Cd is discharged through the delay resistor Rp when it is below the threshold voltage of V_{TCD1}.
When it is above the threshold voltage of V_{TCD1}, the delay capacitance Cd is discharged faster through the internal built-in low impedance switch.

⑤When the Cd/MRB pin voltage reaches V_{TCd1}, V_{RESETB} changes to High level.
The time from $V_{SEN}=V_{DF}+V_{HYS}$ until the V_{RESETB} logic changes is the release delay time t_{DR} (the release time when the capacitor is not connected to the Cd/MRB pin is t_{DR0}).

⑥During the time that the V_{SEN} pin voltage is higher than the detect voltage ($V_{SEN}>V_{DF}$), V_{RESETB} holds High level.

The above operation description is for an Active Low detection product.
For an Active High product, reverse the logic of the reset pin.

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■OPERATIONAL DESCRIPTION (Continued)

<High voltage detection circuit example>

High voltage detects battery voltage (+B) which was divided into R1 and R2.
The calculation method for high voltage detection is given below.
For the circuit schematic, refer to Fig. 3: High voltage detection circuit.

$V_{DF}(H)=V_{DF}(T)\times\{(R1+R2)\div R2\}$
$V_{HYS}(H)=V_{HYS}\times\{(R1+R2)\div R2\}$
$V_{DR}(H)=V_{DF}(H)+V_{HYS}(H)$

Example 1: For detecting 12.0V (+B: Battery voltage), R1=220kΩ and R2=20kΩ are set to divide the battery voltage and the V_{SEN} pin voltage is set to $V_{DF}(T)$=1.0V.
The release voltage $V_{DR}(T)$=1.05V(TYP.) and $V_{HYS}=V_{DR}(T)-V_{DF}(T)$=0.05V(TYP.) are pre-set inside the IC.

$V_{DF}(H)$=12.0V
$V_{HYS}(H)$=0.6V
$V_{DR}(H)$=12.6V

(Note 1) $V_{DF}(H)$ is the detect voltage after external adjustment.
(Note 2) $V_{HYS}(H)$ is the hysteresis range after external adjustment.
(Note 3) $V_{DR}(H)$ is the release voltage after external adjustment.
(Note 4) $V_{DF}(T)$ is the detect voltage.
(Note 5) V_{HYS} is the hysteresis range inside of the IC.
(Note 6) $V_{DR}(T)$ is the release voltage.
(Note 7) The R2 resistance is in parallel with the internal R_{SEN} resistance, and thus to increase the accuracy of the detect voltage and release voltage after external adjustment, select an R2 resistance that is sufficiently small with respect to the R_{SEN} resistance. For R_{SEN} resistance values, refer to SPEC TABLE
(Note 8) If high voltage is to be detected, divide the voltage with resistors R1 and R2 so that V_{SEN} pin≦6V.

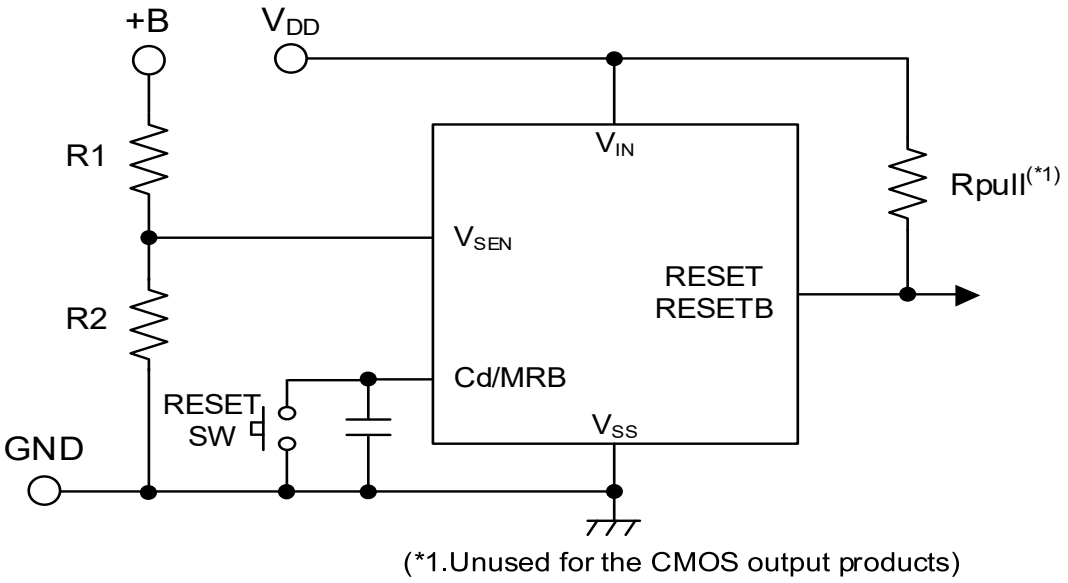

Fig. 3: High Voltage Detection Circuit

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■OPERATIONAL DESCRIPTION (Continued)

<Release delay time / detect delay time>

The release delay time and detect delay time are determined by the delay resistors (Rp and Rn) and the delay capacitance Cd. The ratio of the delay resistances (Rp and Rn) is selectable from 5 options. The delay time is adjustable using the combination of delay resistance and delay capacitance value. (Refer to “Selection Guide”)
The release delay time (t_{DR}) is calculated using Equation (1).

$$t_{DR}=Rp\times Cd\times\{-\ln(1-V_{TCd1}/V_{IN})\}+t_{DR0} \quad \ldots(1)$$

* ln is the natural logarithm.

The delay capacitance pin threshold voltage is $V_{TCd1}=V_{IN}/2$(TYP.), and thus when t_{DR0} can be neglected, the release delay time can be calculated simply using Equation (2).

$$t_{DR}=Rp\times Cd\times[-\ln\{1-(V_{IN}/2)/V_{IN}\}]=Rp\times Cd\times 0.693 \quad \ldots (2)$$

The detect delay time (t_{DF}) is calculated using Equation (3).

$$t_{DF}=Rn\times Cd\times\{-\ln(V_{TCd2}/V_{IN})\}+t_{DF0} \quad \ldots(3)$$

* ln is the natural logarithm.

The delay capacitance pin threshold voltage is $V_{TCd2}=V_{IN}/2$ (TYP.), and thus when t_{DF0} can be neglected, the detect delay can be calculated simply using Equation (4).

$$t_{DF}=Rn\times Cd\times\{-\ln(V_{IN}/2)/V_{IN}\}=Rn\times Cd\times 0.693 \quad \ldots(4)$$

Example 2: When type A is selected (Rp : Rn=144kΩ : 0Ω), the delay times are as follows:
If Cd is set to 0.1uF,

$$t_{DR}=144\times10^{3}\times0.1\times10^{-6}\times0.693=10\text{ms}$$

t_{DF} is the detect delay time (t_{DFO}) when the delay capacitance Cd is not connected.

Example 3: When type B is selected (Rp : Rn=144kΩ : 18kΩ) , the delay times are as follows:
If Cd is set to 0.1uF,

$$t_{DR}=144\times10^{3}\times0.1\times10^{-6}\times0.693=10\text{ms}$$
$$t_{DF}=18\times10^{3}\times0.1\times10^{-6}\times0.693=1.25\text{ms}$$

(Note 9) The release delay times t_{DR} in Examples 2 and 3 are the values calculated from Equation (2).
(Note 10) The detect delay time t_{DF} in Example 3 is the value calculated from Equation (4).
(Note 11) Note that the delay times will vary depending on the actual capacitance value of the delay capacitance Cd.

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■OPERATIONAL DESCRIPTION (Continued)

＜Manual reset function＞

The Cd/MRB pin can also be used as a manual reset pin.
When the Cd and RESET switch are connected to the Cd/MRB pin (refer to Fig.1), and under the release condition, if the RESET switch turns on, then the detect signal is generated at the RESET/RESETB pin forcibly.

For Active Low type (RESETB), under the release condition, if the RESET switch turns on, then the voltage at the RESETB pin changes from H to L after the detect delay time.

For Active High type (RESET), under the release condition, if the RESET switch turns on, then the voltage at the RESET pin changes from L to H after the detect delay time.

Under the detect condition, the condition will be kept even if the RESET switch turns on and off.

In the case that either H level or L level is fed to the Cd/MRB pin without the RESET switch, the behavior of the XC6133 follows the timing chart in Fig. 4.

L level is fed to MRB pin under the detect condition, the RESET switch will be kept.
H level is fed to MRB pin under the detect condition, the RESET switch will be undefined.

Even though the voltage at the V_{SEN} pin changes from a higher voltage than the detect voltage to a lower voltage, as long as H level is fed to the MRB pin, the release condition is kept.

If H level or L level is fed to the Cd/MRB pin forcibly, then even though Cd is connected to the pin, the XC6133 can't have any delay time.

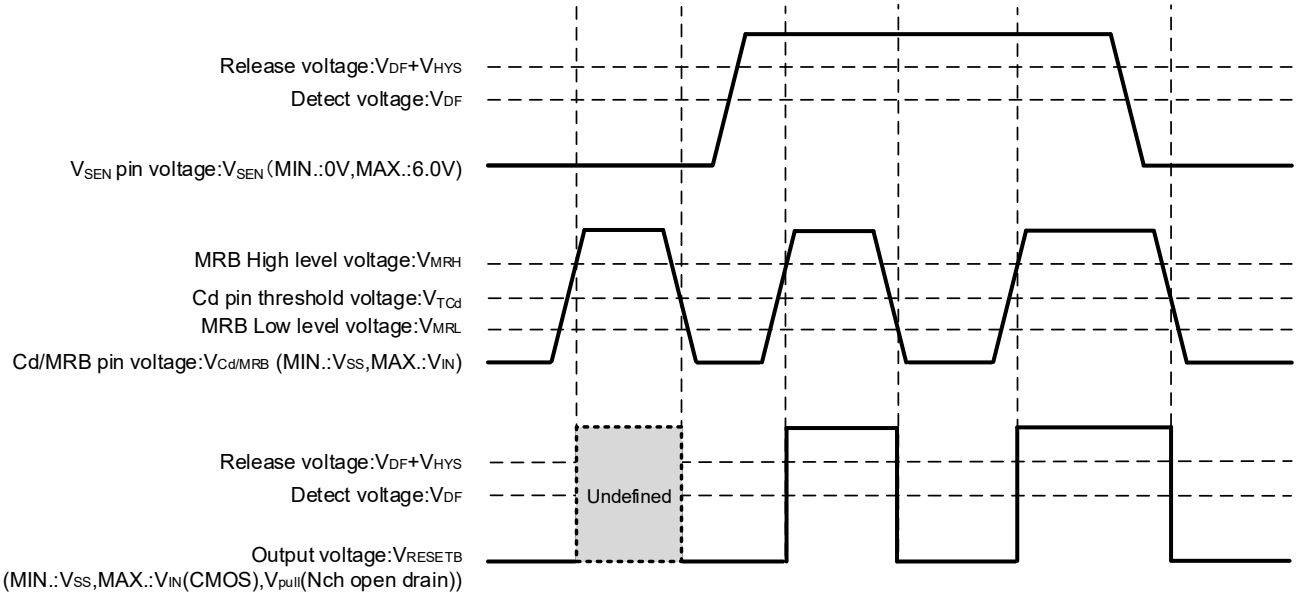

Fig. 4: Manual reset operation using the Cd/MRB pin (V_{IN}=6.0V, Active Low)

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■NOTES ON USE

1) Please use this IC within the stated maximum ratings. For temporary, transitional voltage drop or voltage rising phenomenon, the IC isliable to malfunction should the ratings be exceeded.

2) The power input pin voltage may fall due to the flow through current during IC operation and the resistance component between the power supply and the power input pin.
In the case of CMOS output, a drop in the power input pin voltage may occur in the same way due to the output current. When this happens, if the power input pin voltage drops below the minimum operating voltage, a malfunction may occur.

3) Note that large, sharp changes of the power input pin voltage may lead to malfunction.

4) Power supply noise is sometimes a cause of malfunction. Sufficiently test using the actual device, such as inserting a capacitor between V_{IN} and GND.

5) There is a possibility that oscillation will occur if the resistances of the V_{SEN} pin is high. Use a resistance of 1MΩ or less between the node to monitor and V_{SEN} pin.

6) Exercise caution if V_{IN} and V_{SEN} are started in common, as the output will be undefined until V_{IN} reaches the operating voltage.

7) For a manual reset function, in case when the function is activated by feeding either MRB H level or MRB L level to Cd/MRB pin instead of using a reset switch, please note these phenomena below;

・The RESET output signal will be undefined when MRB H is fed to Cd/MRB pin under the detect condition.
・The RESET output signal will be undefined based on the voltage relationship between V_{SEN} pin and Cd/MRB pin.

8) When an N-ch open drain output is used, the V_{RESETB} voltage at detection and release is determined by the pull-up resistance connected to the output pin. Refer to the following when selecting the resistance value.

At detection:

$V_{RESETB}=V_{pull}/(1+R_{pull}/R_{ON})$

V_{pull} : Voltage after pull-up

R_{ON}(*1) : ON resistance of N-ch driver M4 (calculated from V_{RESETB}/I_{RBOUTN} based on electrical characteristics)

Example: When V_{IN}=2.0V(*2), $R_{ON}=0.3/4.2\times10^{-3}=71.4\Omega$ (MAX.).

If it is desired to make V_{RESETB} at detection 0.1V or less when V_{pull} is 3.0V,

$R_{pull}=\{(V_{pull}/V_{RESETB})-1\}\times R_{ON}=\{(3/0.1)-1\}\times71.4\fallingdotseq2.1k\Omega$

Therefore, to make the output voltage at detection 0.1V or less under the above conditions, the pull-up resistance must be 2.1kΩ or higher.

(*1) Note that R_{ON} becomes larger as V_{IN} becomes smaller.

(*2) For V_{IN} in the calculation, use the lowest value of the input voltage range you will use.

At release:

$V_{RESETB}=V_{pull}/(1+R_{pull}/R_{off})$

V_{pull}: Voltage after pull-up

R_{off}: Resistance when N-ch driver M4 is OFF (calculated from V_{RESETB}/I_{LEAKN} based on electrical characteristics)

Example:When V_{pull} is 6.0V, $R_{off}=6/(0.1\times10^{-6})=60M\Omega$ (MIN.). If it is desired to make V_{RESETB} 5.99V or higher,

$R_{pull}=\{(V_{pull}/V_{RESETB})-1\}\times R_{off}=\{(6/5.99)-1\}\times60\times10^{6}\fallingdotseq100k\Omega$

Therefore, to make the output voltage at release 5.99V or higher under the above conditions, the pull-up resistance must be 100kΩ or less.

9) If the discharge time of the delay capacitance Cd at detection is short and the delay capacitance Cd cannot be discharged to ground level, charging will take place at the next release operation with electric charge remaining in the delay capacitance Cd, and this may cause the release delay time to become noticeably short.

10) If the charging time of the delay capacitance Cd at release is short and the delay capacitance Cd cannot be charged to the V_{IN} level, the delay capacitance Cd will discharge from less than the V_{IN} level at the next detection operation, and this may cause the detect delay time to become noticeably short.

11) Torex places an importance on improving our products and their reliability.
We request that users incorporate fail-safe designs and post-aging protection treatment when using Torex products in their systems.

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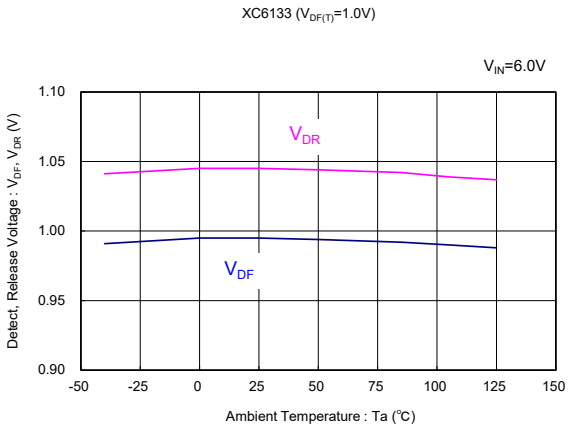
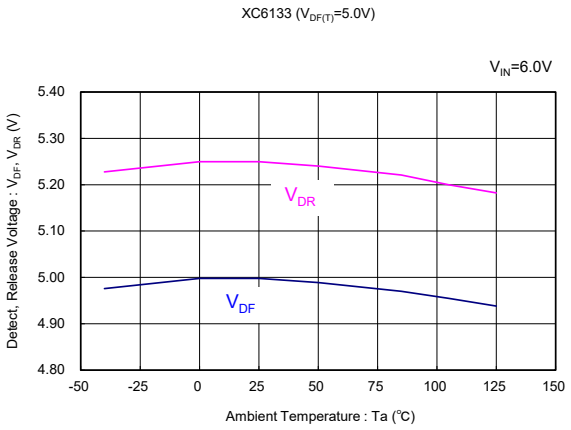
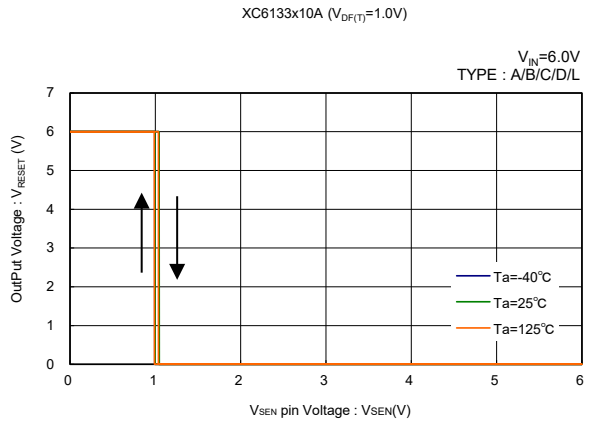
■TYPICAL PERFORMANCE CHARACTERISTICS

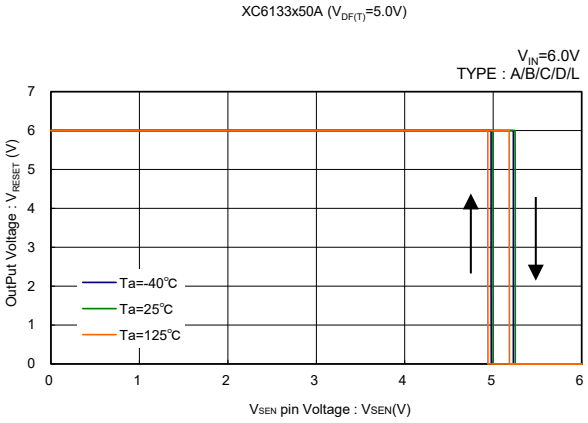
(1) Detect, Release Voltage vs. Ambient Temperature



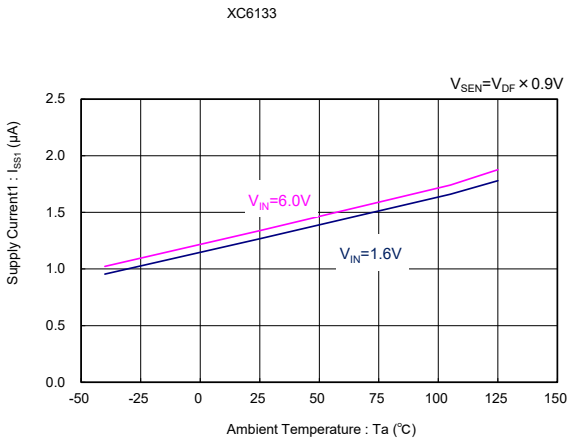


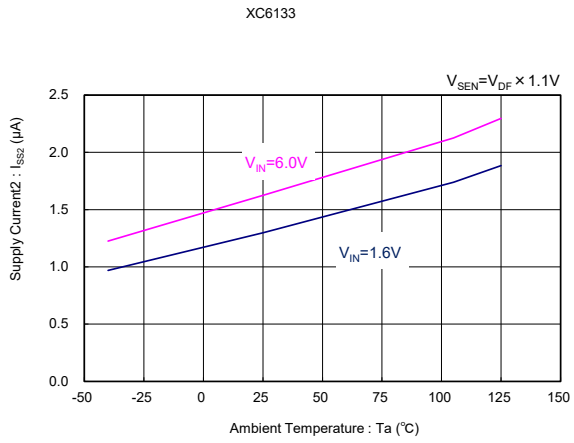
(2) Output Voltage vs Sense Voltage





(3) Supply Current vs. Ambient Temperature





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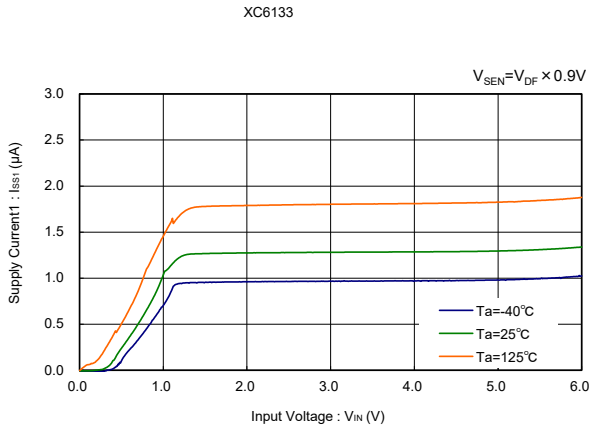
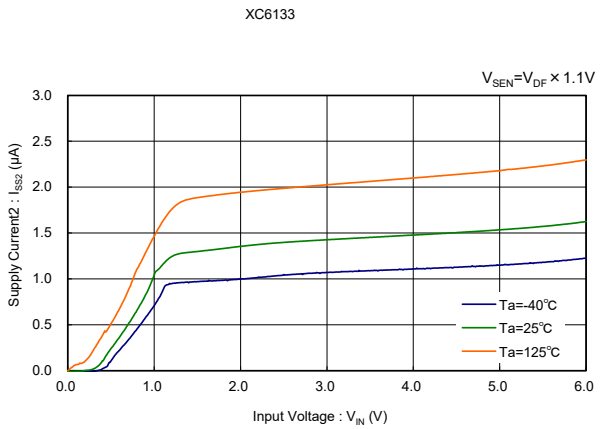
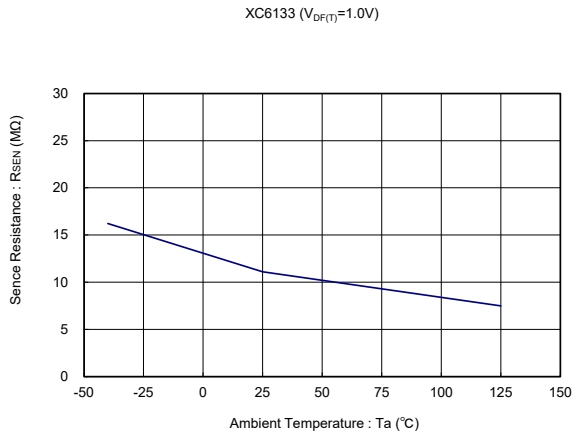
■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

(4) Supply Current vs. Input Voltage

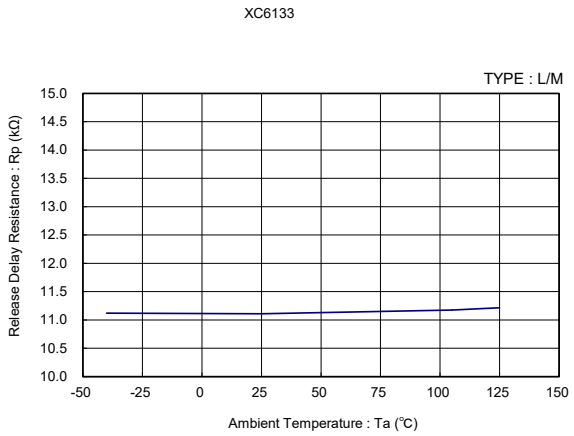


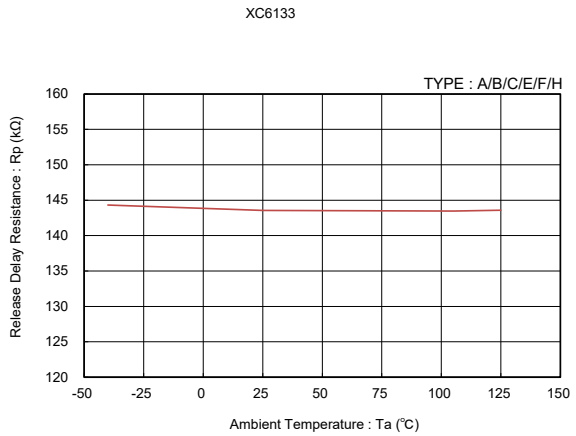


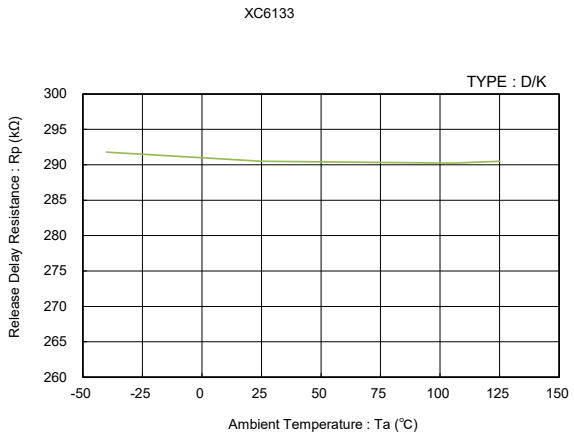
(5) Sense Resistance vs Ambient Temperature



(6) Delay Resistance vs Ambient Temperature







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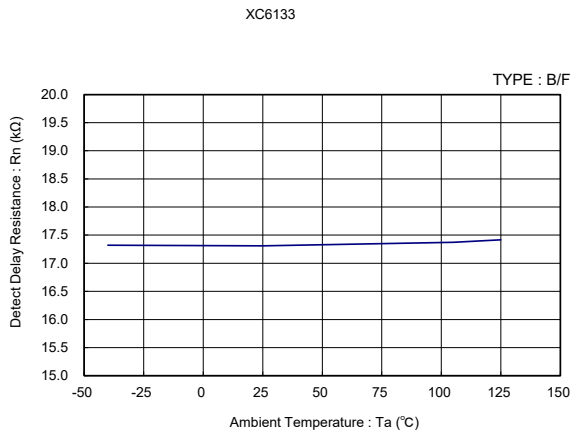
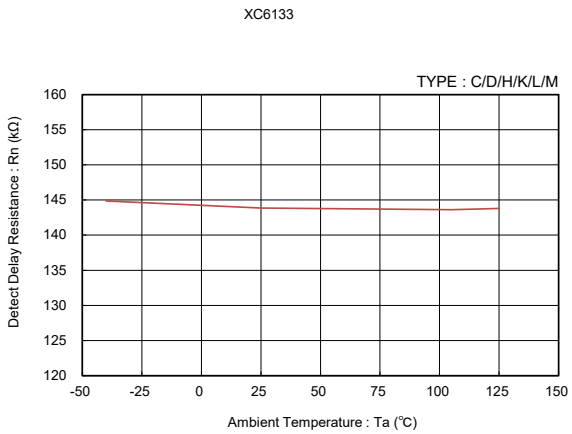
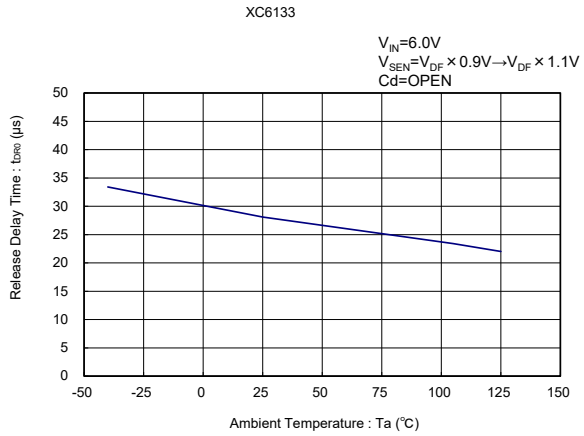
■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

(6) Delay Resistance vs Ambient Temperature (Continued)

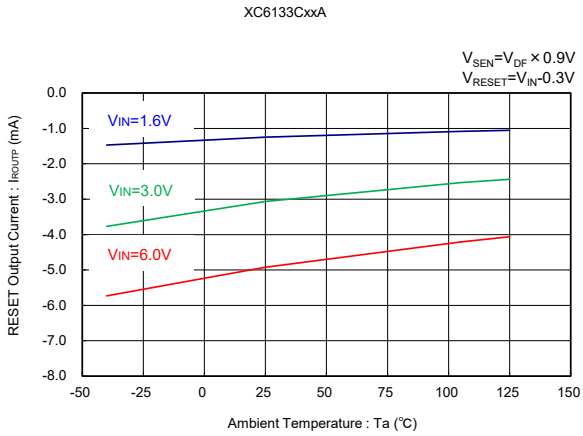




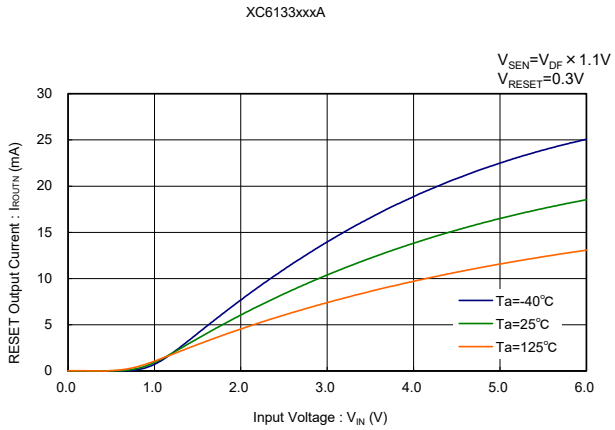
(7) Delay Time vs Ambient Temperature

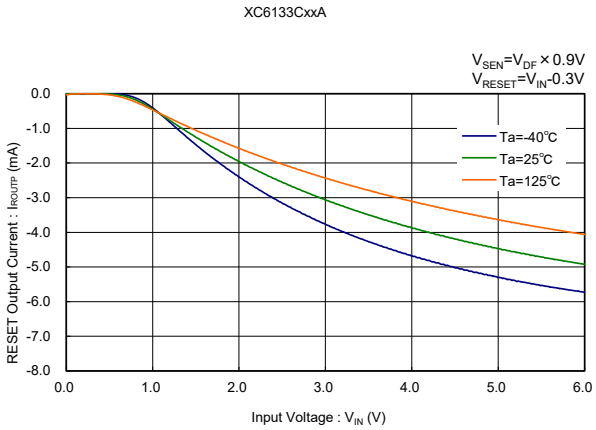


(8) RESET Output Current vs Ambient Temperature (Continued)



(9) RESET Output Current vs Input Voltage





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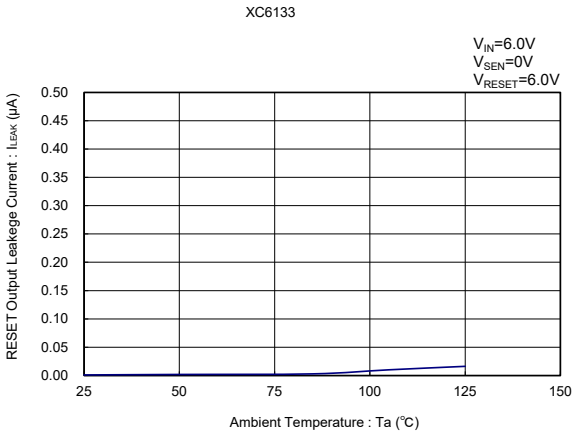
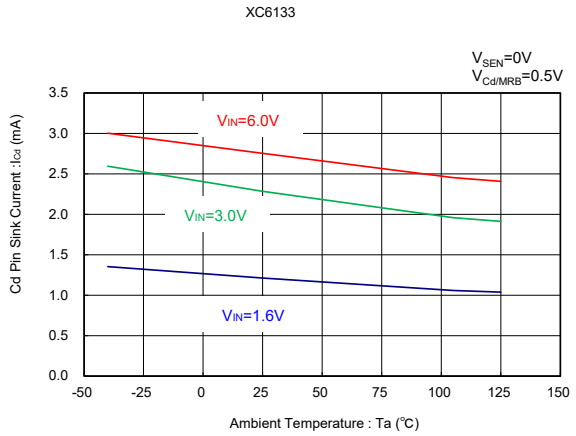
■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

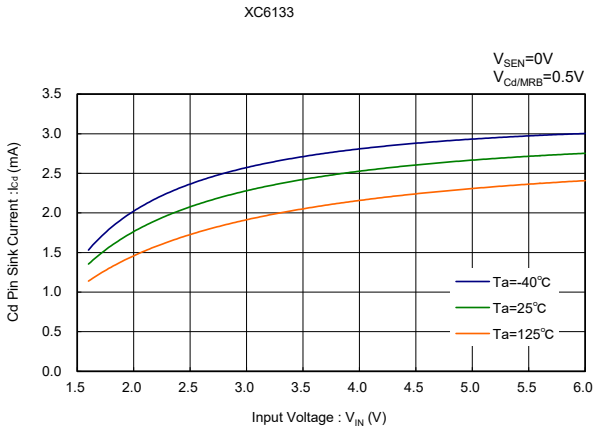
(10) RESET Output Leakage Current vs Ambient Temperature



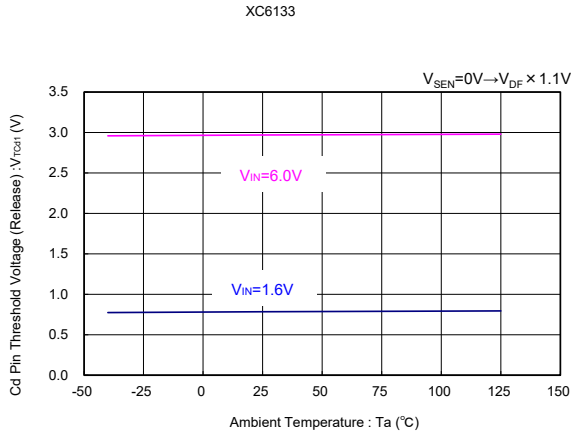
(11) Cd Pin Sink Current vs Ambient Temperature

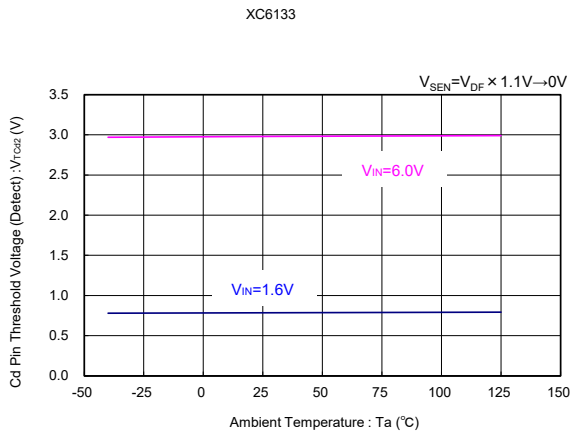


(12) Cd Pin Sink Current vs Input Voltage



(13) Cd Pin Threshold Voltage vs Ambient Temperature





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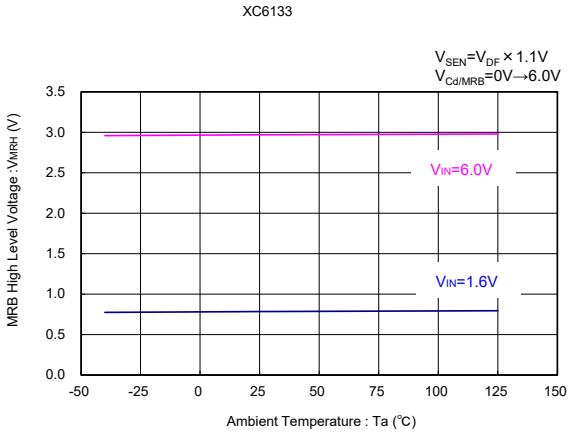
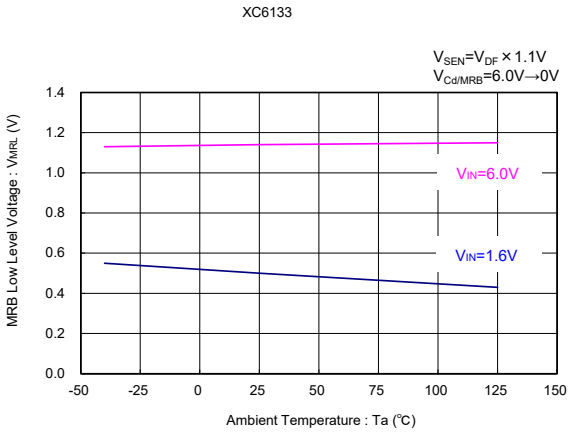
■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

(14) MRB High Level Threshold Voltage vs Ambient Temperature



(15) MRB Low Level Threshold Voltage vs Ambient Temperature



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■PACKAGING INFORMATION

For the latest package information go to, www.torexsemi.com/technical-support/packages

PACKAGE	OUTLINE / LAND PATTERN	THERMAL CHARACTERISTICS
SOT-26	SOT-26 PKG	SOT-26 Power Dissipation
USP-6C	USP-6C PKG	USP-6C Power Dissipation

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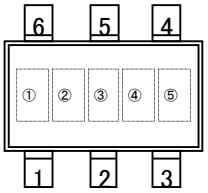
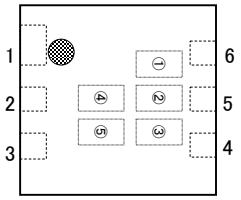
■MARKING RULE

SOT-26



USP-6C



① represents products series

MARK	PRODUCT SERIES
X	XC6133******-G

②,③ represents internal sequential number
01, ⋯, 09, 10, ⋯, 99, A0, ⋯, A9, B0, ⋯, B9, ⋯, Z9⋯ repeated.
(G, I, J, O, Q, W excluded)

④,⑤ represents production lot number
01～09, 0A～0Z, 11～9Z, A1～A9, AA～AZ, B1～ZZ in order.
(G, I, J, O, Q, W excluded)
* No character inversion used.

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