To our customers,

Old Company Name in Catalogs and Other Documents

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Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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RD74LVC16373B

16-bit D-type Transparent Latches with 3-state Outputs

REJ03D0500–0100
Rev.1.00
Jan. 24, 2005

Description

The RD74LVC16373B has sixteen D type latches with three state outputs in a 48 pin package. When the latch enable input is high, the Q outputs will follow the D inputs. When the latch enable goes low, data at the D inputs will be retained at the outputs until latch enable returns high again. When a high logic level is applied to the output control input ($1\overline{G}$, $2\overline{G}$), all outputs go to a high impedance state, regardless of what signals are present at the other inputs and the state of the storage elements. Low voltage and high-speed operation is suitable at the battery drive product (note type personal computer) and low power consumption extends the life of a battery for long time operation.

Features

- V_{CC} = 1.65 V to 5.5 V
- All inputs V_{IH} (Max.) = 5.5 V (@V_{CC} = 0 V to 5.5 V)
- All outputs V_{OUT} (Max.) = 5.5 V (@V_{CC} = 0 V or output off state)
- Typical V_{OL} ground bounce < 0.8 V (@V_{CC} = 3.3 V, Ta = 25°C)
- Typical V_{OH} undershoot > 2.0 V (@V_{CC} = 3.3 V, Ta = 25°C)
- High output current ±4 mA (@V_{CC} = 1.65 V)
  ±8 mA (@V_{CC} = 2.3 V)
  ±12 mA (@V_{CC} = 2.7 V)
  ±24 mA (@V_{CC} = 3.0 V to 5.5 V)
- Ordering Information

Part Name	Package Type	Package Code (Previous Code)	Package Abbreviation	Taping Abbreviation (Quantity)
RD74LVC16373BTEL	TSSOP–48 pin	PTSP0048KA–A (TTP–48DBV)	T	EL (1,000 pcs/reel)

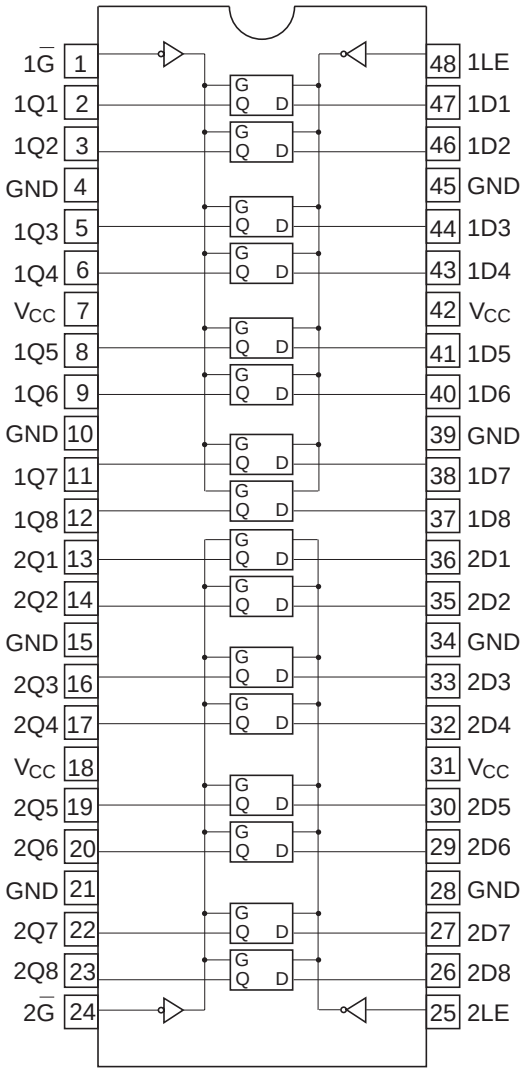
Function Table

Inputs			Output Q
$\overline{G}$	LE	D	
H	X	X	Z
L	H	L	L
L	H	H	H
L	L	X	Q_0

H: High level
L: Low level
X: Immaterial
Z: High impedance
Q_0: Level of Q before the indicated steady input conditions were established.

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Pin Arrangement



(Top view)

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Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	V_{CC}	–0.5 to 7.0	V	
Input diode current	I_{IK}	–50	mA	V_I = –0.5 V
Input voltage	V_I	–0.5 to 7.0	V	
Output diode current	I_{OK}	–50	mA	V_O = –0.5 V
		50		V_O = V_{CC}+0.5 V
Output voltage	V_O	–0.5 to V_{CC}+0.5	V	Output "H" or "L"
		–0.5 to 7.0		Output "Z" or V_{CC}: OFF
Output current	I_O	±50	mA	
V_{CC}, GND current / pin	I_{CC} or I_{GND}	100	mA	
Storage temperature	Tstg	–65 to +150	°C	

Note: The absolute maximum ratings are values, which must not individually be exceeded, and furthermore, no two of which may be realized at the same time.

Recommended Operating Conditions

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	V_{CC}	1.5 to 5.5	V	Data hold
		1.65 to 5.5		At operation
Input/output voltage	V_I	0 to 5.5	V	$\overline{G}$, LE, D
	V_O	0 to V_{CC}		Output "H" or "L"
		0 to 5.5		Output "Z" or V_{CC}: OFF
Operating temperature	Ta	–40 to 85	°C	
Output current	I_{OH}	–4	mA	V_{CC} = 1.65 V
		–8		V_{CC} = 2.3 V
		–12		V_{CC} = 2.7 V
		–24		V_{CC} = 3.0 V to 5.5 V
	I_{OL}	4	mA	V_{CC} = 1.65 V
		8		V_{CC} = 2.3 V
		12		V_{CC} = 2.7 V
		24		V_{CC} = 3.0 V to 5.5 V
Input rise / fall time[*1]	t_r, t_f	20	ns/V	V_{CC} = 1.65 V to 2.7 V
		10		V_{CC} = 3.0 V to 5.5 V

Notes: 1. This item guarantees maximum limit when one input switches.
Waveform: Refer to test circuit of switching characteristics.

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Electrical Characteristics

Item	Symbol	V_{CC} (V)	Ta = –40 to 85°C		Unit	Test Conditions
			Min	Max		
Input voltage	V_{IH}	1.65 to 1.95	V_{CC}×0.65	—	V	
		2.3 to 2.7	1.7	—		
		2.7 to 3.6	2.0	—		
		4.5 to 5.5	V_{CC}×0.7	—		
	V_{IL}	1.65 to 1.95	—	V_{CC}×0.35		
		2.3 to 2.7	—	0.7		
		2.7 to 3.6	—	0.8		
		4.5 to 5.5	—	V_{CC}×0.3		
Output voltage	V_{OH}	1.65 to 5.5	V_{CC}–0.2	—	V	I_{OH} = –100 µA
		1.65	1.2	—		I_{OH} = –4 mA
		2.3	1.7	—		I_{OH} = –8 mA
		2.7	2.2	—		I_{OH} = –12 mA
		3.0	2.4	—		
		3.0	2.2	—		I_{OH} = –24 mA
		4.5	3.8	—		
	V_{OL}	1.65 to 5.5	—	0.2		I_{OL} = 100 µA
		1.65	—	0.45		I_{OL} = 4 mA
		2.3	—	0.7		I_{OL} = 8 mA
		2.7	—	0.4		I_{OL} = 12 mA
		3.0	—	0.55		I_{OL} = 24 mA
		4.5	—	0.55		
Input current	I_{IN}	0 to 5.5	—	±5.0	µA	V_{IN} = 5.5 V or GND
Output leak current	I_{OFF}	0	—	±5.0	µA	V_{IN} / V_{OUT} = 5.5 V
Off state output current	I_{OZ}	2.7 to 5.5	—	±5.0	µA	V_{IN} = V_{CC} or GND V_{OUT} = 5.5 V or GND
Quiescent supply current	I_{CC}	2.7 to 3.6	—	±10.0	µA	V_{IN} = 3.6 to 5.5 V
		2.7 to 5.5	—	10.0	µA	V_{IN} = V_{CC} or GND
	ΔI_{CC}	2.7 to 3.6	—	500	µA	V_{IN} = one input at (V_{CC}–0.6)V, other inputs at V_{CC} or GND

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Switching Characteristics

Item	Symbol	V_{CC} (V)	Ta = –40 to 85°C			Unit	From (Input)	To (Output)
			Min	Typ	Max			
Propagation delay time	t_{PLH}	1.8±0.15	1.0	—	19.1	ns	D	Q
	t_{PHL}	2.5±0.2	1.0	—	9.6			
		2.7	1.0	—	7.7			
		3.3±0.3	1.5	—	7.0			
		5.0±0.5	1.0	—	5.5			
	t_{PLH}	1.8±0.15	1.0	—	19.1	ns	LE	Q
	t_{PHL}	2.5±0.2	1.0	—	9.6			
		2.7	1.0	—	7.7			
		3.3±0.3	1.5	—	7.0			
		5.0±0.5	1.0	—	5.5			
Output enable time	t_{ZH}	1.8±0.15	1.0	—	20.0	ns	$\overline{G}$	Q
	t_{ZL}	2.5±0.2	1.0	—	10.5			
		2.7	1.0	—	8.0			
		3.3±0.3	1.5	—	7.0			
		5.0±0.5	1.0	—	6.0			
Output disable time	t_{HZ}	1.8±0.15	1.0	—	20.0	ns	$\overline{G}$	Q
	t_{LZ}	2.5±0.2	1.0	—	10.5			
		2.7	1.0	—	8.0			
		3.3±0.3	1.5	—	7.0			
		5.0±0.5	1.0	—	6.0			
Setup time	t_{su}	1.8±0.15	6.0	—	—	ns		
		2.5±0.2	4.0	—	—			
		2.7	2.0	—	—			
		3.3±0.3	2.0	—	—			
		5.0±0.5	2.0	—	—			
Hold time	t_h	1.8±0.15	4.0	—	—	ns		
		2.5±0.2	2.0	—	—			
		2.7	1.5	—	—			
		3.3±0.3	1.5	—	—			
		5.0±0.5	1.5	—	—			
Pulse width	t_w	1.8±0.15	9.0	—	—	ns		
		2.5±0.2	4.0	—	—			
		2.7	3.3	—	—			
		3.3±0.3	3.3	—	—			
		5.0±0.5	3.3	—	—			
Between output pins skew[*1]	t_{OSLH}	1.8±0.15	—	—	—	ns		
	t_{OSHL}	2.5±0.2	—	—	—			
		2.7	—	—	—			
		3.3±0.3	—	—	1.0			
		5.0±0.5	—	—	1.0			
Input capacitance	C_{IN}	3.3	—	4.0	—	pF		
Output capacitance	C_O	3.3	—	8.0	—	pF		

Note: 1. This parameter is characterized but not tested.

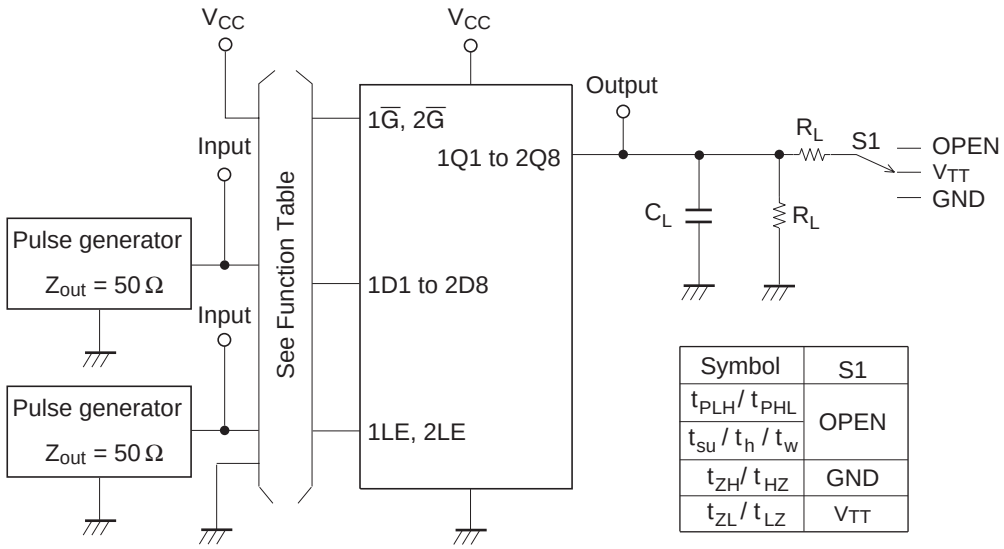
$tos_{LH} = | t_{PLHm} - t_{PLHn} |$, $tos_{HL} = | t_{PHLm} - t_{PHLn} |$

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Operating Characteristics

Item	Symbol	V_{CC} (V)	Ta = 25°C			Unit	Test Conditions
			Min	Typ	Max		
Power dissipation capacitance	C_{PD}	1.8	—	27	—	pF	f = 10 MHz
		2.5	—	28	—		
		3.3	—	30	—		
		5.0	—	35	—		

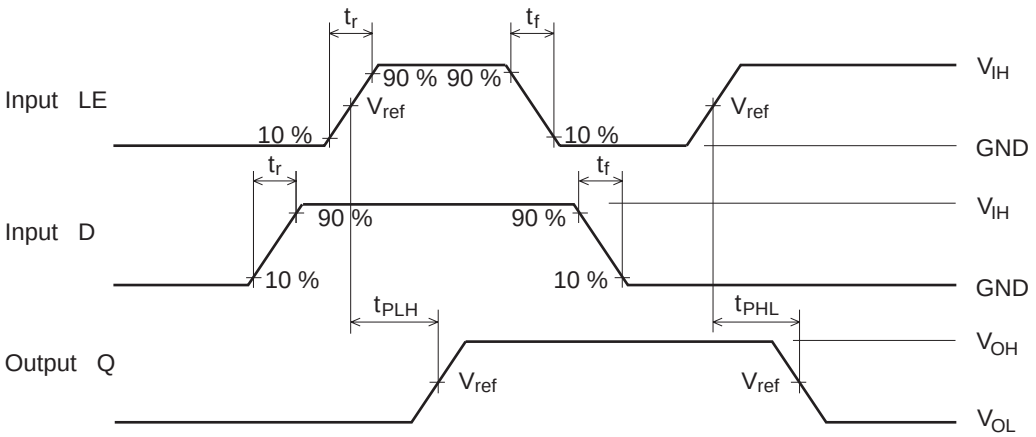
Test Circuit



Symbol	S1
t_{PLH} / t_{PHL}	OPEN
t_{su} / t_h / t_w	
t_{ZH} / t_{HZ}	GND
t_{ZL} / t_{LZ}	VTT

Note: 1. C_L includes probe and jig capacitance.

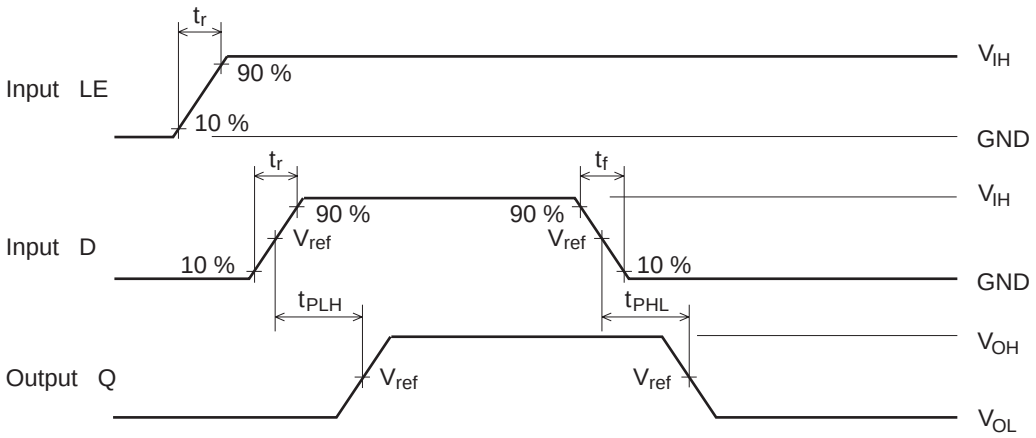
Waveforms – 1



Note: Input waveform: PRR = 10 MHz, duty cycle 50%.

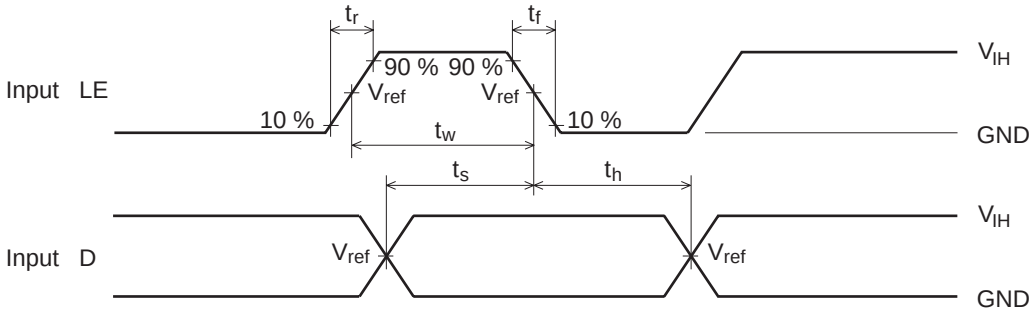
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Waveforms – 2



Note: Input waveform: PRR = 10 MHz, duty cycle 50%.

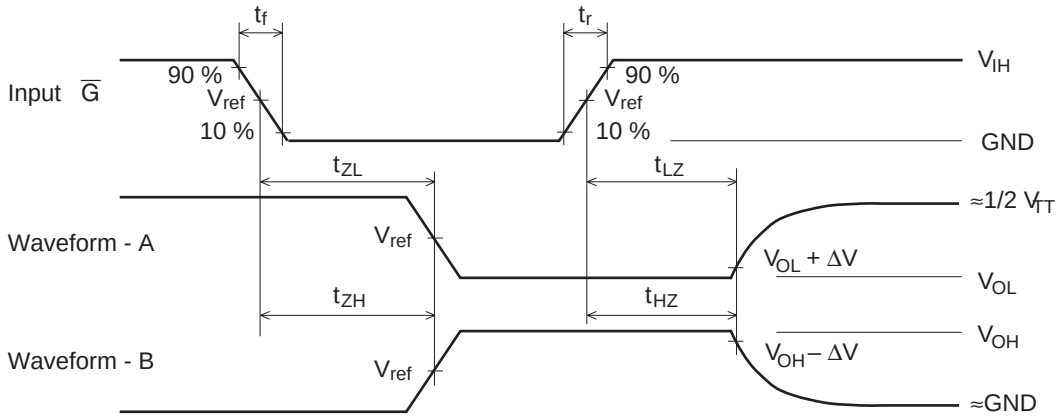
Waveforms – 3



Note: Input waveform: PRR = 10 MHz, duty cycle 50%.

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Waveforms – 4



V_{CC} (V)	INPUTS		Vref	V_{TT}	C_L	R_L	ΔV
	V_{IH}	t_r/t_f					
V_{CC} = 1.8±0.15 V	V_{CC}	≤ 2 ns	1/2 V_{CC}	2× V_{CC}	30 pF	1.0 kΩ	0.15 V
V_{CC} = 2.5±0.2 V	V_{CC}	≤ 2 ns	1/2 V_{CC}	2× V_{CC}	30 pF	500 Ω	0.15 V
V_{CC} = 2.7 V	2.7 V	≤ 2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
V_{CC} = 3.3±0.3 V	2.7 V	≤ 2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
V_{CC} = 5.0±0.5 V	V_{CC}	≤ 2.5 ns	1/2 V_{CC}	2× V_{CC}	50 pF	500 Ω	0.3 V

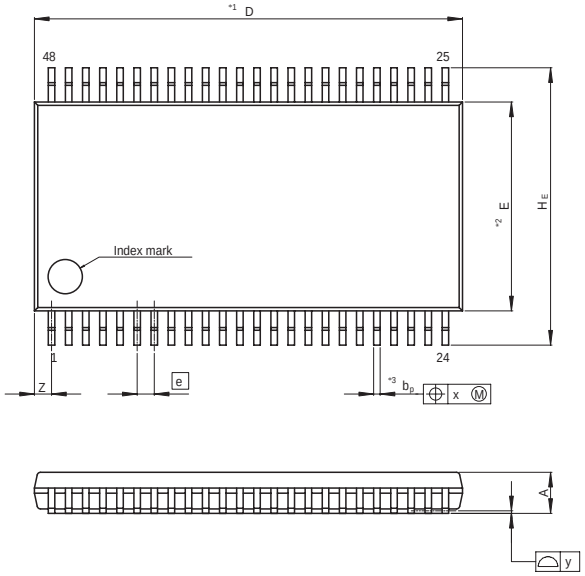
Notes:
1. Input waveform :PRR = 10 MHz, duty cycle 50%
2. Waveform – A shows input conditions such that the output is "L" level when enable by the output control.
3. Waveform – B shows input conditions such that the output is "H" level when enable by the output control.

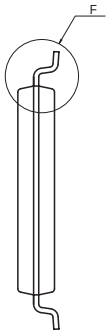
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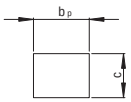
Package Dimensions

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-TSSOP48-6.1x12.5-0.50	PTSP0048KA-A	TTP-48DBV	0.2g

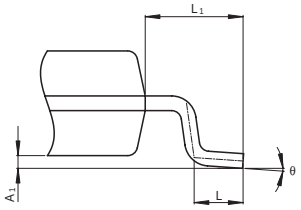
NOTE)
1. DIMENSIONS"*1 (Nom)"AND"*2"
   DO NOT INCLUDE MOLD FLASH
2. DIMENSION"*3"DOES NOT
   INCLUDE TRIM OFFSET.







Terminal cross section
(Ni/Pd/Au plating)



Detail F

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	——	12.5	12.7
E	——	6.10	——
A 2	——	——	——
A 1	0.08	0.13	0.18
A	——	——	1.20
b p	0.14	0.19	0.24
b 1	——	——	——
c	0.10	0.15	0.20
c 1	——	——	——
θ	0°	——	8°
H E	7.90	8.10	8.30
e	——	0.50	——
x	——	——	0.08
y	——	——	0.10
Z	——	——	0.65
L	0.4	0.5	0.6
L 1	——	1.0	——

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