

PerFET™ Power Transistor

FEATURES

- Ultra-low On-resistance
- Wettable Flank leads for Enhanced AOI
- 100% UIS and Rg tested
- 175°C Operating Junction Temperature
- RoHS Compliant
- Halogen-Free according to IEC 61249-2-21

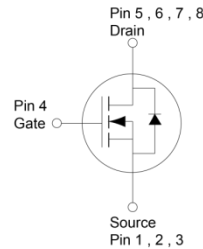
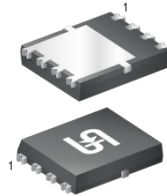
APPLICATIONS

- DC-DC Converters
- Solenoid and Motor Drivers
- Load Switch

PRODUCT SUMMARY			
PARAMETER		VALUE	UNIT
V_{DS}		40	V
$R_{DS(on)}$ (max)	$V_{GS} = 10V$	3.2	mΩ
	$V_{GS} = 7V$	3.8	
Q_g	$V_{GS} = 10V$	45	nC



PDFN56U



Note: MSL 1 (Moisture Sensitivity Level) per J-STD-020

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)				
PARAMETER		SYMBOL	LIMIT	UNIT
Drain-Source Voltage		V_{DS}	40	V
Gate-Source Voltage		V_{GS}	± 20	V
Continuous Drain Current, Silicon limited	$T_C = 25^\circ\text{C}$	I_D	144	A
Continuous Drain Current ^(Note 1)	$T_C = 25^\circ\text{C}$	I_D	81	A
	$T_C = 100^\circ\text{C}$		81	
	$T_A = 25^\circ\text{C}$		23	
Pulsed Drain Current		I_{DM}	324	A
Single Pulse Avalanche Current ^(Note 2)		I_{AS}	32.4	A
Single Pulse Avalanche Energy ^(Note 2)		E_{AS}	157	mJ
Total Power Dissipation	$T_C = 25^\circ\text{C}$	P_D	115	W
	$T_C = 125^\circ\text{C}$		38	
Operating Junction and Storage Temperature Range		T_J, T_{STG}	-55 to +175	$^\circ\text{C}$

THERMAL RESISTANCE			
PARAMETER	SYMBOL	MAXIMUM	UNIT
Thermal Resistance – Junction to Case	$R_{\theta JC}$	1.3	$^\circ\text{C/W}$
Thermal Resistance – Junction to Ambient	$R_{\theta JA}$	50	$^\circ\text{C/W}$

Note: $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistances. The case-thermal reference is defined at the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNIT
Static						
Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = 1mA$	BV_{DSS}	40	--	--	V
Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\mu A$	$V_{GS(TH)}$	2.4	3	3.6	V
Gate-Source Leakage Current	$V_{GS} = \pm 20V, V_{DS} = 0V$	I_{GSS}	--	--	± 100	nA
Drain-Source Leakage Current	$V_{GS} = 0V, V_{DS} = 40V$	I_{DSS}	--	--	1	μA
	$V_{GS} = 0V, V_{DS} = 40V$ $T_J = 125^{\circ}C$		--	--	100	
	Drain-Source On-State Resistance (Note 3)		$V_{GS} = 10V, I_D = 40A$	$R_{DS(on)}$	--	
	$V_{GS} = 7V, I_D = 40A$	--	3.2		3.8	
Forward Transconductance (Note 3)	$V_{DS} = 10V, I_D = 10A$	g_{fs}	--	73	--	S
Dynamic						
Total Gate Charge	$V_{GS} = 7V, V_{DS} = 20V,$ $I_D = 23A$	Q_g	--	32.4	--	nC
Total Gate Charge	$V_{GS} = 10V, V_{DS} = 20V,$ $I_D = 23A$	Q_g	--	45	--	
Gate-Source Charge		Q_{gs}	--	14	--	
Gate-Drain Charge		Q_{gd}	--	9.5	--	
Input Capacitance	$V_{GS} = 0V, V_{DS} = 25V,$ $f = 1.0MHz$	C_{iss}	--	2896	--	pF
Output Capacitance		C_{oss}	--	562	--	
Reverse Transfer Capacitance		C_{rss}	--	32	--	
Gate Resistance	$f = 1.0MHz$	R_g	--	0.7	--	Ω
Switching (Note 4)						
Turn-On Delay Time	$V_{GS} = 10V, V_{DS} = 20V,$ $I_D = 23A, R_G = 3.3\Omega$	$t_{d(on)}$	--	15.7	--	nS
Rise Time		t_r	--	71	--	
Turn-Off Delay Time		$t_{d(off)}$	--	28.6	--	
Fall Time		t_f	--	13	--	
Source-Drain Diode						
Diode Forward Voltage (Note 3)	$V_{GS} = 0V, I_S = 40A$	V_{SD}	--	--	1.1	V
Reverse Recovery Time	$I_S = 23A,$	t_{rr}	--	42	--	nS
Reverse Recovery Charge	$di/dt = 100A/\mu s$	Q_{rr}	--	43	--	nC

Notes:

- Package current limit.
- $L = 0.3mH, V_{GS} = 10V, R_G = 25\Omega$, Starting $T_J = 25^\circ\text{C}$.
- Pulse test: Pulse Width $\leq 300\mu s$, duty cycle $\leq 2\%$.
- Switching time is essentially independent of operating temperature.

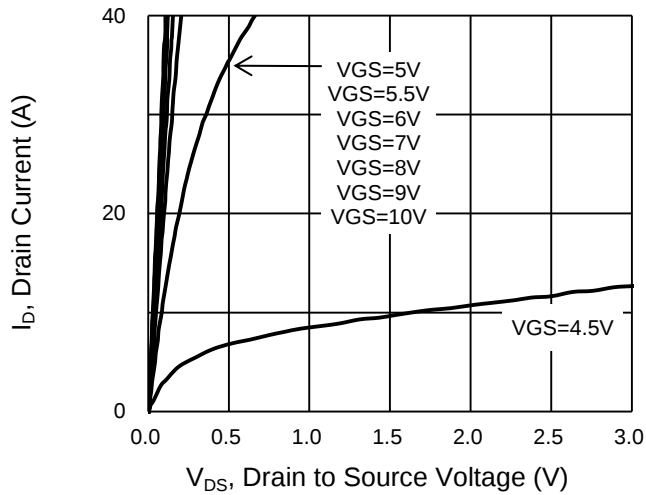
ORDERING INFORMATION

ORDERING CODE	PACKAGE	PACKING
TSM032NH04CR RLG	PDFN56U	2,500pcs / 13" Reel

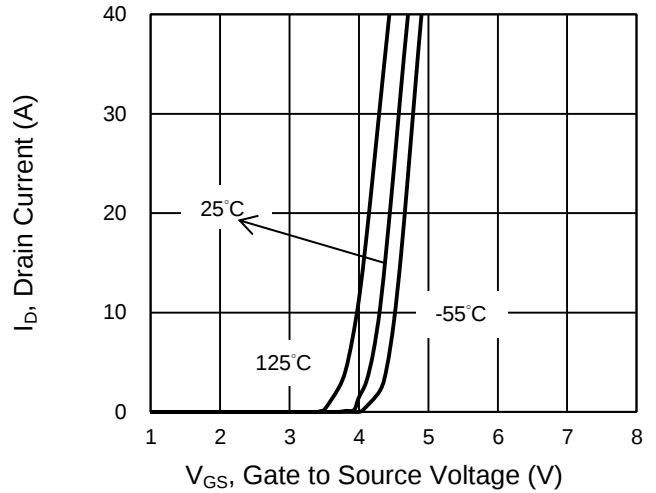
CHARACTERISTICS CURVES

($T_A = 25^\circ\text{C}$ unless otherwise noted)

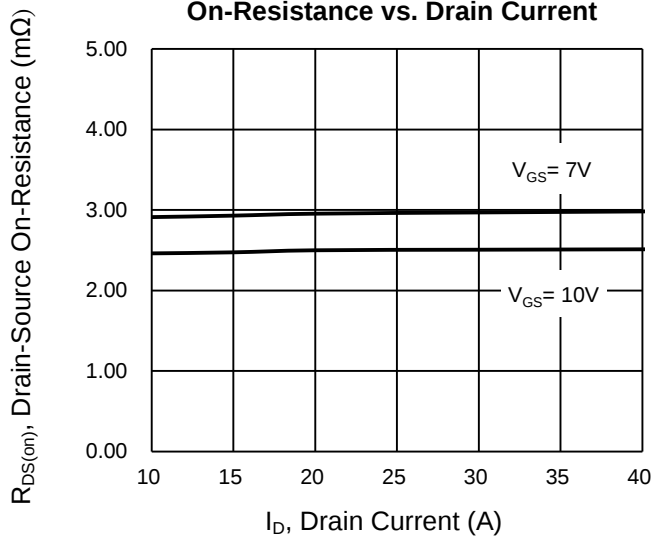
Output Characteristics



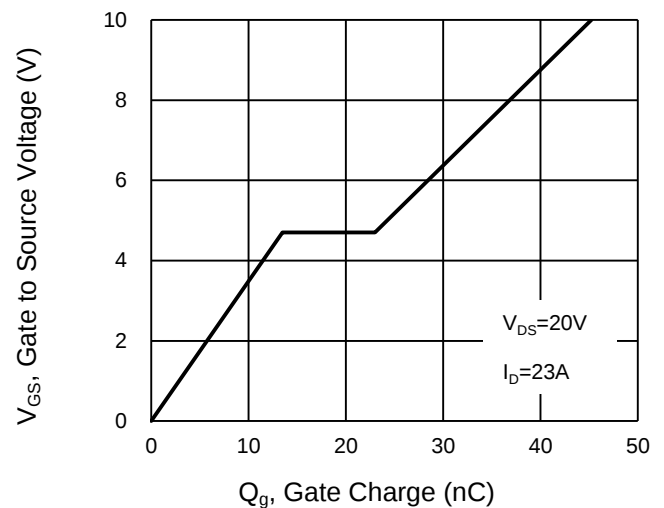
Transfer Characteristics



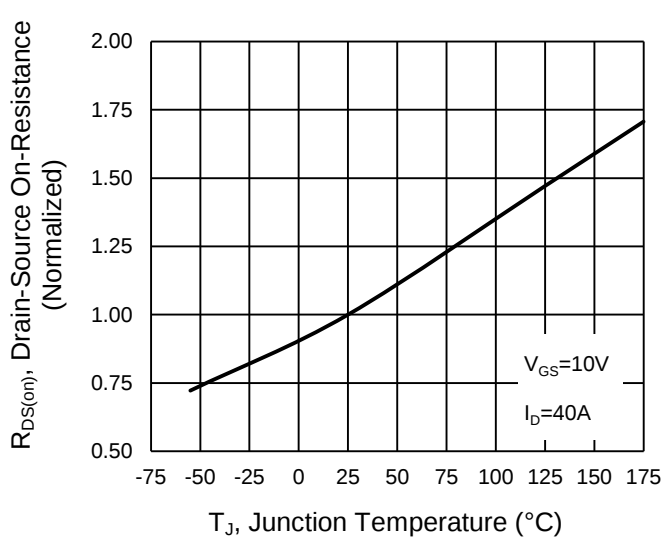
On-Resistance vs. Drain Current



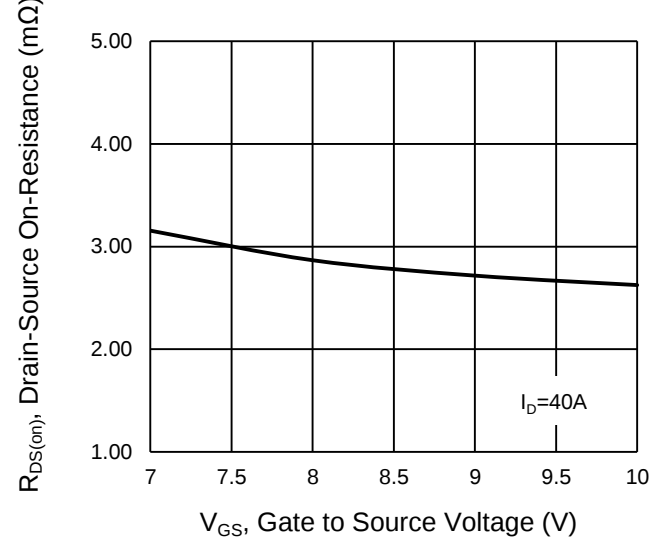
Gate-Source Voltage vs. Gate Charge



On-Resistance vs. Junction Temperature



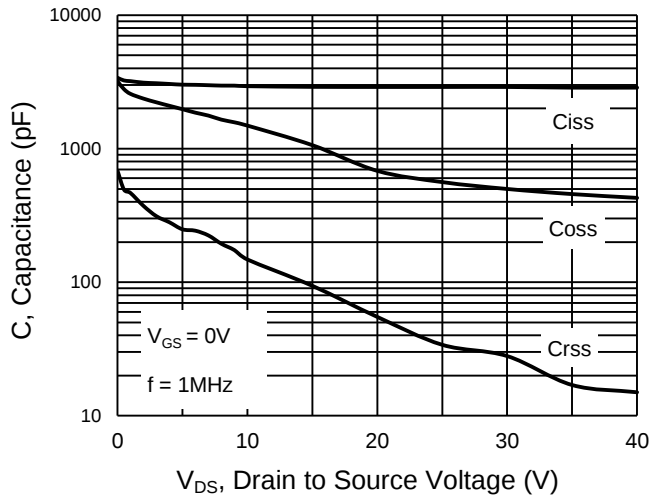
On-Resistance vs. Gate-Source Voltage



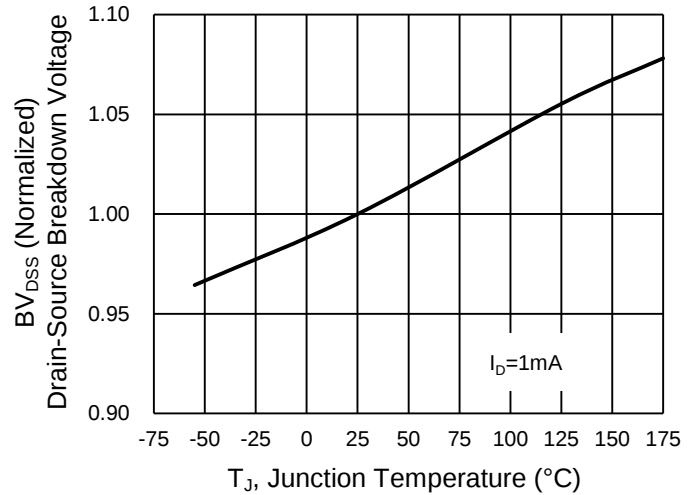
CHARACTERISTICS CURVES

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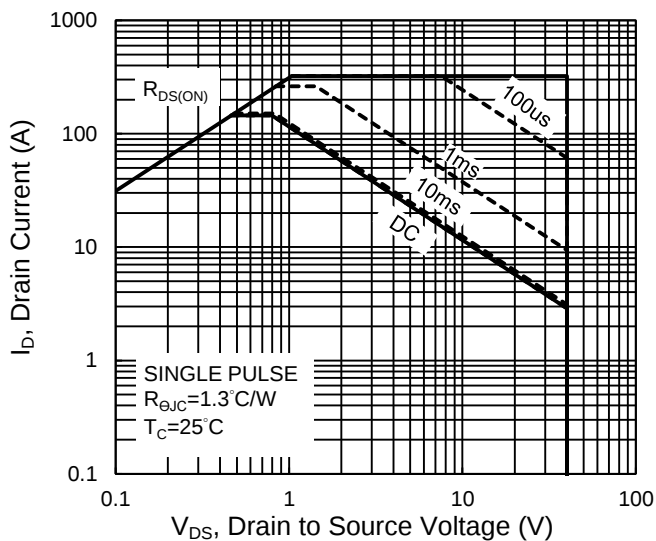
Capacitance vs. Drain-Source Voltage



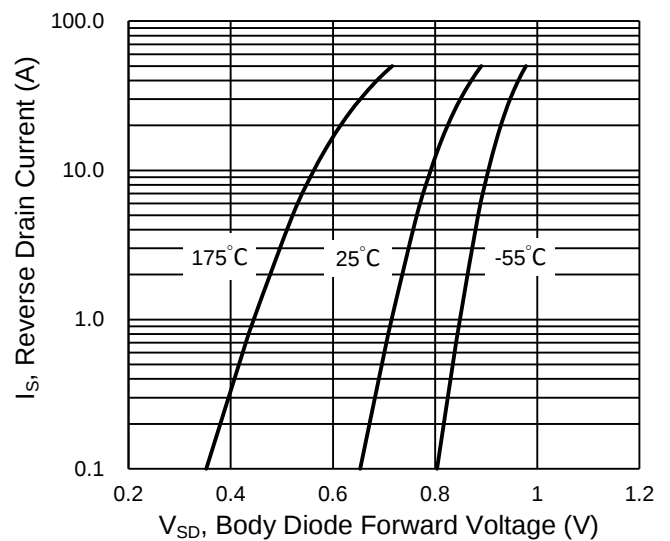
BV_{DSS} vs. Junction Temperature



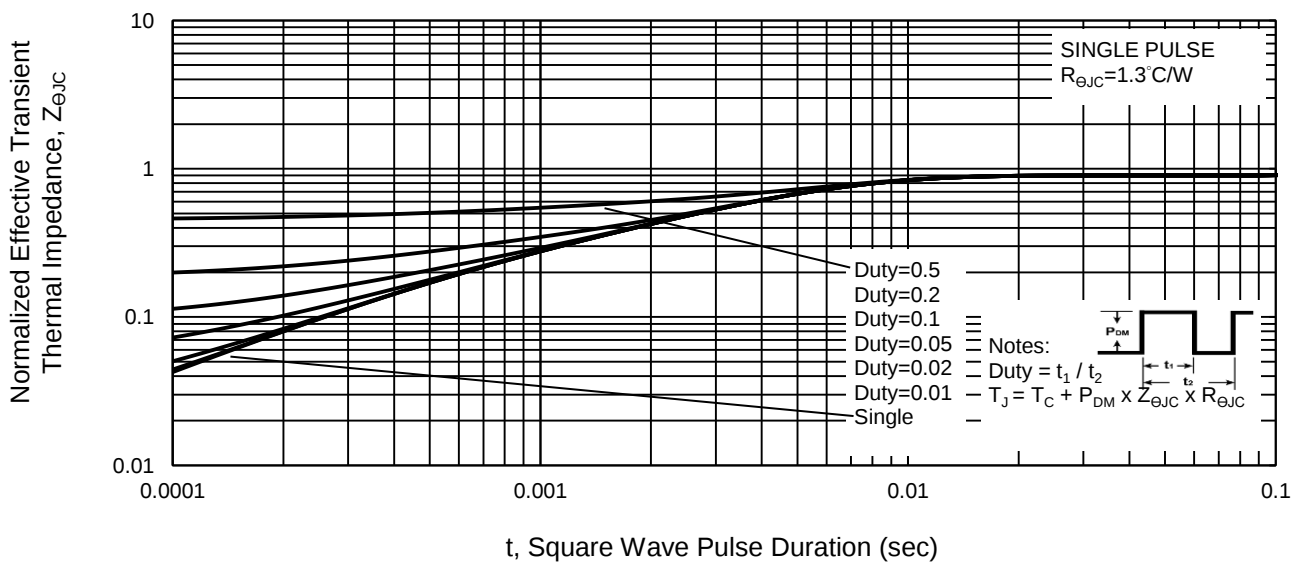
Maximum Safe Operating Area, Junction-to-Case



Source-Drain Diode Forward Current vs. Voltage

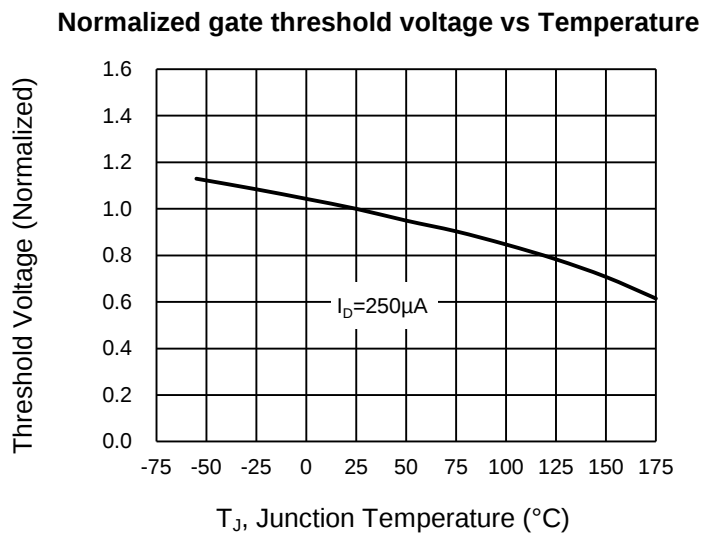
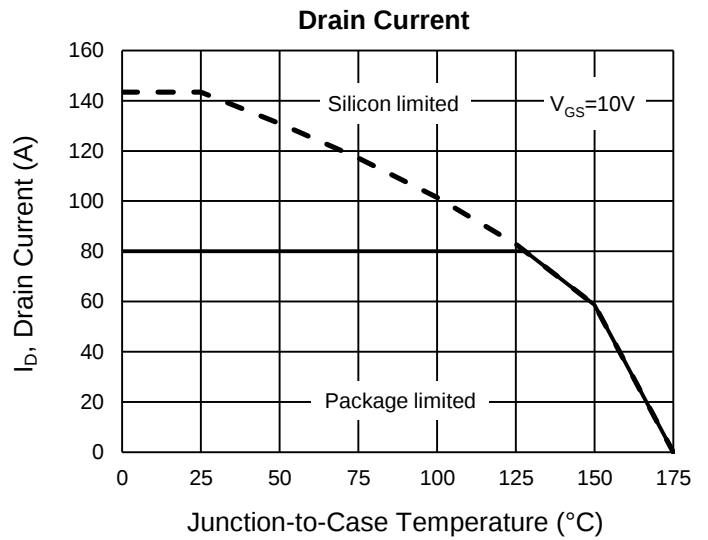
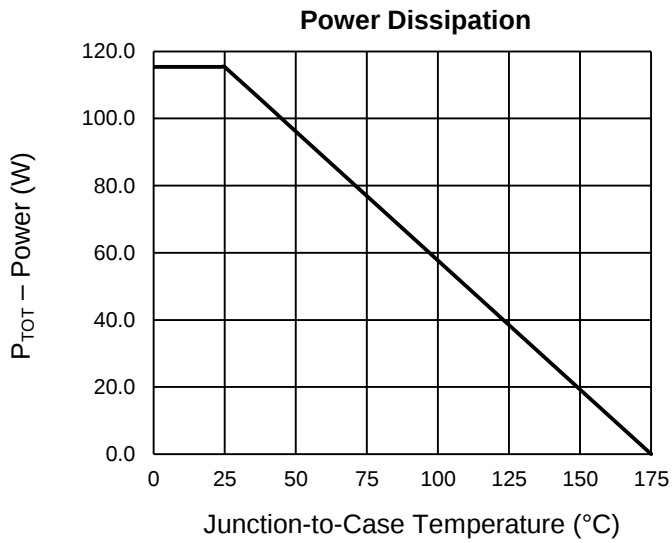


Normalized Thermal Transient Impedance, Junction-to-Case



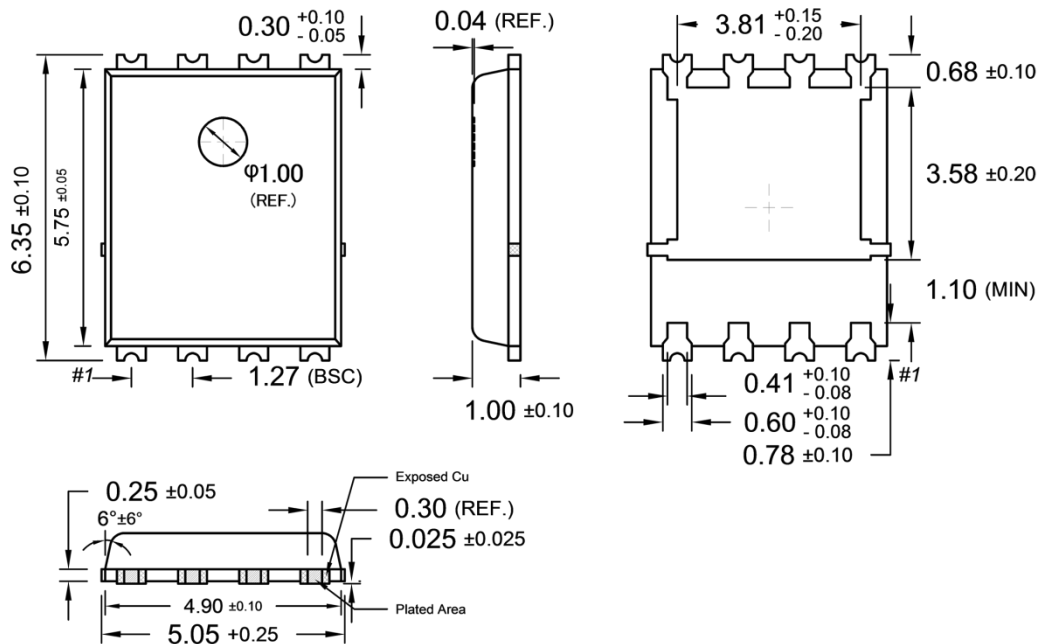
CHARACTERISTICS CURVES

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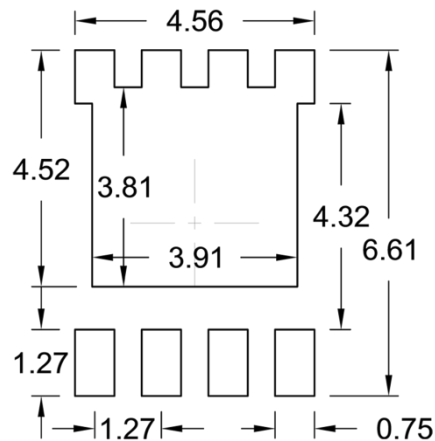


PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)

PDFN56U



SUGGESTED PAD LAYOUT (Unit: Millimeters)



MARKING DIAGRAM



- Y** = Year Code
- WW** = Week Code (01~52)
- L** = Lot Code (1~9, A~Z)
- F** = Factory Code

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