

## 3.3V CMOS 16-BIT TRANSPARENT D-TYPE LATCH WITH 3-STATE OUTPUTS, 5 VOLT TOLERANT I/O AND BUS-HOLD

**IDT74LVCH16373A**  
**OBSOLETE PART**

### FEATURES:

- Typical  $t_{sk(o)}$  (Output Skew) < 250ps
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- $V_{CC} = 3.3V \pm 0.3V$ , Normal Range
- $V_{CC} = 2.7V$  to  $3.6V$ , Extended Range
- CMOS power levels (0.4μW typ. static)
- All inputs, outputs, and I/O are 5V tolerant
- Supports hot insertion
- Available in TSSOP package

### DRIVE FEATURES:

- High Output Drivers:  $\pm 24mA$
- Reduced system switching noise

### APPLICATIONS:

- 5V and 3.3V mixed voltage systems
- Data communication and telecommunication systems

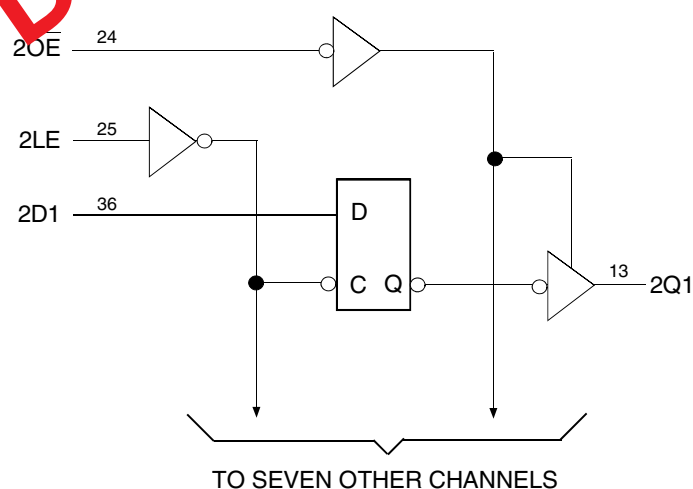
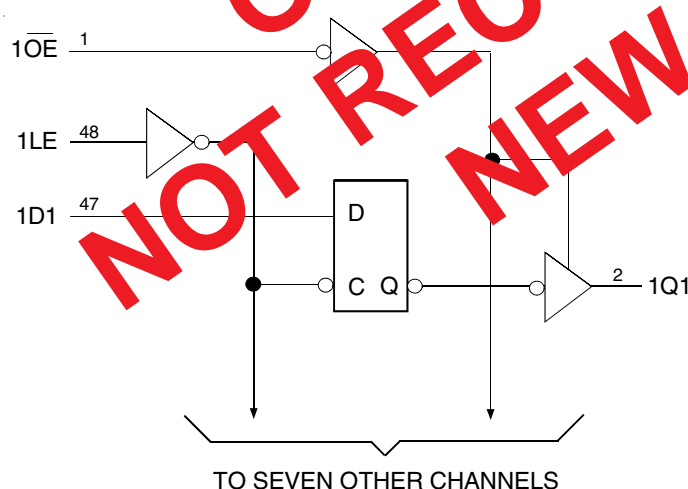
### DESCRIPTION

The LVCH16373A 16-bit transparent D-type latch is built using advanced dual metal CMOS technology. This high-speed, low-power latch is ideal for temporary storage of data. The LVCH16373A can be used for implementing memory address latches, I/O ports, and bus drivers. The Output Enable and Latch Enable controls are organized to operate each device as two 8-bit latches or one 16-bit latch. Flow-through organization of signal pins simplifies layout. All inputs are designed with hysteresis for improved noise margin.

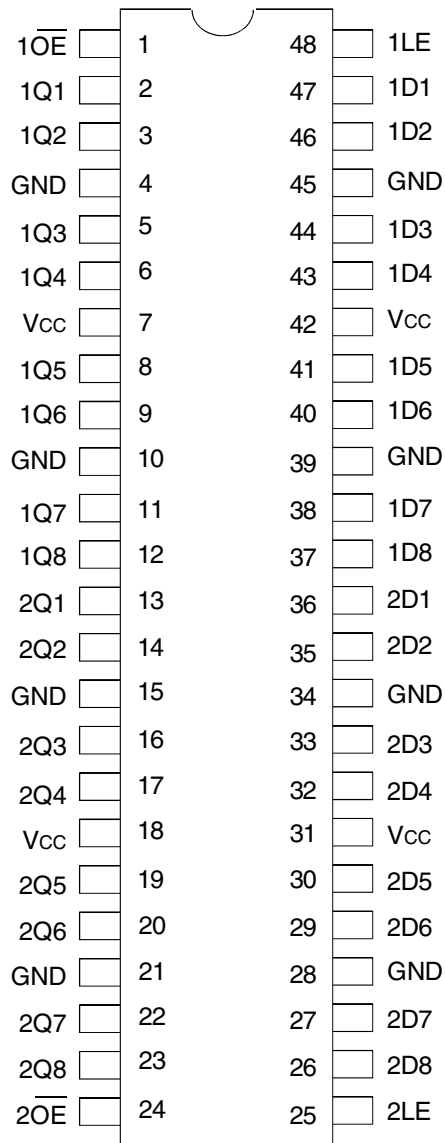
All pins of the LVCH16373A can be driven from either 3.3V or 5V devices. This feature allows the use of the device as a translator in a mixed 3.3V/5V supply system.

The LVCH16373A has "bus hold" which retains the inputs' last state whenever the input goes to a high impedance. This prevents floating inputs and eliminates the need for pull-up/down resistors.

### FUNCTIONAL BLOCK DIAGRAM



## PIN CONFIGURATION



TSSOP  
TOP VIEW

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

Symbol	Description	Max	Unit
V <sub>TERM</sub>	Terminal Voltage with Respect to GND	-0.5 to +6.5	V
T <sub>STG</sub>	Storage Temperature	-65 to +150	°C
I <sub>OUT</sub>	DC Output Current	-50 to +50	mA
I <sub>IK</sub> I <sub>OK</sub>	Continuous Clamp Current, V <sub>I</sub> < 0 or V <sub>O</sub> < 0	-50	mA
I <sub>CC</sub> I <sub>SS</sub>	Continuous Current through each V <sub>CC</sub> or GND	±100	mA

### NOTE:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## CAPACITANCE (T<sub>A</sub> = +25°C, F = 1.0MHz)

Symbol	Parameter <sup>(1)</sup>	Conditions	Typ.	Max.	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 0V	4.5	6	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> = 0V	6.5	8	pF
C <sub>I/O</sub>	I/O Port Capacitance	V <sub>IN</sub> = 0V	6.5	8	pF

### NOTE:

- As applicable to the device type.

## PIN DESCRIPTION

Pin Names	Description
x Dx	Data Inputs <sup>(1)</sup>
x LE	Latch Enable Input
x OE	Output Enable Inputs (Active LOW)
x Qx	3-State Outputs

### NOTE:

- These pins have "Bus-Hold". All other pins are standard inputs, outputs, or I/Os.

## FUNCTION TABLE<sup>(1)</sup>

Inputs			Outputs
x Dx	x LE	x OE	x Qx
H	H	L	H
L	H	L	L
X	L	L	Q <sup>(2)</sup>
X	X	H	Z

### NOTES:

- H = HIGH Voltage Level  
X = Don't Care  
L = LOW Voltage Level  
Z = High-Impedance
- Output level before the indicated steady-state input conditions were established.

## DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Operating Condition:  $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$

Symbol	Parameter	Test Conditions		Min.	Typ. <sup>(1)</sup>	Max.	Unit
$V_{IH}$	Input HIGH Voltage Level	$V_{CC} = 2.3\text{V}$ to $2.7\text{V}$		1.7	—	—	V
		$V_{CC} = 2.7\text{V}$ to $3.6\text{V}$		2	—	—	
$V_{IL}$	Input LOW Voltage Level	$V_{CC} = 2.3\text{V}$ to $2.7\text{V}$		—	—	0.7	V
		$V_{CC} = 2.7\text{V}$ to $3.6\text{V}$		—	—	0.8	
$I_{IH}$ $I_{IL}$	Input Leakage Current	$V_{CC} = 3.6\text{V}$	$V_I = 0$ to $5.5\text{V}$	—	—	$\pm 5$	$\mu\text{A}$
$I_{OZH}$ $I_{OZL}$	High Impedance Output Current (3-State Output pins)	$V_{CC} = 3.6\text{V}$	$V_O = 0$ to $5.5\text{V}$	—	—	$\pm 10$	$\mu\text{A}$
$I_{OFF}$	Input/Output Power Off Leakage	$V_{CC} = 0\text{V}$ , $V_{IN}$ or $V_O \leq 5.5\text{V}$		—	—	$\pm 50$	$\mu\text{A}$
$V_{IK}$	Clamp Diode Voltage	$V_{CC} = 2.3\text{V}$ , $I_{IN} = -18\text{mA}$		—	-0.7	-1.2	V
$V_H$	Input Hysteresis	$V_{CC} = 3.3\text{V}$		—	100	—	mV
$I_{CCL}$ $I_{CCH}$ $I_{CCZ}$	Quiescent Power Supply Current	$V_{CC} = 3.6\text{V}$	$V_{IN} = \text{GND}$ or $V_{CC}$	—	—	10	$\mu\text{A}$
			$3.6 \leq V_{IN} \leq 5.5\text{V}^{(2)}$	—	—	10	
$\Delta I_{CC}$	Quiescent Power Supply Current Variation	One input at $V_{CC} - 0.6\text{V}$ , other inputs at $V_{CC}$ or GND		—	—	500	$\mu\text{A}$

### NOTES:

- Typical values are at  $V_{CC} = 3.3\text{V}$ ,  $+25^{\circ}\text{C}$  ambient.
- This applies in the disabled state only.

## BUS-HOLD CHARACTERISTICS

Symbol	Parameter <sup>(1)</sup>	Test Conditions		Min.	Typ. <sup>(2)</sup>	Max.	Unit
$I_{BHH}$ $I_{BHL}$	Bus-Hold Input Sustain Current	$V_{CC} = 3\text{V}$	$V_I = 2\text{V}$	-75	—	—	$\mu\text{A}$
			$V_I = 0.8\text{V}$	75	—	—	
$I_{BHH}$ $I_{BHL}$	Bus-Hold Input Sustain Current	$V_{CC} = 2.3\text{V}$	$V_I = 1.7\text{V}$	—	—	—	$\mu\text{A}$
			$V_I = 0.7\text{V}$	—	—	—	
$I_{BHHO}$ $I_{BHLO}$	Bus-Hold Input Overdrive Current	$V_{CC} = 3.6\text{V}$	$V_I = 0$ to $3.6\text{V}$	—	—	$\pm 500$	$\mu\text{A}$

### NOTES:

- Pins with Bus-Hold are identified in the pin description.
- Typical values are at  $V_{CC} = 3.3\text{V}$ ,  $+25^{\circ}\text{C}$  ambient.

## OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions <sup>(1)</sup>		Min.	Max.	Unit
VOH	Output HIGH Voltage	VCC = 2.3V to 3.6V	IOH = - 0.1mA	VCC - 0.2	—	V
		VCC = 2.3V	IOH = - 6mA	2	—	
		VCC = 2.3V	IOH = - 12mA	1.7	—	
		VCC = 2.7V		2.2	—	
		VCC = 3V		2.4	—	
		VCC = 3V	IOH = - 24mA	2.2	—	
VOL	Output LOW Voltage	VCC = 2.3V to 3.6V	IOL = 0.1mA	—	0.2	V
		VCC = 2.3V	IOL = 6mA	—	0.4	
			IOL = 12mA	—	0.7	
		VCC = 2.7V	IOL = 12mA	—	0.4	
		VCC = 3V	IOL = 24mA	—	0.55	

**NOTE:**  
1. VIH and VIL must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate VCC range.  
TA = - 40°C to + 85°C.

## OPERATING CHARACTERISTICS, VCC = 3.3V ± 0.3V, TA = 25°C

Symbol	Parameter	Test Conditions	Typical	Unit
CPD	Power Dissipation Capacitance per Latch Outputs enabled	CL = 0pF, f = 10Mhz	39	pF
CPD	Power Dissipation Capacitance per Latch Outputs disabled		6	

## SWITCHING CHARACTERISTICS<sup>(1)</sup>

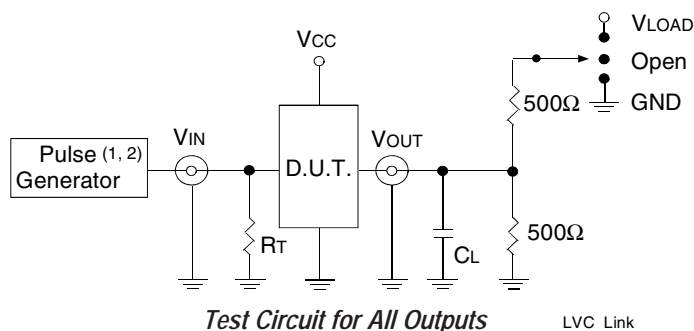
Symbol	Parameter	VCC = 2.7V		VCC = 3.3V ± 0.3V		Unit
		Min.	Max.	Min.	Max.	
tPLH tPHL	Propagation Delay xDx to xQx	—	4.9	1.6	4.2	ns
tPLH tPHL	Propagation Delay xLE to xQx	—	5.3	2.1	4.6	ns
tPZH tPZL	Output Enable Time xOE to xQx	—	5.7	1.3	4.7	ns
tPHZ tPLZ	Output Disable Time xOE to xQx	—	6.3	2.5	5.9	ns
tsu	Set-up Time, data before LE↓ HIGH or LOW	1.7	—	1.7	—	ns
tH	Hold Time, data after LE↓ HIGH or LOW	1.2	—	1.2	—	ns
tW	Pulse Width xLE HIGH	3.3	—	3.3	—	ns
tsk(o)	Output Skew <sup>(2)</sup>	—	—	—	500	ps

**NOTES:**  
1. See TEST CIRCUITS AND WAVEFORMS. TA = - 40°C to + 85°C.  
2. Skew between any two outputs of the same package and switching in the same direction.

# TEST CIRCUITS AND WAVEFORMS

## TEST CONDITIONS

Symbol	V <sub>CC</sub> <sup>(1)</sup> = 3.3V ± 0.3V	V <sub>CC</sub> <sup>(1)</sup> = 2.7V	V <sub>CC</sub> <sup>(2)</sup> = 2.5V ± 0.2V	Unit
V <sub>LOAD</sub>	6	6	2 x V <sub>CC</sub>	V
V <sub>IH</sub>	2.7	2.7	V <sub>CC</sub>	V
V <sub>T</sub>	1.5	1.5	V <sub>CC</sub> / 2	V
V <sub>LZ</sub>	300	300	150	mV
V <sub>HZ</sub>	300	300	150	mV
C <sub>L</sub>	50	50	30	pF



### DEFINITIONS:

C<sub>L</sub> = Load capacitance: includes jig and probe capacitance.

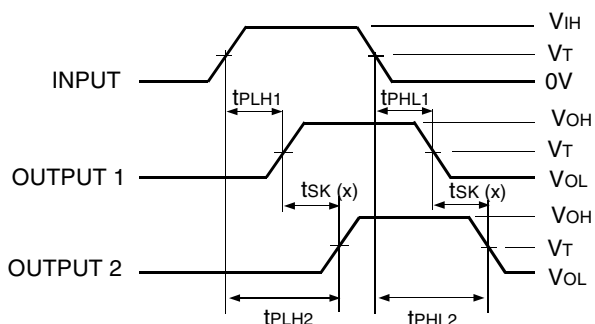
R<sub>T</sub> = Termination resistance: should be equal to Z<sub>OUT</sub> of the Pulse Generator.

### NOTES:

1. Pulse Generator for All Pulses: Rate ≤ 10MHz; t<sub>r</sub> ≤ 2.5ns; t<sub>r</sub> ≤ 2.5ns.
2. Pulse Generator for All Pulses: Rate ≤ 10MHz; t<sub>r</sub> ≤ 2ns; t<sub>r</sub> ≤ 2ns.

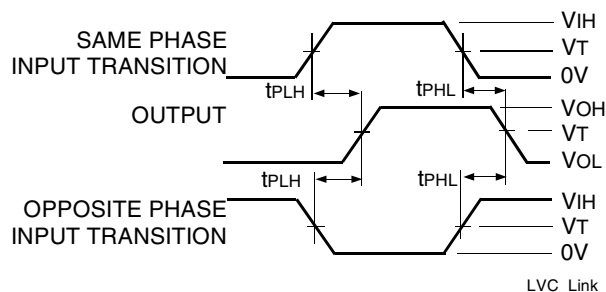
## SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	V <sub>LOAD</sub>
Disable High Enable High	GND
All Other Tests	Open

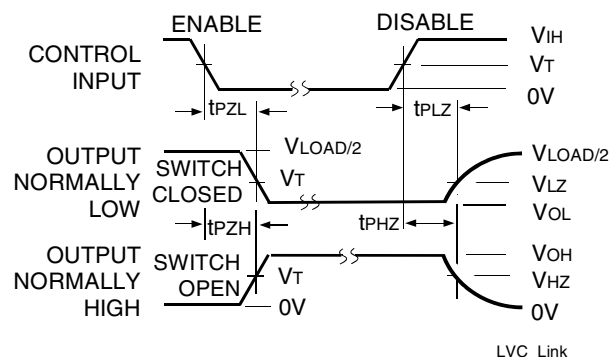


### NOTES:

1. For tsk(o) OUTPUT1 and OUTPUT2 are any two outputs.
2. For tsk(b) OUTPUT1 and OUTPUT2 are in the same bank.



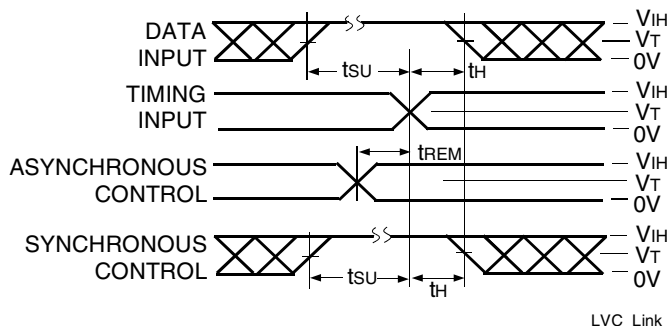
### Propagation Delay



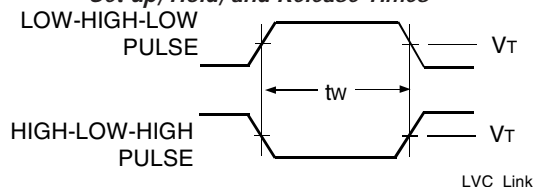
### Enable and Disable Times

#### NOTE:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.



### Set-up, Hold, and Release Times



### Pulse Width

## ORDERING INFORMATION

IDT	XX	LVC	X	XX	XXXX	XX	
	Temp. Range		Bus-Hold	Family	Device Type	Package	
						PA	Thin Shrink Small Outline Package
						PAG	TSSOP - Green
					373A		16-Bit Transparent D-Type Latch with 3- State Outputs
				16			Double-Density, $\pm 24\text{mA}$
			H				Bus-hold
						74	$-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$

## DATASHEET DOCUMENT HISTORY

07/13/2015	PDN# CQ-14-05 issued. See IDT.com for PDN specifics.
09/06/2019	Datasheet changed to Obsolete Status.

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