

3-STATE Octal D-Type Latch

MM74HC573

General Description

The MM74HC573 high speed octal D-type latches utilize advanced silicon-gate P-well CMOS technology. They possess the high noise immunity and low power consumption of standard CMOS integrated circuits, as well as the ability to drive 15 LS-TTL loads. Due to the large output drive capability and the 3-STATE feature, these devices are ideally suited for interfacing with bus lines in a bus organized system.

When the LATCH ENABLE (LE) input is HIGH, the Q outputs will follow the D inputs. When the LATCH ENABLE goes LOW, data at the D inputs will be retained at the outputs until LATCH ENABLE returns HIGH again. When a high logic level is applied to the OUTPUT CONTROL OC input, all outputs go to a high impedance state, regardless of what signals are present at the other inputs and the state of the storage elements.

The 74HC logic family is speed, function, and pinout compatible with the standard 74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical Propagation Delay: 16 ns
- Wide Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μ A Maximum
- Low Quiescent Current: 160 μ A Maximum (74HC Series)
- Compatible with Bus-oriented Systems
- Output Drive Capability: 15 LS-TTL Loads
- This is a Pb-Free Device

TRUTH TABLE

Output Control	Latch Enable	Data	Output
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

NOTES: H = HIGH Level

L = LOW Level

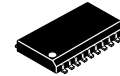
Q_0 = Level of output before steady-state input conditions were established.

Z = High Impedance

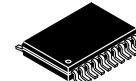
X = Don't Care



SOIC-20 WB
CASE 751D-05

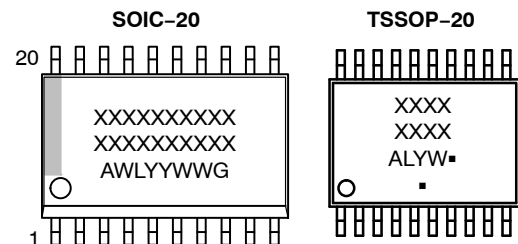


SOIC-20, 300 mils
CASE 751BJ



TSSOP-20 WB
CASE 948E

MARKING DIAGRAMS



XXXXX = Specific Device Code

A = Assembly Location

WL, L = Wafer Lot

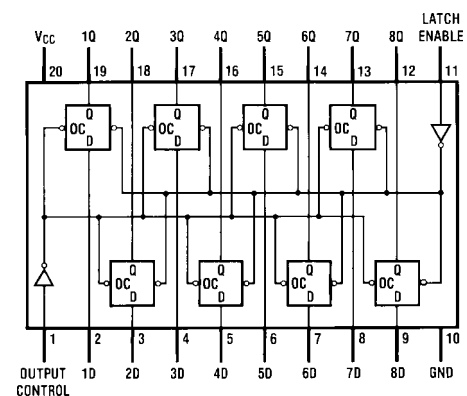
YY, Y = Year

WW, W = Work Week

G, ■ = Pb-Free Package

(Note: Microdot may be in either location)

CONNECTION DIAGRAM



(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information on page 5 of this data sheet.

MM74HC573

ABSOLUTE MAXIMUM RATINGS (Note 1)

Symbol	Rating	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +6.5	V
V_{IN}	DC Input Voltage	-0.5 to $V_{CC} + 0.5$	V
V_{OUT}	DC Output Voltage	-0.5 to $V_{CC} + 0.5$	V
I_{IK}, I_{OK}	Clamp Diode Current	± 20	mA
I_{OUT}	DC Output Current, per pin	± 35	mA
I_{CC}	DC V_{CC} or GND Current, per pin	± 70	mA
T_{STG}	Storage Temperature Range	-65 to +150	°C
P_D	Power Dissipation	SOIC TSSOP 1302 833	mW
T_L	Lead Temperature (Soldering 10 seconds)	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Unless otherwise specified all voltages are referenced to ground.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage	2	6	V
V_{IN}, V_{OUT}	DC Input or Output Voltage	0	V_{CC}	V
T_A	Operating Temperature Range	-55	+125	°C
t_r, t_f	Input Rise or Fall Times	$V_{CC} = 2.0\text{ V}$	1000	ns
		$V_{CC} = 4.5\text{ V}$	500	ns
		$V_{CC} = 6.0\text{ V}$	400	ns

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

MM74HC573

DC ELECTRICAL CHARACTERISTICS (Note 2)

Symbol	Parameter	Conditions	V _{CC}	T _A = 25°C		T _A = -40 to 85°C	T _A = -55 to 125°C	Unit
				Typ	Guaranteed Limits			
V _{IH}	Minimum HIGH Level Input Voltage		2.0 V		1.5	1.5	1.5	V
			4.5 V		3.15	3.15	3.15	V
			6.0 V		4.2	4.2	4.2	V
V _{IL}	Maximum LOW Level Input Voltage		2.0 V		0.5	0.5	0.5	V
			4.5 V		1.35	1.35	1.35	V
			6.0 V		1.8	1.8	1.8	V
V _{OH}	Minimum HIGH Level Output Voltage	V _{IN} = V _{IH} or V _{IL}	2.0 V	2.0	1.9	1.9	1.9	V
		I _{OUT} ≤ 20 μA	4.5 V	4.5	4.4	4.4	4.4	V
			6.0 V	6.0	5.9	5.9	5.9	V
		V _{IN} = V _{IH} or V _{IL}	4.5 V	4.2	3.98	3.84	3.7	V
		I _{OUT} ≤ 6.0 mA	6.0 V	5.7	5.48	5.34	5.2	V
		I _{OUT} ≤ 7.8 mA						
V _{OL}	Maximum LOW Level Output Voltage	V _{IN} = V _{IH} or V _{IL}	2.0 V	0	0.1	0.1	0.1	V
		I _{OUT} ≤ 20 μA	4.5 V	0	0.1	0.1	0.1	V
			6.0 V	0	0.1	0.1	0.1	V
		V _{IN} = V _{IH} or V _{IL}	4.5 V	0.2	0.26	0.33	0.4	V
		I _{OUT} ≤ 6.0 mA	6.0 V	0.2	0.26	0.33	0.4	V
		I _{OUT} ≤ 7.8 mA						
I _{IN}	Maximum Input Current	V _{IN} = V _{CC} or GND	6.0 V		±0.1	±1.0	±1.0	μA
I _{OZ}	Maximum 3-STATE Output Leakage Current	V _{OUT} = V _{CC} or GND OC = V _{IH}	6.0 V		±0.5	±5.0	±10	μA
I _{CC}	Maximum Quiescent Supply Current	V _{IN} = V _{CC} or GND I _{OUT} = 0 μA	6.0 V		8.0	80	160	μA
ΔI _{CC}	Quiescent Supply Current per Input Pin	V _{CC} = 5.5 V V _{IN} = 2.4 V or 0.4 V (Note 2)	OE	1.0	1.5	1.8	2.0	mA
			LE	0.6	0.8	1.0	1.1	mA
			DATA	0.4	0.5	0.6	0.7	mA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. For a power supply of 5 V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5 V. Thus the 4.5 V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5 V and 4.5 V respectively. (The V_{IH} value at 5.5 V is 3.85 V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0 V values should be used.

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5 V, T_A = 25°C, t_r = t_f = 6 ns)

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Unit
t _{PHL} , t _{PLH}	Maximum Propagation Delay, Data to Q	C _L = 45 pF	16	20	ns
t _{PHL} , t _{PLH}	Maximum Propagation Delay, LE to Q	C _L = 45 pF	14	22	ns
t _{PZH} , t _{PZL}	Maximum Output Enable Time	R _L = 1 kΩ, C _L = 45 pF	15	27	ns
t _{PHZ} , t _{PLZ}	Maximum Output Disable Time	R _L = 1 kΩ, C _L = 5 pF	13	23	ns
t _s	Minimum Set Up Time, Data to LE		10	15	ns
t _H	Minimum Hold Time, LE to Data		2	5	ns
t _W	Minimum Pulse Width, LE or Data		10	16	ns

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

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AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	V _{CC}	T _A = 25°C		T _A = -40 to 85°C	T _A = -55 to 125°C	Unit
				Typ	Guaranteed Limits			
t _{PHL} , t _{PLH}	Maximum Propagation Delay, Data to Q	C _L = 50 pF	2.0 V	45	110	138	165	ns
		C _L = 150 pF	2.0 V	55	150	188	225	ns
		C _L = 50 pF	4.5 V	17	22	28	33	ns
		C _L = 150 pF	4.5 V	21	30	38	40	ns
t _{PHL} , t _{PLH}	Maximum Propagation Delay, LE to Q	C _L = 50 pF	6.0 V	15	19	24	29	ns
		C _L = 150 pF	6.0 V	19	26	33	39	ns
		C _L = 50 pF	2.0 V	46	115	138	165	ns
		C _L = 150 pF	2.0 V	60	155	194	233	ns
t _{PZH} , t _{PZL}	Maximum Output Enable Time	C _L = 50 pF	4.5 V	14	23	29	35	ns
		C _L = 150 pF	4.5 V	21	31	47	47	ns
		C _L = 50 pF	6.0 V	12	20	25	30	ns
		C _L = 150 pF	6.0 V	19	27	34	41	ns
t _{PHZ} , t _{PLZ}	Maximum Output Disable Time	R _L = 1 kΩ	2.0 V	55	140	175	210	ns
		C _L = 50 pF	2.0 V	67	180	225	270	ns
		C _L = 50 pF	4.5 V	15	28	35	42	ns
		C _L = 150 pF	4.5 V	24	36	45	54	ns
t _s	Minimum Set Up Time Data to LE	C _L = 50 pF	6.0 V	14	24	30	36	ns
		C _L = 150 pF	6.0 V	22	31	39	47	ns
		R _L = 1 kΩ	2.0 V	40	125	156	188	ns
		C _L = 50 pF	4.5 V	13	25	31	38	ns
t _H	Minimum Hold Time LE to Data	C _L = 50 pF	6.0 V	12	21	27	32	ns
			2.0 V	30	75	95	110	ns
			4.5 V	10	15	19	22	ns
			6.0 V	9	13	16	19	ns
t _w	Minimum Pulse Width LE, or Data		2.0 V	–	25	31	38	ns
			4.5 V	–	5	6	7	ns
			6.0 V	–	4	5	6	ns
			2.0 V	30	80	100	120	ns
t _{THL} , t _{TLH}	Maximum Output Rise and Fall Time, Clock		4.5 V	9	16	20	24	ns
			6.0 V	8	14	18	20	ns
		C _L = 50 pF	2.0 V	25	60	75	90	ns
			4.5 V	7	12	15	18	ns
C _{PD}	Power Dissipation Capacitance (Note 3) (per latch)	OC = V _{CC}	–	5	–	–	–	pF
		OC = GND	–	52	–	–	–	pF
C _{IN}	Maximum Input Capacitance		–	5	10	10	10	pF
C _{OUT}	Maximum Output Capacitance		–	15	20	20	20	pF

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. C_{PD} determines the no load dynamic power consumption, P_D = C_{PD} V_{CC}²f + I_{CC} V_{CC}, and the no load dynamic current consumption, I_S = C_{PD} V_{CC} f + I_{CC}.

MM74HC573

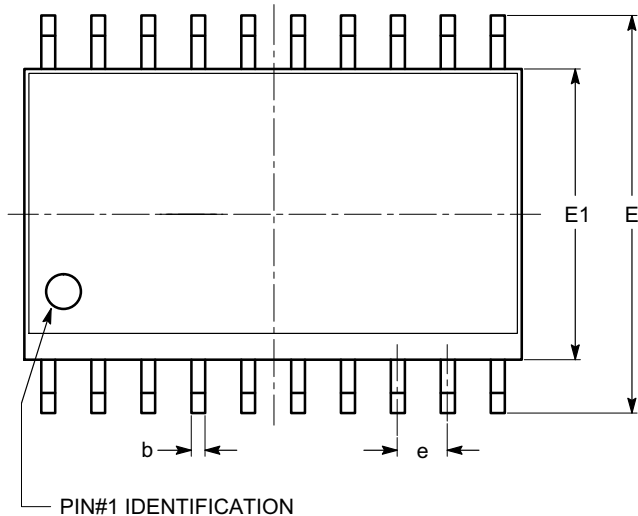
ORDERING INFORMATION

Device	Marking	Package	Shipping [†]
MM74HC573WM	HC573A	SOIC-20 WB (Pb-Free and Halide Free)	38 Units / Tube
MM74HC573WMX	HC573A	SOIC-20, 300 mils (Pb-Free and Halide Free)	1000 Units / Tape & Reel
MM74HC573MTC	HC 573A	TSSOP-20 WB (Pb-Free)	75 Units / Tube
MM74HC573MTCX	HC 573A	TSSOP-20 WB (Pb-Free)	2500 Units / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

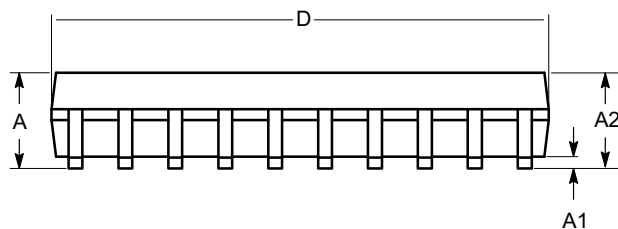
SOIC-20, 300 mils
CASE 751BJ
ISSUE O

DATE 19 DEC 2008

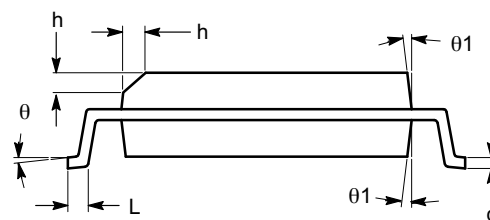


TOP VIEW

SYMBOL	MIN	NOM	MAX
A	2.36	2.49	2.64
A1	0.10		0.30
A2	2.05		2.55
b	0.31	0.41	0.51
c	0.20	0.27	0.33
D	12.60	12.80	13.00
E	10.01	10.30	10.64
E1	7.40	7.50	7.60
e	1.27 BSC		
h	0.25		0.75
L	0.40	0.81	1.27
θ	0°		8°
$\theta 1$	5°		15°



SIDE VIEW



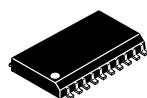
END VIEW

Notes:

- (1) All dimensions are in millimeters. Angles in degrees.
- (2) Complies with JEDEC MS-013.

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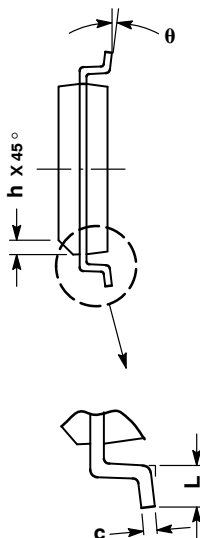
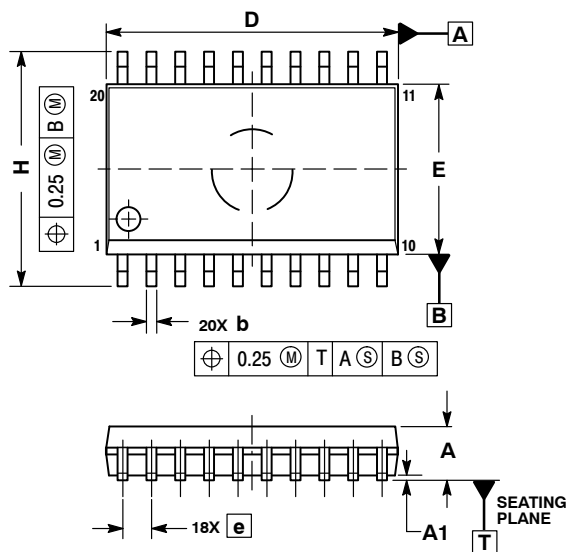
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SCALE 1:1

SOIC-20 WB
CASE 751D-05
ISSUE H

DATE 22 APR 2015

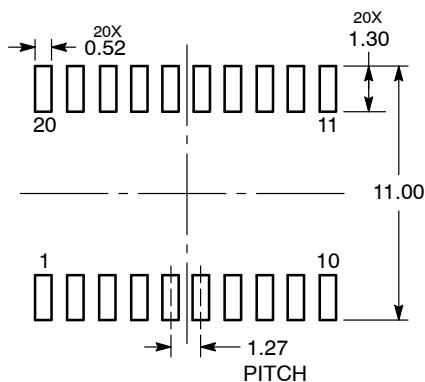


NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS	
	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
b	0.35	0.49
c	0.23	0.32
D	12.65	12.95
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0°	7°

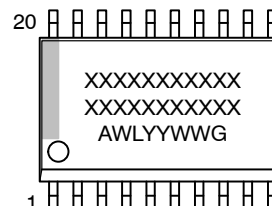
RECOMMENDED
SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC
MARKING DIAGRAM*



XXXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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