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April 2016

FAN7388
3 Half-Bridge Gate-Drive IC

Features

- Floating Channel for Bootstrap Operation to +600 V
- Typically 350 mA / 650 mA Sourcing/Sinking Current Driving Capability for All Channels
- 3 Half-Bridge Gate Driver
- Extended Allowable Negative V_S Swing to -9.8 V for Signal Propagation at V_{BS}=15 V
- Matched Propagation Delay Time Maximum: 50 ns
- 3.3 V and 5 V Input Logic Compatible
- Built-in Shoot-Through Prevention Circuit for All Channels with 270 ns Typical Dead Time
- Built-in Common Mode dv/dt Noise Canceling Circuit
- Built-in UVLO Functions for All Channels

Applications

- 3-Phase Motor Inverter Driver

Related Resources

- *AN-6076 - Design and Application Guide of Bootstrap Circuit for High-Voltage Gate-Drive IC*
- *AN-9052 - Design Guide for Selection of Bootstrap Components*
- *AN-8102 - Recommendations to Avoid Short Pulse Width Issues in HVIC Gate Driver Applications*

Description

The FAN7388 is a monolithic three half-bridge gate-drive IC designed for high-voltage, high-speed driving MOSFETs and IGBTs operating up to +600 V.

Fairchild's high-voltage process and common-mode noise canceling technique provide stable operation of high-side drivers under high-dv/dt noise circumstances.

An advanced level-shift circuit allows high-side gate driver operation up to V_S=-9.8 V (typical) for V_{BS}=15 V.

The UVLO circuits prevent malfunction when V_{DD} and V_{BS} are lower than the specified threshold voltage.

Output drivers typically source/sink 350 mA / 650 mA, respectively, which is suitable for three-phase half-bridge applications in motor drive systems.

20-SOIC



Ordering Information

Part Number	Package	Operating Temperature Range	Packing Method
FAN7388MX	20-SOIC	-40°C to +125°C	Tape & Reel

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Typical Application Circuit

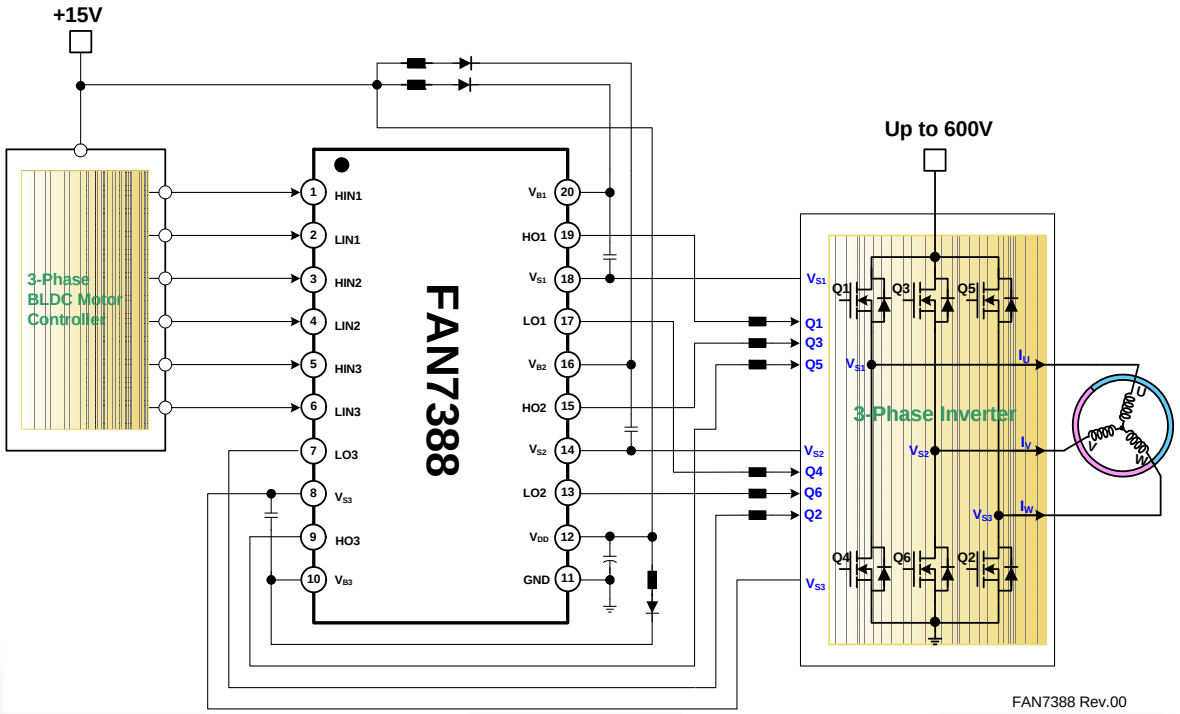


Figure 1. 3-Phase BLDC Motor Drive Application

Internal Block Diagram

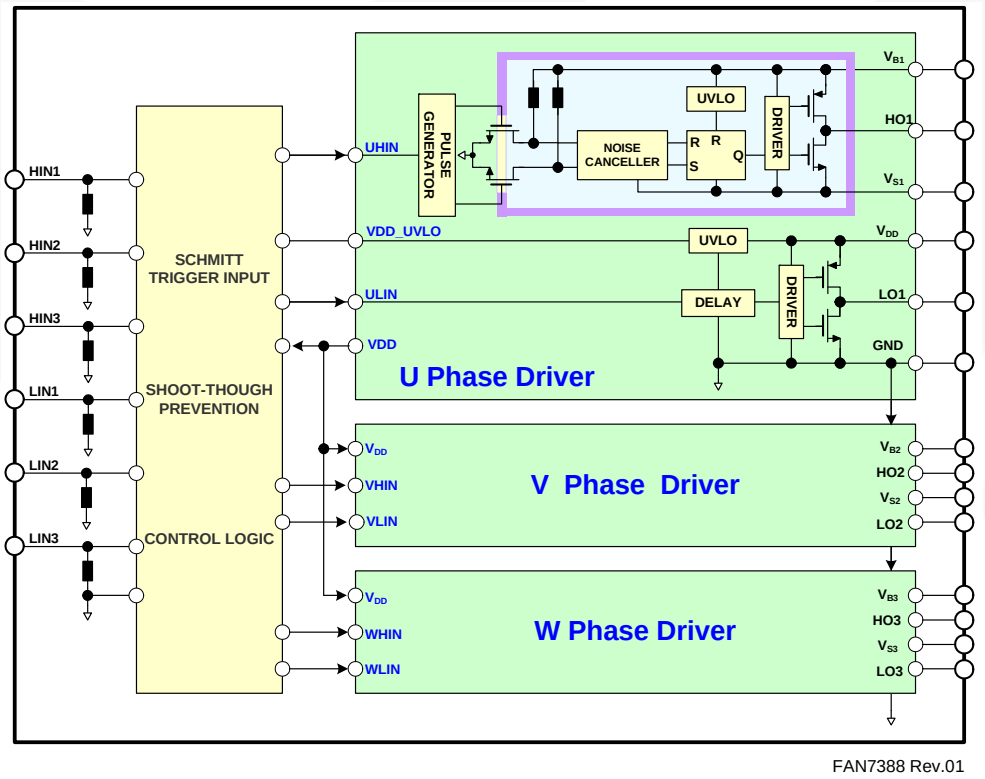


Figure 2. Functional Block Diagram

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Pin Configuration

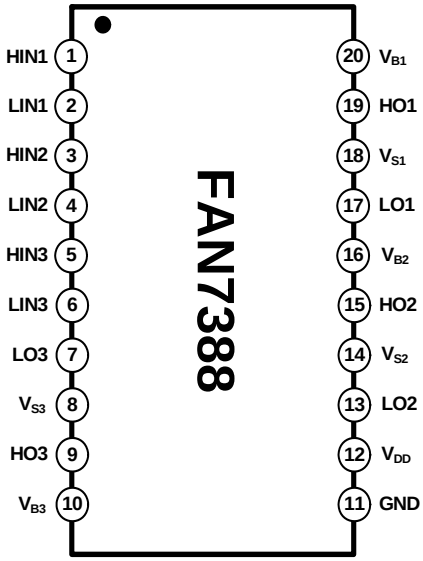


Figure 3. Pin Configuration (Top View)

Pin Definitions

Pin #	Name	Description
1	HIN1	Logic input 1 for high-side gate 1 driver
2	LIN1	Logic input 1 for low-side gate 1 driver
3	HIN2	Logic input 2 for high-side gate 2 driver
4	LIN2	Logic input 2 for low-side gate 2 driver
5	HIN3	Logic input 3 for high-side gate 3 driver
6	LIN3	Logic input 3 for low-side gate 3 driver
7	LO3	Low-side gate driver 3 output
8	V_{S3}	High-side driver 3 floating supply offset voltage
9	HO3	High-side driver 3 gate driver output
10	V_{B3}	High-side driver 3 floating supply voltage
11	GND	Ground
12	V_{DD}	Logic and all low-side gate drivers power supply voltage
13	LO2	Low-side gate driver 2 output
14	V_{S2}	High-side driver 2 floating supply offset voltage
15	HO2	High-side driver 2 gate driver output
16	V_{B2}	High-side driver 2 floating supply voltage
17	LO1	Low-side gate driver 1 output
18	V_{S1}	High-side driver 1 floating supply offset voltage
19	HO1	High-side driver 1 gate driver output
20	V_{B1}	High-side driver 1 floating supply voltage

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Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. T_A=25°C, unless otherwise specified.

Symbol	Parameter	Min.	Max.	Unit
V_B	High-Side Floating Supply Voltage of $V_{B1,2,3}$	-0.3	625.0	V
V_S	High-Side Floating Supply Offset Voltage of $V_{S1,2,3}$	$V_{B1,2,3}$-25	$V_{B1,2,3}$+0.3	V
$V_{HO1,2,3}$	High-Side Floating Output Voltage	$V_{S1,2,3}$-0.3	$V_{B1,2,3}$+0.3	V
V_{DD}	Low-Side and Logic-fixed Supply Voltage	-0.3	25.0	V
$V_{LO1,2,3}$	Low-Side Output Voltage	-0.3	V_{DD}+0.3	V
V_{IN}	Logic Input Voltage (HIN1,2,3 and LIN1,2,3)	-0.3	V_{DD}+0.3	V
dV_S/dt	Allowable Offset Voltage Slew Rate		50	V/ns
P_D	Power Dissipation[1][2][3]		1.47	W
θ_{JA}	Thermal Resistance, Junction-to-ambient		85	°C/W
T_J	Junction Temperature		+150	°C
T_{STG}	Storage Temperature	-55	+150	°C

Notes:

1. Mounted on 76.2 x 114.3 x 1.6 mm PCB (FR-4 glass epoxy material).
2. Refer to the following standards:
   JESD51-2: Integral circuits thermal test method environmental conditions - natural convection
   JESD51-3: Low effective thermal conductivity test board for leaded surface-mount packages.
3. Do not exceed P_D under any circumstances.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Max.	Unit
$V_{B1,2,3}$	High-Side Floating Supply Voltage	$V_{S1,2,3}$+10	$V_{S1,2,3}$+20	V
$V_{S1,2,3}$	High-Side Floating Supply Offset Voltage	6-V_{DD}	600	V
V_{DD}	Supply Voltage	10	20	V
$V_{HO1,2,3}$	High-Side Output Voltage	$V_{S1,2,3}$	$V_{B1,2,3}$	V
$V_{LO1,2,3}$	Low-Side Output Voltage	GND	V_{DD}	V
V_{IN}	Logic Input Voltage (HIN1,2,3 and LIN1,2,3)	GND	V_{DD}	V
T_A	Ambient Temperature	-40	+125	°C

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Electrical Characteristics

V_{BIAS} (V_{DD}, $V_{BS1,2,3}$)=15.0 V, T_A=25°C, unless otherwise specified. The V_{IN} and I_{IN} parameters are referenced to GND. The V_O and I_O parameters are referenced to GND and $V_{S1,2,3}$ and are applicable to the respective outputs LO1,2,3 and HO1,2,3.

Symbol	Characteristics	Condition	Min.	Typ.	Max.	Unit
LOW-SIDE POWER SUPPLY SECTION						
I_{QDD}	Quiescent V_{DD} Supply Current	$V_{LIN1,2,3}$=0 V or 5 V		160	350	µA
$I_{PDD1,2,3}$	Operating V_{DD} Supply Current for each Channel	$f_{LIN1,2,3}$=20 kHz, rms Value		500	900	µA
V_{DDUV+}	V_{DD} Supply Under-Voltage Positive-Going Threshold	V_{DD}=Sweep, V_{BS}=15 V	7.2	8.2	9.0	V
V_{DDUV-}	V_{DD} Supply Under-Voltage Negative-Going Threshold	V_{DD}=Sweep, V_{BS}=15 V	6.8	7.8	8.5	V
V_{DDHYS}	V_{DD} Supply Under-Voltage Lockout Hysteresis	V_{DD}=Sweep, V_{BS}=15 V		0.4		V
BOOTSTRAPPED POWER SUPPLY SECTION						
$I_{QBS1,2,3}$	Quiescent V_{BS} Supply Current for each Channel	$V_{HIN1,2,3}$=0 V or 5 V		50	120	µA
$I_{PBS1,2,3}$	Operating V_{BS} Supply Current for each Channel	$f_{HIN1,2,3}$=20 kHz, rms Value		400	800	µA
V_{BSUV+}	V_{BS} Supply Under-Voltage Positive-going Threshold	V_{DD}=15 V, V_{BS}=Sweep	7.2	8.2	9.0	V
V_{BSUV-}	V_{BS} Supply Under-Voltage Negative-going Threshold	V_{DD}=15 V, V_{BS}=Sweep	6.8	7.8	8.5	V
V_{BSHYS}	V_{BS} Supply Under-Voltage Lockout Hysteresis	V_{DD}=15 V, V_{BS}=Sweep		0.4		V
I_{LK}	Offset Supply Leakage Current	$V_{B1,2,3}$=$V_{S1,2,3}$=600 V			10	µA
GATE DRIVER OUTPUT SECTION						
V_{OH}	High-Level Output Voltage, V_{BIAS}-V_O	I_O=20 mA			1.0	V
V_{OL}	Low-Level Output Voltage, V_O	I_O=20 mA			0.6	V
I_{O+}	Output HIGH Short-Circuit Pulsed Current(4)	V_O=0 V, V_{IN}=5 V with PW <10 µs	250	350		mA
I_{O-}	Output LOW Short-Circuit Pulsed Current(4)	V_O=15 V, V_{IN}=0 V with PW <10 µs	500	650		mA
V_S	Allowable Negative V_S Pin Voltage for IN Signal Propagation to H_O			-9.8	-7.0	V
LOGIC INPUT SECTION (HIN, LIN)						
V_{IH}	Logic "1" Input Voltage		2.5			V
V_{IL}	Logic "0" Input Voltage				1.0	V
I_{IN+}	Logic "1" Input Bias Current	V_{IN}=5 V		25	50	µA
I_{IN-}	Logic "0" Input Bias Current(4)	V_{IN}=0 V			2.0	µA
R_{IN}	Input Pull-Down Resistance		100	200	300	KΩ

Note:

4. This parameter is guaranteed by design.

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Dynamic Electrical Characteristics

T_A=25°C, V_{BIAS} (V_{DD}, $V_{BS1,2,3}$)=15.0 V, $V_{S1,2,3}$=GND, C_{Load}=1000 pF unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
t_{ON}	Turn-on Propagation Delay	$V_{S1,2,3}$=0 V		130	220	ns
t_{OFF}	Turn-off Propagation Delay	$V_{S1,2,3}$=0 V		150	240	ns
t_R	Turn-on Rise Time			50	120	ns
t_F	Turn-off Fall Time			30	80	ns
MT1	Turn-on Delay Matching I $t_{ON(H)}$ -$t_{OFF(L)}$ I				50	ns
MT2	Turn-off Delay Matching I $t_{OFF(H)}$ -$t_{ON(L)}$ I				50	ns
DT	Dead Time		100	270	440	ns
MDT	Dead-time Matching I t_{DT1} -t_{DT2} I				60	ns

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Typical Characteristics

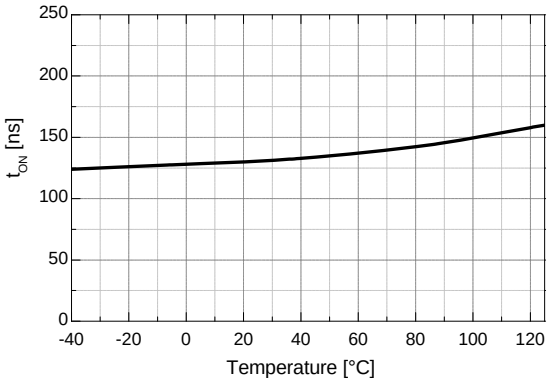


Figure 4. Turn-on Propagation Delay vs. Temp.

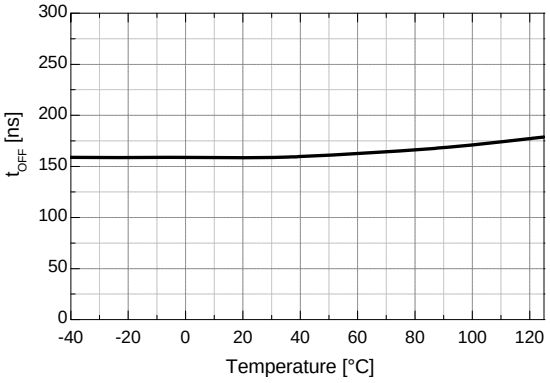


Figure 5. Turn-off Propagation Delay vs. Temp.

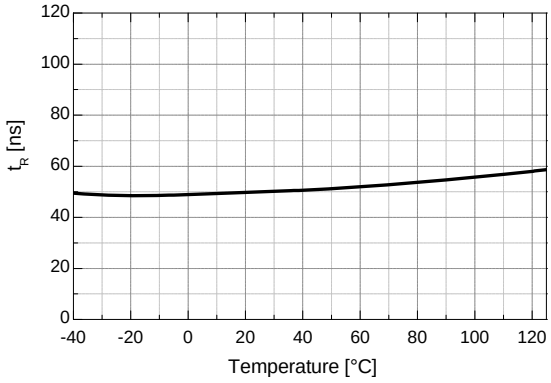


Figure 6. Turn-on Rise Time vs. Temp.

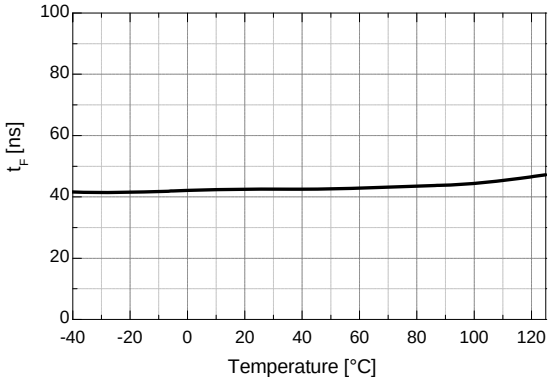


Figure 7. Turn-off Fall Time vs. Temp.

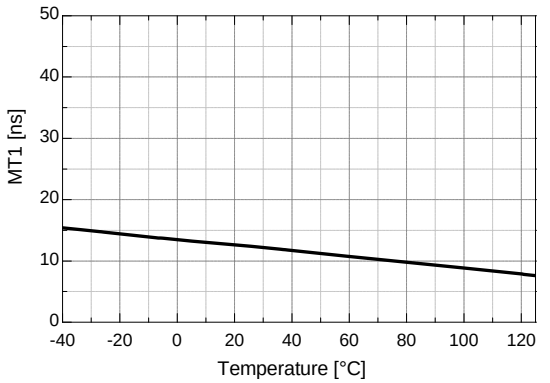


Figure 8. Turn-on Delay Matching vs. Temp.

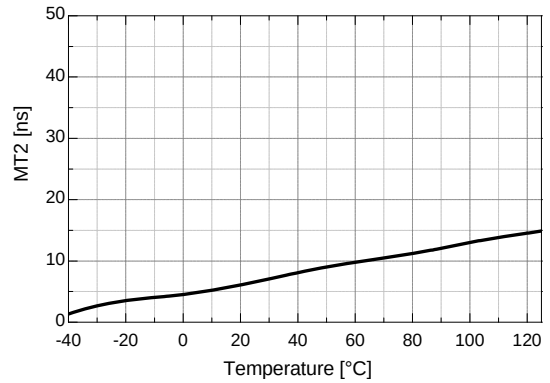


Figure 9. Turn-off Delay Matching vs. Temp.

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Typical Characteristics (Continued)

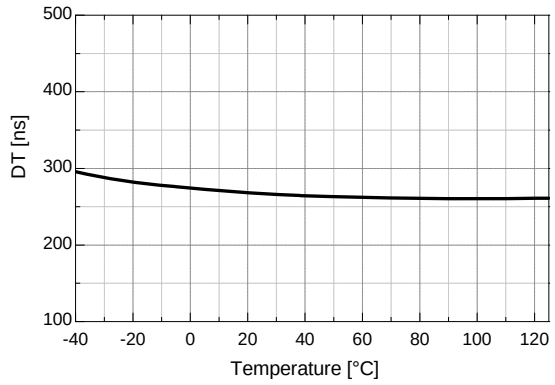


Figure 10. Dead Time vs. Temp.

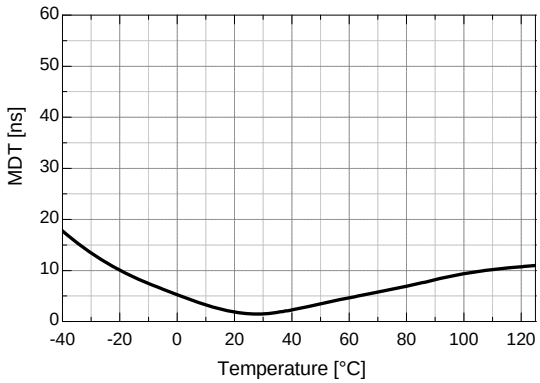


Figure 11. Dead-Time Matching vs. Temp.

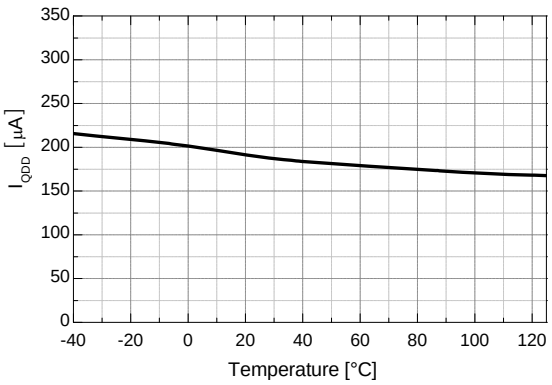


Figure 12. Quiescent V_{DD} Supply Current vs. Temp.

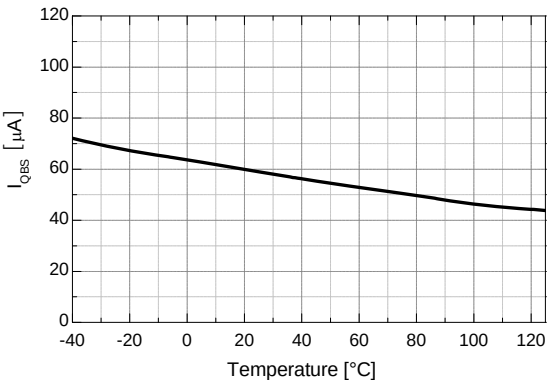


Figure 13. Quiescent V_{BS} Supply Current vs. Temp.

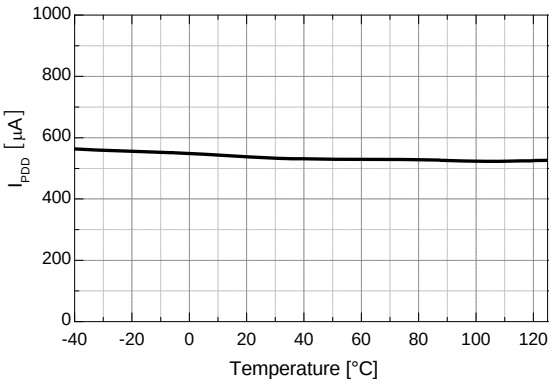


Figure 14. Operating V_{DD} Supply Current vs. Temp.

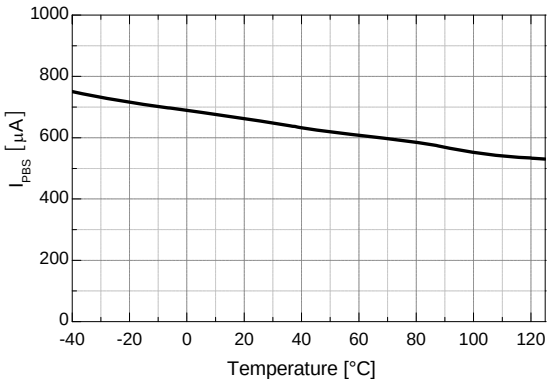


Figure 15. Operating V_{BS} Supply Current vs. Temp.

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Typical Characteristics (Continued)

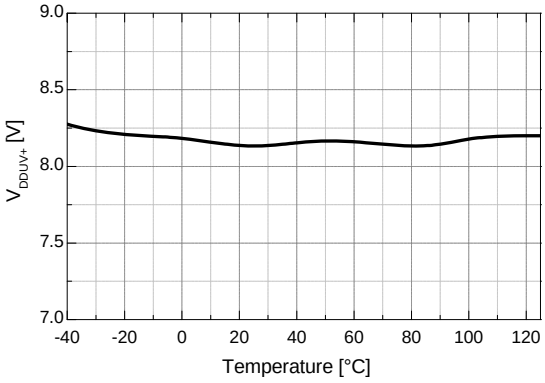


Figure 16. V_{DD} UVLO+ vs. Temp.

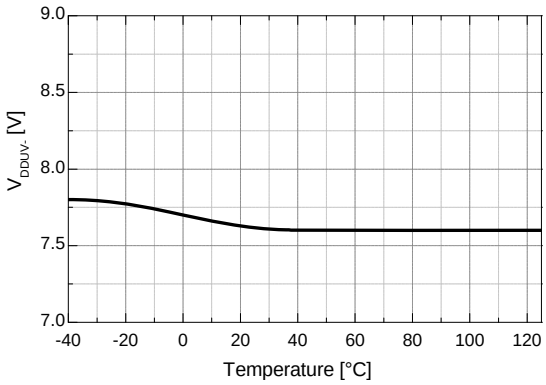


Figure 17. V_{DD} UVLO- vs. Temp.

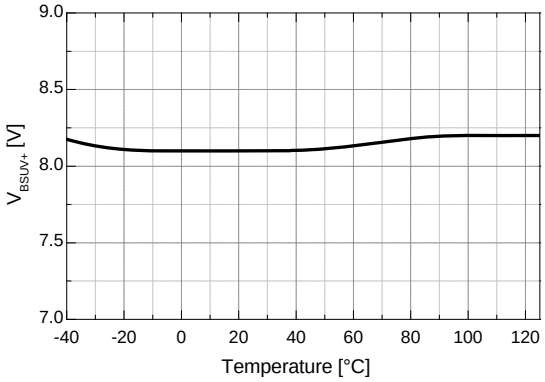


Figure 18. V_{BS} UVLO+ vs. Temp.

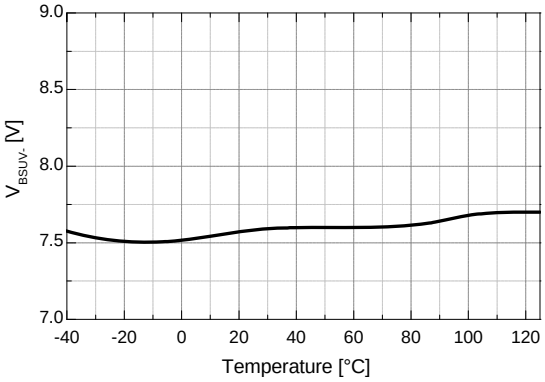


Figure 19. V_{BS} UVLO- vs. Temp.

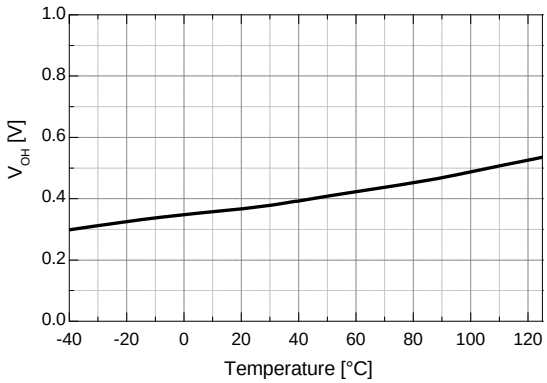


Figure 20. High-Level Output Voltage vs. Temp.

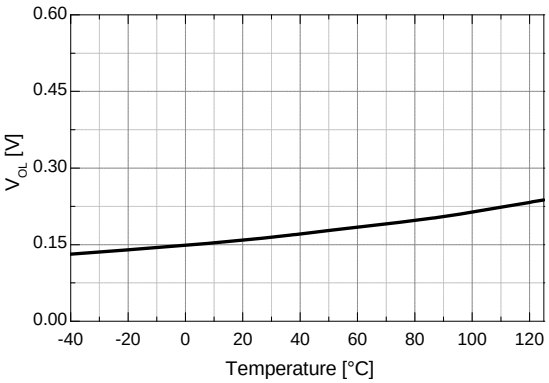


Figure 21. Low-Level Output Voltage vs. Temp.

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Typical Characteristics (Continued)

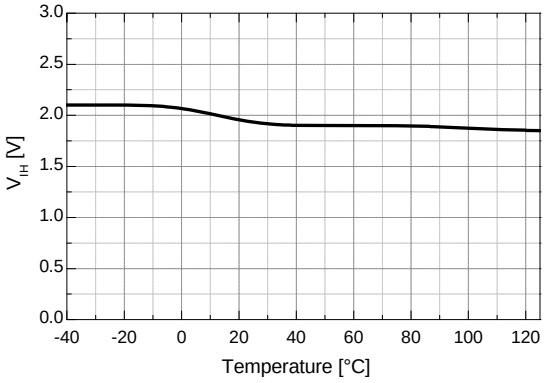


Figure 22. Logic High Input Voltage vs. Temp.

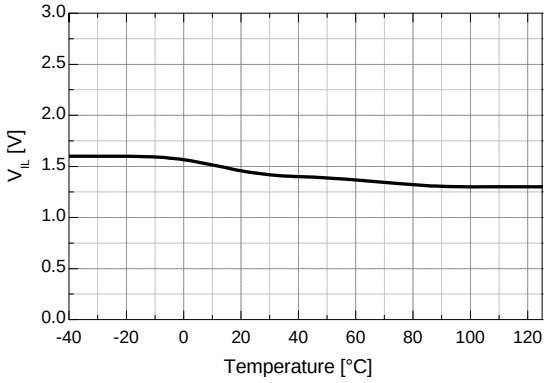


Figure 23. Logic Low Input Voltage vs. Temp.

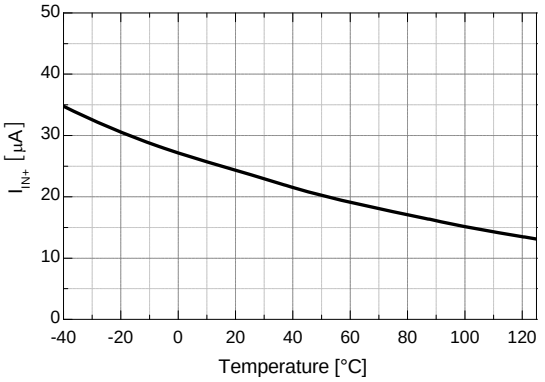


Figure 24. Logic Input High Bias Current vs. Temp.

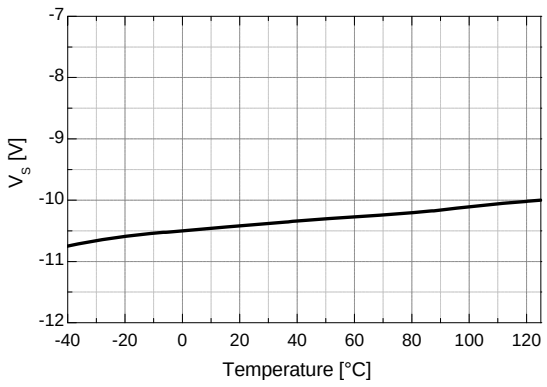


Figure 25. Allowable Negative V_S Voltage vs. Temp.

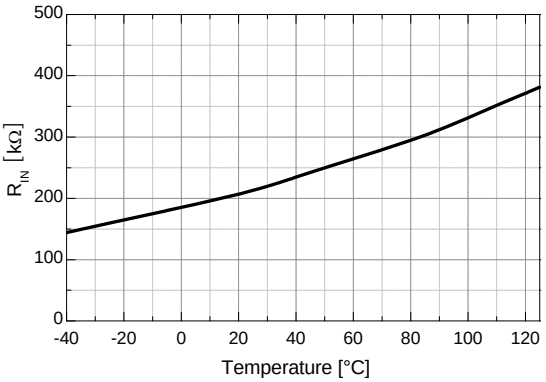


Figure 26. Input Pull-down Resistance vs. Temp.

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Application Information

1. Protection Function

1.1 Under-Voltage Lockout (UVLO)

The high- and low-side drivers include under-voltage lockout (UVLO) protection circuitry for each channel that monitors the supply voltage (V_{DD}) and bootstrap capacitor voltage ($V_{BS1,2,3}$) independently. It can be designed prevent malfunction when V_{DD} and $V_{BS1,2,3}$ are lower than the specified threshold voltage. The UVLO hysteresis prevents chattering during power supply transitions.

1.2 Shoot-Through Prevention Function

The FAN7388 has shoot-through prevention circuitry monitoring the high- and low-side control inputs. It can be designed to prevent outputs of high and low side from turning on at same time, as shown Figure 27 and 28.

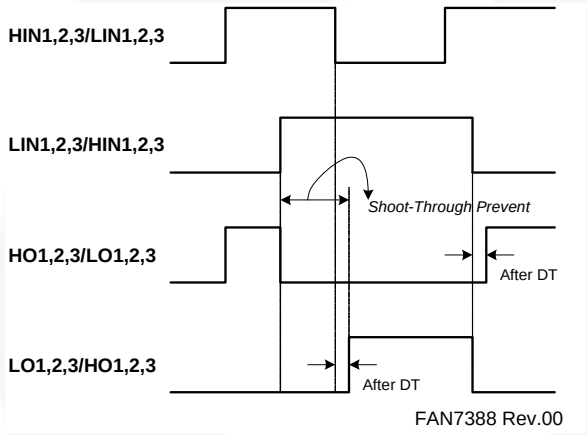


Figure 27. Waveforms for Shoot-Through Prevention

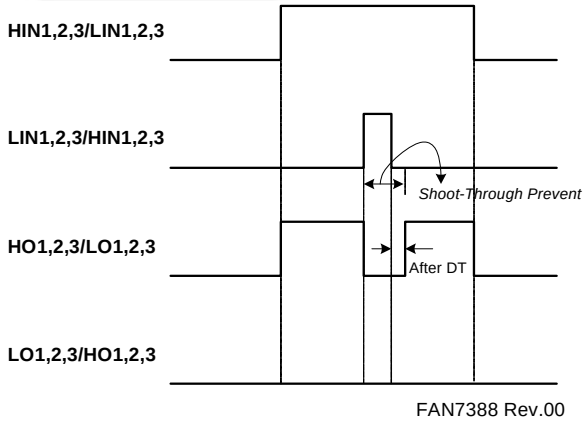


Figure 28. Waveforms for Shoot-Through Prevention

2. Operational Notes

The FAN7388 is a three half-bridge gate driver with internal, typical 270 ns dead-time for the three-phase brushless DC (BLDC) motor drive system, as shown in Figure 1.

Figure 29 shows a switching sequence of 120° electrical commutation for a three-phase BLDC motor drive system. The waveforms are idealized: they assumed that the generated back EMF waveforms are trapezoidal with flat tops of sufficient width to produce constant torque when the line currents are perfectly rectangular, 120° electrical degrees, with the switching sequence as shown in Figure 29. The operating waveforms of the wye-connection reveal that repeat every 60 electrical degrees, with each 60° segment being “commutated” to another phase, as shown in Figure 29.

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Application Information (Continued)

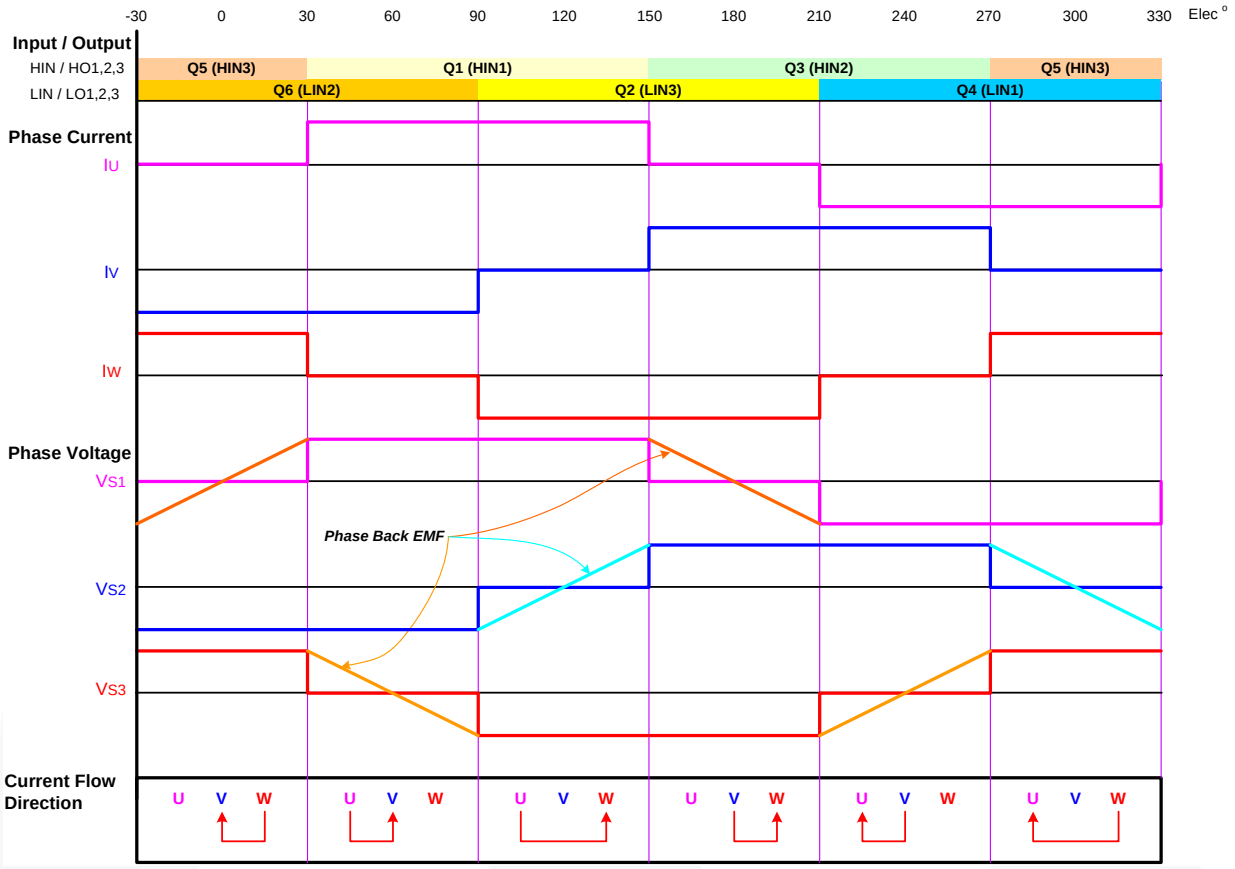


Figure 29. 120° Commutation Operation Waveforms for 3-Phase BLDC Motor Application

Switching Time Diagram

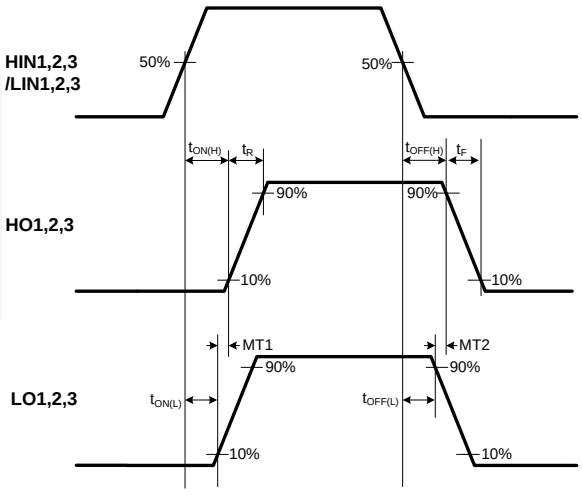
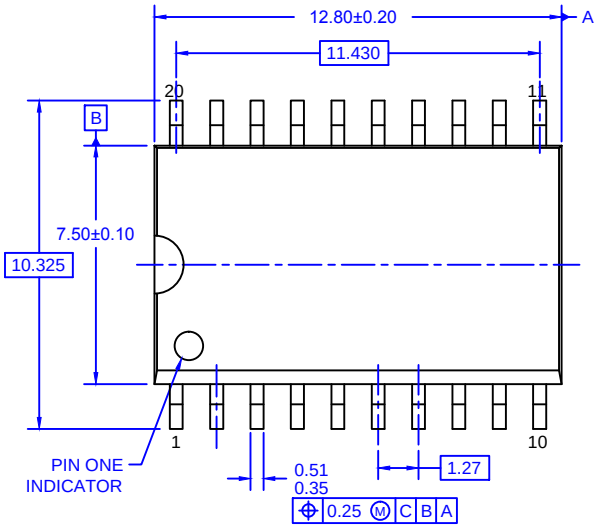
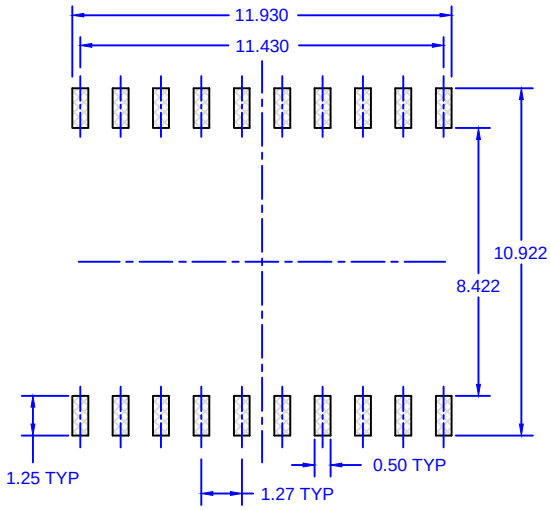


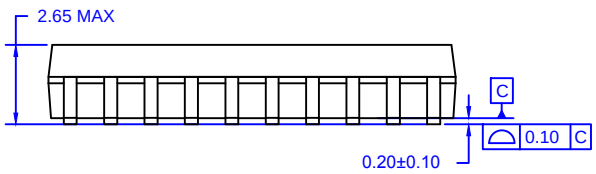
Figure 30. Switching Time Definition

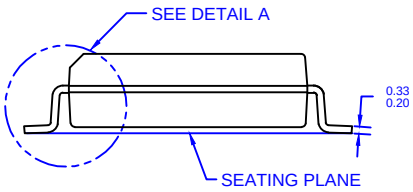
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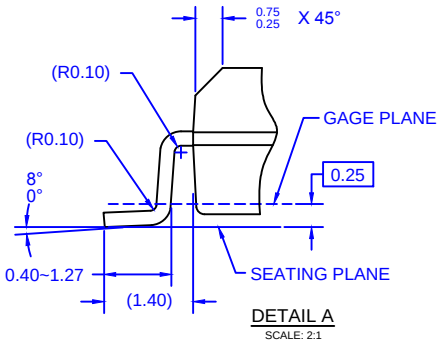




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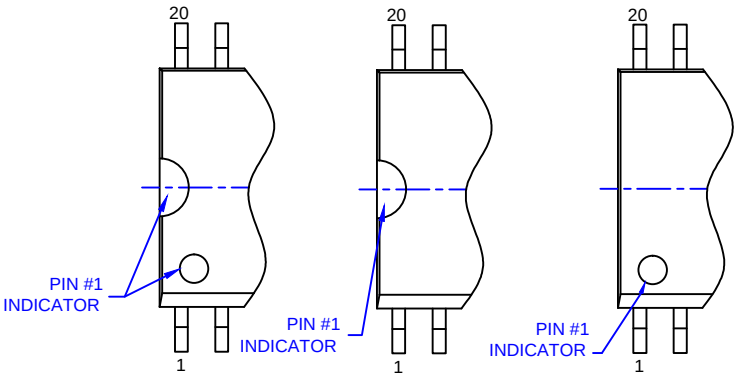






DETAIL A
SCALE: 2:1

PIN#1 IDENTIFICATION OPTIONS



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