# Automotive Intelligent Power Device Dual Channel 30 mΩ High Side Switch

## BV2HB030EUV-C

### General Description

The BV2HB030EUV-C dual channel 30 mΩ Intelligent High Side Power Device integrates an Overcurrent load protection, a dual Temperature Shutdown mechanism which limits the internal thermal transients and reduces the mechanical stress of the IC, and a smart Active-Clamp circuit to dissipate the magnetic energy while switching off inductive loads and to protect internal circuits from overvoltage surges. Embedded Current Sense and Diagnostic features provide real time load current information and open or short circuit feedback in both on and off state. A 3.3 V and 5 V CMOS compatible input pin offers direct microcontroller connection without special interfaces or level shifters. The part is a high performance IPD, specifically designed to drive lamps and other electrical or electronic loads, suitable for 12 V battery connected automotive applications.

### Features

- AEC-Q100 Qualified*(Note 1)*
- Functional Safety Supportive Automotive Products
- Short Circuit Load Protection
- Overcurrent Limitation
- Active Clamp and Overvoltage Protection
- Dual Temperature Shutdown
- Undervoltage Lock Out
- Integrated Current SENSE Circuit
- Loss of Ground Protection
- Open Load and Short to Battery Diagnostics

*(Note 1)* Grade 1

### Applications

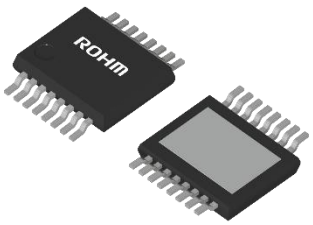
- Driver for Resistive, Inductive and Capacitive Loads
- MOSFET, Relay and Fuse Replacement
  Suitable to drive 4 A Loads and Lamps up to P27W/P21W + R5W

### Key Specifications

| | |
|---|---|
| ■Supply Nominal Voltage Range: | 6 V to 28 V |
| ■Low Operating Voltage (cranking): | 4 V (Max) |
| ■Overvoltage Protection: | 41 V (Min) |
| ■ON Resistance: | 30 mΩ (Typ) |
| ■Overcurrent Limit: | 45 A (Typ) |
| ■Sleep Current: | 0.5 µA (Max) |
| ■Operating Current: | 5 mA (Typ) |
| ■Junction Temperature Range (Tj): | -40 °C to +150 °C |

### Package

| | W (Typ) x D (Typ) x H (Max) |
|---|---|
| HTSSOP-C16 | 4.9 mm x 6.0 mm x 1.0 mm |




- Thermally Enhanced Thin Shrink Small-Outline 16 pin package with 0.5 mm Pin Pitch
- Exposed Pad for improved thermal performance

### Typical Application Circuit

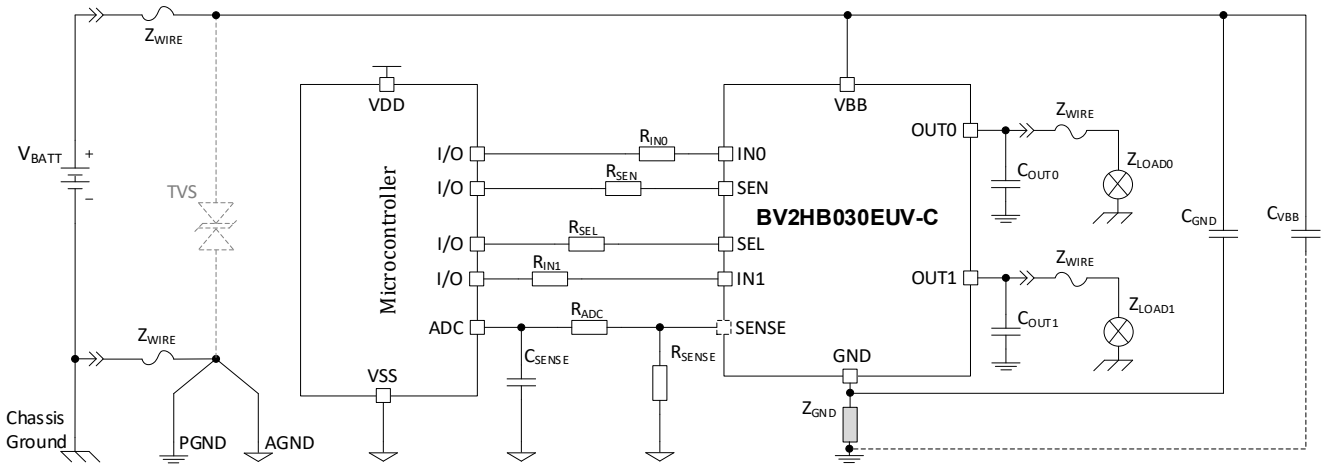



Figure 1. Typical Application Diagram

○Product structure : Silicon integrated circuit ○This product has no designed protection against radioactive rays.


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## Pin Configuration

HTSSOP-C16
(Top View)

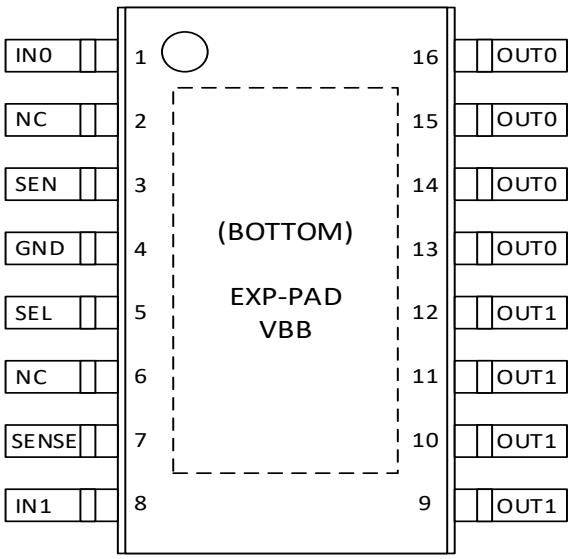



Figure 2. Pin Configuration

## Pin Description

| Pin No. | Pin Name | Function |
|---|---|---|
| 1 | IN0 | Input Pin. Turns on the Switch-Channel 0. Active “High” |
| 2 | NC | Internally not connected |
| 3 | SEN | Current Sense and diagnostic enable. Active “High” |
| 4 | GND | Device Ground pin |
| 5 | SEL | Selection of the Channel to be diagnosed. ”Low” selects Channel 0, “High” Channel 1 |
| 6 | NC | Internally not connected |
| 7 | SENSE | Current Sense analog output pin |
| 8 | IN1 | Input Pin. Turns on the Switch-Channel 1. Active “High” |
| 9 to 12 | OUT1 | High Side Switch Power Output-Channel 1*(Note 1)* |
| 13 to 16 | OUT0 | High Side Switch Power Output-Channel 0*(Note 1)* |
| EXP-PAD | VBB | Exposed-Pad. Power Supply Voltage Line Input |

*(Note 1)* Output pins of given channel are internally shorted. Please connect the respective pins together on the PCB such as the metal traces can withstand the desired maximum current.


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## Definitions

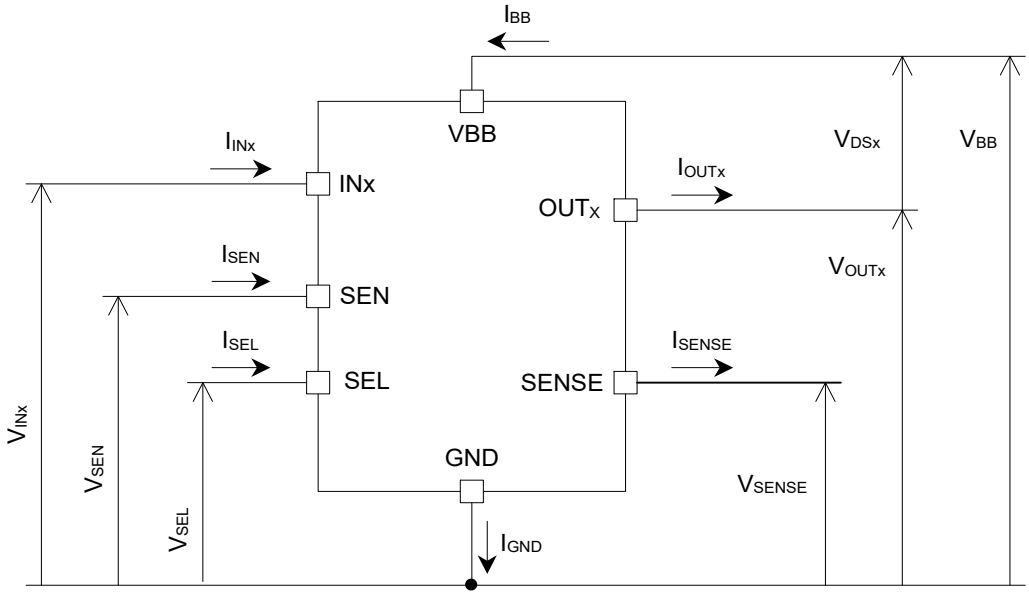



Figure 3. Voltage and Current Definitions


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## Absolute Maximum Ratings

| Parameters | Symbol | Ratings | Unit | Conditions |
|---|---|---|---|---|
| [Power Supply / GND pin] | | | | |
| DC Supply Voltage | $V_{BB}$ | -0.3 to +36 | V | |
| Supply Voltage at load dump | $V_{BB_LD}$ | 40 | V | ISO16750-2, Ri = 2 Ω |
| Supply Voltage (Output to GND short) *(Note 4)* | $V_{BB_SC}$ | -0.3 to +24 | V | AEC-Q100-012 |
| Supply Voltage (When battery is connected in reverse direction) | $V_{BB_REV}$ | -16 | V | less than 2 minutes, Tj = 25 °C, $R_{Lx}$ > 6 Ω, $Z_{GND}$ connected |
| GND Pin Current | $I_{GND}$ | -150 to +50 | mA | less than 2 minutes, Tj = 25 °C, $Z_{GND}$ = 150 Ω |
| [Input Pin] | | | | |
| Input Voltage | $V_{INx}$, $V_{SEN}$, $V_{SEL}$ | -0.3 to +7 | V | |
| Input Current | $I_{INx}$, $I_{SEN}$, $I_{SEL}$ | -2 to +2 | mA | Tj = 25 °C, $R_{INx}$, $R_{SEN}$, $R_{SEL}$ ≥ 4.7 kΩ |
| | | -5 to +10 | mA | less than 2 minutes, Tj = 25 °C, $R_{INx}$, $R_{SEN}$, $R_{SEL}$ ≥ 15 kΩ |
| [SENSE pin] | | | | |
| SENSE Voltage | $V_{SENSE}$ | -1 to +7 | V | |
| SENSE Current | $I_{SENSE}$ | -20 to internal limitation *(Note 1)* | mA | $R_{SENSE}$ = 1 kΩ |
| [OUTx pin] | | | | |
| Power Supply to Output Voltage | $V_{DSx}$ | -0.3 to internal limitation *(Note 2)* | V | |
| Maximum Output Current | $I_{OUTx}$ | internal limitation *(Note 3)* | A | Maximum $V_{BB}$ = 28 V |
| Single Pulse Energy Rating *(Note 4)* | $E_{AS_25°C}$ | 100 | mJ | Tj = 25 °C, $V_{BB}$ = 28 V, $I_{OUT(START)}$ = 3 A |
| | $E_{AS_150°C}$ | 50 | mJ | Tj = 150 °C, $V_{BB}$ = 28 V, $I_{OUT(START)}$ = 3 A |
| [Temperature] | | | | |
| Storage Temperature Range | Tstg | -55 to +150 | °C | |
| Junction Temperature Range | Tj | -40 to +150 | °C | |
| Maximum Junction Temperature | Tjmax | 150 | °C | |
| [ESD] *(Note 5)* | | | | |
| Electrostatic-Discharge Capability Human Body Model - HBM | VBB, OUTx pins | ±4 | kV | |
| | INx, SEN, SEL, SENSE pins | ±2 | kV | |
| Electrostatic-Discharge Capability Charged Device Model - CDM | All pins | ±750 | V | |

*(Note 1)* Internal limitation by SENSE voltage clamp and current-limitation protection. Please see the "*Electrical Characteristics*" section for more details.
*(Note 2)* Internal limitation by output active-clamp overvoltage protection. Please see the "*Electrical Characteristics*" section for more details.
*(Note 3)* Internal limitation by output overcurrent protection. Please see the "*Electrical Characteristics*" section for more details.
*(Note 4)* Specified by design and/or statistical analysis of correlated parameters tested in production.
*(Note 5)* Measured as per EIA/JEDEC and AEC-Q100 Standard. HMB-Measured as per JESD22-A114D and AEC-Q100-002.
CDM-Measured as per JESD22-C101C and AEC-Q100-011.

***Caution 1**: Exposure to the absolute maximum ratings may cause permanent damage to the IC, may affect the device reliability and lifetime. Therefore, operation at or above the absolute maximum ratings is not recommended. The above-described values represent stress ratings and functional operation is not implied. In addition, no destructive conditions such as short or open can be assumed.*

***Caution 2**: If the IC is used in a manner that exceeds the maximum junction temperature the original characteristics of the IC will be degraded. If the junction temperature exceeds the maximum specified temperature, increase the board size, increase the area of copper foil for heat dissipation, or use a heat sink. Consider reducing the thermal resistance so that the maximum junction temperature is not exceeded.*

***Caution 3**: When an inductive load is turned off, the $V_{OUT}$ voltage drops below ground level. An integrated active-clamp (overvoltage) protection limits the maximum $V_{DS}$ across the power transistor and the inductive energy is dissipated internally. The energy can be calculated using the following equation:*


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### Absolute Maximum Ratings – continued

$$E_{AS} = V_{DSCLP} \times \left[\frac{V_{BB} - V_{DSCLP}}{R_L} \times \ln\left(1 - \frac{R_L \times I_{OUT(START)}}{V_{BB} - V_{DSCLP}}\right) + I_{OUT(START)}\right] \times \frac{L}{R_L}$$

Where:
$L$ is the inductance value of the load.
$R_L$ is the resistance value of the load.
$V_{BB}$ is the supply voltage.
$V_{DSCLP}$ is the clamping voltage.
$I_{OUT(START)}$ is the current flowing through the load at the instance the inductive load is turned off.

In simplified form, if $R_L$ is neglected.

$$E_{AS} = \frac{1}{2} \times L \times I_{OUT(START)}{}^2 \times \left(1 - \frac{V_{BB}}{V_{BB} - V_{DSCLP}}\right)$$

***Caution 4**: The maximum $E_{AS}$ energy the device can dissipate for a given $I_{OUT(START)}$ is limited by the maximum thermal transient the power transistor can handle, hence the maximum inductance L must be selected with respect to the maximum given $I_{OUT(START)}$.*

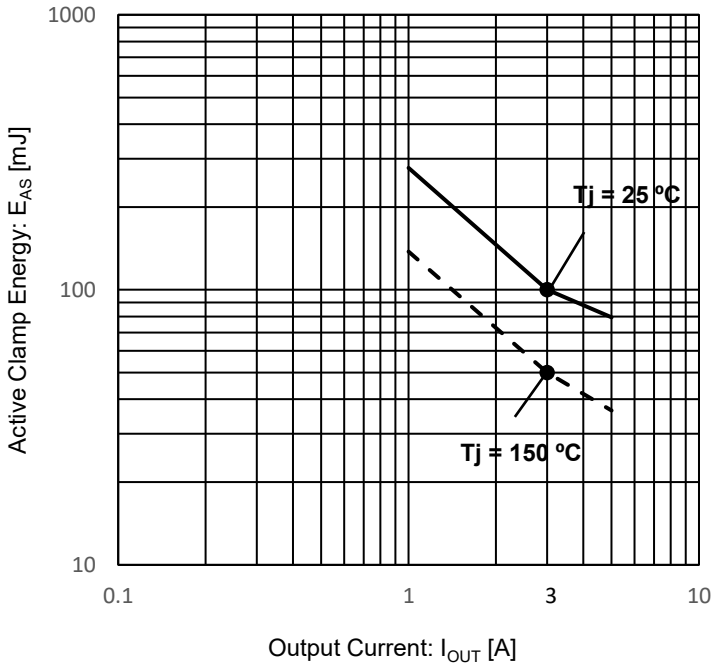



Figure 4. Active Clamp Energy vs Output Current

### Recommended Operating Conditions

| Parameters | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Supply Nominal Voltage Range *(Note 1)* | $V_{BB}$ | 6 | 14 | 28 | V |
| Input Voltage | $V_{INx}$, $V_{SEN}$, $V_{SEL}$ | 0 | - | 5.5 | V |
| Operating Junction Temperature | Tj | -40 | +25 | +150 | °C |
| Input Frequency | $f_{INx}$ | - | - | 1 | kHz |

*(Note 1)* An extended supply operating voltage range from 4.0 V up to 28 V is possible after start-up; protections are operational. The device is functional up to 36 V and protections are active, however parameter deviations are possible. Please refer to the "*Electrical Characteristics*" section and the "*Features Description*" section.


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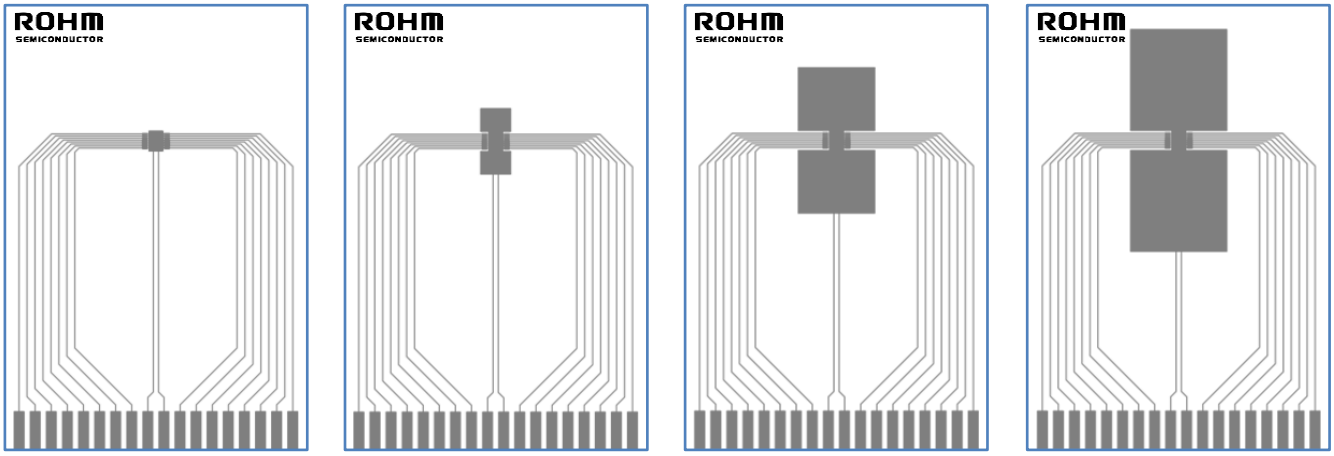
### Thermal Resistance *(Note 1)*

| Parameters | Symbol | Typ | Unit | Conditions | |
|---|---|---|---|---|---|
| HTSSOP-C16 (One Output-Channel Active) | | | | | |
| Thermal Resistance between junction and ambient temperature | $\theta_{JA}$ | 113.3 | °C/W | 1s | *(Note 2)* |
| | | 30.6 | °C/W | 2s | *(Note 3)* |
| | | 26.4 | °C/W | 2s2p | *(Note 4)* |
| Thermal characterization parameter between junction and top center of the outside surface of the component package | $\Psi_{JT}$ | 14 | °C/W | 1s | *(Note 2)* |
| | | 5 | °C/W | 2s | *(Note 3)* |
| | | 5 | °C/W | 2s2p | *(Note 4)* |

*(Note 1)* Based on JESD51-2A(Still-Air). Specified by design.
*(Note 2)* Using a PCB board based on JESD51-3.
*(Note 3)* Using a PCB board based on JESD51-5.
*(Note 4)* Using a PCB board based on JESD51-5, 7.

***Caution**: The values presented here were measured/simulated under a specific set of conditions and should be regarded only as a guideline on how to estimate the thermal behavior of the application and should not be used as design parameters. A careful evaluation of the actual application values should be done to confirm the estimated results.*

■ PCB Layout 1 Layer (1s)




Footprint 100 $mm^2$ 600 $mm^2$ 1200 $mm^2$

Figure 5. PCB Layout 1 Layer (1s)

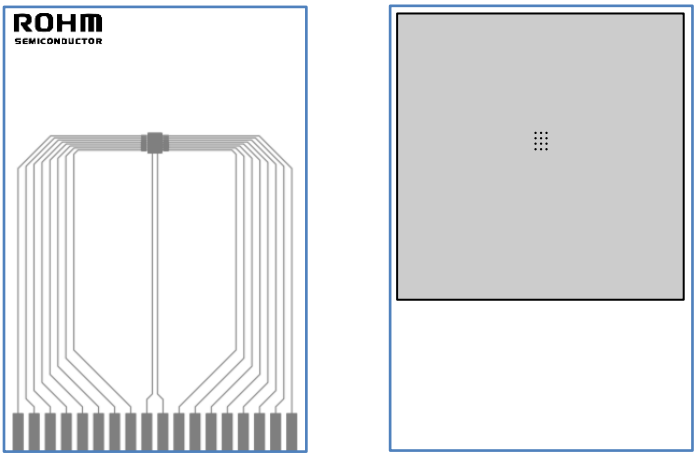
| Dimension | Value |
|---|---|
| Board Finish Thickness | 1.57 mm |
| Board Dimension | 76.2 mm x 114.3 mm |
| Board Material | FR4 |
| Copper Thickness | 0.070 mm (Cu: 2 oz) |
| Copper Foil Area | Footprint / 100 $mm^2$ / 600 $mm^2$ / 1200 $mm^2$ |


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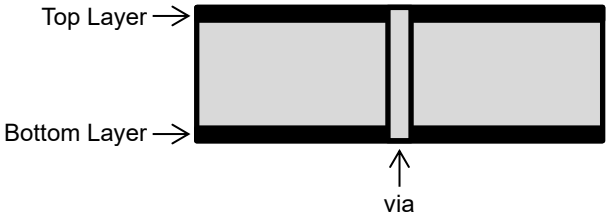
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### Thermal Resistance – continued

■ PCB Layout 2 Layers (2s)




Top Layer Bottom Layer




Cross Section

Figure 6. PCB Layout 2 Layers (2s)

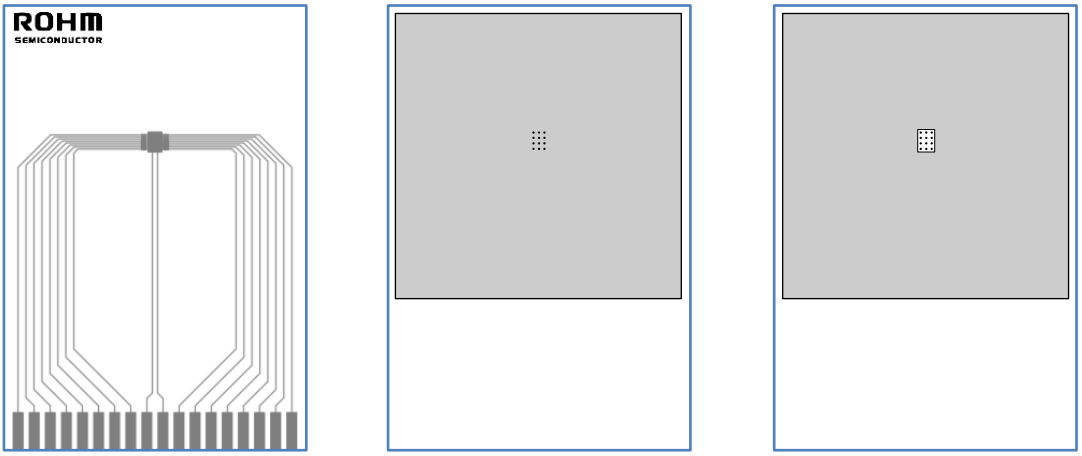
| Dimension | Value |
|---|---|
| Board Finish Thickness | 1.60 mm |
| Board Dimension | 76.2 mm x 114.3 mm |
| Board Material | FR4 |
| Copper Thickness (Top / Bottom Layers) | 0.070 mm (Cu: 1 oz + plating) |
| Thermal Vias Separation / Diameter | 1.2 mm / 0.3 mm |


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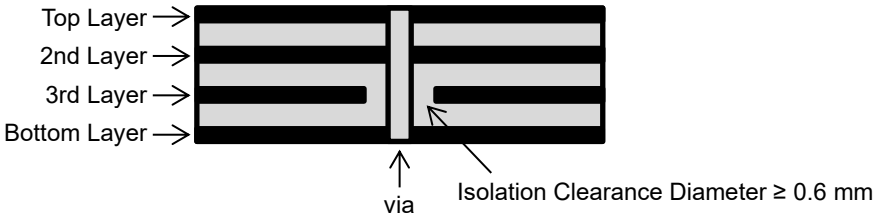
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### Thermal Resistance – continued

■ PCB Layout 4 Layers (2s2p)




Top Layer 2nd / Bottom Layer 3rd Layer




Cross Section

Figure 7. PCB Layout 4 Layers (2s2p)

| Dimension | Value |
|---|---|
| Board Finish Thickness | 1.60 mm |
| Board Dimension | 76.2 mm x 114.3 mm |
| Board Material | FR4 |
| Copper Thickness (Top / Bottom Layers) | 0.070 mm (Cu: 1 oz + plating) |
| Copper Thickness (Inner Layers) | 0.035 mm |
| Thermal Vias Separation / Diameter | 1.2 mm / 0.3 mm |


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### Thermal Resistance – continued

■ Thermal Resistance Graphs

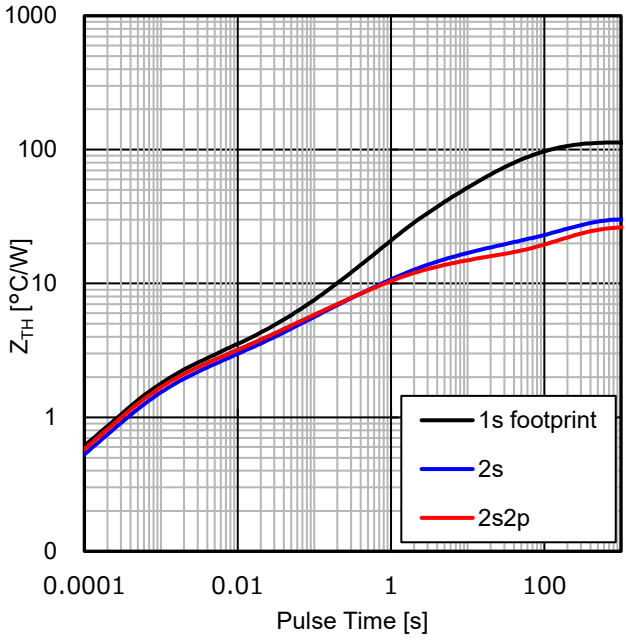



Figure 8. Transient Thermal Resistance (One Output-Channel Active)

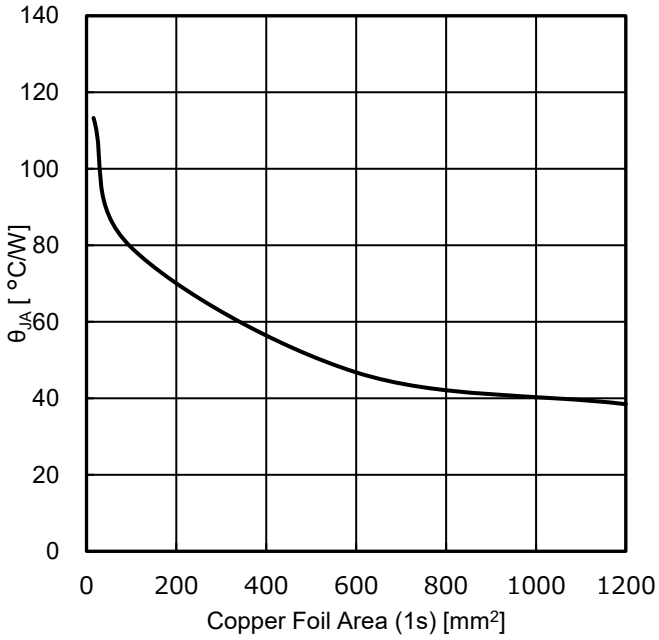



Figure 9. Thermal Resistance (One Output-Channel Active)


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## Electrical Characteristics

(Unless otherwise specified $V_{BB}$ = 6 V to 28 V, Tj = -40 °C to +150 °C, $R_{SENSE}$ = 1 kΩ)

| Parameters | Symbol | Ratings | | | Unit | Conditions |
|---|---|---|---|---|---|---|
| | | Min | Typ | Max | | |
| [Power Supply Section] | | | | | | |
| Sleep Mode Current | $I_{BBL1}$ | - | - | 0.5 | µA | $V_{BB}$ = 18 V, $V_{INx}$ = 0 V, $V_{SEN}$ = 0 V, $V_{SEL}$ = 0 V, $V_{OUTx}$ = 0 V, Tj = 25 °C |
| | $I_{BBL2}$ *(Note 1)* | - | - | 0.5 | µA | $V_{BB}$ = 18 V, $V_{INx}$ = 0 V, $V_{SEN}$ = 0 V, $V_{SEL}$ = 0 V, $V_{OUTx}$ = 0 V, Tj = 85 °C |
| | $I_{BBL3}$ | - | - | 24 | µA | $V_{BB}$ = 18 V, $V_{INx}$ = 0 V, $V_{SEN}$ = 0 V, $V_{SEL}$ = 0 V, $V_{OUTx}$ = 0 V, Tj = 150 °C |
| Standby Mode Current (Diagnostic Function ON) | $I_{GNDL}$ | - | 0.9 | 1.5 | mA | $V_{BB}$ = 18 V, $V_{INx}$ = 0 V, $V_{SEN}$ = 5 V |
| Operating Mode Current | $I_{GNDH1CH}$ | - | 3.0 | 5.0 | mA | $V_{BB}$ = 18 V, $V_{IN0}$ = 5 V, $V_{IN1}$ = 0 V |
| | $I_{GNDH2CH}$ | - | 5.0 | 8.0 | mA | $V_{BB}$ = 18 V, $V_{IN0}$ = $V_{IN1}$= 5 V |
| UVLO Threshold Voltage | $V_{UVLOH}$ | - | 4.2 | 4.8 | V | $V_{BB}$: sweep-up, $V_{INx}$ = 5 V, $V_{OUTx}$ reaches more than $V_{BB}$ - 1 V |
| | $V_{UVLOL}$ | - | 3.5 | 4.0 | V | $V_{BB}$: sweep-down, $V_{INx}$ = 5 V, $V_{OUTx}$ reaches less than 1 V |
| UVLO Hysteresis Voltage | $V_{UVHYS}$ | - | 0.7 | - | V | $V_{UVHYS}$ = $V_{UVLOH}$ - $V_{UVLOL}$ |
| $V_{BB}$ Overvoltage Protection | $V_{BBCLP}$ | 41 | 45 | 49 | V | $I_{BB}$ = 10 mA |
| [Input Section] | | | | | | |
| High Level Input Voltage | $V_{IH}$ | 2.1 | - | - | V | |
| Low Level Input Voltage | $V_{IL}$ | - | - | 0.9 | V | |
| Input Hysteresis Voltage | $V_{IHYS}$ | - | 0.25 | - | V | |
| High Level Input Current | $I_{IH}$ | 2.0 | 10.5 | 19.0 | µA | $V_{INx}$, $V_{SEN}$, $V_{SEL}$ = 2.1 V |
| Low Level Input Current | $I_{IL}$ | 1.0 | 4.5 | 8.0 | µA | $V_{INx}$, $V_{SEN}$, $V_{SEL}$ = 0.9 V |
| [Output Section] | | | | | | |
| Output ON Resistance | $R_{ON1x}$ | - | 30 | - | mΩ | $V_{BB}$ ≥ 8 V, Tj = 25 °C, $I_{OUTx}$ = 3 A |
| | $R_{ON2x}$ | - | - | 60 | mΩ | $V_{BB}$ ≥ 8 V, Tj = 150 °C, $I_{OUTx}$ = 1.5 A |
| | $R_{ON3x}$ | - | - | 60 | mΩ | $V_{BB}$ = 5 V, Tj = 25 °C, $I_{OUTx}$ = 3 A |
| Output Leakage Current per Channel | $I_{OUTL1}$ | - | - | 0.5 | µA | $V_{BB}$ = 18 V, $V_{INx}$ = 0 V, $V_{SEN}$ = 0 V, $V_{OUTx}$ = 0 V, Tj = 25 °C |
| | $I_{OUTL2}$ *(Note 1)* | - | - | 0.5 | µA | $V_{BB}$ = 18 V, $V_{INx}$ = 0 V, $V_{SEN}$ = 0 V, $V_{OUTx}$ = 0 V, Tj = 85 °C |
| | $I_{OUTL3}$ | - | - | 12 | µA | $V_{BB}$ = 18 V, $V_{INx}$ = 0 V, $V_{SEN}$ = 0 V, $V_{OUTx}$ = 0 V, Tj = 150 °C |
| $V_{DS}$ Voltage at Light Load *(Note 1)* | $V_{DSSL}$ | - | 13 | - | mV | $V_{INx}$ = 5 V, $I_{OUTx}$ = 100 mA |
| Output Slew Rate when ON | $SR_{ON}$ | - | 0.35 | 0.70 | V/µs | $V_{BB}$ = 14 V, $R_{Lx}$ = 6 Ω, Tj = 25 °C, $V_{OUTx}$ = 30 % to 70 % of $V_{BB}$ |
| Output Slew Rate when OFF | - $SR_{OFF}$ | - | 0.35 | 0.70 | V/µs | $V_{BB}$ = 14 V, $R_{Lx}$ = 6 Ω, Tj = 25 °C, $V_{OUTx}$ = 70 % to 30 % of $V_{BB}$ |
| Output Slew Rate Matching | ΔSR | -0.15 | - | +0.15 | V/µs | $V_{BB}$ = 14 V, $R_{Lx}$ = 6 Ω, Tj = 25 °C |
| Output Propagation Time Delay when Turning ON | $t_{OD_ON}$ | - | 70 | 140 | µs | $V_{BB}$ = 14 V, $R_{Lx}$ = 6 Ω, Tj = 25 °C, $V_{OUTx}$ rises to 20 % of $V_{BB}$ |
| Output Propagation Time Delay when Turning OFF | $t_{OD_OFF}$ | - | 50 | 100 | µs | $V_{BB}$ = 14 V, $R_{Lx}$ = 6 Ω, Tj = 25 °C, $V_{OUTx}$ drops to 80 % of $V_{BB}$ |
| Switch ON Time | $t_{ON}$ | - | 90 | - | µs | $V_{BB}$ = 14 V, $R_{Lx}$ = 6 Ω, Tj = 25 °C $V_{OUTx}$ rises to 80 % of $V_{BB}$ |
| Switch OFF Time | $t_{OFF}$ | - | 90 | - | µs | $V_{BB}$ = 14 V, $R_{Lx}$ = 6 Ω, Tj = 25 °C $V_{OUTx}$ drops to 20 % of $V_{BB}$ |
| Differential Pulse Skew | $t_{SKEW}$ | -60 | - | +40 | µs | $V_{BB}$ = 14 V, $R_{Lx}$ = 6 Ω, Tj = 25 °C |
| Switch ON Energy | $E_{ON}$ | - | 0.25 | - | mJ | $V_{BB}$ = 14 V, $R_{Lx}$ = 6 Ω, Tj = 25 °C |
| Switch OFF Energy | $E_{OFF}$ | - | 0.25 | - | mJ | $V_{BB}$ = 14 V, $R_{Lx}$ = 6 Ω, Tj = 25 °C |
| Reverse Current *(Note 1)* | $I_{REVC}$ | - | -4 | - | A | $V_{INx}$ = 5 V, Tj = 25 °C |
| Body Diode Voltage | $V_{DSDI}$ | - | 0.5 | 0.7 | V | $I_{OUTx}$ = -1.5 A, Tj = 150 °C |

*(Note 1)* Specified by design and/or statistical analysis of correlated parameters tested in production.


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**Electrical Characteristics – continued**
(Unless otherwise specified $V_{BB}$ = 6 V to 28 V, Tj = -40 °C to +150 °C, $R_{SENSE}$ = 1 kΩ)

| Parameters | Symbol | Ratings | | | Unit | Conditions |
|---|---|---|---|---|---|---|
| | | Min | Typ | Max | | |
| [Output Protection Section] | | | | | | |
| $V_{DS}$ Active Clamping Voltage | $V_{DSCLP}$ | 41 | 45 | 49 | V | $I_{OUTx}$ = 10 mA |
| Overcurrent Detection Value *(Note 1,2)* | $I_{OCD_6V_-40}$ | 32 | 43 | 54 | A | $V_{DSx}$ = 6 V, Tj = -40 °C |
| | $I_{OCD_6V_25}$ | 34 | 45 | 56 | A | $V_{DSx}$ = 6 V, Tj = 25 °C |
| | $I_{OCD_6V_150}$ | - | 37 | - | A | $V_{DSx}$ = 6 V, Tj = 150 °C |
| | $I_{OCD_6V_TSD}$ | - | 23 | - | A | $V_{DSx}$ = 6 V, thermal toggling, Tj ≥ $T_{TSD}$ |
| | $I_{OCD_28V}$ | - | 23 | - | A | $V_{DSx}$ = 28 V, or $V_{BB}$ ≥ $V_{BB_JS}$ |
| Supply Voltage Threshold for Overcurrent Reduction *(Note 1,2)* | $V_{BB_JS}$ | - | 19.5 | - | V | Jump Start Condition |
| Temperature Shutdown Detection Threshold *(Note 1,2)* | $T_{TSD}$ | 150 | 175 | 200 | °C | |
| Temperature Shutdown Detection Hysteresis *(Note 1)* | $T_{TSDHYS}$ | - | 15 | - | °C | |
| Dynamic Temperature Protection Threshold *(Note 1,2)* | $T_{DTj}$ | - | 65 | - | K | Differential temperature |
| [Diagnostic / SENSE Section] | | | | | | |
| Open Load at OFF $V_{DS}$ Detect | $V_{DSOL}$ | 1.5 | 2.2 | 2.9 | V | $V_{INx}$ = 0 V, $V_{SEN}$ = 5 V |
| Output Pull Down Resistor | $R_{PD}$ | - | 200 | - | kΩ | |
| SENSE Leakage Current | $I_{SENSEL}$ | - | - | 0.5 | µA | $V_{INx}$ = 5 V, $V_{SEN}$ = 0 V, $V_{SENSE}$ = -1 V to +5 V |
| | $I_{SENSELD}$ | - | - | 1.0 | µA | $V_{BB}$ = 18 V, $V_{INx}$ = 5 V, $V_{SEN}$ = 5 V, $V_{SENSE}$ = 0 V, $V_{SEL}$ = 0 V, $I_{OUT0}$ = 0 A, $I_{OUT1}$ = 3 A |
| Diagnostic Error Flag Current | $I_{SENSEH}$ | 6 | 18 | 30 | mA | $V_{BB}$ ≥ 8 V, $V_{SENSE}$ = 0 V |
| Diagnostic Error Flag Voltage | $V_{SENSEH1}$ | 4.7 | 5.4 | 5.8 | V | $V_{BB}$ ≥ 8 V, $R_{SENSE}$ = 1 kΩ |
| | $V_{SENSEH2}$ | 5.0 | 5.4 | 5.8 | V | $V_{BB}$ ≥ 10 V, $R_{SENSE}$ = 1 kΩ |
| SENSE Output Delay Time when the Device Turns ON | $t_{DS_ON}$ | - | 90 | 190 | µs | $R_{Lx}$ = 6 Ω, $V_{SEN}$ = $V_{INx}$ = 0 V to 5 V |
| SENSE Output Delay Time when Diagnostic Turns ON | $t_{DS_DON}$ | - | 15 | 50 | µs | $R_{Lx}$ = 6 Ω, $V_{INx}$ = 5 V, $V_{SEN}$ = 0 V to 5 V |
| SENSE Output Delay Time when Diagnostic Turns OFF | $t_{DS_DOFF}$ | - | 5 | 30 | µs | $R_{Lx}$ = 6 Ω, $V_{INx}$ = 5 V, $V_{SEN}$ = 5 V to 0 V |
| SENSE Settling Time during Load Current Changing | $t_{DS_CHG_H}$ | - | - | 20 | µs | $V_{INx}$ = $V_{SEN}$ = 5 V, $I_{OUTx}$ = 3 A to 5 A |
| | $t_{DS_CHG_L}$ | - | - | 1000 | µs | $V_{INx}$ = $V_{SEN}$ = 5 V, $I_{OUTx}$ = 3 A to 0.1 A |
| SENSE Settling Time during Channel Change | $t_{DS_CH_CHG_LH}$ | - | - | 50 | µs | $V_{INx}$ = $V_{SEN}$ = 5 V, $V_{SEL}$ = 0 V to 5 V, $I_{OUT0}$ = 0.1 A, $I_{OUT1}$ = 3 A |
| | $t_{DS_CH_CHG_HL}$ | - | - | 100 | µs | $V_{INx}$ = $V_{SEN}$ = 5 V, $V_{SEL}$ = 5 V to 0 V, $I_{OUT0}$ = 0.1 A, $I_{OUT1}$ = 3 A |
| | $t_{DS_CH_CHG_HT}$ | - | - | 50 | µs | $V_{INx}$ = $V_{SEN}$ = 5 V, $V_{SEL}$ = 0 V to 5 V, $I_{OUT0}$ = 5 A, $I_{OUT1}$ = 3 A |
| Open Load at OFF Detection Mask Time *(Note 1,2)* | $t_{OLDMSK}$ | - | 300 | - | µs | $V_{DSx}$ = 0 V, $V_{SEN}$ = 5 V, $V_{INx}$ = 5 V to 0 V |
| Error Flag Release Time *(Note 1,2)* | $t_{ERRFD}$ | - | 600 | 1000 | µs | $V_{INx}$ = $V_{SEN}$ = 5 V, fault is removed |

*(Note 1)* Specified by design and/or statistical analysis of correlated parameters tested in production.
*(Note 2)* Functional test only.


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**Electrical Characteristics – continued**

(Unless otherwise specified $V_{BB}$ = 6 V to 28 V, Tj = -40 °C to +150 °C, $R_{SENSE}$ = 1 kΩ)

| Parameters | Symbol | Ratings | | | Unit | Conditions |
|---|---|---|---|---|---|---|
| | | Min | Typ | Max | | |
| Current Sense Ratio 1 | $K_1$ | -50 % | 1700 | +50 % | - | $V_{BB}$ = 14 V, $I_{OUTx}$ = 0.1 A, $V_{INx}$ = $V_{SEN}$ = 5 V |
| Current Sense Ratio 2 | $K_2$ | -30 % | 1620 | +30 % | - | $V_{BB}$ = 14 V, $I_{OUTx}$ = 0.25 A, $V_{INx}$ = $V_{SEN}$ = 5 V |
| Current Sense Ratio 3 | $K_3$ | -20 % | 1620 | +20 % | - | $V_{BB}$ = 14 V, $I_{OUTx}$ = 0.5 A, $V_{INx}$ = $V_{SEN}$ = 5 V |
| Current Sense Ratio 4 | $K_4$ | -10 % | 1620 | +10 % | - | $V_{BB}$ = 14 V, $I_{OUTx}$ = 1.5 A, $V_{INx}$ = $V_{SEN}$ = 5V |
| Current Sense Ratio 5 | $K_5$ | -7 % | 1620 | +7 % | - | $V_{BB}$ = 14 V, $I_{OUTx}$ = 3 A, $V_{INx}$ = $V_{SEN}$ = 5 V |
| Current Sense Ratio 6 | $K_6$ | -5 % | 1620 | +5 % | - | $V_{BB}$ = 14 V, $I_{OUTx}$ = 5 A, $V_{INx}$ = $V_{SEN}$ = 5 V |
| Current Sense Derating *(Note 1)* | $\Delta K_1$ | -30 | - | +30 | % | $K_1$ vs $K_2$, Tj = 25 °C |
| | $\Delta K_2$ | -5 | - | +5 | % | $K_5$ vs $K_6$, Tj = 25 °C |
| Output Load Open Detection ON | $I_{OUT_ONOLD}$ | 7 | 17 | 35 | mA | $I_{SENSE}$ = 10 µA = (17 mA / 1700) |

*(Note 1)* Specified by design and/or statistical analysis of correlated parameters tested in production.


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### Typical Performance Curves

(Unless otherwise specified $V_{BB}$ = 14 V, Tj = 25 °C)

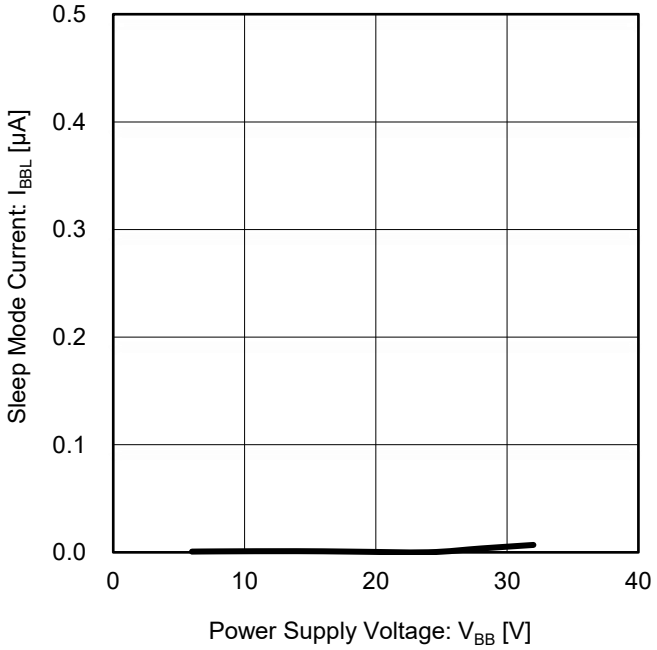



Figure 10. Sleep Mode Current vs Power Supply Voltage

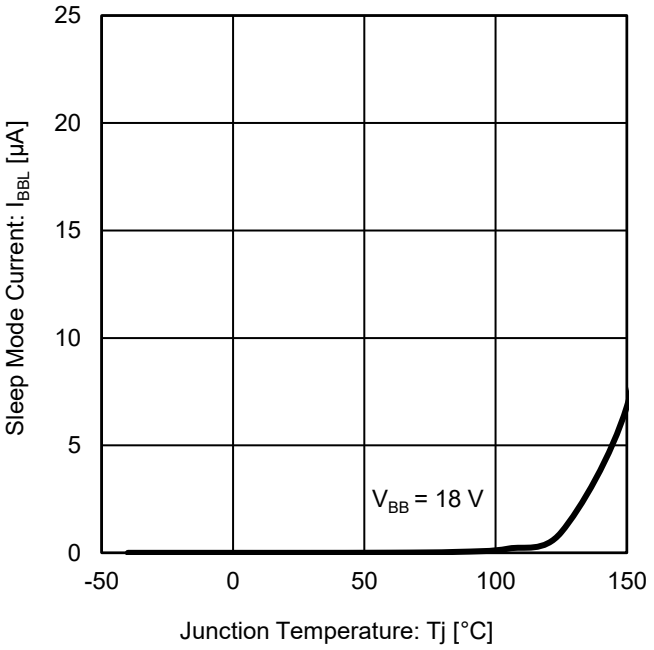



Figure 11. Sleep Mode Current vs Junction Temperature

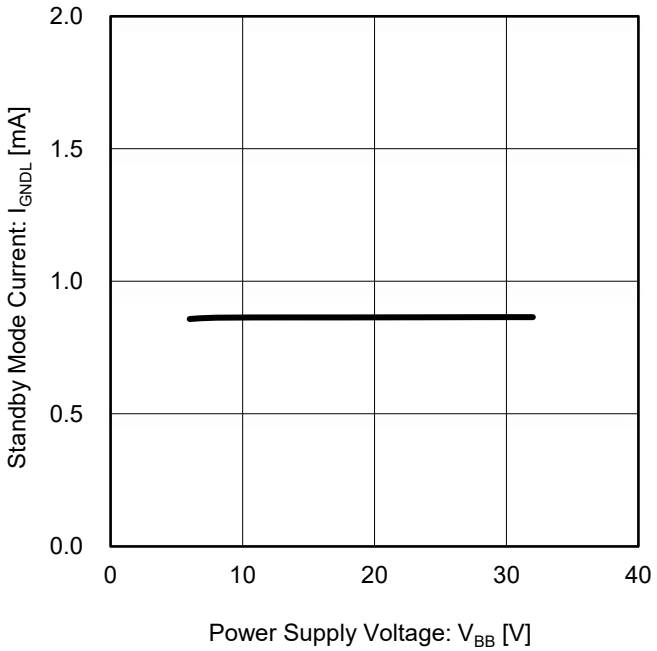



Figure 12. Standby Mode Current vs Power Supply Voltage

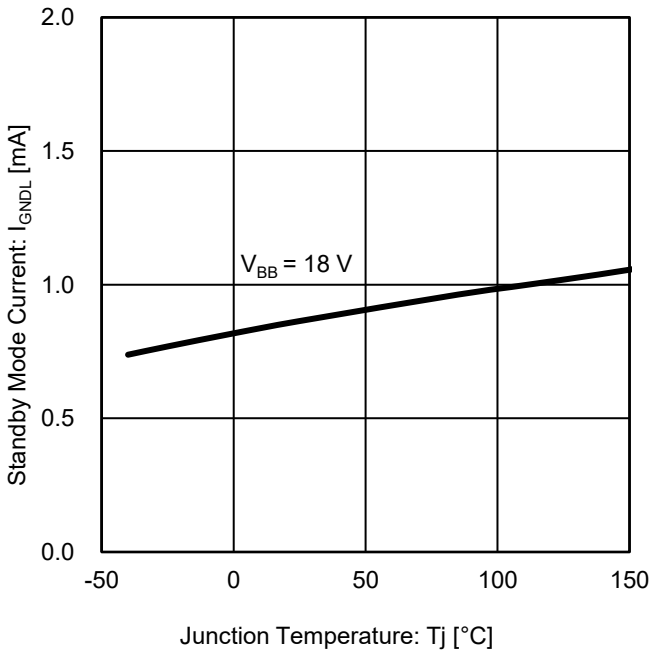



Figure 13. Standby Mode Current vs Junction Temperature


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**Typical Performance Curves – continued**
(Unless otherwise specified $V_{BB}$ = 14 V, Tj = 25 °C)

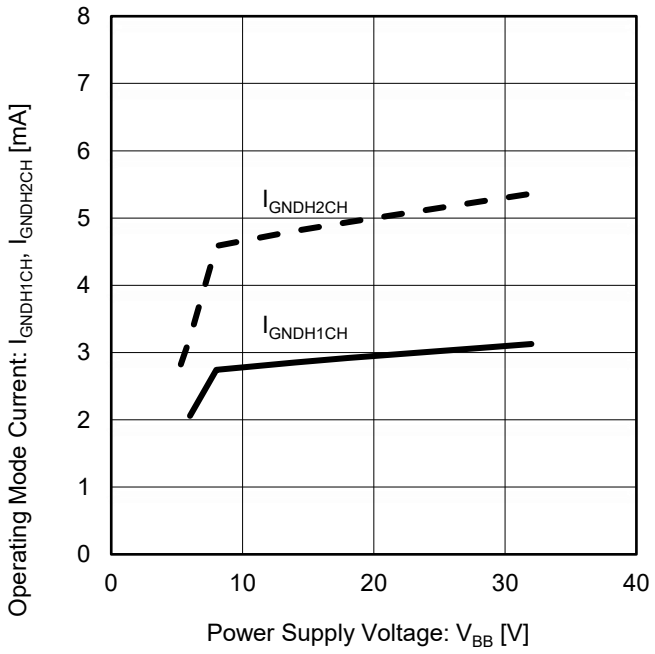



Figure 14. Operating Mode Current vs Power Supply Voltage

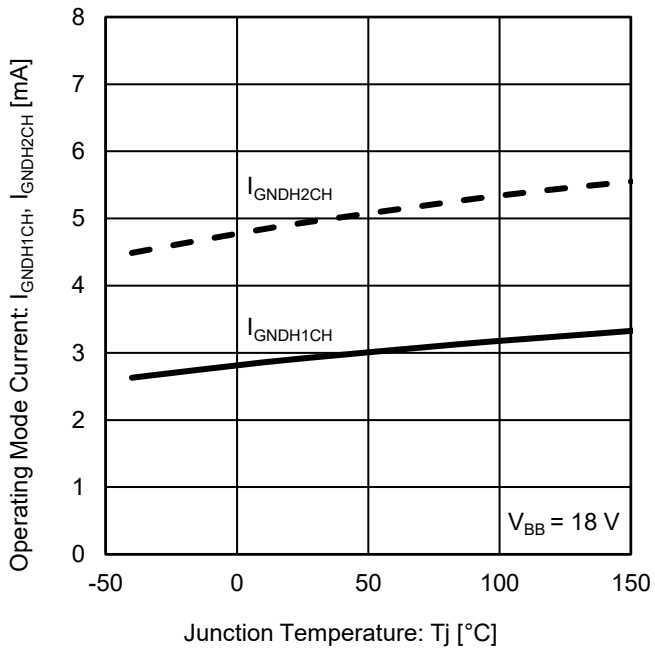



Figure 15. Operating Mode Current vs Junction Temperature

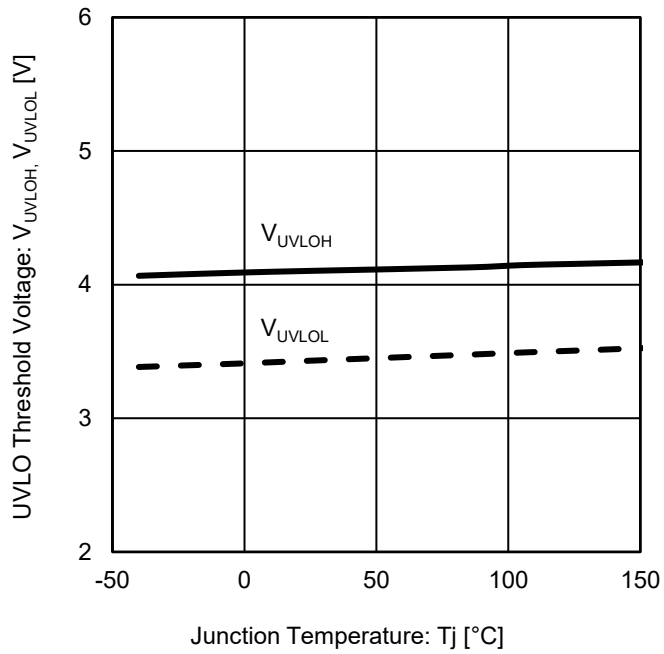



Figure 16. UVLO Threshold Voltage vs Junction Temperature

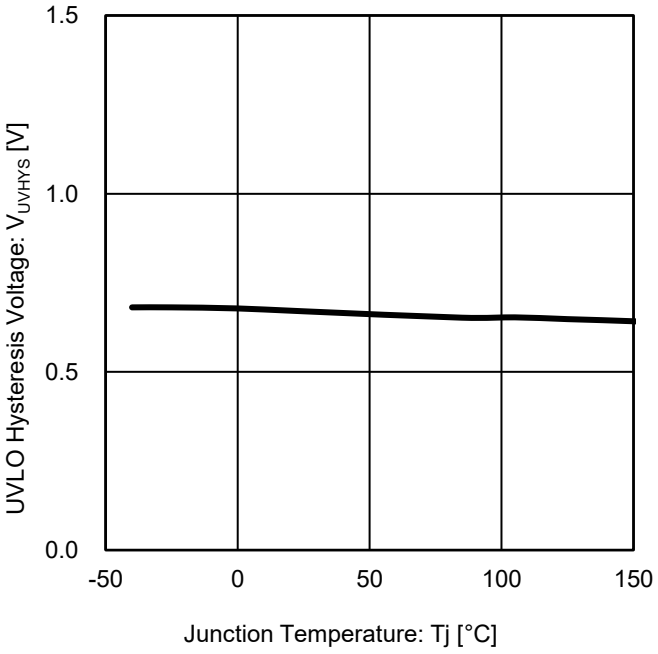



Figure 17. UVLO Hysteresis Voltage vs Junction Temperature


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**Typical Performance Curves – continued**
(Unless otherwise specified $V_{BB}$ = 14 V, Tj = 25 °C)

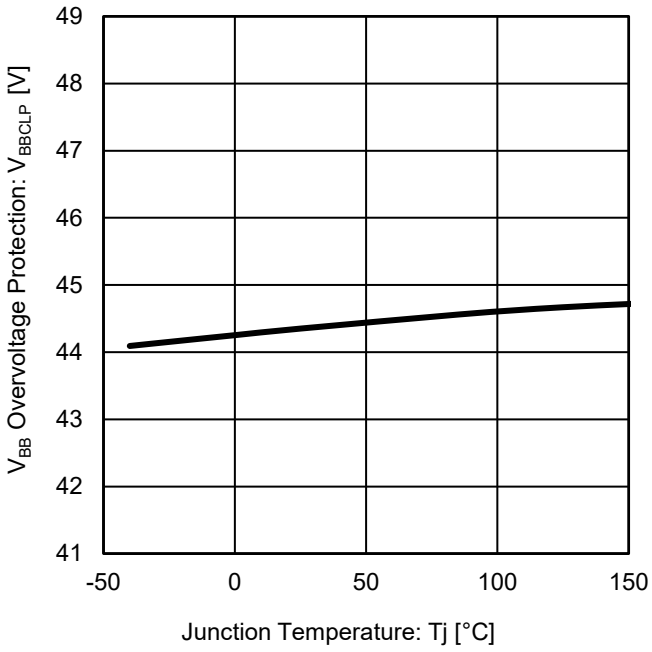



Figure 18. $V_{BB}$ Overvoltage Protection vs Junction Temperature

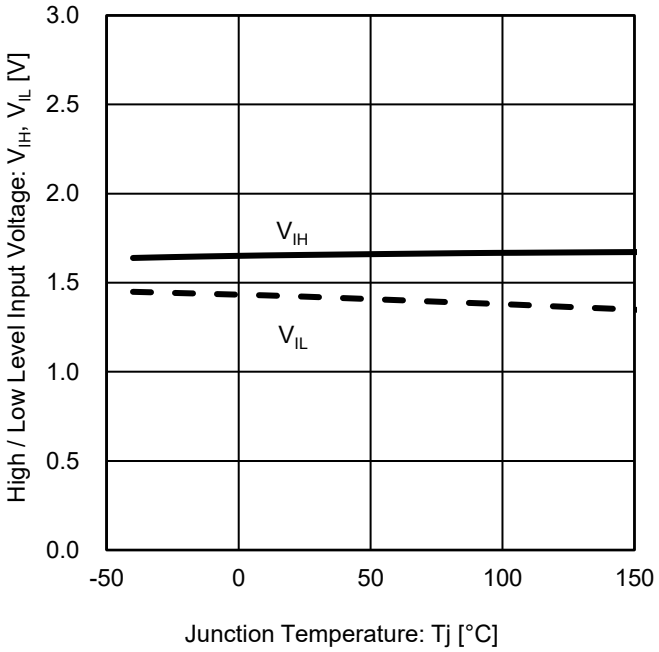



Figure 19. High / Low Level Input Voltage vs Junction Temperature

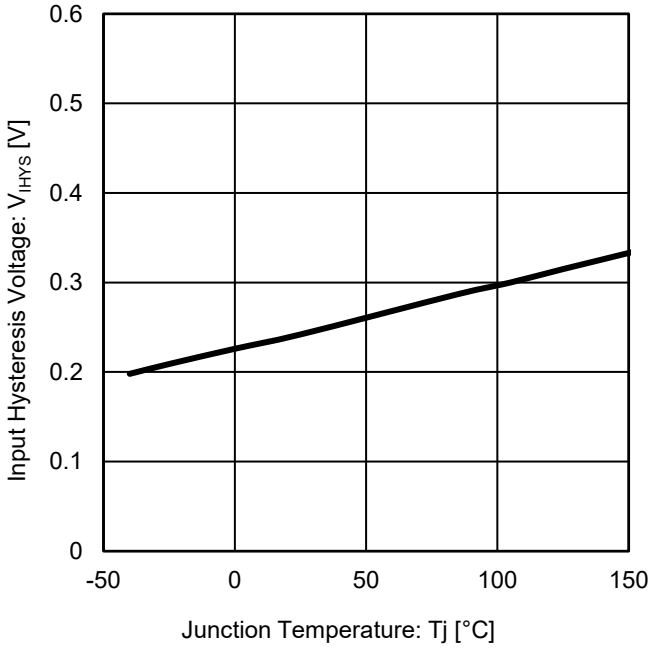



Figure 20. Input Hysteresis Voltage vs Junction Temperature

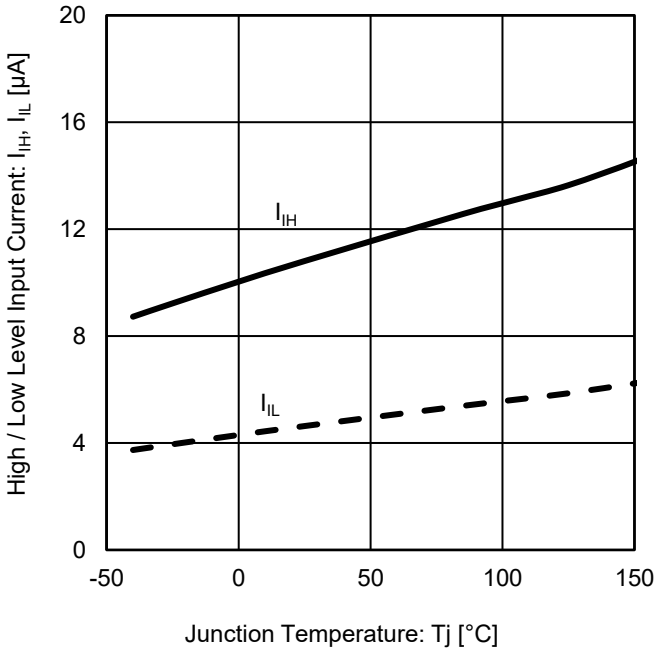



Figure 21. High / Low Level Input Current vs Junction Temperature


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**Typical Performance Curves – continued**
(Unless otherwise specified $V_{BB}$ = 14 V, Tj = 25 °C)

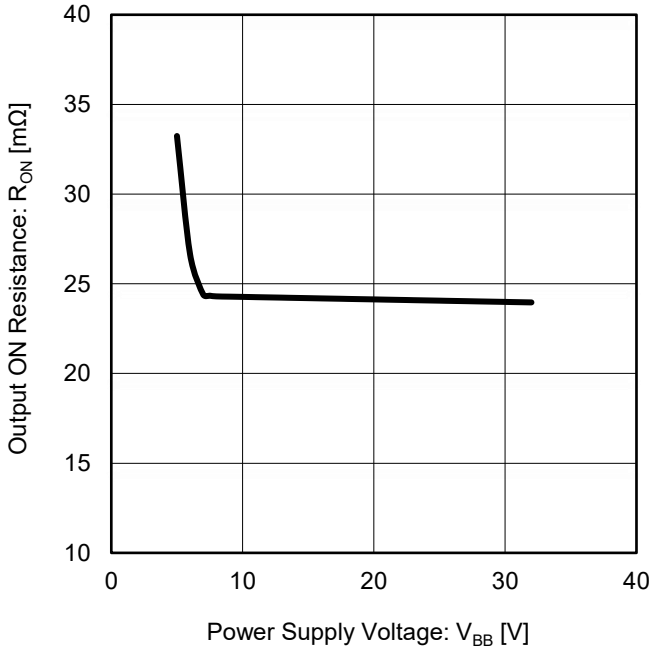



Figure 22. Output ON Resistance vs Power Supply Voltage

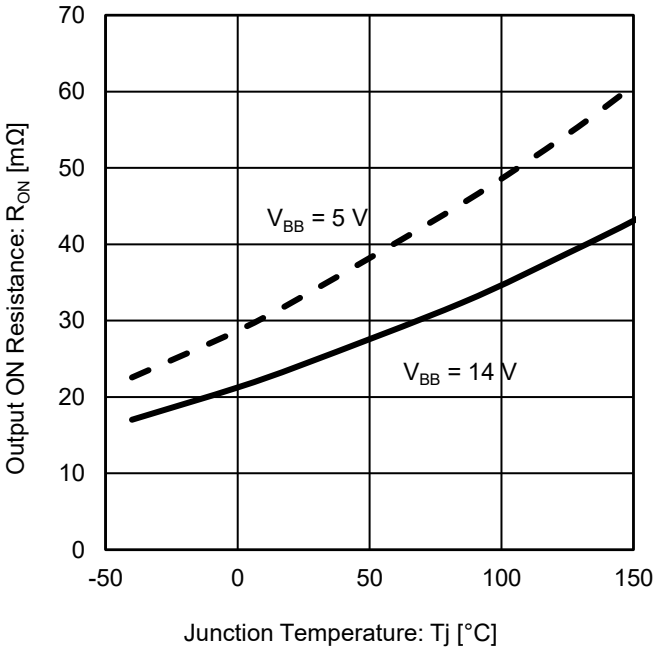



Figure 23. Output ON Resistance vs Junction Temperature

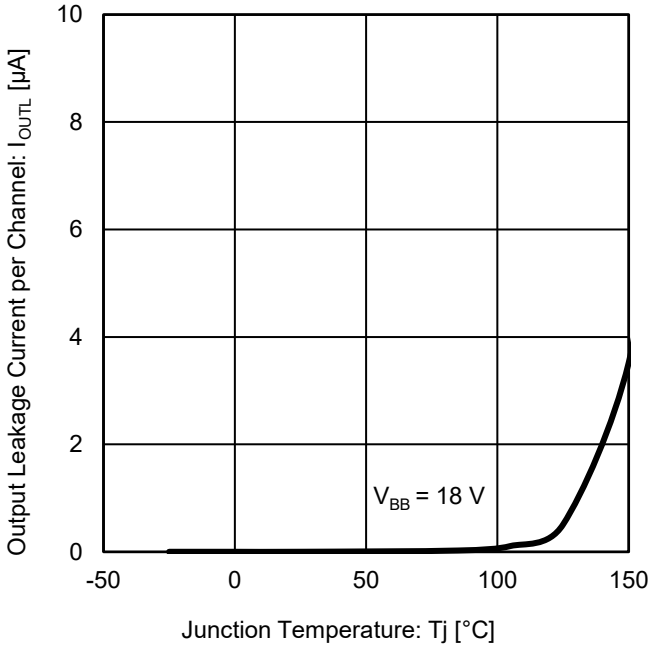



Figure 24. Output Leakage Current per Channel vs Junction Temperature

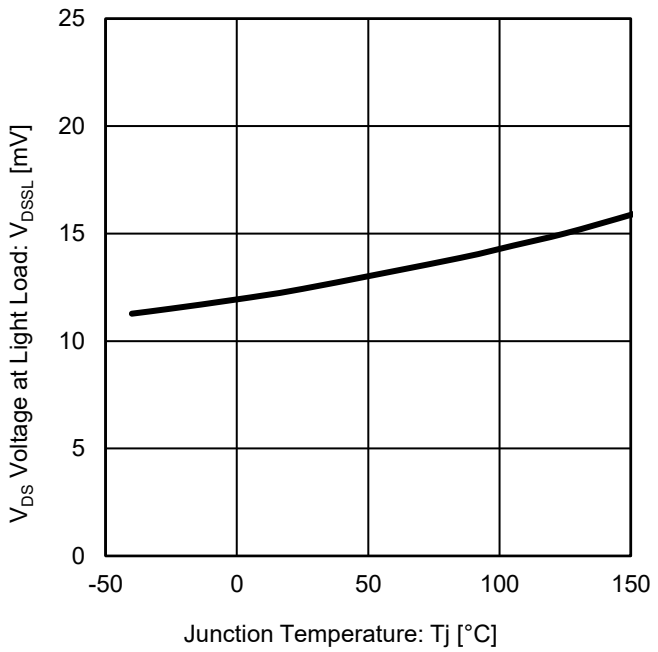



Figure 25. $V_{DS}$ Voltage at Light Load vs Junction Temperature


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**Typical Performance Curves – continued**
(Unless otherwise specified $V_{BB}$ = 14 V, Tj = 25 °C)

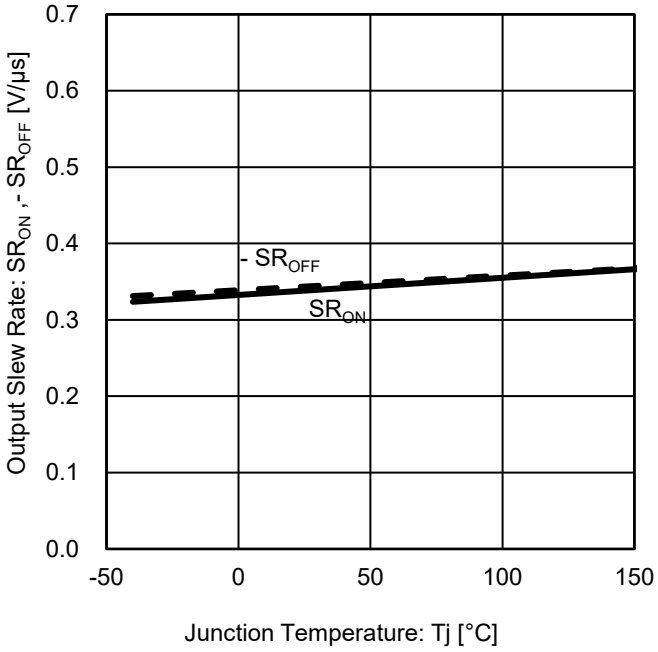



Figure 26. Output Slew Rate vs Junction Temperature

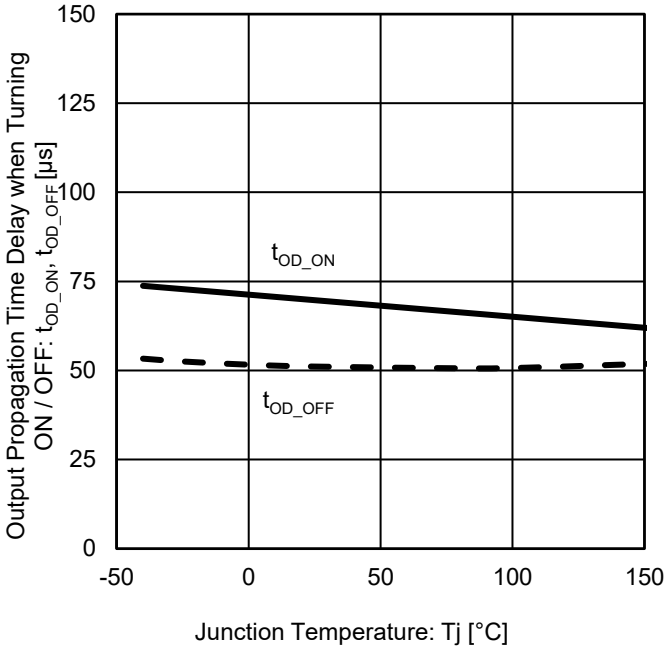



Figure 27. Output Propagation Time Delay when Turning ON / OFF vs Junction Temperature

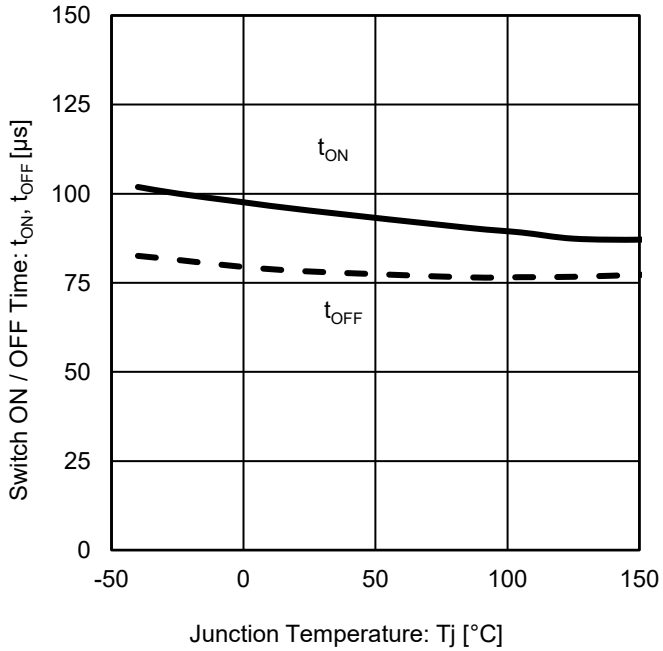



Figure 28. Switch ON / OFF Time vs Junction Temperature

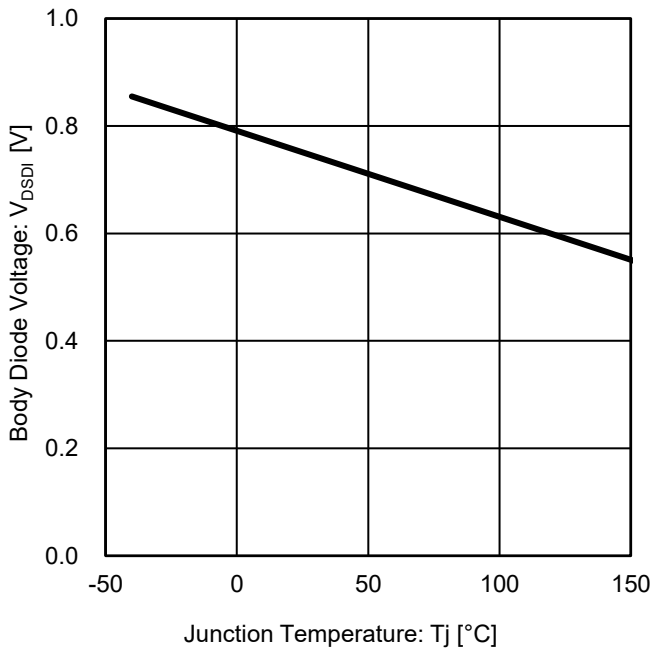



Figure 29. Body Diode Voltage vs Junction Temperature


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**Typical Performance Curves – continued**
(Unless otherwise specified $V_{BB}$ = 14 V, Tj = 25 °C)

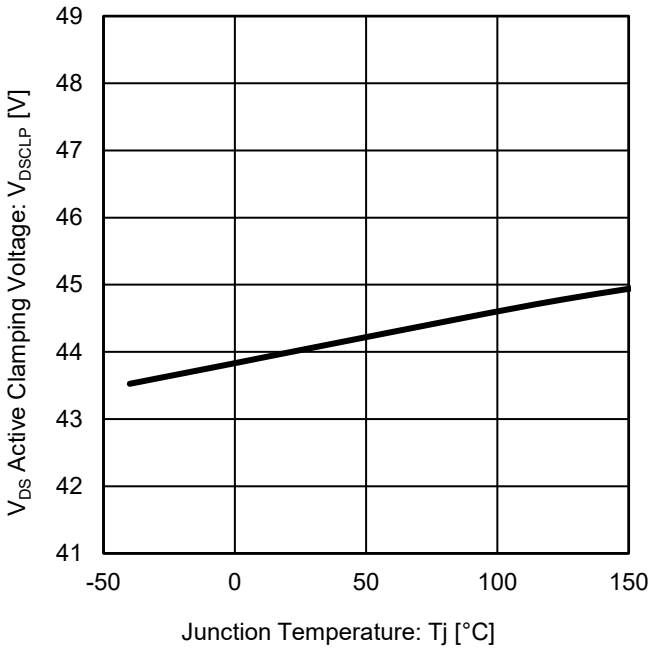



Figure 30. $V_{DS}$ Active Clamping Voltage vs Junction Temperature

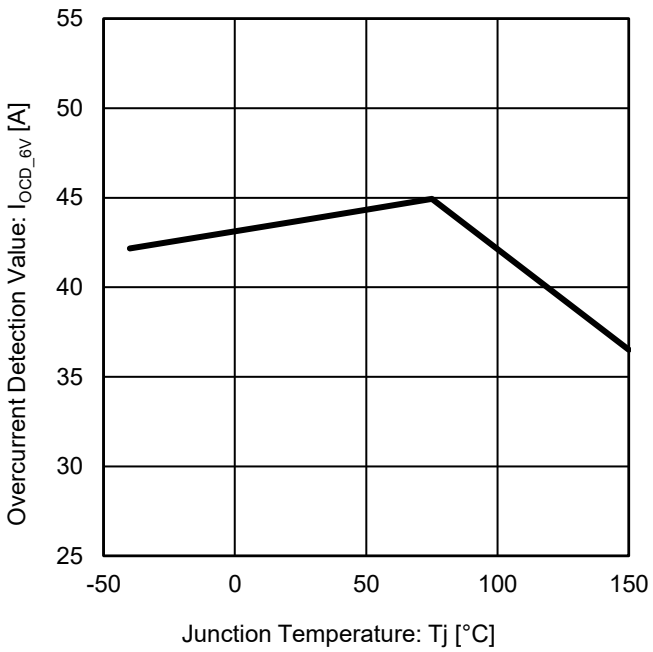



Figure 31. Overcurrent Detection Value vs Junction Temperature

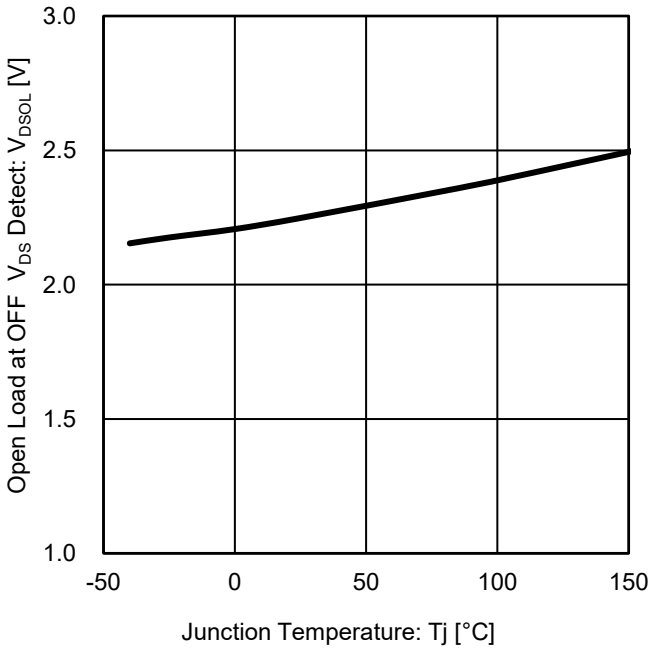



Figure 32. Open Load at OFF $V_{DS}$ Detect vs Junction Temperature

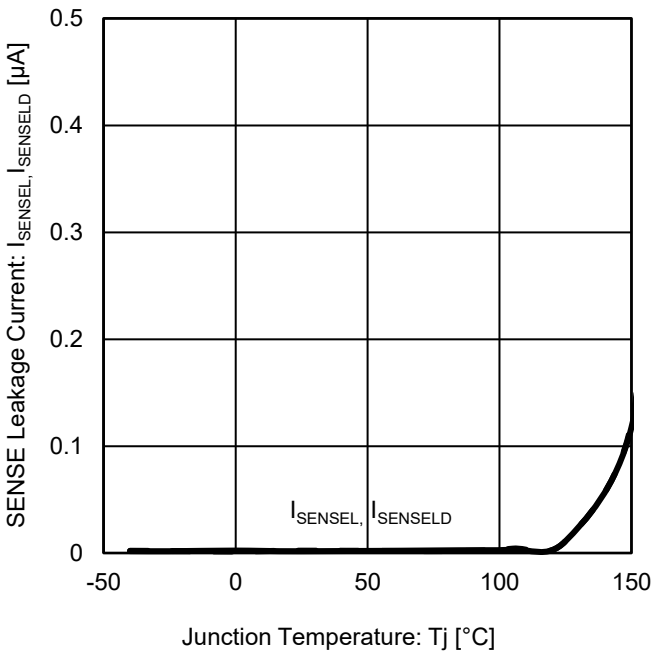



Figure 33. SENSE Leakage Current vs Junction Temperature


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**Typical Performance Curves – continued**
(Unless otherwise specified $V_{BB}$ = 14 V, Tj = 25 °C)

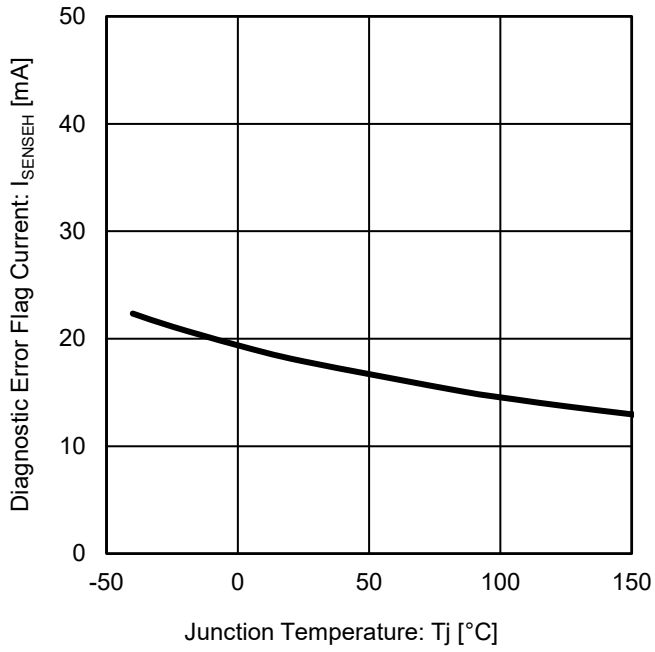



Figure 34. Diagnostic Error Flag Current vs Junction Temperature

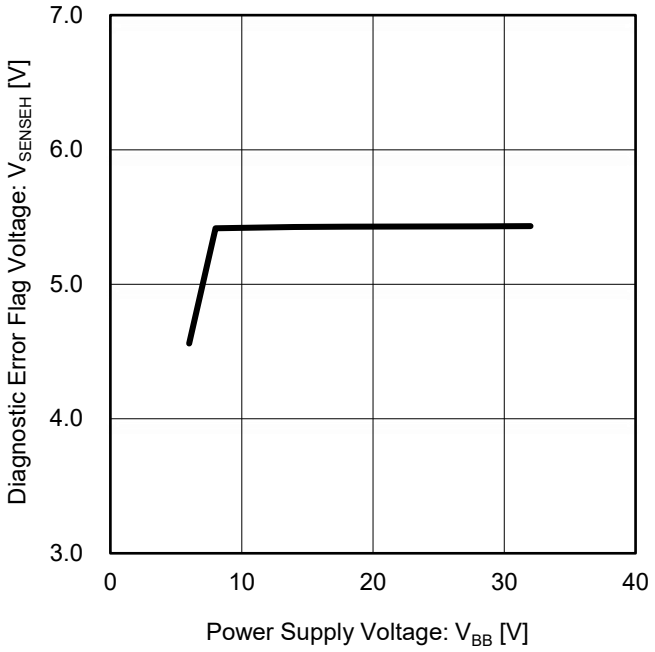



Figure 35. Diagnostic Error Flag Voltage vs Power Supply Voltage

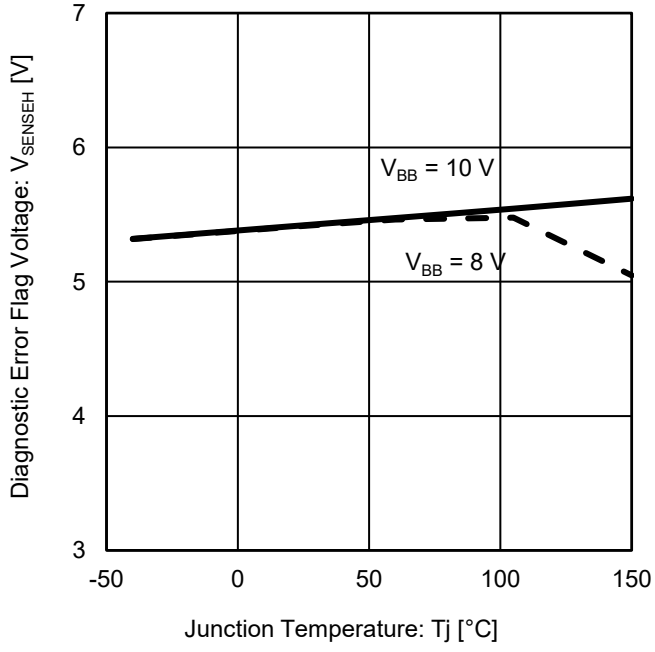



Figure 36. Diagnostic Error Flag Voltage vs Junction Temperature

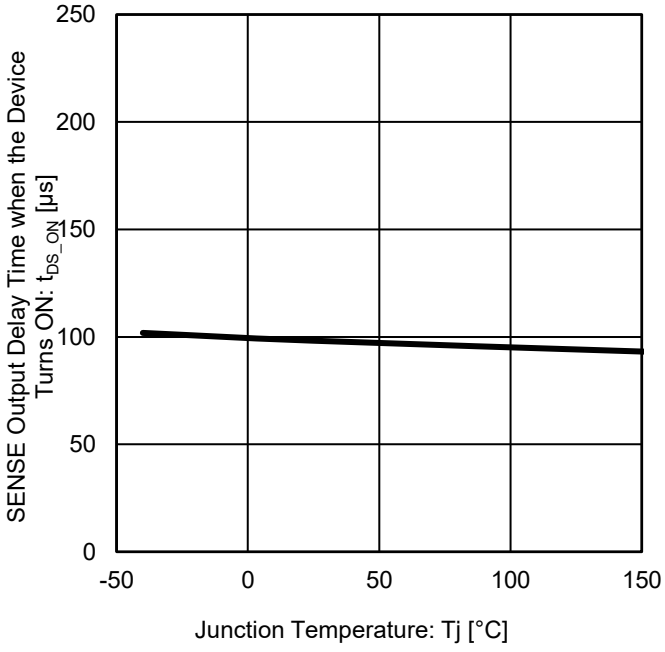



Figure 37. SENSE Output Delay Time when the Device Turns ON vs Junction Temperature


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**Typical Performance Curves – continued**
(Unless otherwise specified $V_{BB}$ = 14 V, Tj = 25 °C)

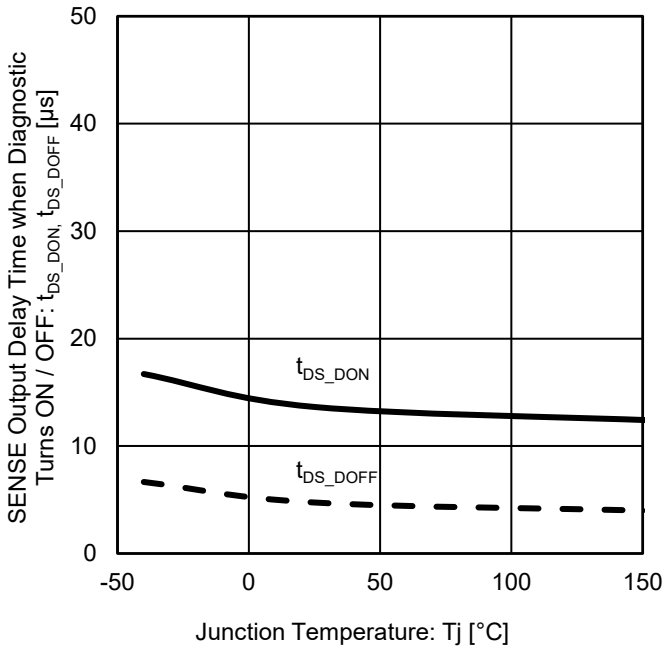



Figure 38. SENSE Output Delay Time when Diagnostic Turns ON / OFF vs Junction Temperature

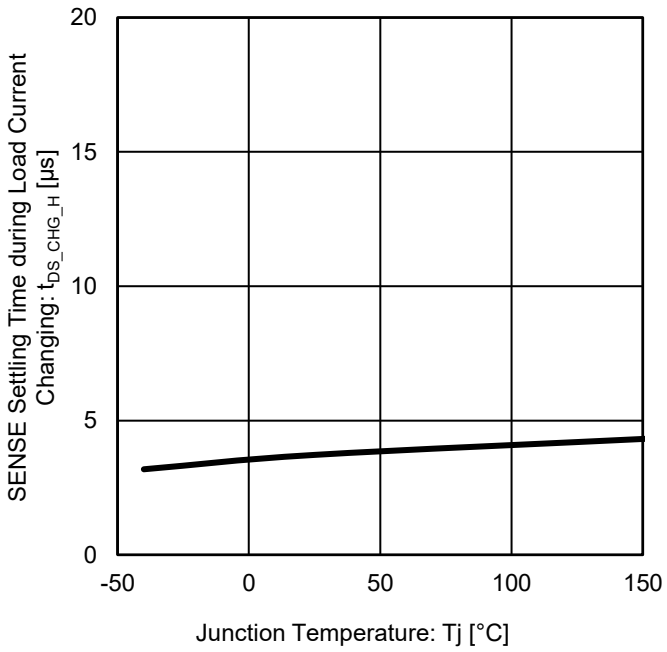



Figure 39. SENSE Settling Time during Load Current Changing vs Junction Temperature

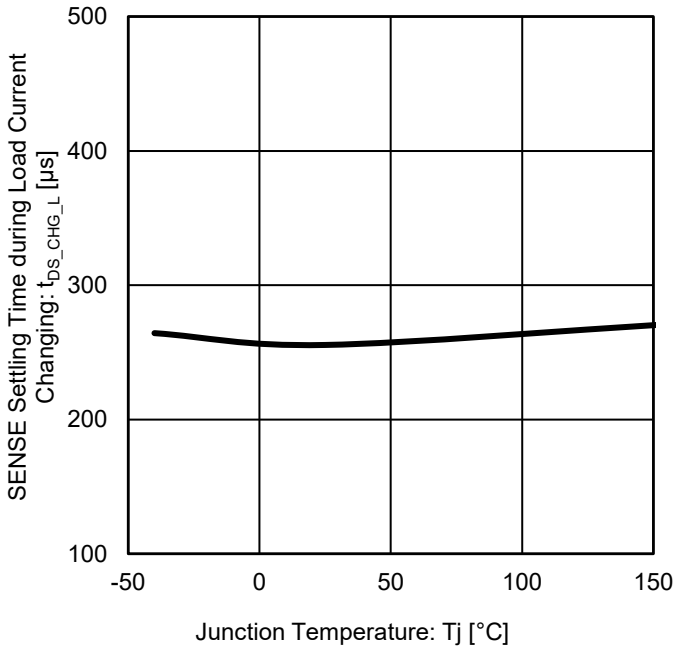



Figure 40. SENSE Settling Time during Load Current Changing vs Junction Temperature

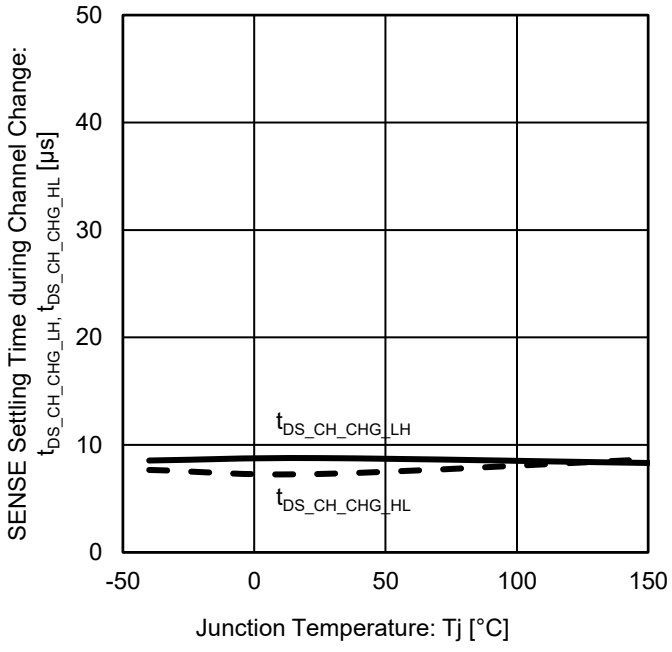



Figure 41. SENSE Settling Time during Channel Change vs Junction Temperature


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**Typical Performance Curves – continued**
(Unless otherwise specified $V_{BB}$ = 14 V, Tj = 25 °C)

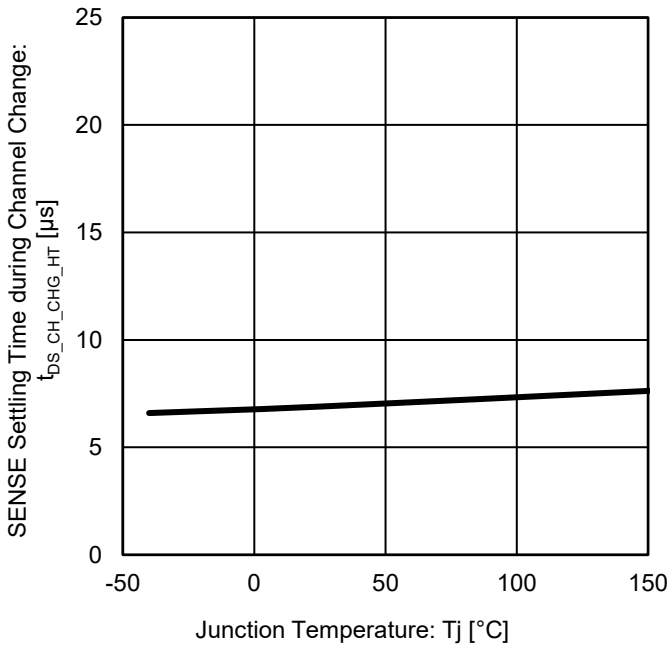



Figure 42. SENSE Settling Time during Channel Change vs Junction Temperature

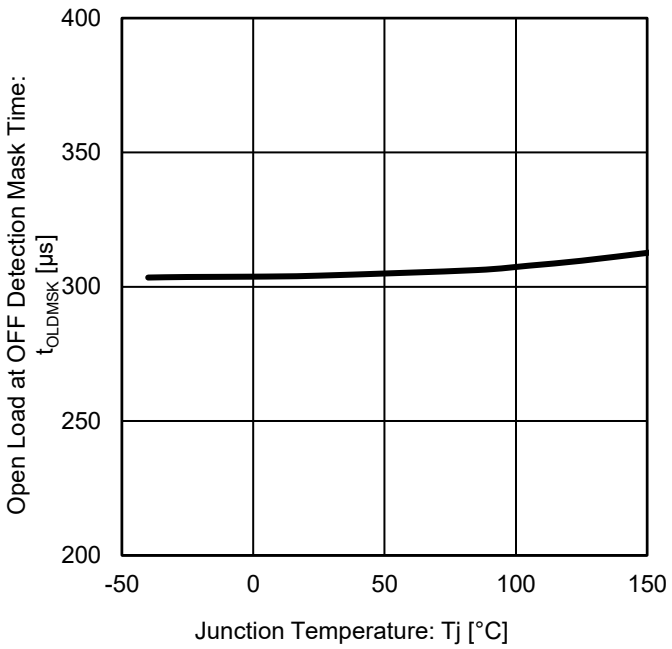



Figure 43. Open Load at OFF Detection Mask Time vs Junction Temperature

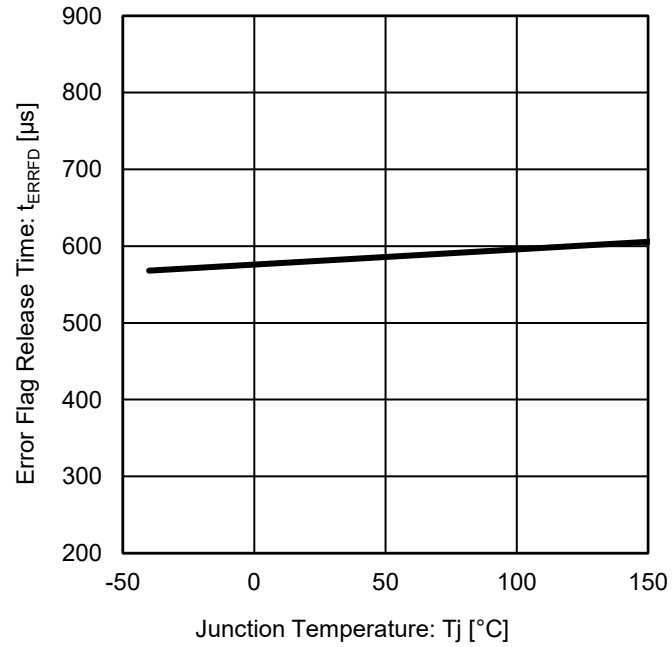



Figure 44. Error Flag Release Time vs Junction Temperature

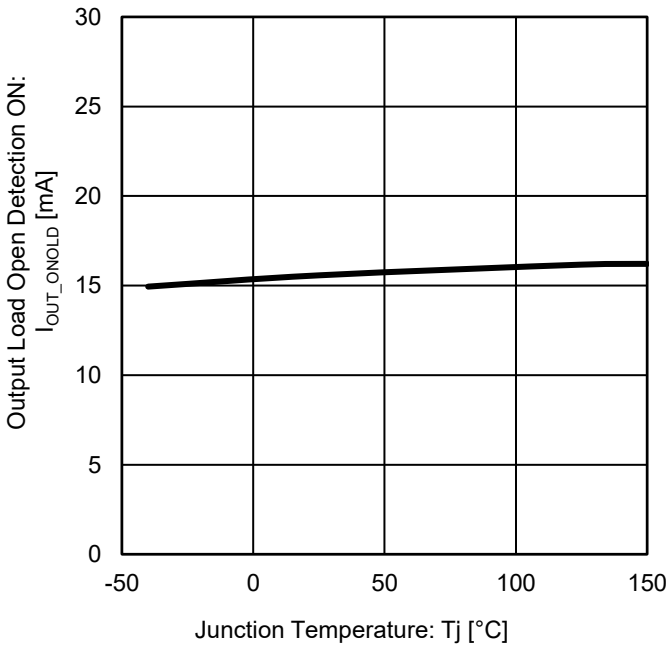



Figure 45. Output Load Open Detection ON vs Junction Temperature


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## Measurement Circuit Diagram

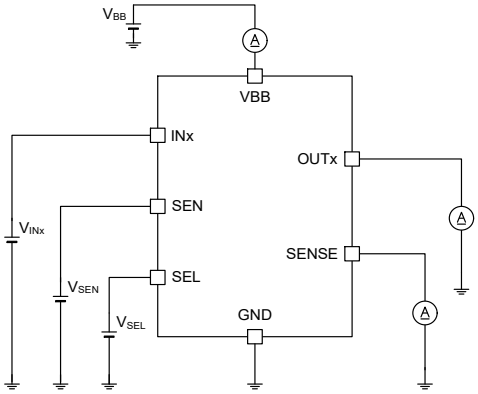



Figure 46. Sleep Mode Current
Output Leakage Current per Channel
SENSE Leakage Current

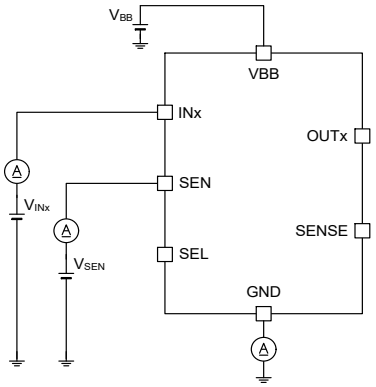



Figure 47. Standby Mode Current
Operating Mode Current

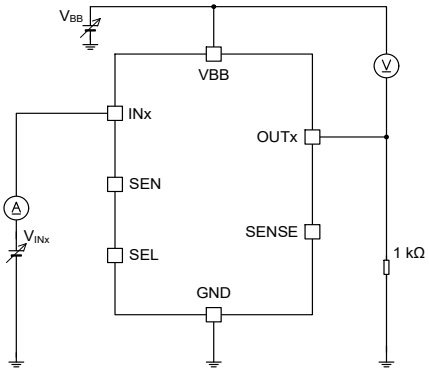



Figure 48. UVLO Threshold / Hysteresis Voltage
High / Low Level Input Voltage (IN)
Input Hysteresis Voltage (IN)
High / Low Level Input Current (IN)

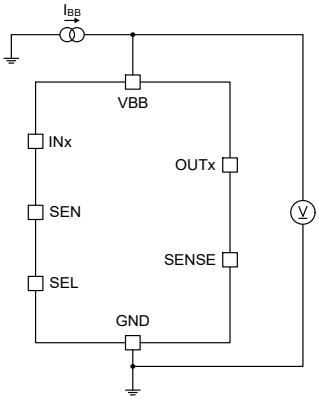



Figure 49. $V_{BB}$ Overvoltage Protection

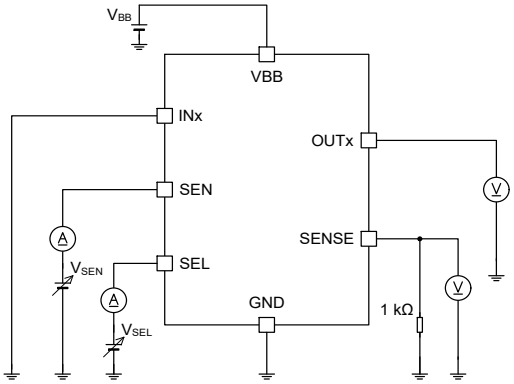



Figure 50. High / Low Level Input Voltage (SEN, SEL)
Input Hysteresis Voltage (SEN, SEL)
High / Low Level Input Current (SEN, SEL)

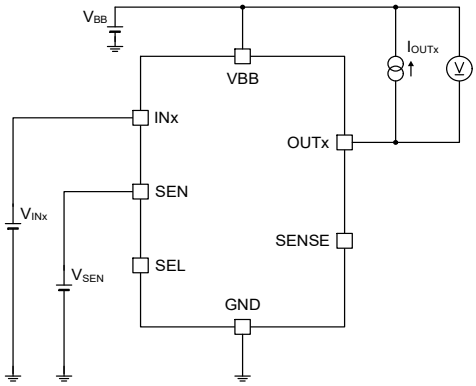



Figure 51. Output ON Resistance
$V_{DS}$ Voltage at Light Load
Body Diode Voltage
$V_{DS}$ Active Clamping Voltage


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## Measurement Circuit Diagram – continued

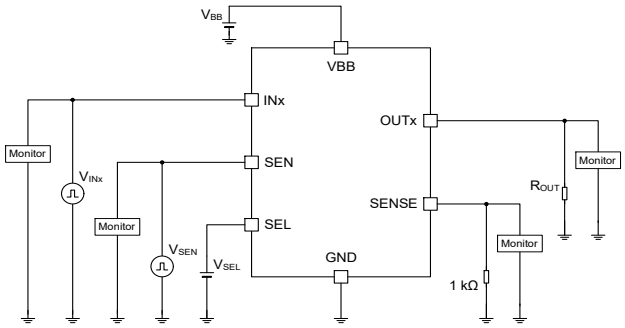



Figure 52. Output Slew Rate when ON / OFF
Output Propagation Time Delay when Turning ON / OFF
Switch ON / OFF Time
SENSE Output Delay Time when the Device Turns ON
SENSE Output Delay Time when Diagnostic Turns ON / OFF

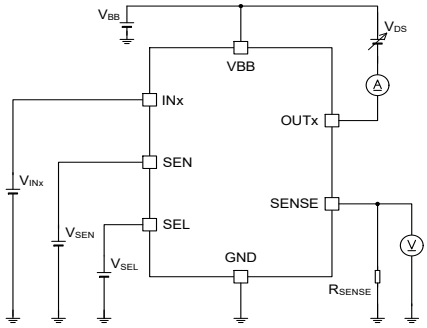



Figure 53. Open Load at OFF $V_{DS}$ Detect Diagnostic Error Flag Voltage

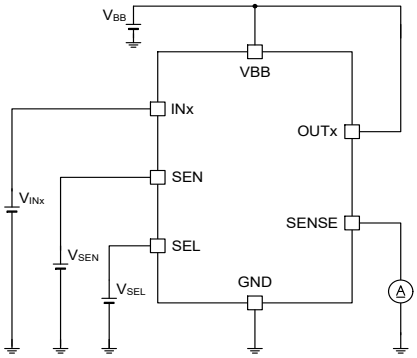



Figure 54. Diagnostic Error Flag Current

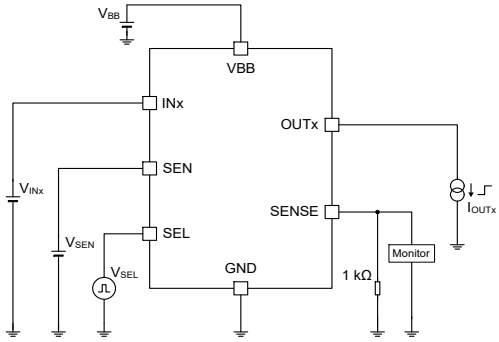



Figure 55. SENSE Settling Time during Load Current Changing
SENSE Settling Time during Channel Change

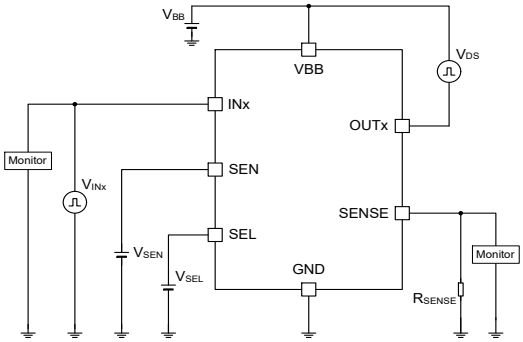



Figure 56. Open Load at OFF Detection Mask Time
Error Flag Release Time

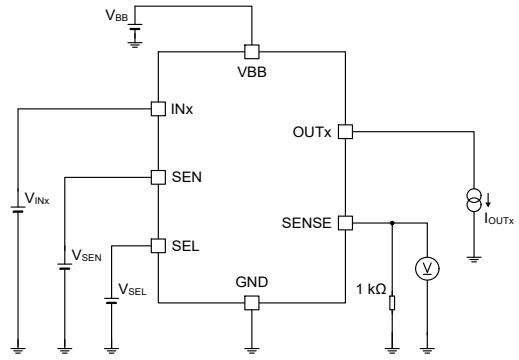



Figure 57. Current Sense Ratio


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## Block Diagram

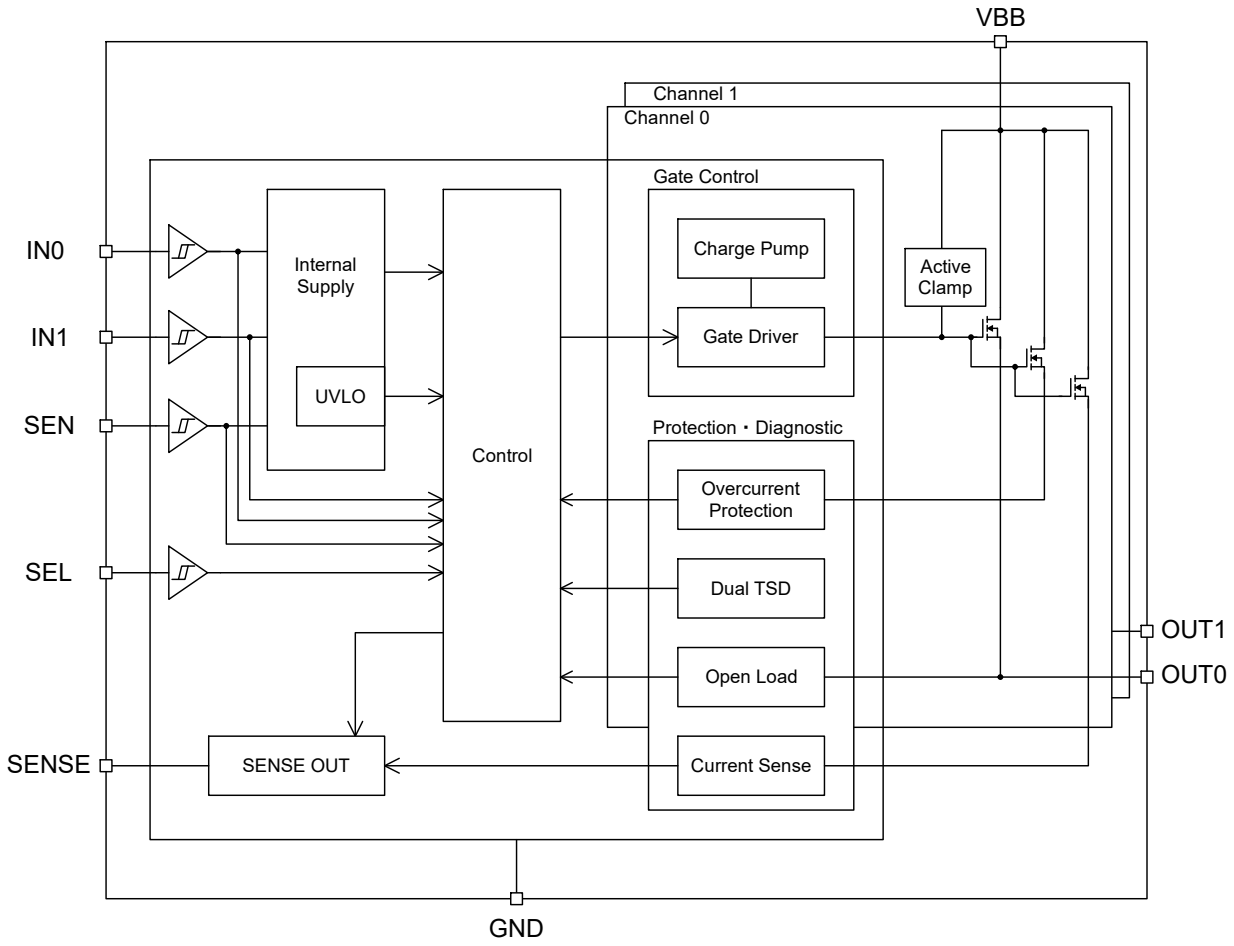



Figure 58. Block Diagram


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## Features Description

### Input Pins

The input circuitry is compatible with 3.3 V and 5 V microcontrollers. The INx, SEN and SEL pins must be connected to the microcontroller via 4.7 kΩ resistors. In case not used, the pins shall be connected to ground via resistors; 4.7 kΩ or more is recommended.

The input circuitry reacts to voltage thresholds and avoids undefined states by use of internal hysteresis. Setting the INx pin voltage above 2.1 V the High Side Power Switch output turns on. The device is in Operating Mode. Setting the SEN pin voltage above 2.1 V the diagnostic functions are activated. Setting the INx pin voltage below 0.9 V the output is turned off. Setting the SEN pin voltage below 0.9 V the diagnostic functions are deactivated.

With INx, SEN and SEL input pins “low” the device enters Sleep Mode; all internal circuits are switched off to prevent current consumption from the power supply, output is turned off and no protection is active. In case the INx pin is de-asserted i.e., INx is “low” and the SEN pin is kept “high” then the device enters in a Standby Mode with diagnostic functions activated. In this scenario the current consumption is reduced, but not stopped.

Setting the SEL pin voltage above 2.1 V Channel 1 is selected to be diagnosed. Setting the SEL pin voltage below 0.9 V Channel 0 is selected to be diagnosed.

In case the connection is interrupted, the input pins are pulled down internally; only in case all input pins are low the Sleep Mode is activated. The internal pull-down is implemented with a resistance. Furthermore, internal de-bounce filters make sure the circuits are not activated or deactivated by high frequency noise or other voltage spikes at the pins.

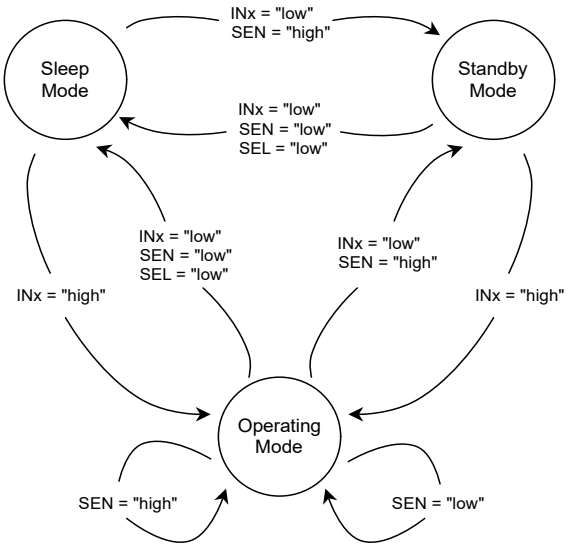



Figure 59. State Diagram

### Internal Supply and Under Voltage Lock Out (UVLO)

The Power Supply Line Input $V_{BB}$ is used to energize and supply internal circuitry and generate internal volage references. The Intelligent High Side Power Device is designed to operate down to very low battery cranking voltages. However, as with any battery powered device it still needs a certain minimum voltage to operate. An undervoltage protection circuit with hysteresis makes sure the device does nothing until the supply voltage is high enough and a predictable behavior can be maintained. The UVLO circuit prevents an undefined output state and/or unintended diagnostic functions turn on when the $V_{BB}$ voltage is below the specified threshold.

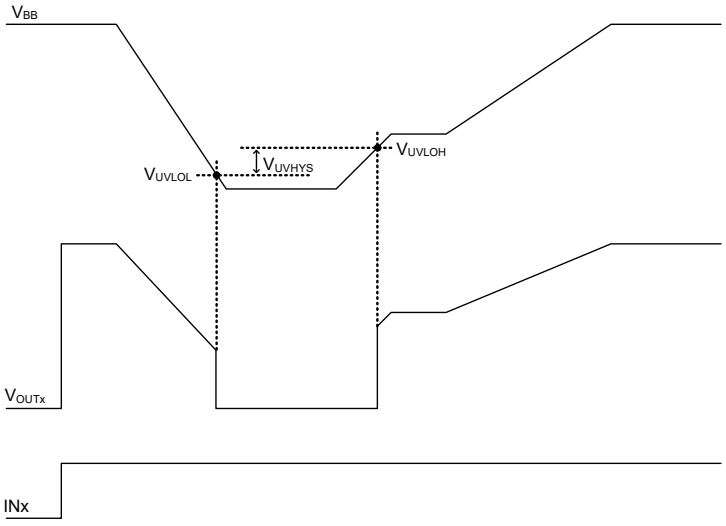



Figure 60. UVLO Functionality


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## Features Description – continued

### Control Circuitry

The device integrates logic circuits that control the operation of the Intelligent High Side Power Switch. Based on the state of the protection circuits and given inputs the control logic performs state transitions and produces outputs as such.

### Gate Control Circuitry

The device integrates a gate driving circuit that acts as interface between the control logic and the N-channel power transistor. A charge pump acts as internal supply allowing to turn on the MOSFET and drive it in the deep triode operation region. The integrated charge pump operates at a fixed frequency improving the EMI performance of the IC. Moreover, the switching behavior of the power transistor is regulated via the gate-driver hence the on and off switching times and slew rates are current-controlled to further improve the EMC. The differential pulse skew $t_{SKEW}$ is defined as the difference between $t_{OFF}$ and $t_{ON}$ times as per the below figure.

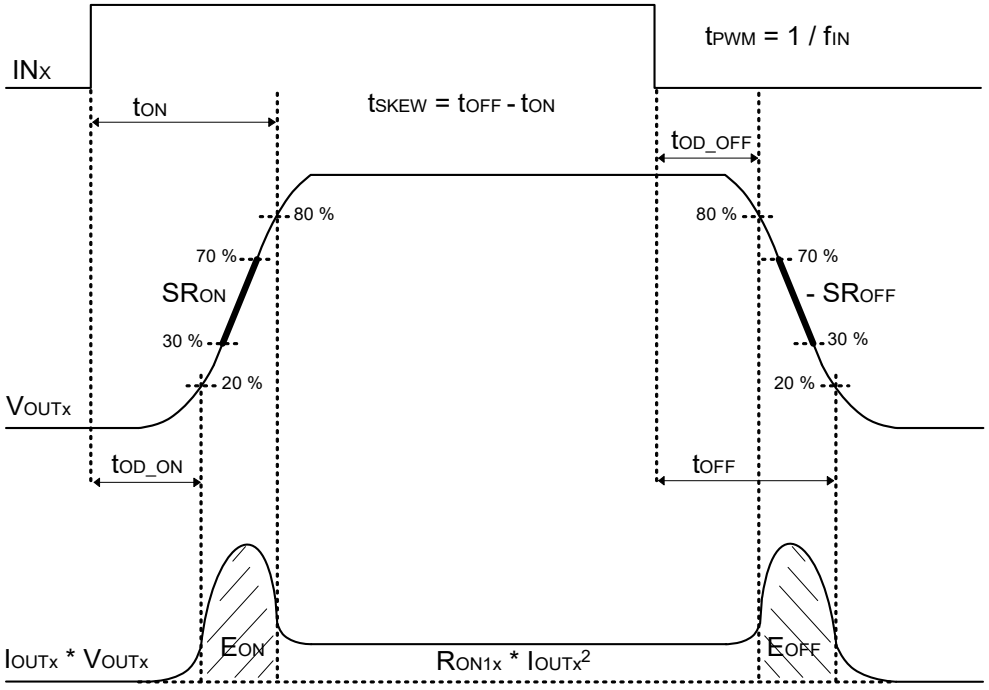



Figure 61. Switching Resistive Loads

### Active Clamp Protection

An intelligent integrated active clamp protection limits the maximum $V_{DS}$ across the power transistor when switching inductive loads at the output pin and the inductive energy is dissipated internally. Moreover, a VBB to GND internal clamp circuit protects the internal circuits from overvoltage surges.

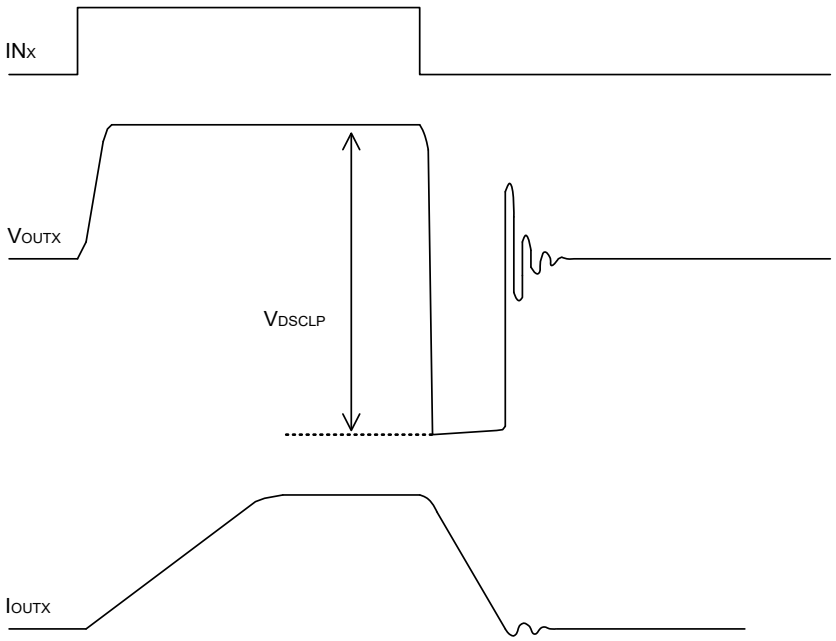



Figure 62. Switching Inductive Loads


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## Features Description – continued

### Loss of Ground Protection

When the module's ground becomes open, the outputs switch off. However, it is recommended to add resistors connected between the input pins and the microcontroller. Furthermore, it is recommended to keep all the digital inputs pulled either all high or all low to avoid creating parasitic ground paths that could prevent the outputs from switching off. If the GND pin is open when an inductive load is driven, the active clamp protection safeguards the IC.

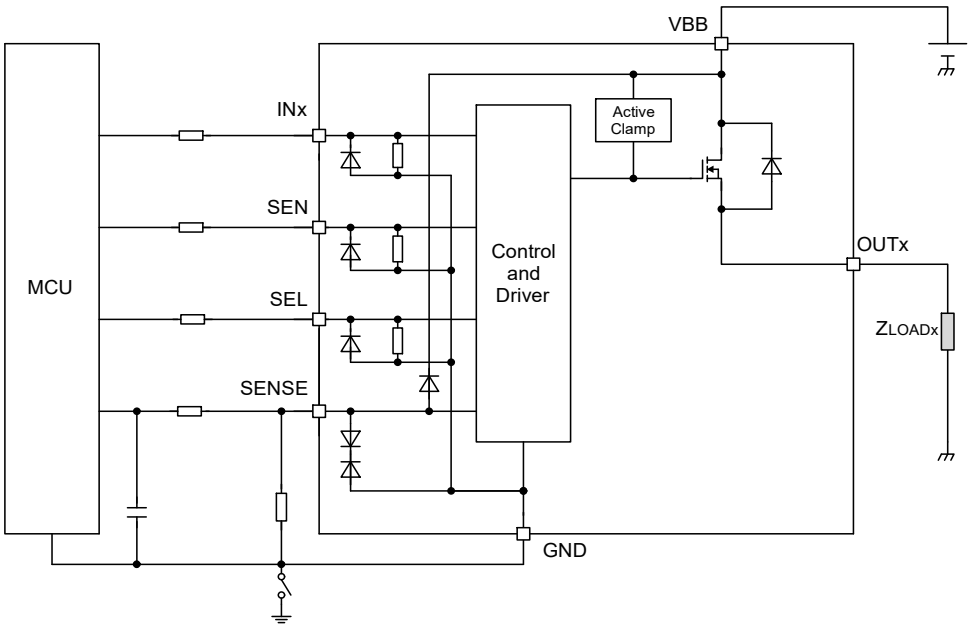



Figure 63. Loss of Ground Protection Diagram

### Load Dump and Overvoltage Protection

The integrated VBB to GND overvoltage protection will safeguard the internal circuits from overvoltage transients. In order for the overvoltage protection to work a ground resistance $R_{GND}$ is necessary. However, a ground shift needs to be considered versus the microcontroller ground when looking at the input voltage threshold levels while in normal operation. Furthermore, the active clamp protection limits the maximum $V_{DS}$ across the power transistor. Moreover, in case the $V_{BB}$ voltage exceeds the $V_{BBCLP}$ level the input pins can start to conduct as well, hence input resistors are mandatory as per the above explanations.

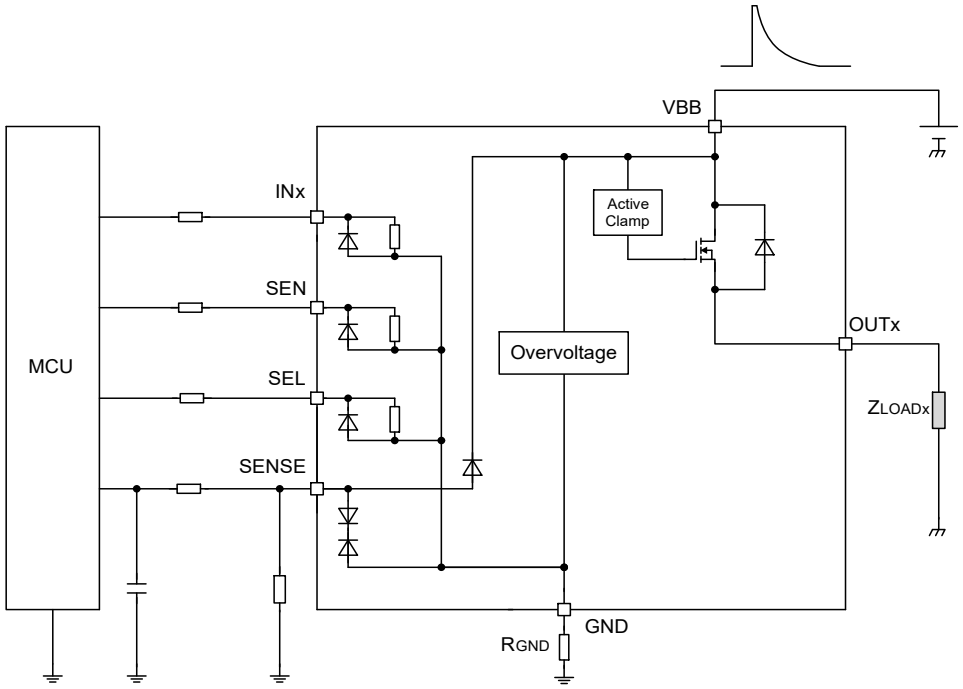



Figure 64. Load Dump Protection Diagram


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## Features Description – continued

### Loss of Battery Protection

When the connection to the battery becomes open the device can dissipate the energy of the wire harness for inductivities up to 10 µH without degrading its robustness. The integrated VBB to GND overvoltage protection will act as a freewheeling path and the active clamp at the output(s) will close the path for the current to flow safeguarding the IC. In applications where the nominal load currents are exceeded, and more load inductivity is expected, an external load freewheeling diode is necessary and/or a transient voltage suppressor must be present on the battery line.

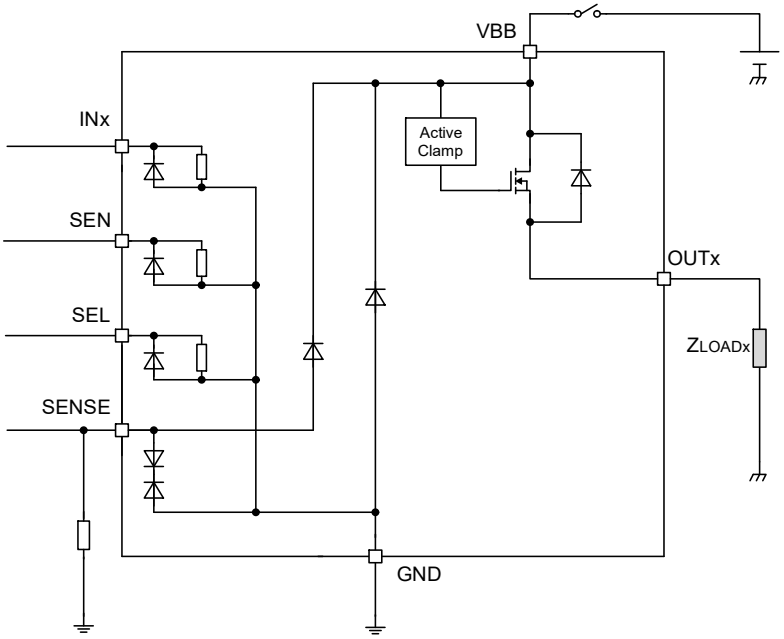



Figure 65. Loss of Battery Diagram

### Reverse Battery Protection

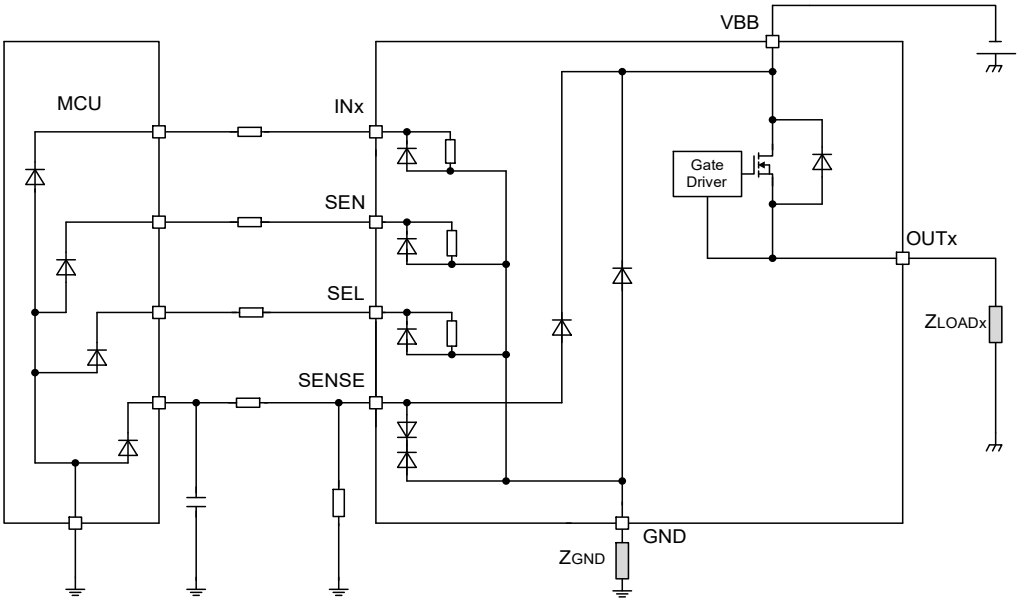



Figure 66. Reverse Battery Diagram

To limit the current through the input pins and the SENSE pin in case of reverse battery connection and negative or positive ISO transients on the battery line, the device's interface pins must be protected with resistors connected between the micro controller and the IC. Furthermore, a ground network $Z_{GND}$ is recommended to help improve the robustness of the IC in such scenarios. $Z_{GND}$ can be either a resistor or a diode.

A ground resistor at the IC GND pin will protect the IC in reverse battery and in case of negative or positive ISO transients on the battery line. Moreover, the ground resistor safeguards the IC during load dump or overvoltage. However, a ground shift needs to be considered versus the microcontroller ground when looking at the input voltage threshold levels due to the chip's current consumption in normal operation. Resistor power dissipation needs to be considered during reverse battery conditions.


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## Features Description – continued

A diode at the IC GND pin will increase the protection level in both reverse battery and negative ISO pulse transients, however it will reduce the positive ISO pulse robustness of the IC and it will diminish the load dump and overvoltage protection ability of the IC. Furthermore, it will lessen the loss of battery protection in case of wire harness inductivity; a parallel resistor to the diode is recommended in this case. However, a small value resistance in series with the diode could be used to increase the positive ISO pulse robustness. If a diode is used the load dump, overvoltage and loss of battery scenarios need careful examination and external transient voltage suppressors or/and load freewheeling diodes need to be considered. Moreover, a ground shift will be present versus the microcontroller ground. However, the diode could be shared between multiple devices.

During reverse battery the device allows the load current to flow through the body diode of the power MOSFET; the current must be limited by the resistance of the load. However, in case the load is inductive, special care must be taken to ensure safe operation. A reverse polarity diode on the battery line would be a possible solution.

A compromise between the above options must be found depending on the specific application requirements and the targeted loads.

### Dual Temperature Shutdown Protection

A dual temperature shutdown (Dual TSD) mechanism limits the internal thermal transients and reduces the mechanical stress of the IC increasing its cyclic short-circuit robustness. The device integrates a per channel absolute and dynamic overtemperature protection circuit. When the chip's junction temperature rises above either the $T_{DTj}$ or the $T_{TSD}$ threshold, the respective output turns off. A thermal hysteresis restart mechanism is implemented. When the chip's temperature falls below a predefined threshold, the output automatically restarts, and operation is resumed accordingly. Moreover, the TSD circuits safeguard the IC in case of overload operation (high inrush current) with the output current below the $I_{OCD}$ thresholds i.e., before the overcurrent protection activates. When the TSD protection is triggered, the SENSE pin acts as an error flag and signals the fault to the microcontroller. The voltage at the SENSE pin is forced to be $V_{SENSEH}$.

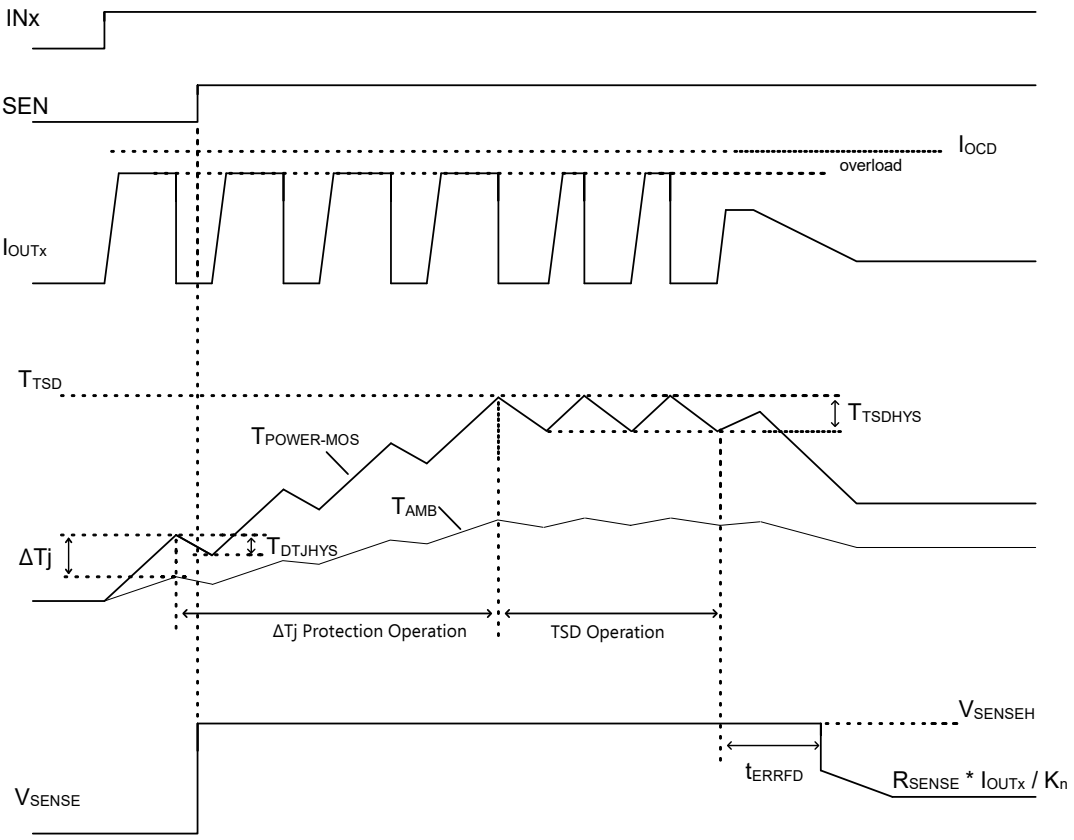



Figure 67. Overtemperature Protection


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## Features Description – continued

### Over Current Protection

The IC has a built-in overcurrent protection feature. If an excessive current flows at the output of the High Side Power Switch, a current limitation aims to protect the IC and peripheral components. Given that a fault is present (short-circuit to ground), or high inrush current at start-up occurs, then the output current is limited to safe operating levels. Moreover, the output current limit is designed to have $V_{DS}$ voltage dependency in favor of an increased robustness of the device. When the load current is above the $I_{OCD}$ threshold the SENSE pin acts as an error flag and signals the fault to the microcontroller. The voltage at the SENSE pin is forced to be $V_{SENSEH}$. Furthermore, the overtemperature - dual temperature shutdown (TSD) protection - circuits complement the overcurrent protection. In case the overtemperature protection is triggered during current limitation the power MOSFET is turned off, hence the output current will toggle accordingly - a restart happens when the chip has cooled down sufficiently.

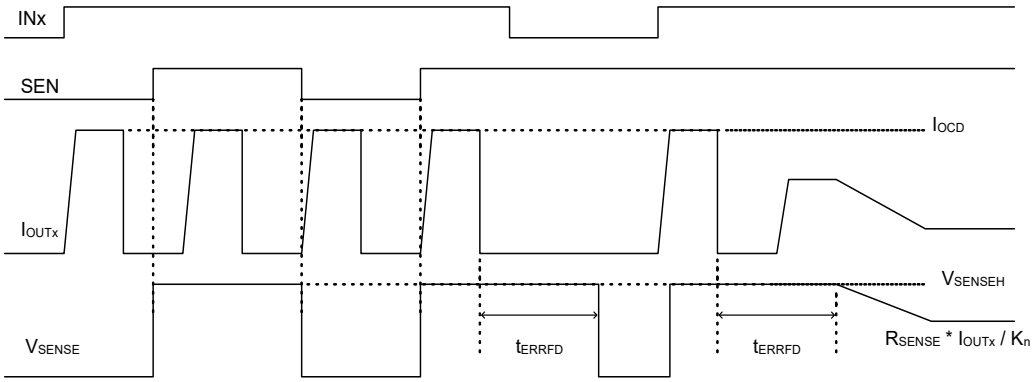



Figure 68. Overcurrent Protection

### Reverse Current Protection

The IC allows reverse current to flow through the power MOSFET when the $V_{OUT}$ voltage level is higher than $V_{BB}$. Furthermore, as long as the current is maintained within the nominal range and the package's thermal limitations are not exceeded the IC can maintain its operating state. If one channel operates in reverse current the other channel can operate unaffected and its load current monitored via the SENSE pin without disturbance.


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## Features Description – continued

### Diagnostic / SENSE Functions

#### Diagnosis Overview

| SEL | SEN | SENSE | OUTx |
|---|---|---|---|
| High / Low | Low | Hi-Z | Not Relevant |
| Low | High | Diagnosis Channel 0 | OUT0 |
| High | High | Diagnosis Channel 1 | OUT1 |

#### Diagnosis / SENSE Output *(Note 1)*

| Mode | INx | SEN | SENSE | OUTx |
|---|---|---|---|---|
| Normal Operation | Low | High | Hi-Z | Low |
| Open Load | Low | High | Hi-Z | < $V_{BB}$ - $V_{DSOL}$ |
| | Low | High | $V_{SENSEH}$ | ≥ $V_{BB}$ - $V_{DSOL}$ |
| Short to Battery | Low | High | $V_{SENSEH}$ | High |
| Thermal Shutdown | Low | High | Hi-Z | Low |
| Short to Ground | Low | High | Hi-Z | Low |
| Reverse Current | Low | High | $V_{SENSEH}$ | High |
| Normal Operation | High | High | $I_{OUTx}$ / $K_n$ | High |
| Open Load | High | High | $I_{OUTx_ONOLD}$ / $K_n$ | High |
| Short to Battery | High | High | < $I_{OUTx}$ / $K_n$ | High |
| Thermal Shutdown | High | High | $V_{SENSEH}$ | Low |
| Short to Ground | High | High | $V_{SENSEH}$ | Low |
| Reverse Current | High | High | Hi-Z | High |
| All modes | - | Low | Hi-Z | - |

*(Note 1)* All values in the above table are Typ values and SENSE is considered Hi-Z looking into the pin i.e., $R_{SENSE}$ is ignored.

The current sense and diagnostic functions are enabled by setting the voltage $V_{SEN}$ = High. The operation is as per the above table. However, an external resistor $R_{SENSE}$ must be connected between SENSE and GND pins. The simplified implementation is described in the below diagram.

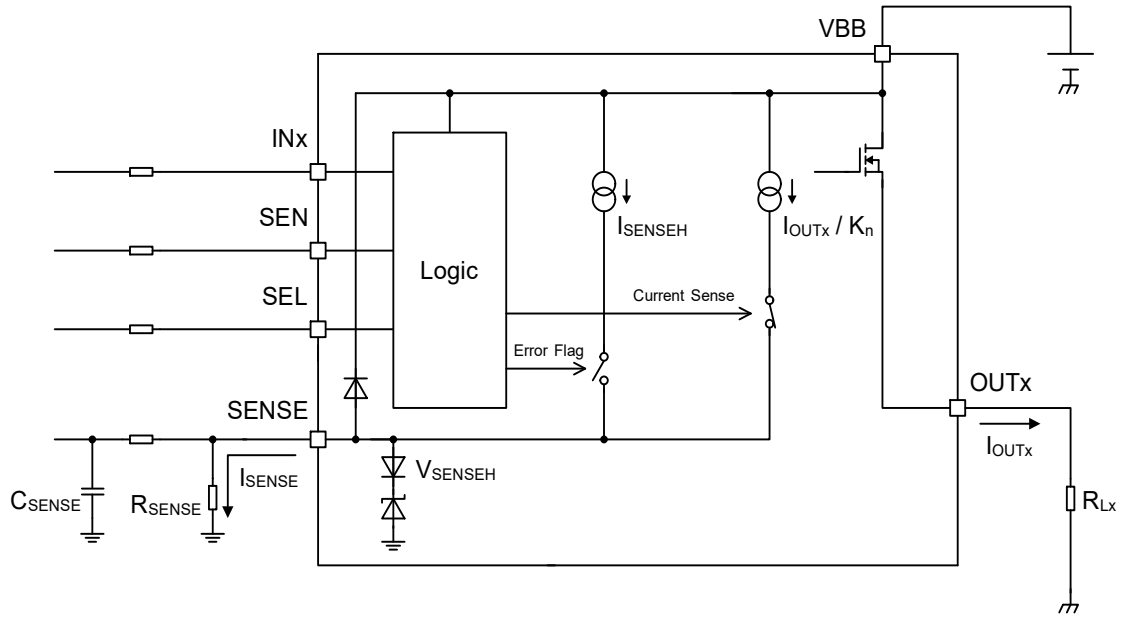



Figure 69. Diagnostic Output Block Diagram


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## Features Description – continued

### Current Sense

When the diagnostic is enabled, and the high side power switch is turned on, a current proportional to the load current is flowing through the SENSE pin. The current $I_{SENSE}$ becomes equal to $I_{OUTx}$ / $K_n$, ($K_n$: Current sense ratio). An external resistor $R_{SENSE}$ is recommended, hence for example the voltage at the SENSE pin is equal to:

$$V_{SENSE} = \frac{R_{SENSE} \times I_{OUT}}{K_n}$$

### Current Sense Ratio Accuracy

The below diagram shows the load current sense ratio dependency vs. the output current through the power MOSFET. The accuracy of the current sense ratio depends on the load current, technological process, voltage and temperature. A higher-precision current sense ratio could be obtained with additional calibration on the application side. The device allows derating at a specific point ($\Delta K_n$, Tj = 25 °C). Moreover, to reduce signal ripple at the microcontroller side, it is recommended to insert an external RC filter between the SENSE pin and the ADC input pin.

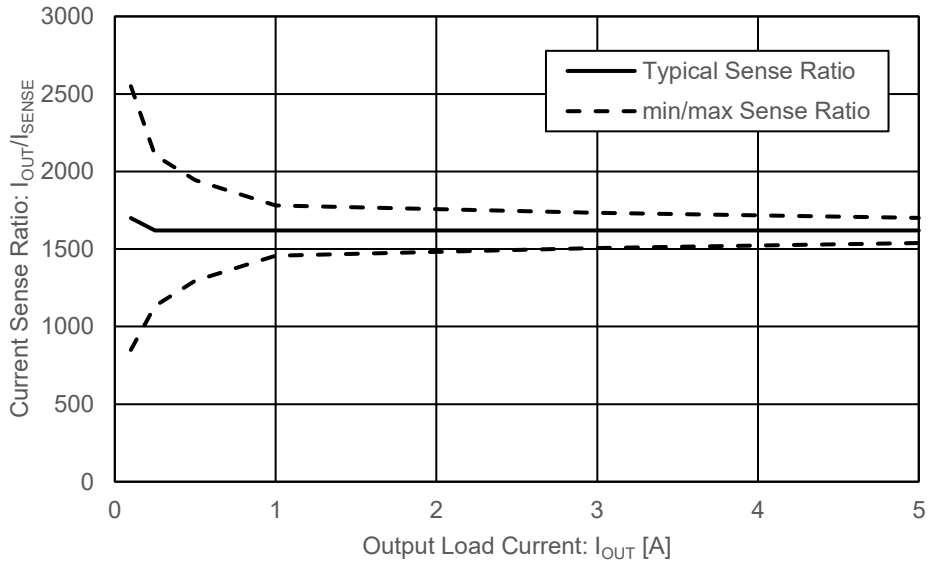



Figure 70. Current Sense Ratio vs Output Load Current

Furthermore, an open load at ON condition can be recognized via the sense ratio if the load current falls below a certain threshold. This is given by the $I_{OUT_ONOLD}$ parameter.

### Open Load Detection

Open load at OFF can be detected by connecting an external resistance $R_{OLD}$ between power supply VBB and OUT.

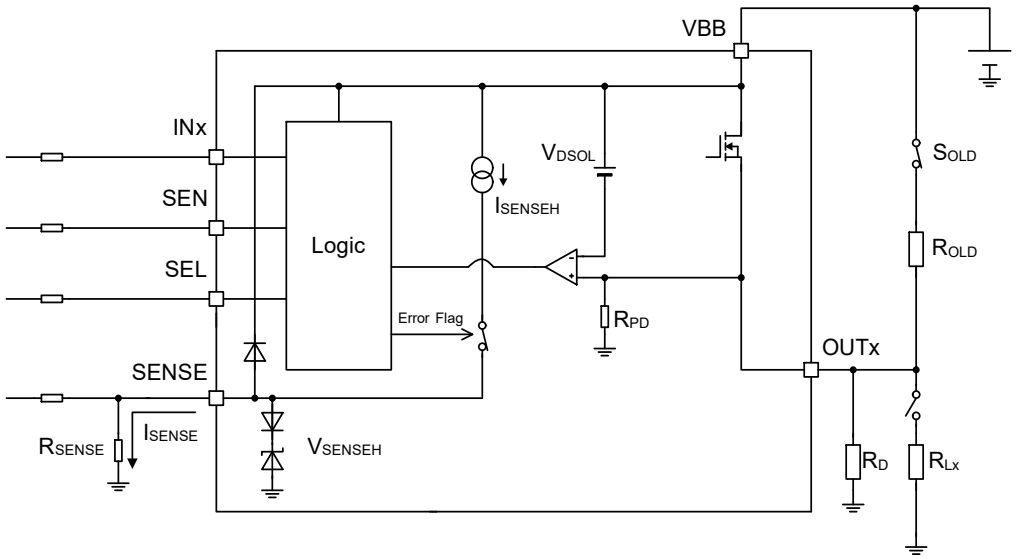



Figure 71. Open Load Detection Block Diagram


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## Features Description – continued

When the output load is disconnected, input pin INx is low and SEN is high, and open load will be flagged at the SENSE pin by the $V_{SENSEH}$ voltage if the load is missing or the output is shorted to the VBB battery line. To reduce the standby current of the system, an open load switch $S_{OLD}$ is recommended. $R_D$ represents the minimum parasitic resistance at the output pin. In case $R_D$ is not considered the device integrates a 200 kΩ $R_{PD}$ resistance.

The value of external resistance $R_{OLD}$ is decided based on the maximum power supply voltage ($V_{BB}$), parasitic resistance $R_D$ and open detection threshold $V_{DSOL}$. The equation for calculating the $R_{OLD}$ value is shown below.

$$R_{OLD} < \frac{R_D \times R_{PD}}{R_D + R_{PD}} \times \left( \frac{V_{DSOL(min)}}{V_{BB(max)} - V_{DSOL(min)}} \right)$$

### Open Load Masking Time

The IC diagnoses open load detection after the mask time $t_{OLDMSK}$ after the INx pin is de-asserted to allow for the output voltage to drop while in normal operation (load connected).

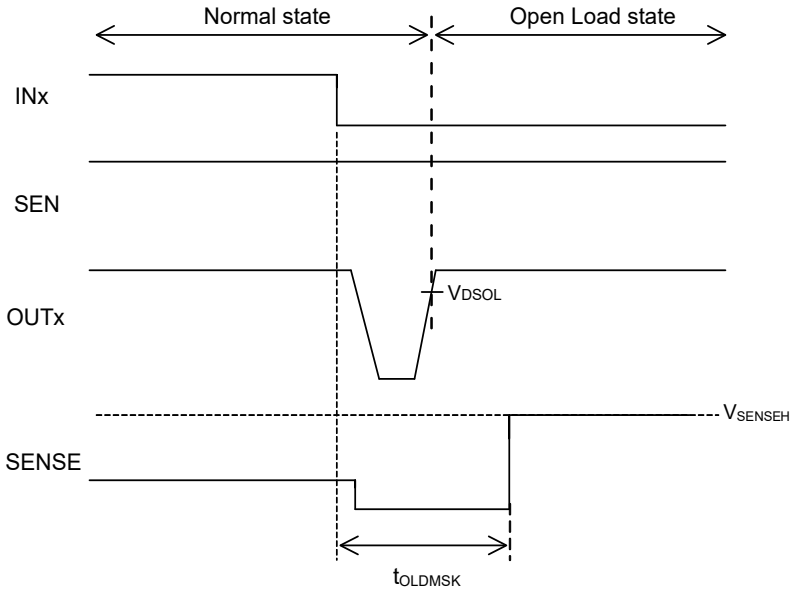



Figure 72. Open Load Mask Timing Chart

### Diagnostic Timings

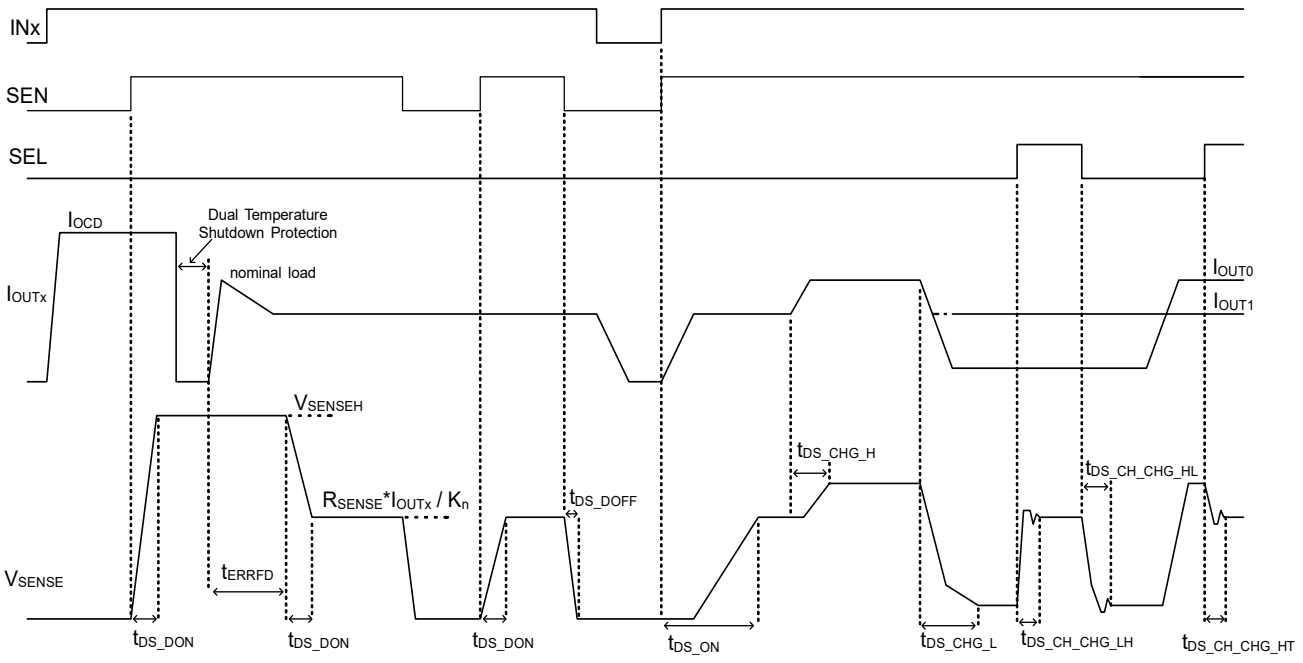



Figure 73. Diagnostics Timing Diagram


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## Application Circuit Example

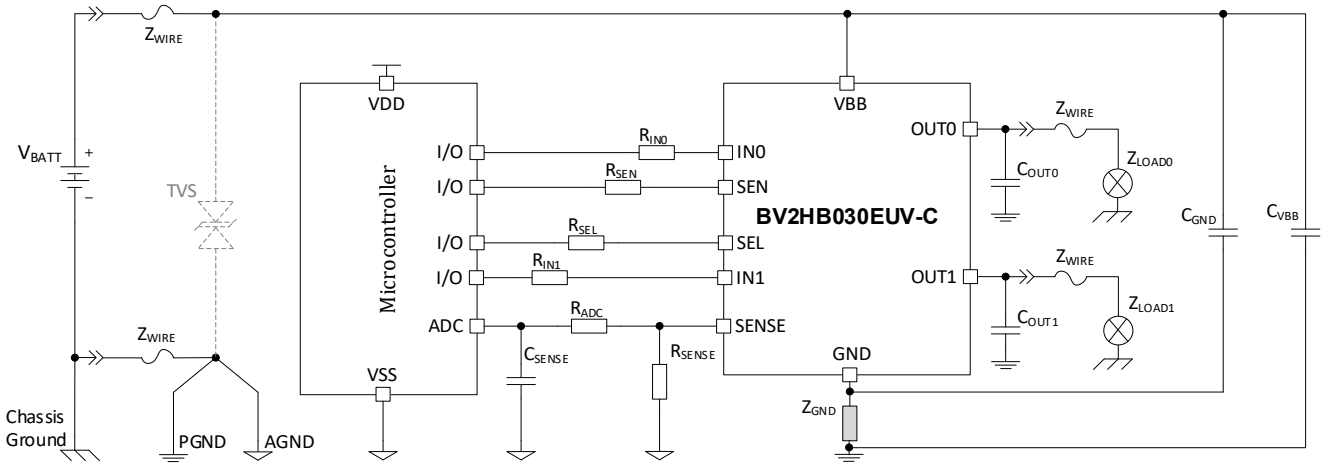



Figure 74. Application Schematic

## Recommended External Components Example

Example with Resistive Ground Protection Network*(Note 1)*:

| Item | Symbol | Standard Value | Unit |
|---|---|---|---|
| Input Pin Resistance | $R_{INx}$ | 4.7 | kΩ |
| Diagnostic Enable Input Pin Resistance | $R_{SEN}$ | 4.7 | kΩ |
| Channel Selection Input Pin Resistance | $R_{SEL}$ | 4.7 | kΩ |
| Microcontroller SENSE Pin Resistance | $R_{ADC}$ | 4.7 | kΩ |
| SENSE Pin Resistance | $R_{SENSE}$ | 1 | kΩ |
| SENSE Filter Capacitance | $C_{SENSE}$ | 100 | pF |
| Output EMC/ESD Capacitance | $C_{OUTx}$ | 10 | nF |
| Battery Line Filter Capacitance | $C_{VBB}$ | 100 | nF |
| Buffer Capacitance | $C_{GND}$ | 47 | nF |
| Chip Ground Protection Resistance | $Z_{GND} = R_{GND}$ | 150 | Ω |
| Transient Voltage Suppressor Diode | TVS | 36 | V |

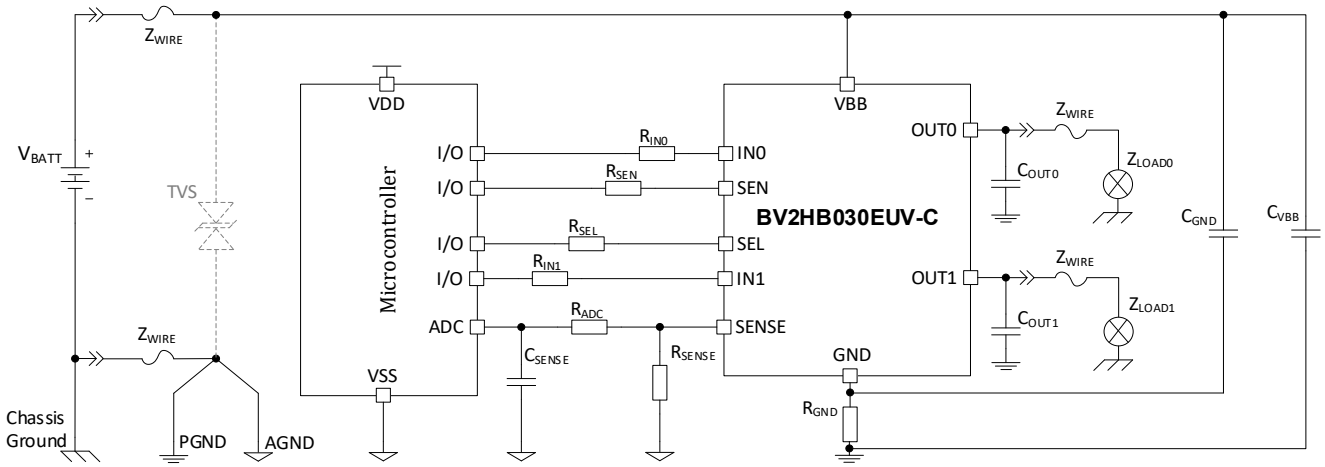



Figure 75. Application Schematic Example – Resistive Ground Network

*(Note 1)* It is recommended, but not mandatory to add a high frequency bypass capacitor $C_{GND}$ as close as possible to the VBB and GND pins


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## Recommended External Components Example – continued

Example with Semiconductor Diode Ground Protection Network:

| Item | Symbol | | Standard Value | Unit |
|---|---|---|---|---|
| Input Pin Resistance | $R_{INx}$ | | 4.7 | kΩ |
| Diagnostic Enable Input Pin Resistance | $R_{SEN}$ | | 4.7 | kΩ |
| Channel Selection Input Pin Resistance | $R_{SEL}$ | | 4.7 | kΩ |
| Microcontroller SENSE Pin Resistance | $R_{ADC}$ | | 4.7 | kΩ |
| SENSE Pin Resistance | $R_{SENSE}$ | | 1 | kΩ |
| SENSE Filter Capacitance | $C_{SENSE}$ | | 100 | pF |
| Output EMC/ESD Capacitance | $C_{OUTx}$ | | 10 | nF |
| Battery Line Filter Capacitance | $C_{VBB}$ | | 100 | nF |
| Chip Ground Protection Impedance Network | $R_{GND}$ *(Note 1)* | | 4.7 | kΩ |
| | $D_{GND}$ *(Note 2)* | $V_F$ | 0.6 | V |
| | | $V_R$ | 200 | V |
| | $R_G$ *(Note 3)* | | 10 | Ω |
| Transient Voltage Suppressor Diode | TVS | | 36 | V |

*(Note 1)* $R_{GND}$ in parallel with the Ground Protection Diode is optional. $R_{GND}$ is needed in case of loss of $V_{BB}$ with wire harness inductivity or inductive load.
*(Note 2)* The $V_F$ of $D_{GND}$ is the forward bias voltage, and the $V_R$ of $D_{GND}$ is the reverse bias voltage. $V_F$ depends on the forward current through $D_{GND}$. Please refer to the "*Operating Mode Current ($I_{GNDH}$)*" parameter from "*Electrical Characteristics*" section when selecting a diode.
*(Note 3)* $R_G$ in series with the impedance created by the $D_{GND}$ and the parallel $R_{GND}$ is optional. $R_G$ grants increased positive ISO pulse robustness to the IC.

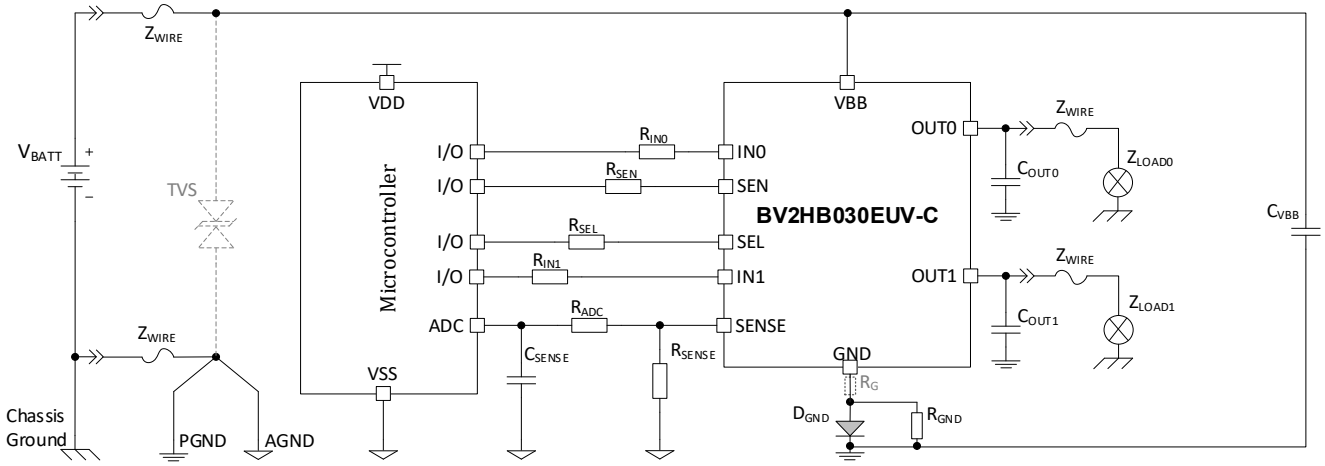
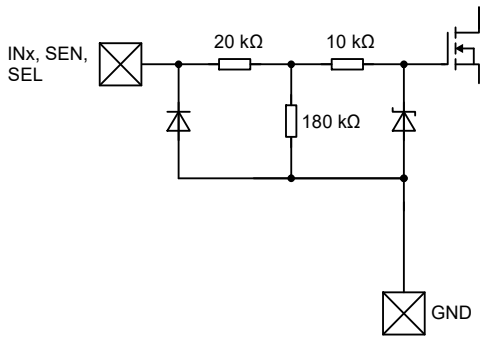
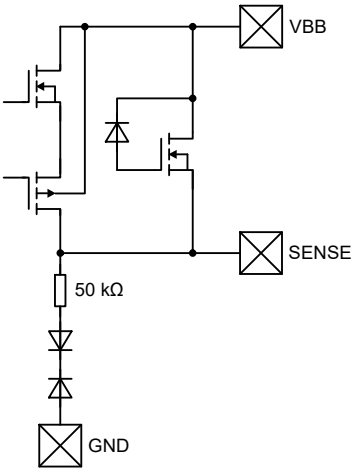
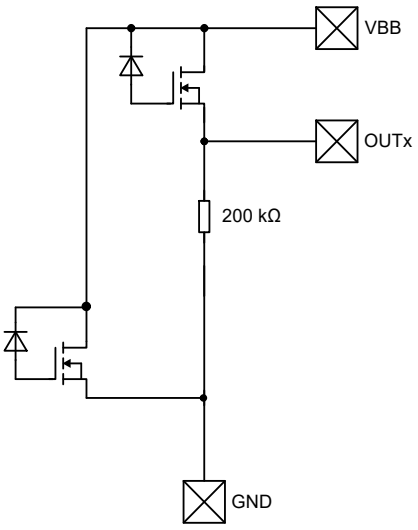



Figure 76. Application Schematic Example – Semiconductor Diode Ground Protection Network


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## I/O Equivalence Circuits

| INx, SEN, SEL | SENSE |
|---|---|
|  |  |
| **VBB, OUTx** | |
|  | |








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## Operational Notes

1. **Recommended Operating Conditions**
   The IC is designed to operate in 12 V automotive board net applications. The functions and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions specified by the electrical characteristics. The IC can withstand transient voltages beyond the recommended operating conditions; however, parameter deviations are possible when used outside of the supply nominal voltage range. Exposure to the absolute maximum ratings may cause permanent damage to the IC.

2. **Inrush Current**
   When a load is being activated by the IC inrush currents may flow. The IC is designed to drive high inrush current loads; however, careful consideration must be completed when pairing the IC with the load. In case special recommendations are not available in the Datasheet the minimum overcurrent protection level of the IC should be higher than the maximum expected inrush current for proper load driving.

3. **Testing on Application Boards**
   When testing the IC on an application board, it is recommended to always discharge capacitors completely after each evaluation step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

4. **Inter-pin Short and Mounting Errors**
   Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

5. **Ceramic Capacitor**
   When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

6. **Thermal Shutdown Function (TSD)**
   This IC has a built-in thermal shutdown function that prevents heat damage to the IC. Normal operation should always be within the IC's maximum junction temperature rating. If however, the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD function that will turn OFF power output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.
   Note that the TSD function operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances should the TSD function be used in a set design or for any purpose other than protecting the IC from heat damage.

7. **Over Current Protection Function (OCP)**
   This IC integrates an overcurrent limitation protection function that is activated when the load is shorted towards ground. This protection function is effective in preventing damage due to sudden and unexpected fault events. However, the IC should not be used in applications characterized by continuous operation of the protection function.

8. **Active Clamp Protection**
   The IC integrates an active clamp protection to internally dissipate the magnetic energy $E_{AS}$ generated when an inductive load is switched off. The maximum $E_{AS}$ energy the device can handle for a given $I_{OUT(START)}$ is limited by the maximum thermal design of the power FET. Therefore, the maximum inductance L must be selected with respect to the maximum $I_{OUT(START)}$. Please refer to single pulse $E_{AS}$ energy diagram in *Figure 4. Active Clamp Energy vs Output Current*.

9. **Reverse Battery Connection**
   Connecting the power supply i.e., the battery with a reversed polarity can damage the IC. Precautions must be taken against reverse polarity when connecting the power supply, such as mounting an external diode between the battery feed and the IC's power supply, blocking all current paths. Alternatively, inserting a blocking diode or resistance in series with the IC's GND pin will prevent or limit the current from flowing into the control circuits of the high side switch respectively. However, current thorough the body diode of the integrated power FET must be limited by the resistive component of the load. The current through the Digital inputs and SENSE pins must be limited too with protection resistors.

10. **Functional Safety**
    ROHM defined three functional safety product categories as follows:
    a) "Functional Safety Supportive Automotive Product" - a product that has been developed for automotive use and is capable of supporting safety analysis with regards to functional safety.
    b) "Safety Mechanism is Implemented to Support Functional Safety (ASIL-*)" - a product that has implemented safety mechanism to meet ASIL level requirements described in the datasheet.
    c) "ISO 26262 Process Compliant to Support ASIL-*" - a product that has been developed based on an ISO 26262 design process compliant to the ASIL level described in the datasheet.
    Note: "ASIL-*" is stands for the ratings of "ASIL-A", "-B", "-C" or "-D" specified by each product's datasheet.


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## Operational Notes – continued

**11. Power Supply and PCB Layout**

Design the PCB layout in order to provide sufficient cooling to the IC. Connect the exposed pad with sufficient thermal vias to power supply copper plane to dissipate as much as possible thermal energy to the environment. Furthermore, connect as close as possible to the IC a capacitor between power supply and ground pins. Minimize the input capacitance of the digital input pins by placing the protection resistors as close as possible to the IC. Place the ground network as close as possible to the IC. Place the sense pin resistance as close as possible to the IC and the R-C filtering network close to the microcontroller. Place the output capacitors as close as possible to the IC. Short all output pins of the respective channel on the PCB to ensure equal current distribution. It is usually recommended to use a PCB with an internal copper layer as a power supply plane and another internal copper layer as a ground plane for thermal and EMC considerations respectively.

**12. Ground Shift and Ground Wiring Pattern**

When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. The IC is robust against small ground shift, however, ensure that the ground traces of external components do not cause big variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance. Big ground shifts could cause additional switching losses and electromagnetic emissions.

**13. Reverse Current**

A capacitive or inductive type of load can cause the output of the IC to rise above the input power supply level. The IC is designed to accept reverse current and normal operation is maintained as long as the reverse current is below the specified levels. Therefore, give special consideration to the maximum amount of reverse current that can flow through the device.

**14. Undervoltage or Loss of Battery**

The IC is designed to automatically switch off in case of loss of battery/power supply or undervoltage events. The IC will restart once the battery exceeds the specified operation threshold. In case the load is inductive a resistor on the ground network is recommended if loss of battery is foreseen at the same time in the application.

**15. Loss of Ground**

The IC cannot operate without the appropriate ground connection; nonetheless, the IC will automatically switch off in case of loss of ground. However, careful consideration of the external state of the inputs must be considered in order to avoid creating parasitic paths to another ground in the application via the external circuitry.

**16. Load Dump and Overvoltage Protection**

The IC is designed with integrated overvoltage protection to safeguard its internal circuits. For the overvoltage protection to work a ground resistance $R_{GND}$ is necessary. Furthermore, input pins' protection resistors are mandatory. In case of Load dump external TVS protection diodes must be connected to safeguard the system.

**17. Open Load or Short to Battery**

An open load event is not considered dangerous to the IC; moreover, the IC can detect such failure and signal the fault to the microcontroller. In case a short to battery is present the load is turned on independent of the state of the IC. The device can be used to detect such a failure and signal the fault to the microcontroller.

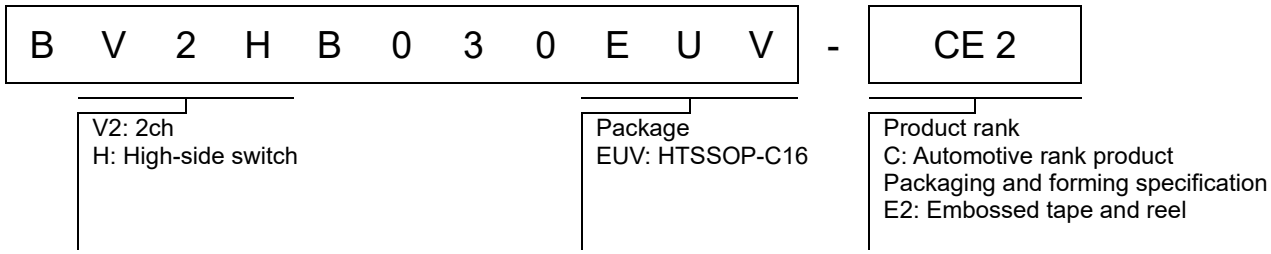
**18. Internally Not Connected (N.C.) Pins**

Pins that are specified as internally not connected have no physical connection to the IC. For mechanical reasons it is recommended to solder them on the PCB. Electrically they can remain not connected in the circuit or may be connected to different signals especially when using high current outputs.

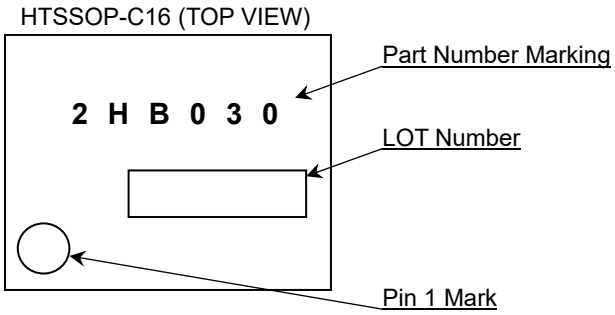

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### Ordering Information




### Marking Diagram



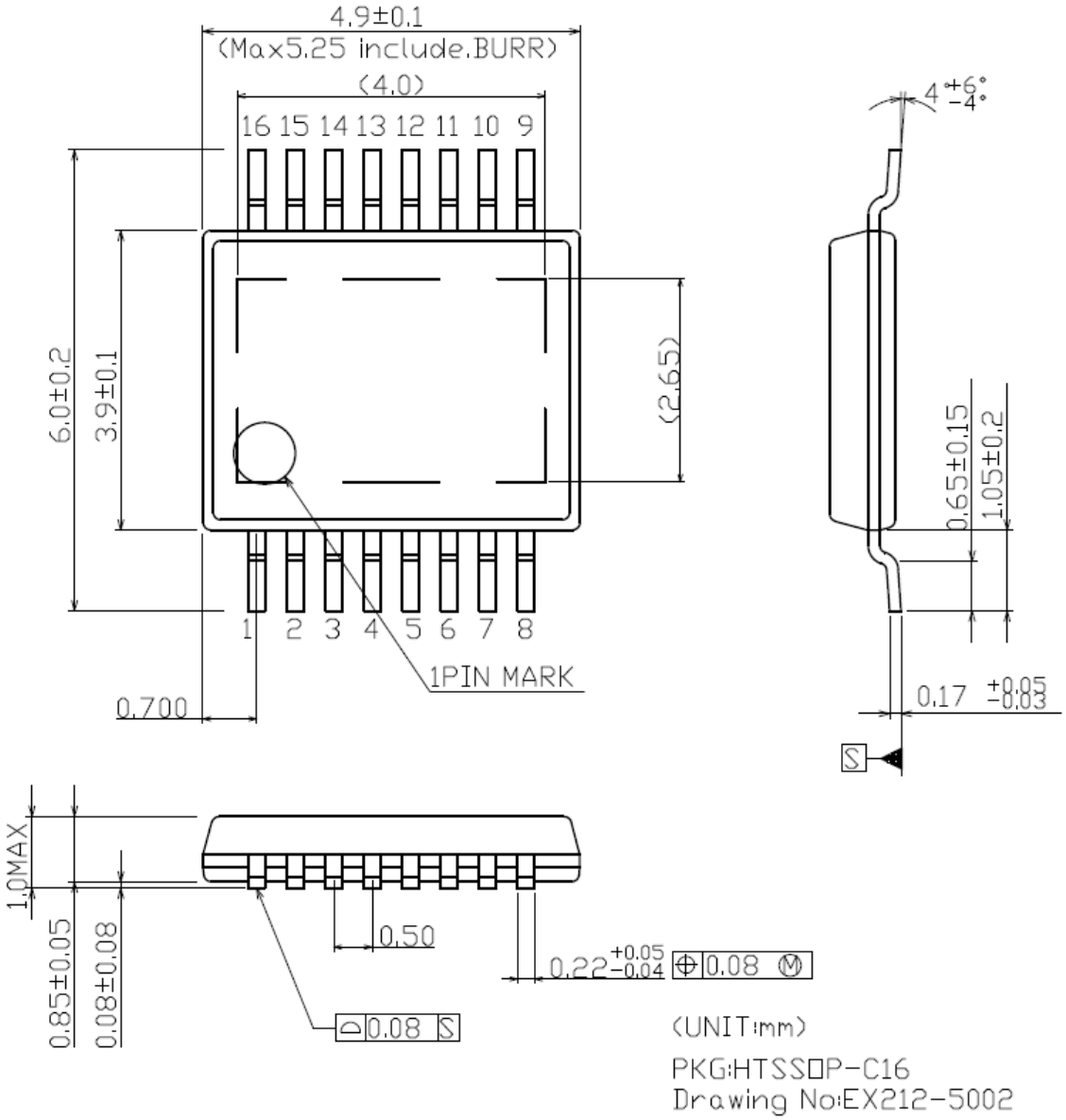


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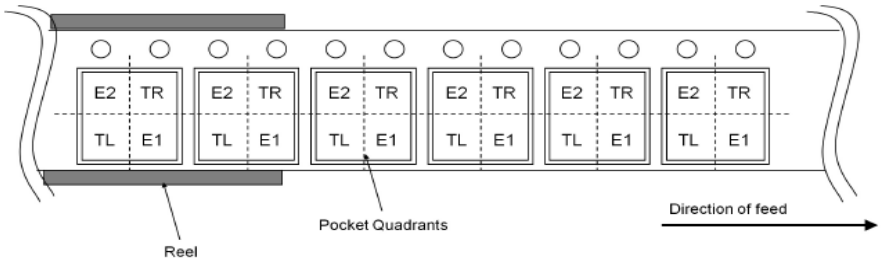
**Physical Dimension and Packaging Information**

| Package Name | HTSSOP-C16 |
|---|---|




< Tape and Reel Information >

| | |
|---|---|
| Tape | Embossed carrier tape |
| Quantity | 2500pcs |
| Direction of feed | E2<br>The direction is the pin 1 of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand |





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## Revision History

| Date | Ver. | Contents |
|---|---|---|
| 6.Mar.2026 | 001 | New Release |


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(Note1) Medical Equipment Classification of the Specific Applications

| JAPAN | USA | EU | CHINA |
|---|---|---|---|
| CLASSⅢ | CLASSⅢ | CLASSⅡb | CLASSⅢ |
| CLASSⅣ | | CLASSⅢ | |

2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
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   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including $Cl_2$, $H_2S$, $NH_3$, $SO_2$, and $NO_2$
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (Exclude cases where no-clean type fluxes is used. However, recommend sufficiently about the residue.); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse, is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

## Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification


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## Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

## Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

## Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   - [a] the Products are exposed to sea winds or corrosive gases, including $Cl_2$, $H_2S$, $NH_3$, $SO_2$, and $NO_2$
   - [b] the temperature or humidity exceeds those recommended by ROHM
   - [c] the Products are exposed to direct sunshine or condensation
   - [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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