

SN54HC573, SN74HC573 OCTAL D-TYPE TRANSPARENT LATCHES WITH 3-STATE OUTPUTS

D2684, DECEMBER 1982—REVISED SEPTEMBER 1987

- High-Current 3-State Output Drive Bus-Lines Directly or Up to 15 LSTTL Loads
- Bus-Structured Pinout
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

description

These 8-bit latches feature three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight latches are transparent D-type latches. While the enable (C) is high the (Q) outputs will respond to the data (D) inputs. When the enable is taken low the outputs will be latched to retain the data that was set up.

An output-control ($\overline{OC}$) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components.

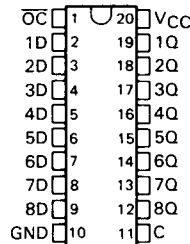
The output control ($\overline{OC}$) does not affect the internal operation of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN54HC573 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74HC573 is characterized for operation from -40°C to 85°C .

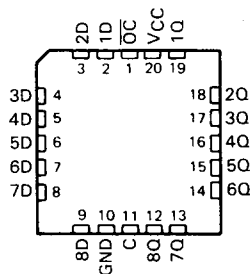
FUNCTION TABLE
(EACH LATCH)

INPUTS			OUTPUT Q
ENABLE			
$\overline{OC}$	C	D	
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

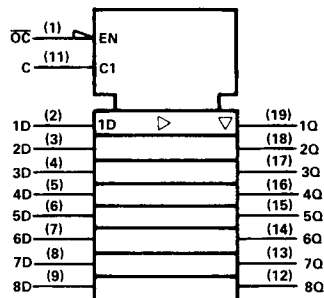
SN54HC573 . . . J PACKAGE
SN74HC573 . . . DW OR N PACKAGE
(TOP VIEW)



SN54HC573 . . . FK PACKAGE
(TOP VIEW)



logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

TEXAS
INSTRUMENTS

Copyright © 1982, Texas Instruments Incorporated

POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

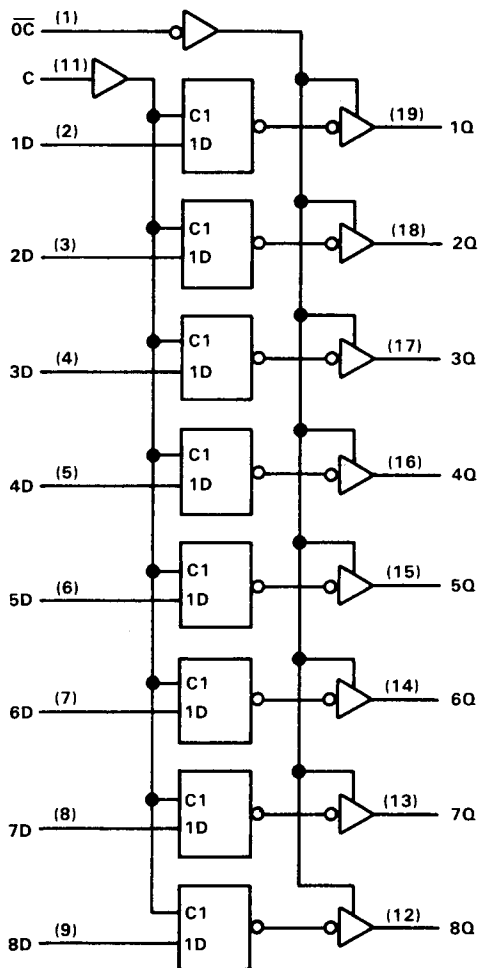
2-507

2

HCMOS Devices

SN54HC573, SN74HC573
OCTAL D-TYPE TRANSPARENT LATCHES WITH 3-STATE OUTPUTS

logic diagram (positive logic)



2

HCMOS Devices

SN54HC573, SN74HC573

OCTAL D-TYPE TRANSPARENT LATCHES WITH 3-STATE OUTPUTS

absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC}	-0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	± 20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 35 mA
Continuous current through V_{CC} or GND pins	± 70 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package	300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: DW or N package	260°C
Storage temperature range	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54HC573			SN74HC573			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	$V_{CC} = 2$ V $V_{CC} = 4.5$ V $V_{CC} = 6$ V	1.5 3.15 4.2			1.5 3.15 4.2			V
V_{IL}	Low-level input voltage	$V_{CC} = 2$ V $V_{CC} = 4.5$ V $V_{CC} = 6$ V	0 0 0	0.3 0.9 1.2		0 0 0	0.3 0.9 1.2		V
V_I	Input voltage		0	V_{CC}		0	V_{CC}		V
V_O	Output voltage		0	V_{CC}		0	V_{CC}		V
t_t	Input transition (rise and fall) times	$V_{CC} = 2$ V $V_{CC} = 4.5$ V $V_{CC} = 6$ V	0 0 0	1000 500 400		0 0 0	1000 500 400		ns
T_A	Operating free-air temperature		-55		125	-40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	$T_A = 25^\circ\text{C}$			SN54HC573		SN74HC573		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	$V_I = V_{IH}$ or V_{IL} , $I_{OH} = -20 \mu\text{A}$	2 V	1.9	1.998		1.9		1.9		V
		4.5 V	4.4	4.499		4.4		4.4		
		6 V	5.9	5.999		5.9		5.9		
	$V_I = V_{IH}$ or V_{IL} , $I_{OH} = -6 \text{ mA}$	4.5 V	3.98	4.30		3.7		3.84		
		6 V	5.48	5.80		5.2		5.34		
V_{OL}	$V_I = V_{IH}$ or V_{IL} , $I_{OL} = 20 \mu\text{A}$	2 V		0.002	0.1		0.1		0.1	V
		4.5 V		0.001	0.1		0.1		0.1	
		6 V		0.001	0.1		0.1		0.1	
	$V_I = V_{IH}$ or V_{IL} , $I_{OL} = 6 \text{ mA}$	4.5 V		0.17	0.26		0.4		0.33	
		6 V		0.15	0.26		0.4		0.33	
I_I	$V_I = V_{CC}$ or 0	6 V		± 0.1	± 100		± 1000		± 1000	nA
I_{OZ}	$V_O = V_{CC}$ or 0	6 V		± 0.01	± 0.5		± 10		± 5	μA
I_{CC}	$V_I = V_{CC}$ or 0, $I_O = 0$	6 V			8		160		80	μA
C_i		2 to 6 V		3	10		10		10	pF

2

HCMS Devices

SN54HC573, SN74HC573

OCTAL D-TYPE TRANSPARENT LATCHES WITH 3-STATE OUTPUTS

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

	V _{CC}	T _A = 25 °C		SN54HC573		SN74HC573		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t _w Pulse duration, C high	2 V	80		120		100		ns
	4.5 V	16		24		20		
	6 V	14		20		17		
t _{su} Setup time, data before enable C↓	2 V	50		75		63		ns
	4.5 V	10		15		13		
	6 V	9		13		11		
t _h Hold time, data after enable C↓	2 V	5		5		5		ns
	4.5 V	5		5		5		
	6 V	5		5		5		

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC}	T _A = 25 °C			SN54HC573		SN74HC573		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{pd}	D	Q	2 V		77	175		265		220	ns
			4.5 V		26	35		53		44	
			6 V		23	30		45		38	
t _{pd}	C	Any Q	2 V		87	175		265		220	ns
			4.5 V		27	35		53		44	
			6 V		23	30		45		38	
t _{en}	$\overline{OC}$	Any Q	2 V		68	150		225		190	ns
			4.5 V		24	30		45		38	
			6 V		21	26		38		32	
t _{dis}	$\overline{OC}$	Any Q	2 V		47	150		225		190	ns
			4.5 V		23	30		45		38	
			6 V		21	26		38		32	
t _t		Any Q	2 V		28	60		90		75	ns
			4.5 V		8	12		18		15	
			6 V		6	10		15		13	

C _{pd}	Power dissipation capacitance per latch	No load, T _A = 25 °C	50 pF typ
-----------------	---	---------------------------------	-----------

Note 1: Load circuits and voltage waveforms are shown in Section 1.

SN54HC573, SN74HC573 OCTAL D-TYPE TRANSPARENT LATCHES WITH 3-STATE OUTPUTS

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), $C_L = 150 \text{ pF}$ (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	$T_A = 25^\circ\text{C}$			SN54HC573		SN74HC573		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	D	Q	2 V		95	200		300		250	ns
			4.5 V		33	40		60		50	
			6 V		21	34		51		43	
t_{pd}	C	Any Q	2 V		103	225		335		285	ns
			4.5 V		33	45		67		57	
			6 V		29	38		57		48	
t_{en}	$\overline{OC}$	Any Q	2 V		85	200		300		250	ns
			4.5 V		29	40		60		50	
			6 V		26	34		51		43	
t_t		Any Q	2 V		60	210		315		265	ns
			4.5 V		17	42		63		53	
			6 V		14	36		53		45	

Note 1: Load circuits and voltage waveforms are shown in Section 1.

2

HC MOS Devices