

MOSFET – N-Channel, Logic Level, POWERTRENCH®

60 V, 1.6 A, 98 mΩ

FDN5632N-F085

Features

- $R_{DS(on)}$ = 98 mΩ at $V_{GS} = 4.5$ V, $I_D = 1.6$ A
- $R_{DS(on)}$ = 82 mΩ at $V_{GS} = 10$ V, $I_D = 1.7$ A
- Typ $Q_{g(TOT)}$ = 9.2 nC at $V_{GS} = 10$ V
- Low Miller Charge
- UIS Capability
- AEC-Q101 Qualified and PPAP Capable
- This Device is Pb-Free, Halide Free and is RoHS Compliant

Applications

- DC/DC Converter
- Motor Drives

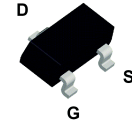
MOSFET MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Ratings	Unit
V_{DS}	Drain to Source Voltage	60	V
V_{GS}	Gate to Source Voltage	± 20	V
I_D	Drain Current Continuous ($V_{GS} = 10$ V)	1.7	A
	Pulsed	10	
E_{AS}	Single Pulse Avalanche Energy (Note 1)	74	mJ
P_D	Power Dissipation	1.1	W
T_J, T_{STG}	Operating and Storage Temperature	-55 to $+150$	$^\circ\text{C}$
$R_{\theta JC}$	Thermal Resistance Junction to Case	75	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance Junction to Ambient TO-252, 1 in ² Copper Pad Area	111	$^\circ\text{C/W}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

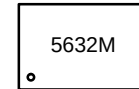
1. E_{AS} of 74 mJ is 100% test at $L = 80$ mH, $I_{AS} = 1.4$ A, starting $T_J = 25^\circ\text{C}$

V_{DD}	$r_{DS(on)}$ MAX	I_D MAX
60 V	82 mΩ @ 10 V	1.6 A
	98 mΩ @ 4.5 V	



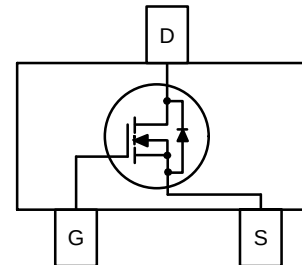
SOT-23/SUPERSOT™-23, 3 LEAD, 1.4x2.9
CASE 527AG

MARKING DIAGRAM



5632 = Specific Device Code
M = Date Code

PIN ASSIGNMENT



ORDERING INFORMATION

See detailed ordering and shipping information on page 5 of this data sheet.

FDN5632N-F085

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

$B_{V_{DS}}$	Drain to Source Breakdown Voltage	$I_D = 250\ \mu\text{A}$, $V_{GS} = 0\ \text{V}$	60	–	–	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 48\ \text{V}$, $V_{GS} = 0\ \text{V}$	–	–	1	μA
		$V_{DS} = 48\ \text{V}$, $V_{GS} = 0\ \text{V}$, $T_A = 125^\circ\text{C}$	–	–	250	
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 20\ \text{V}$	–	–	± 100	nA

ON CHARACTERISTICS

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 250\ \mu\text{A}$	1	2.0	3	V
$r_{DS(on)}$	Drain to Source On Resistance	$I_D = 1.7\ \text{A}$, $V_{GS} = 10\ \text{V}$	–	57	82	$\text{m}\Omega$
		$I_D = 1.6\ \text{A}$, $V_{GS} = 6\ \text{V}$	–	62	88	
		$I_D = 1.6\ \text{A}$, $V_{GS} = 4.5\ \text{V}$	–	70	98	
		$I_D = 1.7\ \text{A}$, $V_{GS} = 10\ \text{V}$, $T_A = 150^\circ\text{C}$	–	107	135	

DYNAMIC CHARACTERISTICS

C_{iss}	Input Capacitance	$V_{DS} = 15\ \text{V}$, $V_{GS} = 0\ \text{V}$, $f = 1\ \text{MHz}$	–	475	–	pF
C_{oss}	Output Capacitance		–	60	–	pF
C_{rss}	Reverse Transfer Capacitance		–	30	–	pF
R_G	Gate Resistance	$f = 1\ \text{MHz}$	–	1.4	–	Ω
$Q_{g(TOT)}$	Total Gate Charge at 10 V	$V_{GS} = 0$ to 10 V, $V_{DD} = 20\ \text{V}$, $I_D = 1.7\ \text{A}$	–	9.2	12	nC
Q_{gs}	Gate to Source Gate Charge	$V_{DD} = 20\ \text{V}$, $I_D = 1.7\ \text{A}$	–	1.5	–	nC
Q_{gd}	Gate to Drain "Miller" Charge		–	1.4	–	nC

SWITCHING CHARACTERISTICS

t_{on}	Turn-On Time	$V_{DD} = 30\ \text{V}$, $I_D = 1.0\ \text{A}$ $V_{GS} = 10\ \text{V}$, $R_{GEN} = 6\ \Omega$	–	–	30	ns
$t_{d(on)}$	Turn-On Delay Time		–	15	–	ns
t_r	Rise Time		–	1.7	–	ns
$t_{d(off)}$	Turn-Off Delay Time		–	5.2	–	ns
t_f	Fall Time		–	1.3	–	ns
t_{off}	Turn-Off Time		–	–	12.9	ns

DRAIN-SOURCE DIODE CHARACTERISTICS

V_{SD}	Source to Drain Diode Voltage	$I_{SD} = 1.7\ \text{A}$	–	0.8	1.25	V
		$I_{SD} = 0.85\ \text{A}$	–	0.8	1.0	
t_{rr}	Reverse Recovery Time	$I_{SD} = 1.7\ \text{A}$, $di_{SD}/dt = 100\ \text{A}/\mu\text{s}$	–	16.0	21	ns
Q_{rr}	Reverse Recovery Charge		–	7.9	10.3	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL CHARACTERISTICS

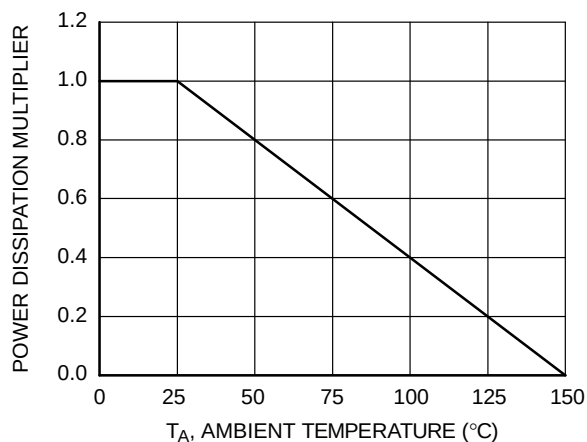


Figure 1. Normalized Power Dissipation vs. Case Temperature

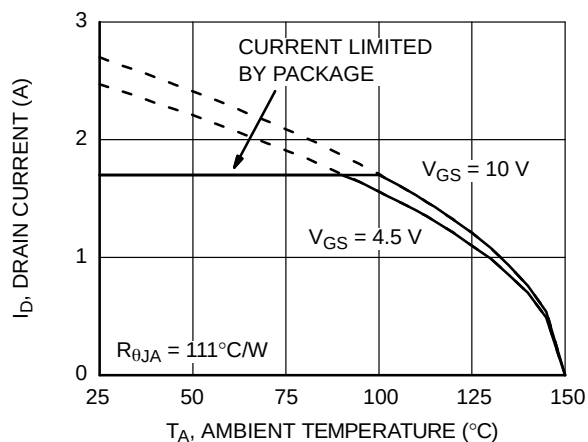


Figure 2. Maximum Continuous Drain Current vs. Case Temperature

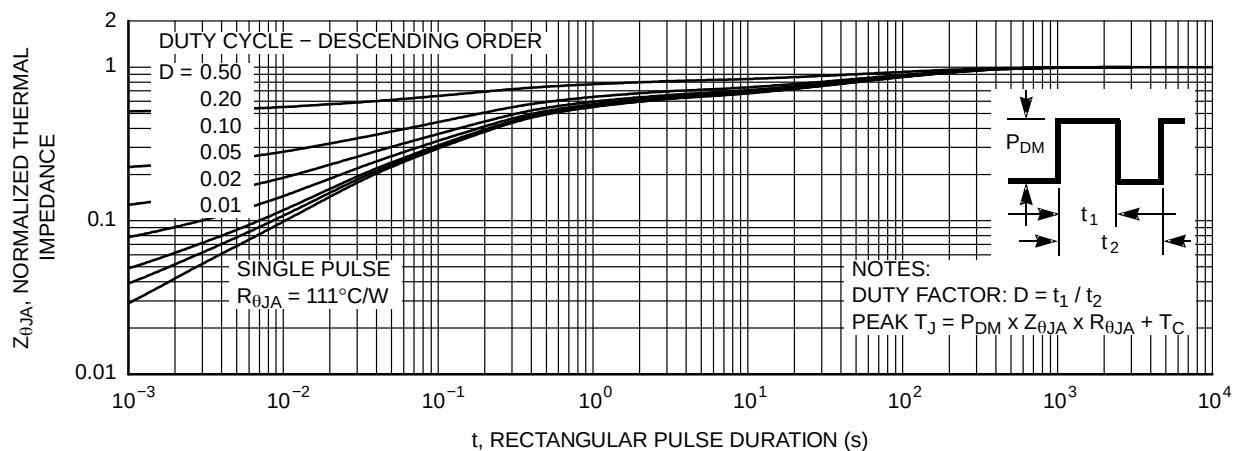


Figure 3. Normalized Maximum Transient Thermal Impedance

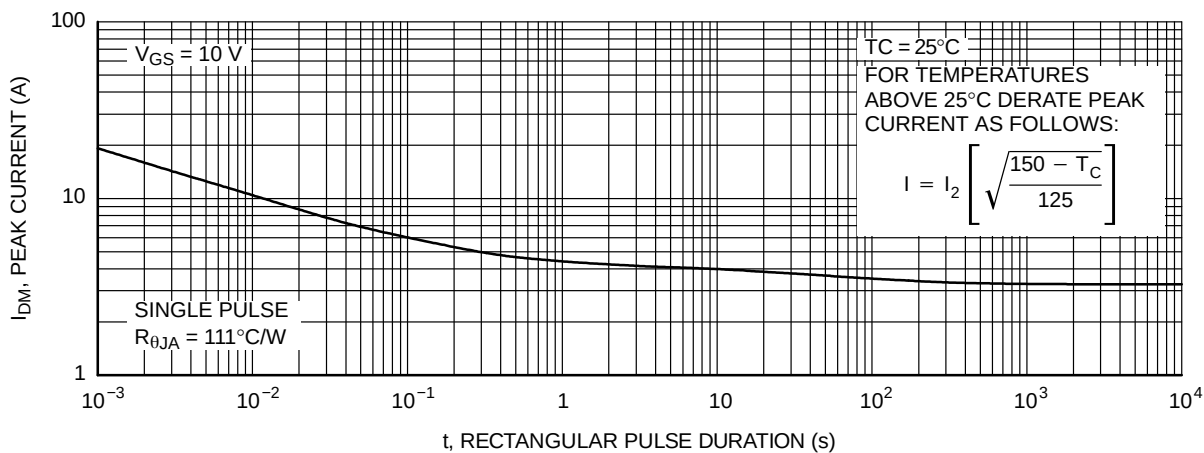


Figure 4. Peak Current Capability

TYPICAL CHARACTERISTICS

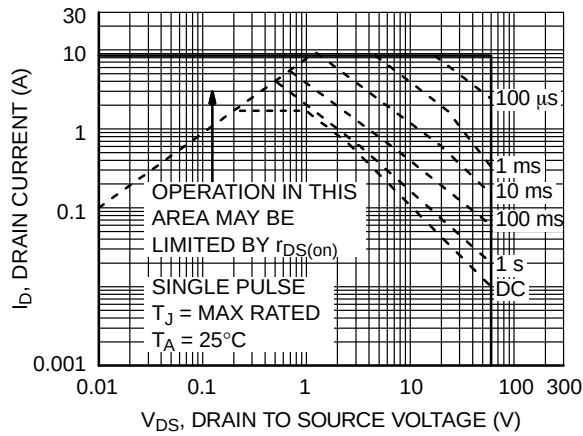


Figure 5. Forward Bias Safe Operating Area

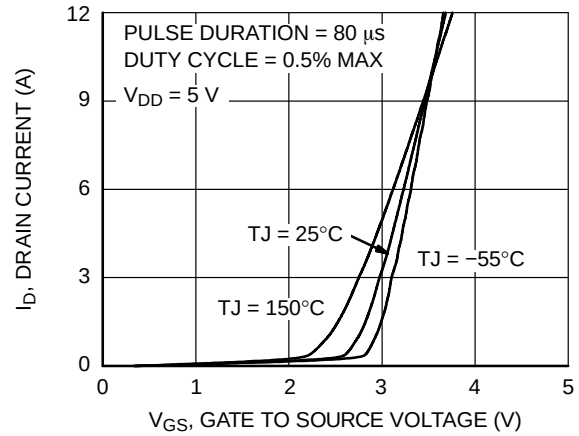


Figure 6. Transfer Characteristics

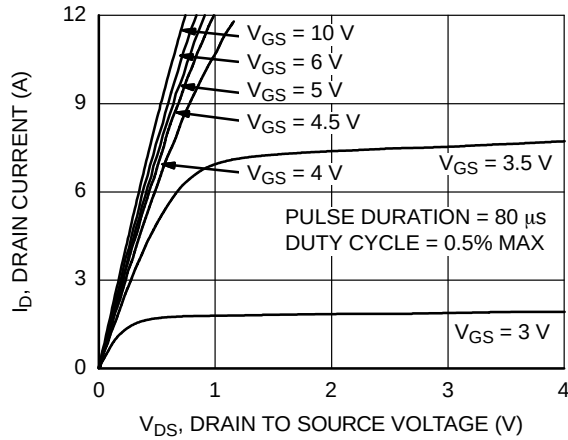


Figure 7. Saturation Characteristics

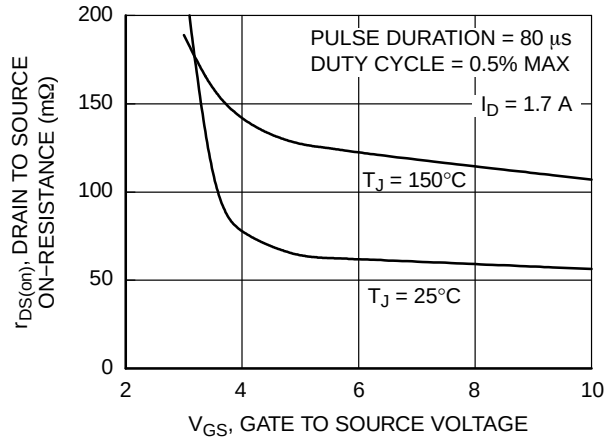


Figure 8. Drain to Source On-Resistance Variation vs. Gate to Source Voltage

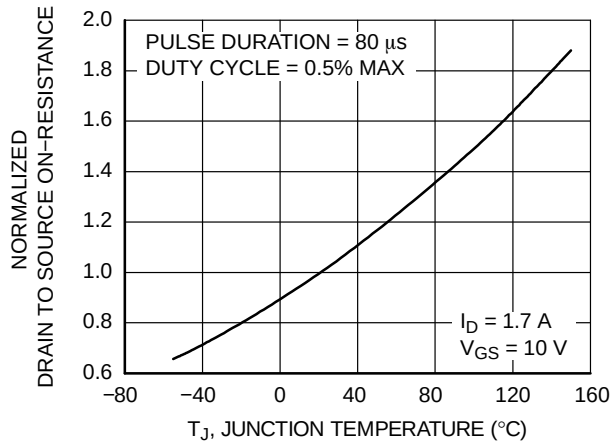


Figure 9. Normalized Drain to Source On-Resistance vs. Junction Temperature

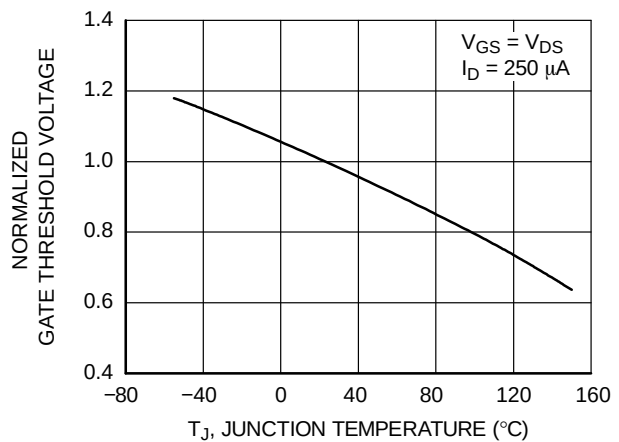


Figure 10. Normalized Gate Threshold Voltage vs. Junction Temperature

TYPICAL CHARACTERISTICS

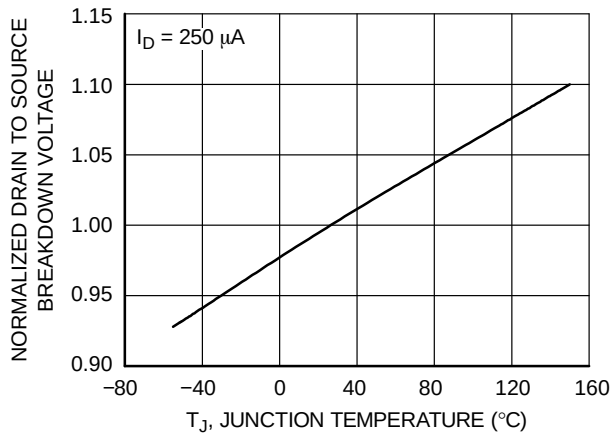


Figure 11. Normalized Drain to Source Breakdown Voltage vs. Junction Temperature

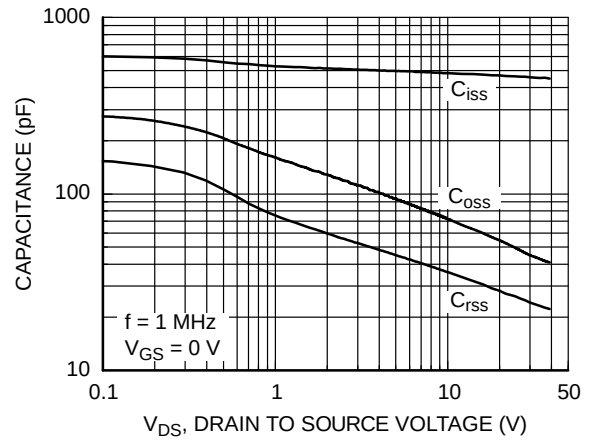


Figure 12. Capacitance vs. Drain to Source Voltage

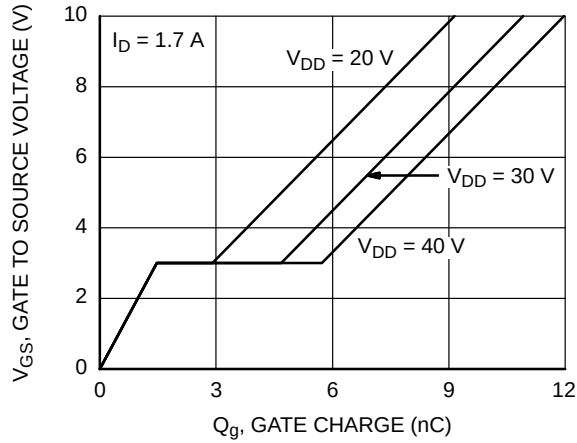


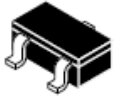
Figure 13. Gate Charge vs. Gate to Source Voltage

PACKAGE MARKING AND ORDERING INFORMATION

Device	Device Marking	Package	Reel Size	Tape Width	Shipping [†]
FDN5632N-F085	5632	SOT-23/SUPERSOT-23, 3 LEAD, 1.4x2.9 (Pb-Free, Halide Free)	7"	8 mm	3000 / Tape & Reel

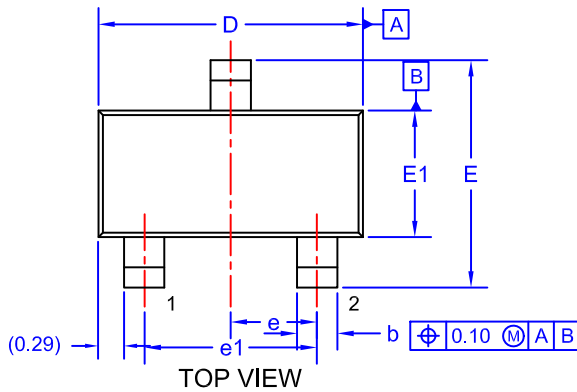
[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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SOT-23/SUPERSOT™ –23, 3 LEAD, 1.4x2.9
CASE 527AG
ISSUE A

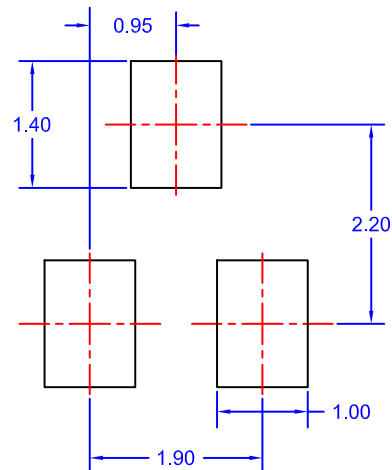
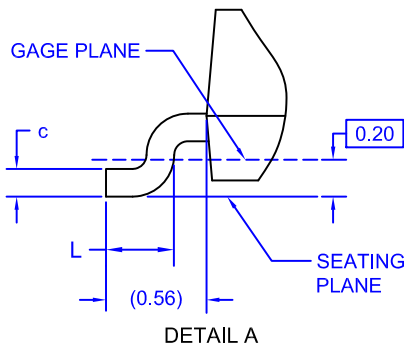
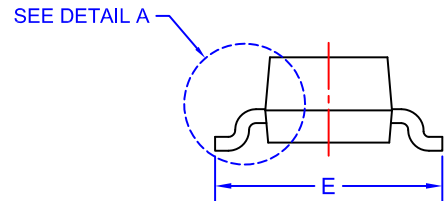
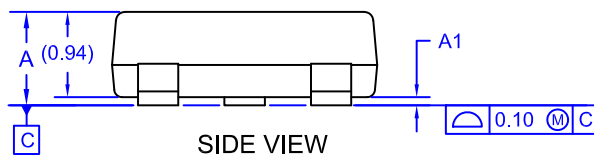
DATE 09 DEC 2019



NOTES: UNLESS OTHERWISE SPECIFIED

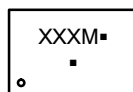
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR EXTRUSIONS.

DIM	MIN.	NOM.	MAX.
A	0.85	0.95	1.12
A1	0.00	0.05	0.10
b	0.370	0.435	0.508
c	0.085	0.150	0.180
D	2.80	2.92	3.04
E	2.31	2.51	2.71
E1	1.20	1.40	1.52
e	0.95 BSC		
e1	1.90 BSC		
L	0.33	0.38	0.43



*FOR ADDITIONAL INFORMATION ON OUR Pb-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXX = Specific Device Code
M = Month Code
▪ = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	SOT-23/SUPERSOT-23, 3 LEAD, 1.4X2.9	PAGE 1 OF 1

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