REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Added device type 03. Updated format, editorial changes throughout.	94-08-10	M. A. Frye
B	Boilerplate update, part of 5 year review. ksr	07-05-25	Robert M. Heber

FIRST PAGE HAS BEEN REPLACED

REV																			
SHEET																			
REV	B	B	B	B	B	B													
SHEET	15	16	17	18	19	20													

REV STATUS	REV	B	B	B	B	B	B	B	B	B	B	B	B	B	B
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

PREPARED BY
Kenneth Rice

CHECKED BY
Rajesh Pithadia

APPROVED BY
Michael Frye

DRAWING APPROVAL DATE
93-08-05

REVISION LEVEL
B

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43218-3990
http://www.dscc.dla.mil

MICROCIRCUIT, MEMORY, DIGITAL, CMOS, UV ERASABLE PROGRAMMABLE LOGIC DEVICE, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**5962-92062**

SHEET 1 OF 20

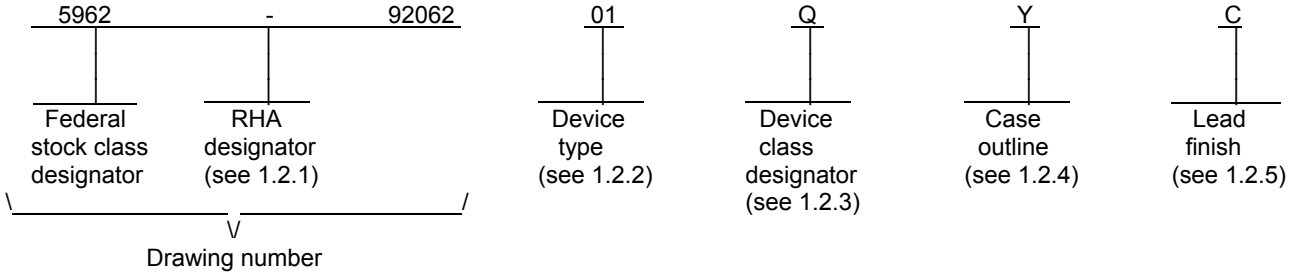
DSCC FORM 2233
APR 97

5962-E316-07

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number 1/	Circuit function	Propagation delay time
01		192 Macrocell EPLD	40 ns
02		192 Macrocell EPLD	30 ns
03		192 Macrocell EPLD	35 ns

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	GQCC1-J84E	84	"J" lead chip carrier 2/
Y	CMGA15-P84E	84	Pin grid array 2/
Z	CMGA3-P84E	84	Pin grid array 2/

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1/ Generic numbers are listed on the Standard Microcircuit Drawing Source Approval Bulletin at the end of this document and will also be listed in QML-38535 and MIL-HDBK-103 (see 6.6 herein).

2/ Lid shall be transparent to permit ultraviolet light erasure.

1.3 Absolute maximum ratings. 3/

Supply voltage range (V_{CC}) ---------- -2.0 V dc to +7.0 V dc
DC input voltage range ---------- -2.0 V dc to +7.0 V dc 4/
Maximum power dissipation ---------- 2.5 W 5/
Lead temperature (soldering, 10 seconds) ---------- +260°C
Thermal resistance, junction-to-case (θ_{JC}):
Case outlines X, Y, and Z ---------- See MIL-STD-1835
Junction temperature (T_J) ---------- +175°C
Storage temperature range ---------- -65°C to +150°C
Temperature under bias range ---------- -55°C to +125°C
Endurance ---------- 25 erase/write cycles (minimum)
Data retention ---------- 10 years (minimum)

1.4 Recommended operating conditions.

Supply voltage range (V_{CC}) ---------- +4.5 V dc to +5.5 V dc
Ground voltage (GND) ---------- 0 V dc
Input high voltage (V_{IH}) ---------- 2.2 V dc minimum
Input low voltage (V_{IL}) ---------- 0.8 V dc maximum
Case operating temperature range (T_C) ---------- -55°C to +125°C 6/
Input rise time (t_R) ---------- 100 ns maximum
Input fall time (t_F) ---------- 100 ns maximum

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ or http://assist.daps.dla.mil from the Standardization Document Order Desk, 700 Robins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

3/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

4/ Minimum dc input voltage is -0.3 V. During transitions, inputs may undershoot to -2.0 V for periods less than 20 ns. Maximum dc voltage on output pins is V_{CC} + 0.3 V, which may overshoot to +7.0 V for periods less than 20 ns under no load conditions.

5/ Must withstand the added P_D due to short circuit test (e.g., I_{SC}).

6/ Case temperatures are instant on.

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation.

AMERICAN SOCIETY FOR TESTING AND MATERIALS (ASTM)

ASTM Standard F1192-00 - Standard Guide for the Measurement of Single Event Phenomena from Heavy Ion Irradiation of Semiconductor Devices.

(Applications for copies of ASTM publications should be addressed to: ASTM International, PO Box C700, 100 Barr Harbor Drive, West Conshohocken, PA 19428-2959; http://www.astm.org.)

ELECTRONICS INDUSTRIES ASSOCIATION (EIA)

JEDEC Standard EIA/JESD78 - IC Latch-Up Test.

(Applications for copies should be addressed to the Electronics Industries Association, 2500 Wilson Boulevard, Arlington, VA 22201; http://www.jedec.org.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table(s). The truth table shall be as specified on figure 2.

3.2.4.1 Unprogrammed devices. The truth table for unprogrammed devices for contracts involving no altered item drawing shall be as specified on figure 2. When required in screening (see 4.2 herein), or qualification conformance inspection groups A, B, C, or D (see 4.4 herein), the devices shall be programmed by the manufacturer prior to test. A minimum of 50 percent of the total number of gates shall be programmed or at least 25 percent of the total number of gates to any altered item drawing.

3.2.4.2 Programmed devices. The truth table for programmed devices shall be as specified by an attached altered item drawing.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change that affects this drawing.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 42 (see MIL-PRF-38535, appendix A).

3.11 Processing EPLDs. All testing requirements and quality assurance provisions herein shall be satisfied by the manufacturer prior to delivery.

3.12.1 Erasure of EPLDs. When specified, devices shall be erased in accordance with the procedures and characteristics specified in 4.6.

3.12.2 Programmability of EPLDs. When specified, devices shall be programmed to the specified pattern using the procedures and characteristics specified in 4.5.

3.12.3 Verification of erasure or programmed EPLDs. When specified, devices shall be verified as either programmed (see 4.5) to the specified pattern or erased (see 4.6). As a minimum, verification shall consist of performing a functional test (subgroup 7) to verify that all bits are in the proper state. Any bit that does not verify to be in the proper state shall constitute a device failure, and shall be removed from the lot.

3.13 Endurance. A reprogrammability test shall be completed as part of the vendor's reliability monitor. This reprogrammability test shall be done only for initial characterization and after any design or process changes which may affect the reprogrammability of the device. The methods and procedures may be vendor specific, but will guarantee the number of program/erase endurance cycles listed in section 1.3 herein. The vendors procedure shall be under document control and shall be made available upon request.

3.14 Data retention. A data retention stress test shall be completed as part of the vendor's reliability process. This test shall be done initially and after any design or process change which may affect data retention. The methods and procedures may be vendor specific, but will guarantee the number of years listed in section 1.3 herein. The vendors procedure shall be under document control and shall be made available upon request. Data retention capability shall be guaranteed over the full military temperature range.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limit		Unit
					Min	Max	
Output high voltage	V_{OH}	V_{CC} = 4.5 V, I_{OH} = -4 mA V_{IH} = 2.2 V, V_{IL} = 0.8 V	1,2,3	All	2.4		V
Output low voltage	V_{OL}	V_{CC} = 4.5 V, I_{OL} = 8 mA V_{IH} = 2.2 V, V_{IL} = 0.8 V				0.45	
Input high voltage 1/ 2/	V_{IH}				2.2		
Input low voltage 1/ 2/	V_{IL}					0.8	
Input leakage current	I_{IX}	V_{CC} = 5.5 V, V_{IN} = 5.5 V and GND			-10	+10	µA
Output leakage current	I_{OZ}	V_{CC} = 5.5 V, V_{IN} = 5.5 V and GND			-40	+40	
Output short circuit current 3/ 4/	I_{SC}	V_{CC} = 5.5 V, V_{OUT} = 0.5 V			-30	-90	mA
Power supply current 4/ 5/	I_{CC1}	V_{CC} = 5.5 V, I_{OUT} = 0 mA, V_{IN} = V_{CC} or GND f = 1.0 MHz				480	
Power supply current (standby)	I_{CC2}	V_{CC} = 5.5 V, I_{OUT} = 0 mA, V_{IN} = V_{CC} or GND,				435	
Input capacitance 2/	C_{IN}	V_{CC} = 5.0 V, T_A = +25°C, f = 1 MHz, (see 4.4.1f)	4			10	pF
Output capacitance 2/	C_{OUT}	V_{CC} = 5.0 V, T_A = +25°C, f = 1 MHz, (see 4.4.1f)	4			20	
Functional testing		See 4.4.1c	7,8A,8B				
Dedicated input to combinatorial output delay 7/	t_{PD1}	See figures 3 (circuit A) and 4 6/	9,10,11	01		40	ns
				02		30	
				03		35	
I/O input to combinatorial output delay 8/	t_{PD2}			01		65	
				02		45	
				03		55	
Dedicated input to combinatorial output delay with expander delay 9/	t_{PD3}			01		65	
				02		44	
				03		55	
I/O input to combinatorial output delay with expander delay 2/ 4/ 10/	t_{PD4}			01		90	
				02		59	
				03		75	
Input to output enable delay 4/ 7/	t_{EA}			01		40	
				02		30	
				03		35	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limit		Unit
					Min	Max	
Input to output disable delay 4/ 7/	t_{ER}	See figures 3 (circuit B) and 4 6/	9,10,11	01		40	ns
				02		30	
				03		35	
Synchronous clock input to output delay	t_{CO1}	See figures 3 (circuit A) and 4 6/		01		23	
				02		16	
				03		20	
Synchronous clock to local feedback to combinatorial output 4/ 11/	t_{CO2}			01		48	
				02		35	
				03		42	
Dedicated input or feedback setup time to synchronous clock input 7/ 12/	t_{S1}	See figures 3 (circuit A) and 4 6/		01	28		
				02	20		
				03	25		
I/O input setup time to synchronous clock input 4/ 7/ 12/	t_{S2}			01	52		
				02	39		
				03	45		
Input hold time from synchronous clock input 7/	t_H			All	0		
Synchronous clock input high time 2/	t_{WH}			01	15		
				02	10		
				03	12.5		
Synchronous clock input low time 2/	t_{WL}			01	15		
				02	10		
				03	12.5		
Asynchronous clear width 2/ 4/ 7/	t_{RW}			01	40		
				02	30		
				03	35		
Asynchronous clear recovery time 2/ 4/ 7/	t_{RR}			01	40		
				02	30		
				03	35		
Asynchronous clear to registered output delay 2/ 7/	t_{RO}			01		40	
				02		30	
				03		35	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limit		Unit
					Min	Max	
Asynchronous preset width 2/ 4/ 7/	t_{PW}	See figures 3 (circuit A) and 4 6/	9,10,11	01	40		ns
				02	30		
				03	35		
Asynchronous preset recovery time 2/ 4/ 7/	t_{PR}			01	40		
				02	30		
				03	35		
Asynchronous preset to registered output delay 2/ 7/	t_{PO}			01		40	
				02		30	
				03		35	
Synchronous clock to local feedback input 4/ 13/	t_{CF}			01		7	
				02		3	
				03		5	
External synchronous clock period ($1/f_{MAX3}$) 4/	t_P			01	30		
				02	20		
				03	25		
External feedback maximum frequency ($1/(t_{CO1} + t_{S1})$) 4/ 14/	f_{MAX1}			01	19.6		MHz
				02	27.7		
				03	22.2		
Internal local feedback maximum frequency, lesser of ($1/(t_{S1} + t_{CF})$) or ($1/t_{CO1}$) 4/ 15/	f_{MAX2}			01	28.5		
				02	43		
				03	33		
Data path maximum frequency, least of $1/(t_{WL} + t_{WH})$, $1/(t_{S1} + t_H)$ or ($1/t_{CO1}$) 4/ 16/	f_{MAX3}			01	33.3		
				02	50		
				03	40		
Maximum register toggle frequency ($1/(t_{WL} + t_{WH})$) 4/ 17/	f_{MAX4}			01	33.3		
				02	50		
				03	40		
Output data stable time from synchronous clock input 4/ 18/	t_{OH}			All	3		ns
External asynchronous switching characteristics							
Dedicated asynchronous clock input to output delay 6/	t_{ACO1}	See figures 3 (circuit A) and 4 6/	9,10,11	01		45	ns
				02		30	
				03		35	
Asynchronous clock input to local feedback to combinatorial output 2/ 19/	t_{ACO2}			01		64	
				02		46	
				03		55	
Dedicated input or feedback setup time to asynchronous clock input 6/	t_{AS1}			01	10		
				02	6		
				03	8		
I/O input setup time to asynchronous clock input 4/ 6/	t_{AS2}			01	33		
				02	27		
				03	30		
Input hold time from asynchronous clock input 6/	t_{AH}			01	12		
				02	8		
				03	10		
Asynchronous clock input high time 2/ 6/	t_{AWH}			01	20		
				02	14		
				03	16		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limit		Unit
					Min	Max	
Asynchronous clock input low time 2/ 7/ 20/	t_{AWL}	See figures 3 (circuit A) and 4 6/	9,10,11	01	20		ns
				02	11		
				03	14		
Asynchronous clock to local feedback input 4/ 21/	t_{ACF}			01		26	
				02		18	
				03		22	
External asynchronous clock period ($1/f_{MAXA4}$) 4/	t_{AP}			01	40		
				02	25		
				03	30		
External feedback maximum frequency in asynchronous mode $1/(t_{ACO1} + t_{AS1})$ 4/ 22/	f_{MAXA1}			01	18		MHz
				02	27		
				03	23		
Maximum internal asynchronous frequency 4/ 23/	f_{MAXA2}			01	25		
				02	40		
				03	33.3		
Data path maximum frequency in asynchronous mode 4/ 24/	f_{MAXA3}			01	22.2		
				02	33.3		
				03	28.5		
Maximum asynchronous register toggle frequency $1/(t_{AWH} + t_{AWL})$ 4/ 25/	f_{MAXA4}			01	25		
				02	40		
				03	33.3		
Output data stable time from asynchronous clock input 4/ 26/	t_{AOH}			All	15		ns

1/ These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
2/ Tested initially and after any design or process changes that affect that parameter, and therefore shall be guaranteed to the limits specified in table I.
3/ For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 1 second.
4/ May not be tested but shall be guaranteed to the limits specified in table I.
5/ Measured with device programmed as a 16-bit counter in each LAB.
6/ AC tests are performed with input rise and fall times of 6 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V, and the output loads on figure 3.
7/ This specification is a measure of the delay from input signal applied to a dedicated input to combinatorial output on any output pin. This delay assumes no expander terms are used to form the logic function. When this note is appled to any parameter specification it indicates that the signal (data, asynchronous clock, asynchronous clear, and/or asynchronous preset) is applied to a dedicated input only and no signal path (either clock or data) employs expander logic. If an input signal is applied to an I/O pin, an additional delay equal to t_{PIA} should be added to the comparable delay for a dedicated input. If expanders are used, add the maximum expander delay t_{EXP} to the overall delay for the comparable delay without expanders.
8/ This specification is a measure of the delay from input signal applied to an I/O macrocell pin to any output. This delay assumes no expander terms are used to form the logic function.
9/ This specification is a measure of the delay from an input signal applied to a dedicated input to combinatorial output on any output pin. This delay assumes expander terms are used to form the logic function and includes the worst-case expander logic delay for one pass through the expander logic.
10/ This specification is a measure of the delay from an input signal applied to an I/O macrocell pin to any output. This delay assumes expander terms are used to form the logic function and includes the worst-case expander logic delay for one pass through the expander logic.

TABLE I. Electrical performance characteristics - Continued.

11/ This specification is a measure of the delay from synchronous register clock to internal feedback of the register output signal to the input of the LAB logic array and then to a combinatorial output. This delay assumes no expanders are used, register is synchronously clocked and all feedback is within the same LAB.

12 If data is applied to an I/O input for capture by a macrocell register, the I/O pin set-up time minimums should be observed. These parameters are t_{S2} for synchronous operation and t_{AS2} for asynchronous operation.

13/ This specification is a measure of the delay associated with the internal register feedback path. This is the delay from synchronous clock to LAB logic array input. This delay plus the register set-up time, t_{S1}, is the minimum internal period for an internal synchronous state machine configuration. This delay is for feedback within the same LAB.

14/ This specification indicates the guaranteed maximum frequency, in synchronous mode, at which a state machine configuration with external feedback can operate. It is assumed that all data inputs and feedback signals are applied to dedicated inputs. All feedback is assumed to be local, originating within the same LAB.

15/ This specification indicates the guaranteed maximum frequency at which a state machine, with internal-only feedback, can operate. If register output states must also control external points, this frequency can still be observed as long as this frequency is less than $1/t_{CO1}$.

16/ This frequency indicates the maximum frequency at which the device may operate in data path mode. This delay assumes data input signals are applied to dedicated inputs and no expander logic is used. If any of the data inputs are I/O pins, t_{S2} is the appropriate t_S for calculation.

17/ This specification indicates the guaranteed maximum frequency, in synchronous mode, at which an individual output or buried register can be cycled by a clock signal applied to the dedicated clock input pin.

18/ This parameter indicates the minimum time after a synchronous register clock input that the previous register output data is maintained on the output pin.

19/ This specification is a measure of the delay from an asynchronous register clock input to internal feedback of the register output signal to the input of the LAB logic array and then to a combinatorial output. This delay assumes no expanders are used in the logic of combinatorial output or the asynchronous clock input. The clock signal is applied to a dedicated input pin and all feedback is within a single LAB.

20/ This parameter is measured with a positive-edge triggered clock at the register. For negative edge triggering, the t_{AWH} and t_{AWL} parameters must be swapped. If a given input is used to clock multiple registers with both positive and negative polarity, t_{AWH} should be used for both t_{AWH} and t_{AWL}.

21/ This specification is a measure of the input delay associated with the internal register feedback path for an asynchronous clock to LAB logic array input. This delay plus the asynchronous register set-up time, t_{AS1}, is the minimum internal period for an internal asynchronous clocked state machine configuration. This delay is for feedback within the same LAB, assumes no expander logic in the clock path, and assumes that the clock input signal is applied to a dedicated input pin.

22/ This specification indicates the guaranteed maximum frequency at which an asynchronously clocked state machine configuration with external feedback can operate. It is assumed that all data inputs, clock inputs, and feedback signals are applied to dedicated inputs, and that no expander logic is employed in the clock signal path or data path.

23/ This specification indicates the guaranteed maximum frequency at which an asynchronously clocked state machine with internal-only feedback can operate. This parameter is determined by the lesser of $(1/(t_{ACF} + 1/t_{AS1}))$ or $(1/(t_{AWH} + t_{AWL}))$. If register output states must also control external points, this frequency can still be observed as long as this frequency is less than $1/t_{ACO1}$.

24/ This frequency is the maximum frequency at which the device may operate in the asynchronously clocked data path mode. This specification is determined by the least of $1/(t_{AWH} + t_{AWL})$,$1/(t_{AS1} + t_{AH})$ or $1/t_{ACO1}$. It assumes data and clock input signals are applied to dedicated input pins and no expander logic is used.

25/ This specification indicates the guaranteed maximum frequency at which an individual output or buried register can be cycled in asynchronously clocked mode by a clock signal applied to an external dedicated input pin.

26/ This parameter indicates the minimum time that the previous register output data is maintained on the output after an asynchronous register clock input applied to an external dedicated input pin.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Delete the sequence specified as initial (preburn-in) electrical parameters through interim (postburn-in) electrical parameters of method 5004 and substitute lines 1 through 6 of table IIA herein.

b. Prior to burn-in, the devices shall be programmed (see 4.5 herein) with a checkerboard pattern or equivalent (manufacturers at their option may employ an equivalent pattern provided it is a topologically true alternating bit pattern). The pattern shall be read before and after burn-in. Devices having bits not in the proper state after burn-in shall constitute a device failure and shall be included in the PDA calculation and shall be removed from the lot (see 4.2.3 herein). The manufacturer as an option may use built-in test circuitry by testing the entire lot to verify programmability and AC performance without programming the user array.

c. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015.

(1) Dynamic burn-in (method 1015 of MIL-STD-883, test condition D; for circuit, see 4.2.1b herein).

d. Interim and final electrical test parameters shall be as specified in table IIA herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 5 and 6 of table I of method 5005 of MIL-STD-883 shall be omitted.

c. For device class M, subgroups 7, 8A, and 8B tests shall be sufficient to verify the truth table. For device classes Q and V, subgroups 7, 8A, and 8B shall include verifying the functionality of the device, these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).

d. Devices shall be tested for programmability and ac performance compliance to the requirements of Group A, subgroups 9, 10, and 11. Either of two techniques is acceptable:

(1) Testing all devices submitted for test using additional built-in test circuitry which allows the manufacturer to verify programmability and ac performance without programming the user array. If this is done, the resulting test patterns shall be verified on all devices during subgroups 9, 10, and 11, group A testing per the sampling plan specified in MIL-STD-883, method 5005.

(2) If such compliance cannot be tested on an unprogrammed device, all samples submitted for testing shall be programmed in accordance with 3.2.4.1 or 3.2.4.2 as applicable. After completion of all testing, the devices shall be erased and verified except devices submitted to groups C and D testing.

e. O/V (latch-up) tests shall be measured only for initial qualification and after any design or process changes which may affect the performance of the device. For device class M, procedures and circuits shall be maintained under document revision level control by the manufacturer and shall be made available to the preparing activity or acquiring activity upon request. For device classes Q and V, the procedures and circuits shall be under the control of the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the preparing activity or acquiring activity upon request. Testing shall be on all pins, on five devices with zero failures. Latch-up test shall be considered destructive. Information contained in JEDEC Standard EIA/JESD78 may be used for reference.

f. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for initial qualification and after any process or design changes which may affect input or output capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency of 1 MHz. Sample size is 15 devices with no failures, and all input and output terminals tested.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ± 5°C, after exposure, to the subgroups specified in table IIA herein.

Case outline X

Device types	All	Device types	All	Device types	All
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	INPUT / CLK	35	I/O	68	I/O
2	INPUT	36	I/O	69	I/O
3	V_{CC}	37	I/O	70	I/O
4	I/O	38	I/O	71	I/O
5	I/O	39	GND	72	I/O
6	I/O	40	GND	73	I/O
7	I/O	41	INPUT	74	I/O
8	I/O	42	INPUT	75	I/O
9	I/O	43	INPUT	76	I/O
10	I/O	44	INPUT	77	I/O
11	I/O	45	V_{CC}	78	I/O
12	I/O	46	I/O	79	I/O
13	I/O	47	I/O	80	I/O
14	I/O	48	I/O	81	GND
15	I/O	49	I/O	82	GND
16	I/O	50	I/O	83	INPUT
17	I/O	51	I/O	84	INPUT
18	GND	52	I/O		
19	GND	53	I/O		
20	I/O	54	I/O		
21	I/O	55	I/O		
22	I/O	56	I/O		
23	I/O	57	I/O		
24	V_{CC}	58	I/O		
25	I/O	59	I/O		
26	I/O	60	GND		
27	I/O	61	GND		
28	I/O	62	I/O		
29	I/O	63	I/O		
30	I/O	64	I/O		
31	I/O	65	I/O		
32	I/O	66	V_{CC}		
33	I/O	67	I/O		
34	I/O				

FIGURE 1. Terminal connections.

Case outline Y

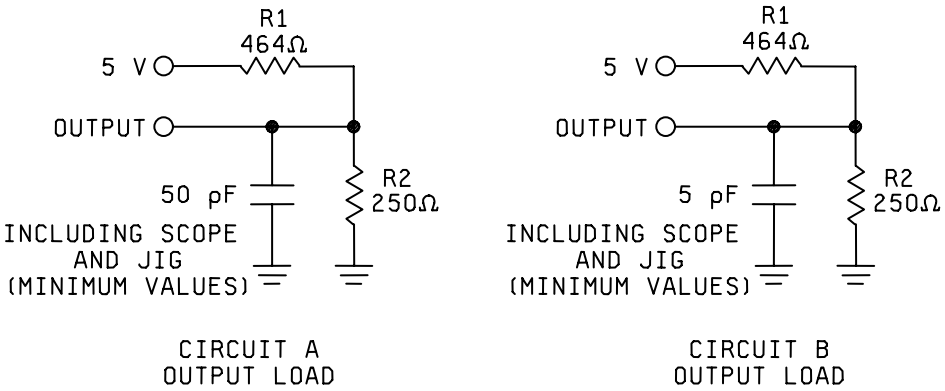
Device types	All	Device types	All	Device types	All
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
A1	I/O	C11	I/O	J2	I/O
A2	I/O	D1	I/O	J5	I/O
A3	I/O	D2	I/O	J6	INPUT
A4	I/O	D10	I/O	J7	INPUT
A5	INPUT	D11	I/O	J10	I/O
A6	INPUT / CLK	E1	GND	J11	I/O
A7	GND	E2	GND	K1	I/O
A8	I/O	E3	I/O	K2	I/O
A9	I/O	E9	I/O	K3	I/O
A10	I/O	E10	V_{CC}	K4	I/O
A11	I/O	E11	I/O	K5	GND
B1	I/O	F1	I/O	K6	INPUT
B2	I/O	F2	I/O	K7	V_{CC}
B3	I/O	F3	I/O	K8	I/O
B4	I/O	F9	I/O	K9	I/O
B5	V_{CC}	F10	I/O	K10	I/O
B6	I/O	F11	I/O	K11	I/O
B7	GND	G1	I/O	L1	I/O
B8	I/O	G2	V_{CC}	L2	/O
B9	I/O	G3	I/O	L3	I/O
B10	I/O	G9	I/O	L4	I/O
B11	I/O	G10	GND	L5	GND
C1	I/O	G11	GND	L6	I/O
C2	I/O	H1	I/O	L7	INPUT
C5	I/O	H2	I/O	L8	I/O
C6	INPUT	H10	I/O	L9	I/O
C7	INPUT	H11	I/O	L10	I/O
C10	I/O	J1	I/O	L11	I/O

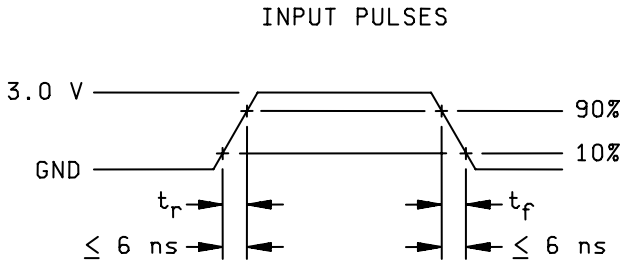
FIGURE 1. Terminal connections – Continued.

Truth Table		
Input pins		Output pins
I / CLK	I	I/O
X	X	Z

NOTES:
1. X = Don't care.
2. Z = High impedance.

FIGURE 2. Truth table (unprogrammed).





AC test conditions

Input pulse level	GND to 3.0 V
Input rise and fall levels	≤ 6 ns
Input timing reference levels	1.5 V
Output reference levels	1.5 V

FIGURE 3. Output load circuits and test conditions.

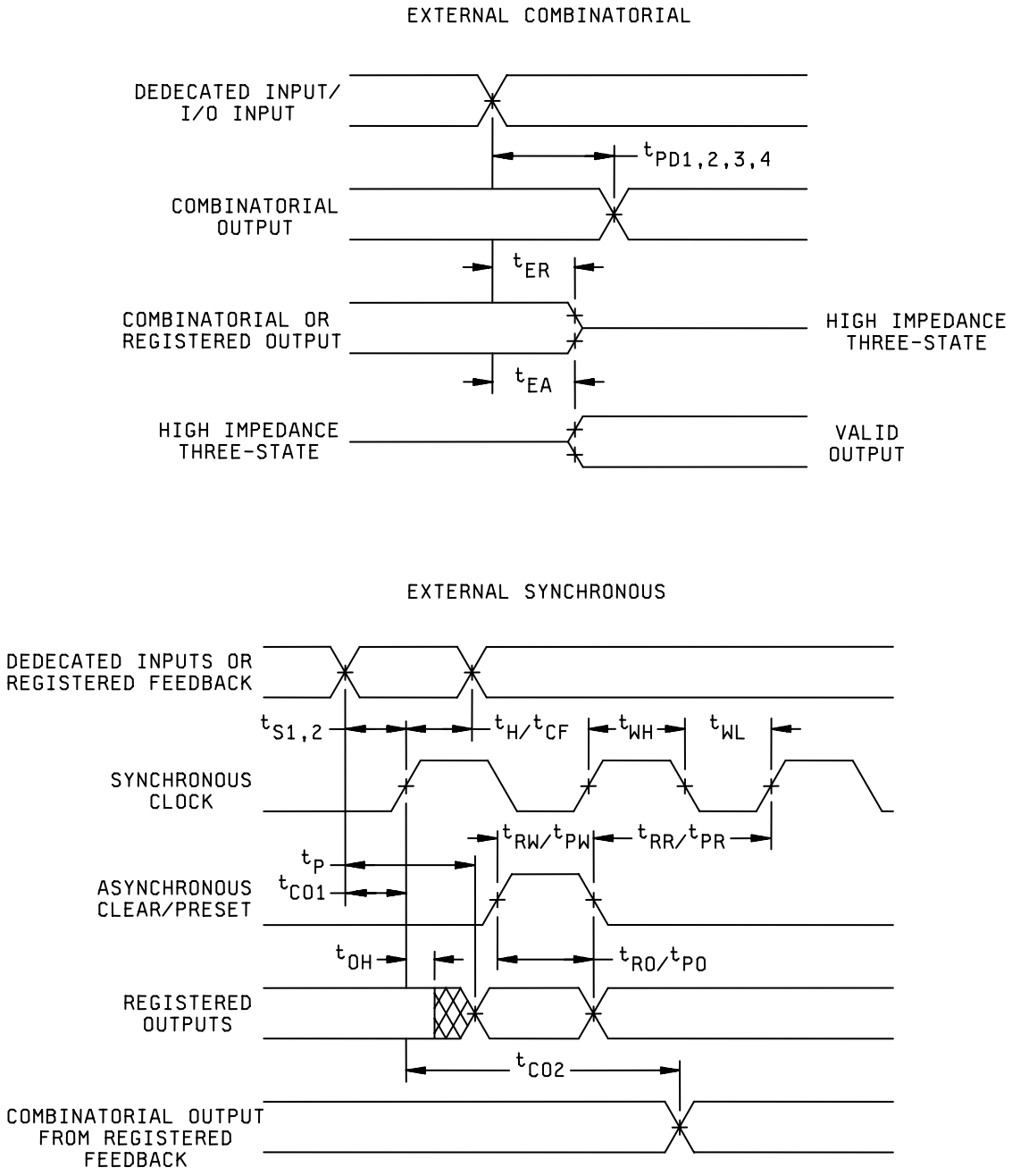


FIGURE 4. Switching waveforms.

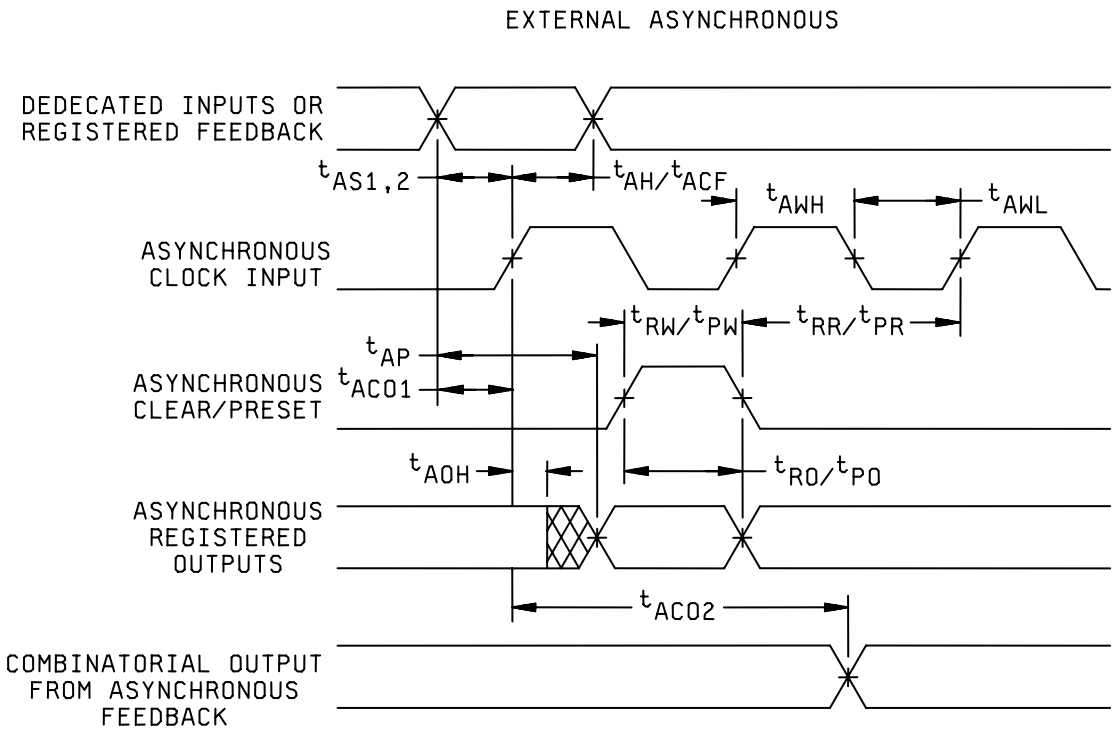


FIGURE 4. Switching waveforms - Continued.

TABLE IIA. Electrical test requirements. 1/ 2/ 3/ 4/ 5/ 6/ 7/

Line no.	Test requirements	Subgroups (in accordance with MIL-STD-883, TM 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
		Device class M	Device class Q	Device class V
1	Interim electrical parameters (see 4.2)		1, 7, 9	1, 7, 9
2	Static burn-in (method 1015)	Not required	Not required	Required
3	Same as line 1			1*, 7* Δ
4	Dynamic burn-in (method 1015)	Required	Required	Required
5	Same as line 1			1*, 7* Δ
6A	Final electrical parameters (see 4.2) (unprogrammed devices)	1*, 2, 3, 7*, 8A, 8B	1*, 2, 3, 7*, 8A, 8B	1*, 2, 3, 7*, 8A, 8B
6B	Final electrical parameters (see 4.2) (programmed devices)	1*, 2, 3, 7*, 8A, 8B,9	1*, 2, 3, 7*, 8A, 8B,9	1*, 2, 3, 7*, 8A, 8B,9
7	Group A test requirements (see 4.4)	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11
8	Group C end-point electrical parameters (see 4.4)	2, 3, 7, 8A, 8B	2, 3, 7, 8A, 8B Δ	2, 3, 7, 8A, 8B, 9, 10, 11 Δ
9	Group D end-point electrical parameters (see 4.4)	2, 3, 7, 8A, 8B	2, 3, 7, 8A, 8B	2, 3, 7, 8A, 8B
10	Group E end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9	1, 7, 9

1/ Blank spaces indicate tests are not applicable.
2/ Any or all subgroups may be combined when using high-speed testers.
3/ Subgroups 7 and 8 functional tests shall verify the truth table.
4/ * indicates PDA applies to subgroup 1 and 7.
5/ ** see 4.4.1f.
6/ See 4.4.1e.
7/ Δ indicates delta limit (see table IIB) shall be required where specified, and the delta values shall be computed with reference to the previous interim electrical parameters (see line 1).

Table IIB. Delta limits at +25°C.

Parameter 1/	Device types
	All
I_{OZ}	±4 μA of specified value in table I
I_{IX}	±1.0 μA of specified value in table I

1/ The above parameter shall be recorded before and after the required burn-in and life tests to determine the delta.

4.5 Programming procedure. The programming procedures shall be as specified by the device manufacturer and shall be made available upon request.

4.6 Erasing procedures. The recommended erasure procedure is exposure to shortwave ultraviolet light which has a wavelength of 2537 angstroms (Å). The integrated dose (i.e., ultraviolet intensity x exposure time) for erasure should be a minimum of fifteen (15) Ws/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with a 1200 $\mu W/cm^2$ power rating. The device should be placed within one inch of the lamp tubes during erasure. The maximum integrated dose the device can be exposed to without damage is 7258 Ws/cm^2 (1 week at 12,000 $\mu W/cm^2$). Exposure of the device to high intensity ultraviolet light for long periods may cause permanent damage.

4.7 Delta measurements for device classes Q and V. Delta measurements, as specified in table IIA, shall be made and recorded before and after the required burn-in screens and steady-state life tests to determine delta compliance. The electrical parameters to be measured, with associated delta limits are listed in table IIB. The device manufacturer may, at his option, either perform delta measurements or within 24 hours after burn-in perform final electrical parameter tests, subgroups 1, 7, and 9.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

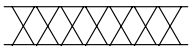
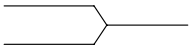
6.4 Comments. Comments on this drawing should be directed to DSCC-VA , Columbus, Ohio 43218-3990, or telephone (614) 692-0547.

6.5 Symbols, definitions, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535, MIL-STD-1331, and as follows:

C_{IN} ..... Input terminal capacitance.
C_{OUT} ..... Output terminal capacitance.
GND ..... Ground zero voltage potential.
I_{CC} ..... Supply current.
I_{IX} ..... Input current.
I_{OZ} ..... Output current.
T_C ..... Case temperature.
V_{CC} ..... Positive supply voltage.

6.5.1 Timing limits. The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. For example, address setup time would be shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. For example, the access time would be shown as a maximum since the device never provides data later than that time.

6.5.2 Waveforms.

Waveform symbol	Input	Output
	MUST BE VALID	WILL BE VALID
	CHANGE FROM H TO L	WILL CHANGE FROM H TO L
	CHANGE FROM L TO H	WILL CHANGE FROM L TO H
	DON'T CARE ANY CHANGE PERMITTED	CHANGING STATE UNKNOWN
		HIGH IMPEDANCE

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 07-05-25

Approved sources of supply for SMD 5962-92062 are listed below for immediate acquisition only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DSCC maintains an online database of all current sources of supply at http://www.dscc.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9206201MXA	0C7V7	CY7C341-40HMB
5962-9206201MYC	3/ 0C7V7	EPM5192GM883B CY7C341-40RMB
5962-9206201MZA	3/	EPM5192GM883B
5962-9206202MXA	0C7V7	CY7C341-30HMB
5962-9206202MYC	3/ 0C7V7	EPM5192GM883B-2 CY7C341-30RMB
5962-9206202MZA	3/	EPM5192GM883B-2
5962-9206203MXA	65786 0C7V7	CY7C341-35HMB CY7C341-35HMB
5962-9206203MYC	0C7V7	CY7C341-35RMB

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed, contact the Vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

3/ Not available from an approved source of supply.

Vendor CAGE number	Vendor name and address
65786	Cypress Semiconductor 3901 N. First Street San Jose, CA 95134-1506
0C7V7	QP Semiconductor 2945 Oakmead Village Ct. Santa Clara, CA 95051-0812