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NCV4275C

Voltage Regulator - Low-Drop, Reset

450 mA

The NCV4275C is an integrated low dropout regulator designed for use in harsh automotive environments. It includes wide operating temperature and input voltage ranges. The output is regulated at 5.0 V or 3.3 V and is rated to 450 mA of output current. It also provides a number of features, including overcurrent protection, overtemperature protection and a programmable microprocessor reset. The NCV4275C is available in the DPAK and D^{2}PAK surface mount packages. The output is stable over a wide output capacitance and ESR range. The NCV4275C is pin for pin compatible with NCV4275A.

Features

- 5.0 V or 3.3 V ±2% Output Voltage Options
- 450 mA Output Current
- Very Low Current Consumption
- Active Reset Output
- Reset Low Down to V_Q = 1.0 V
- 500 mV (max) Dropout Voltage
- Fault Protection
  - +45 V Peak Transient Voltage
  - −42 V Reverse Voltage
  - Short Circuit Protection
  - Thermal Overload Protection
- AEC−Q100 Qualified and PPAP Capable
- These are Pb−Free Devices

Applications

- Auto Body Electronics

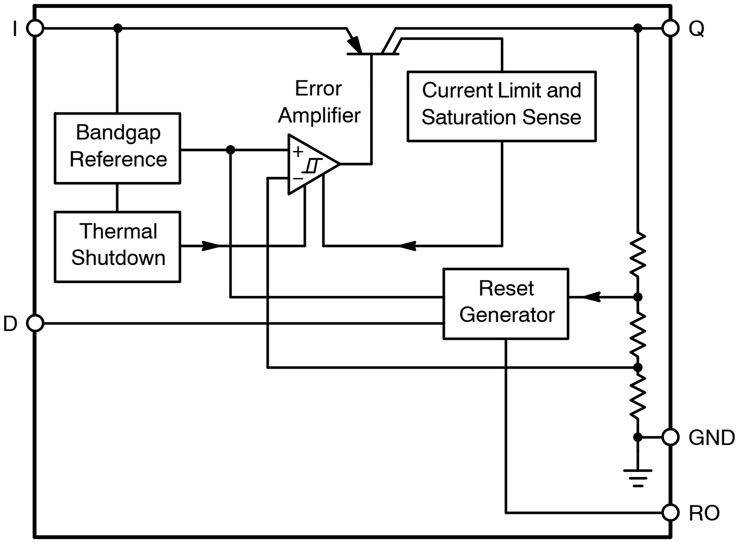

Figure 1. Block Diagram

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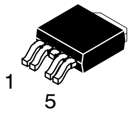
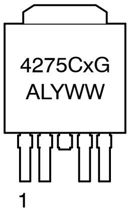
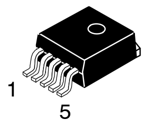
MARKING DIAGRAMS

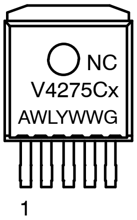


DPAK
5−PIN
DT SUFFIX
CASE 175AA





D^{2}PAK
5−PIN
DS SUFFIX
CASE 936A



x = 5 (5.0 V Output)
or 3 (3.3 V Output)
A = Assembly Location
WL, L = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

ORDERING INFORMATION

See detailed ordering and shipping information on page 13 of sheet.

October, 2019 − Rev. 0

PIN FUNCTION DESCRIPTION

Pin No. DPAK−5 D2PAK−5	Symbol	Description
1	I	Input; Battery Supply Input Voltage. Bypass to ground with a ceramic capacitor.
2	RO	Reset Output; Open Collector Active Reset (accurate when I > 1.0 V).
3, TAB	GND	Ground; Pin 3 internally connected to tab.
4	D	Reset Delay; timing capacitor to GND for Reset Delay function.
5	Q	Output; ±2.0%, 450 mA output. Bypass with 22 μF capacitor, ESR < 4.5 Ω (5.0 V Version), 3.5 Ω (3.3 V Version).

MAXIMUM RATINGS

Rating		Symbol	Min	Max	Unit
Input Voltage		V_I	−42	45	V
Input Peak Transient Voltage		V_I	–	45	V
Output Voltage		V_Q	−1.0	16	V
Reset Output Voltage		V_{RO}	−0.3	25	V
Reset Output Current		I_{RO}	−5.0	5.0	mA
Reset Delay Voltage		V_D	−0.3	7.0	V
Reset Delay Current		I_D	−2.0	2.0	mA
ESD Susceptibility (Note 1)	– Human Body Model – Machine Model – Charge Device Model	ESD_{HBM} ESD_{MM} ESD_{CDM}	4.0 200 1000	– – –	kV V V
Junction Temperature		T_J	−40	150	°C
Storage Temperature		T_{stg}	−55	150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. This device incorporates ESD protection and is tested by the followign methods: ESD Human Body Model tested per AEC−Q100−002, ESD Machine Model tested per AEC−Q100−003, ESD Charged Device Model tested per AEC−Q100−011, Latch−up tested per AEC−Q100−004.

OPERATING RANGE

Rating	Symbol	Min	Max	Unit
Input Voltage Operating Range, 5.0 V Output	V_I	5.5	42	V
Input Voltage Operating Range, 3.3 V Output	V_I	4.4	42	V
Junction Temperature	T_J	−40	150	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

LEAD TEMPERATURE SOLDERING REFLOW AND MSL (Note 2)

Rating	Symbol	Min	Max	Unit
Lead Free, 60 sec−150 sec above 217°C	T_{SLD}	–	265 Peak	°C
Moisture Sensitivity Level	MSL	1		

THERMAL CHARACTERISTICS

Characteristic	Test Conditions (Typical Value)		Unit
DPAK 5−PIN PACKAGE			
	Min Pad Board (Note 3)	1 in Pad Board (Note 4)	
Junction−to−Tab ($R_{\theta JT}$)	5.1	5.5	°C/W
Junction−to−Ambient ($R_{\theta JA}$)	82.4	58.1	°C/W
D^{2}PAK 5−PIN PACKAGE			
	0.4 sq. in. Spreader Board (Note 5)	1.2 sq. in. Spreader Board (Note 6)	
Junction−to−Tab ($R_{\theta JT}$)	4.5	4.8	°C/W
Junction−to−Ambient ($R_{\theta JA}$)	66.0	49.0	°C/W

2. PR_R IPC / JEDEC J−STD−020C
3. 1 oz. copper, 0.26 inch^2 (168 mm^2) copper area, 0.062″ thick FR4.
4. 1 oz. copper, 1.14 inch^2 (736 mm^2) copper area, 0.062″ thick FR4.
5. 1 oz. copper, 0.373 inch^2 (241 mm^2) copper area, 0.062″ thick FR4.
6. 1 oz. copper, 1.222 inch^2 (788 mm^2) copper area, 0.062″ thick FR4.

ELECTRICAL CHARACTERISTICS (V_I = 13.5 V; −40°C < T_J < 150°C; unless otherwise noted.)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Output						
Output Voltage	V_Q	100 µA ≤ I_Q ≤ 400 mA 6.0 V ≤ V_I ≤ 28 V (5.0 V Version) 4.4 V ≤ V_I ≤ 28 V (3.3 V version)	4.9 3.23 (2%)	5.0 3.3	5.1 3.37 (2%)	V
Output Voltage	V_Q	100 µA ≤ I_Q ≤ 200 mA 6.0 V ≤ V_I ≤ 40 V (5.0 V Version) 4.4 V ≤ V_I ≤ 40 V (3.3 V version)	4.9 3.23 (2%)	5.0 3.3	5.1 3.37 (2%)	V
Output Current Limitation	I_Q	$V_Q = 0.9 \times V_{Q,typ}$	450	650	–	mA
Quiescent Current $I_q = I_I - I_Q$	I_q	I_Q = 1.0 mA, T_J = 25°C	–	135	150	µA
		I_Q = 1.0 mA	–	150	200	µA
		I_Q = 250 mA	–	10	15	mA
		I_Q = 400 mA	–	23	35	mA
Dropout Voltage (Note 7)	V_{dr}	I_Q = 300 mA $V_{dr} = V_I - V_Q$	–	250	500	mV
Load Regulation	ΔV_Q	I_Q = 5.0 mA to 400 mA	−30	15	30	mV
Line Regulation	ΔV_Q	ΔV_I = 8.0 V to 32 V, I_Q = 5.0 mA	−15	5.0	15	mV
Power Supply Ripple Rejection	PSRR	f_r = 100 Hz, V_r = 0.5 V_{pp}	–	60	–	dB
Temperature Output Voltage Drift	dV_Q/dT	––	–	0.5	–	mV/K
Reset Timing D and Output RO						
Reset Switching Threshold 5.0 V Version 3.3 V Version	$V_{Q,rt}$	V_{out} decreasing V_{in} > 5.5 V V_{in} > 4.4 V	90 90	93 93	96 96	% V_{out}
Reset Output Low Voltage	V_{ROL}	$R_{ext} \geq 5.0$ kΩ, $V_Q \geq 1.0$ V	–	0.2	0.4	V
Reset Output Leakage Current	I_{ROH}	V_{ROH} = 5.0 V	–	0	10	µA
Reset Charging Current	$I_{D,C}$	V_D = 1.0 V	3.0	5.5	9.0	µA
Upper Timing Threshold	V_{DU}	––	1.5	1.8	2.2	V
Lower Timing Threshold	V_{DL}	––	0.2	0.4	0.7	V
Reset Delay Time	t_{rd}	C_D = 47 nF	10	16	22	ms
Reset Reaction Time	t_{rr}	C_D = 47 nF	–	1.5	4.0	µs
Thermal Shutdown						
Shutdown Temperature (Note 8)	T_{SD}	––	150	–	210	°C

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

7. Only for 5 V Version. Measured when the output voltage V_Q has dropped 100 mV from the nominal value obtained at V_I = 13.5 V.
8. Guaranteed by design, not tested in production.

TYPICAL PERFORMANCE CHARACTERISTICS

5.0 V Version

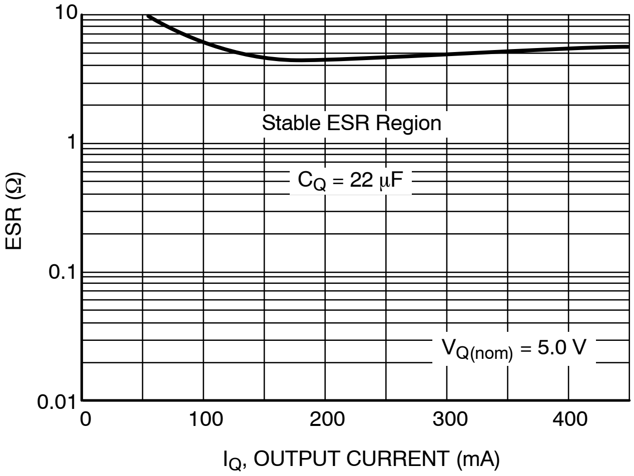


Figure 2. Output Stability with Output Capacitor ESR

3.3 V Version

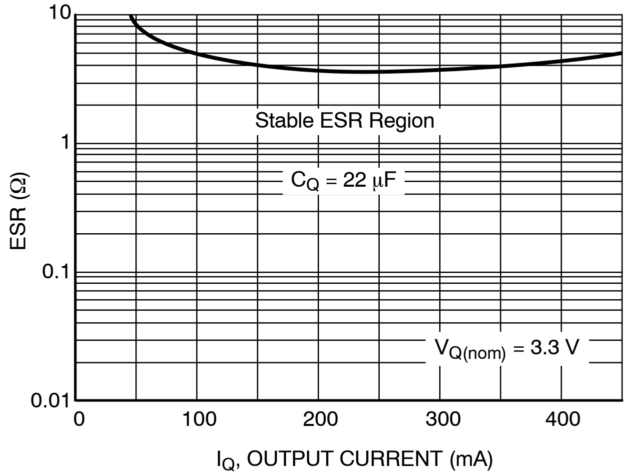


Figure 3. Output Stability with Output Capacitor ESR

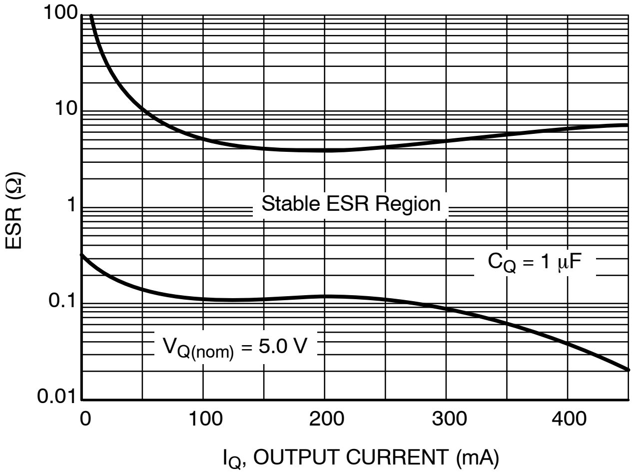


Figure 4. Output Stability with Output Capacitor ESR

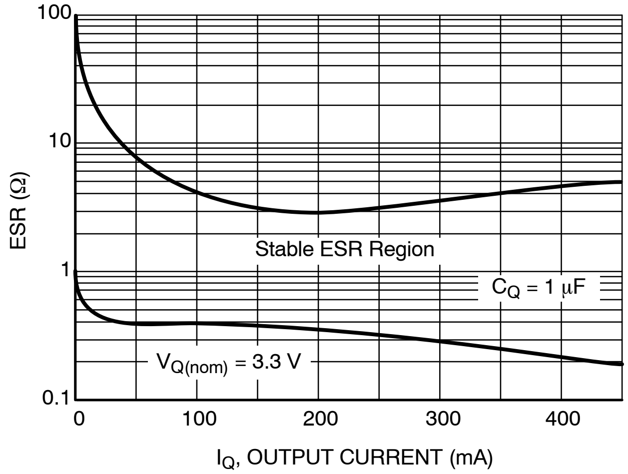


Figure 5. Output Stability with Output Capacitor ESR

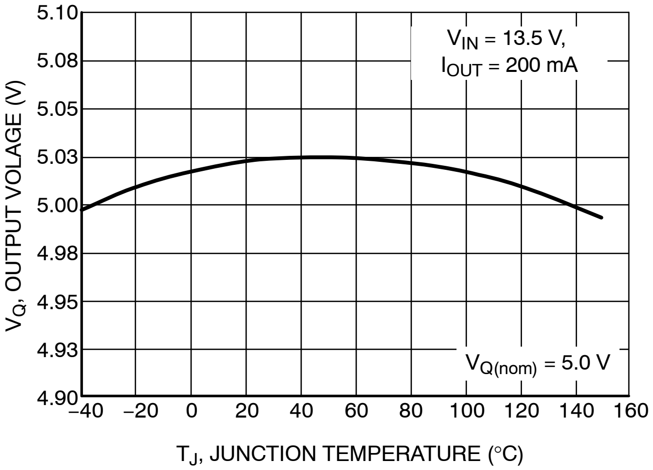


Figure 6. Output Voltage V_Q vs. Temperature T_J

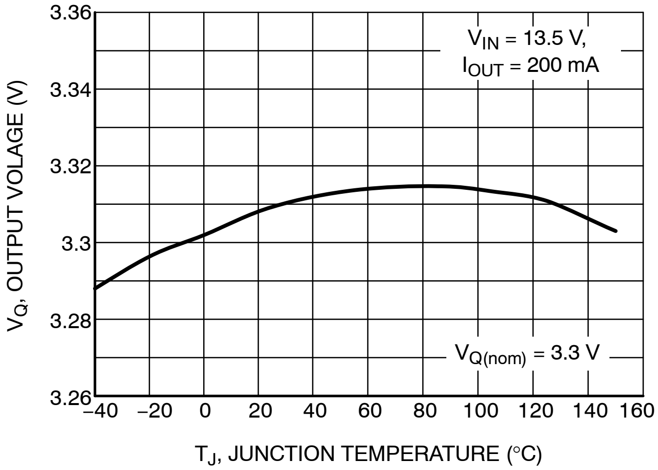


Figure 7. Output Voltage V_Q vs. Temperature T_J

TYPICAL PERFORMANCE CHARACTERISTICS

5.0 V Version

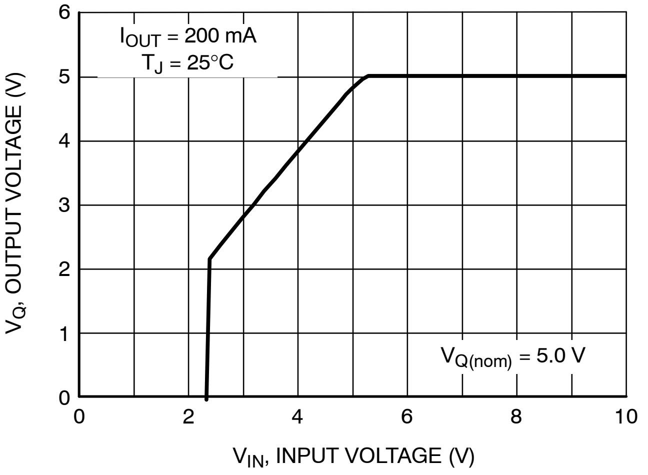


Figure 8. Output Voltage V_Q vs. Input Voltage V_{IN}

3.3 V Version

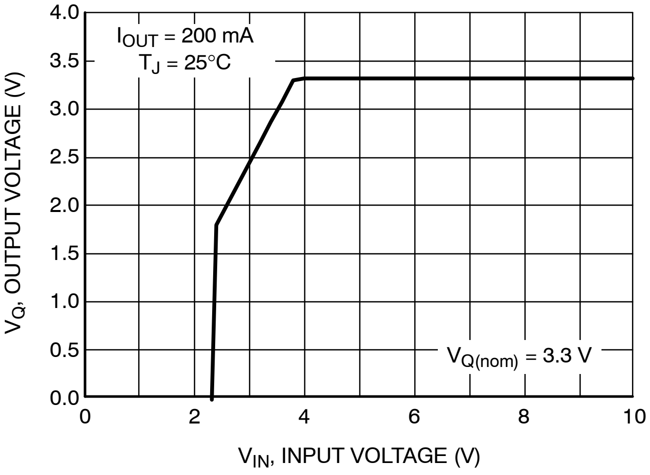


Figure 9. Output Voltage V_Q vs. Input Voltage V_{IN}

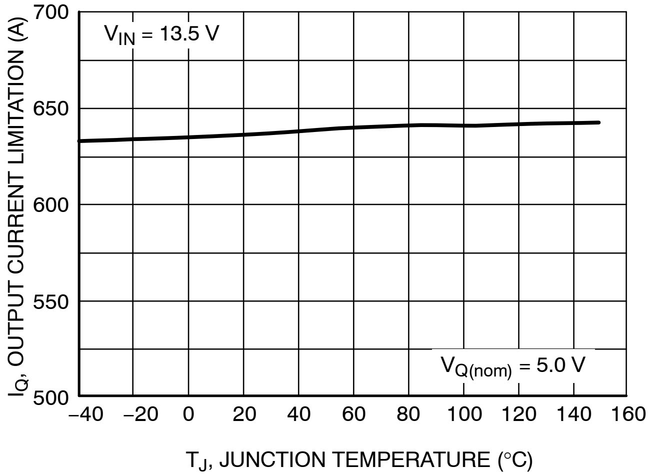


Figure 10. Output Current I_Q vs. Temperature T_J

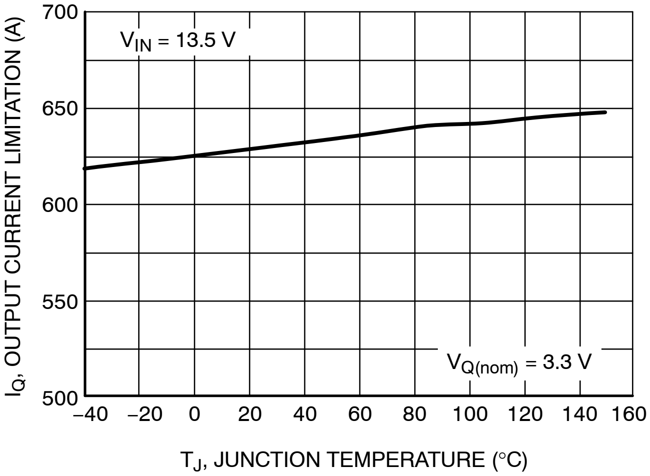


Figure 11. Output Current I_Q vs. Temperature T_J

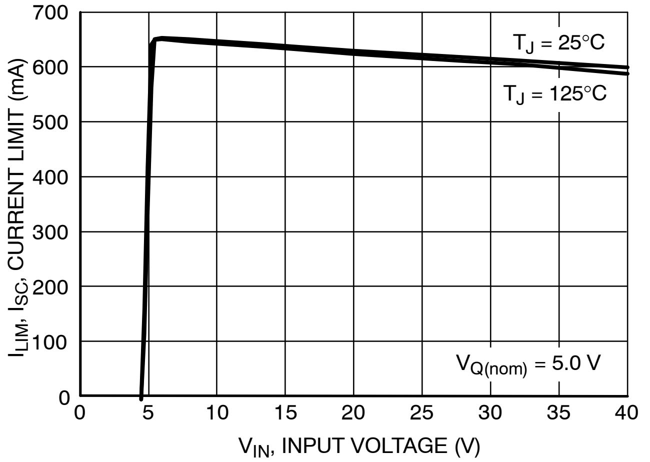


Figure 12. Output Current I_Q vs. Input Voltage V_{IN}

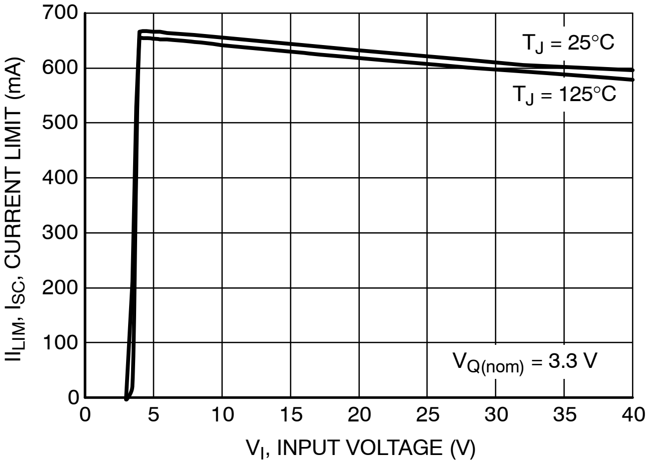


Figure 13. Output Current I_Q vs. Input Voltage V_{IN}

TYPICAL PERFORMANCE CHARACTERISTICS

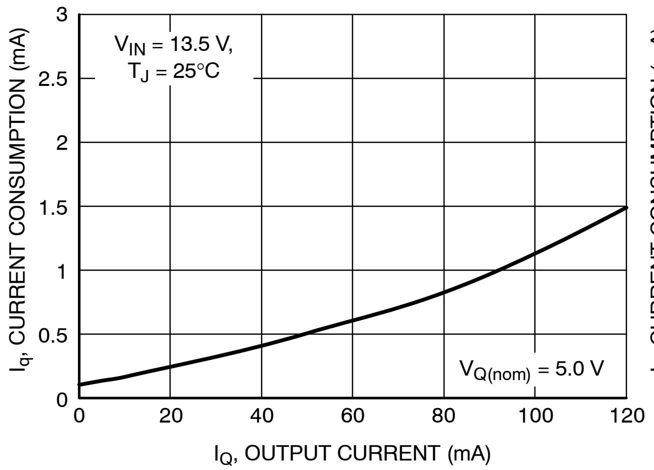


Figure 14. Current Consumption I_q vs. Output Current I_Q

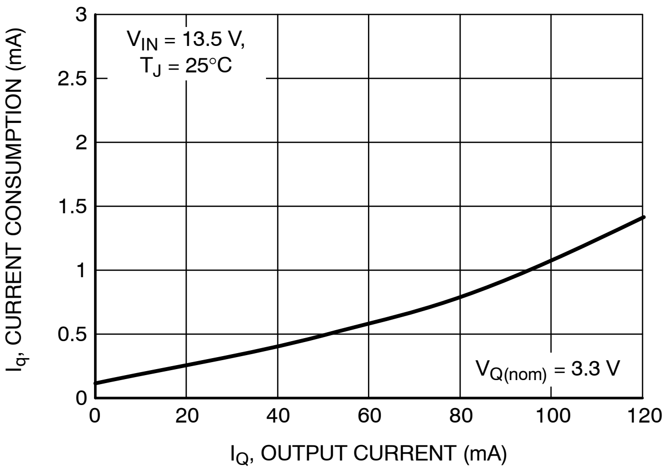


Figure 15. Current Consumption I_q vs. Output Current I_Q

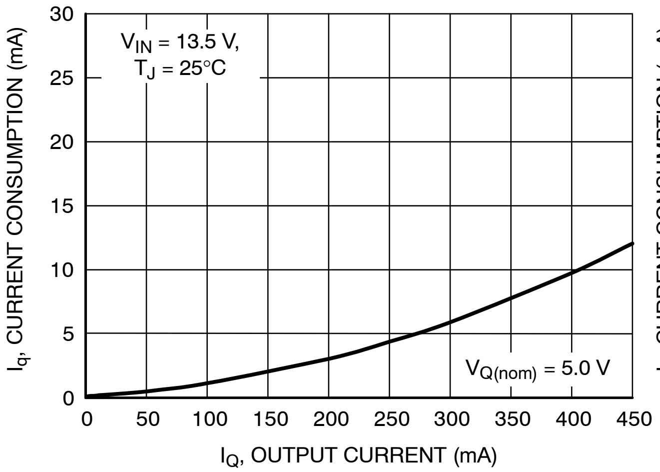


Figure 16. Current Consumption I_q vs. Output Current I_Q

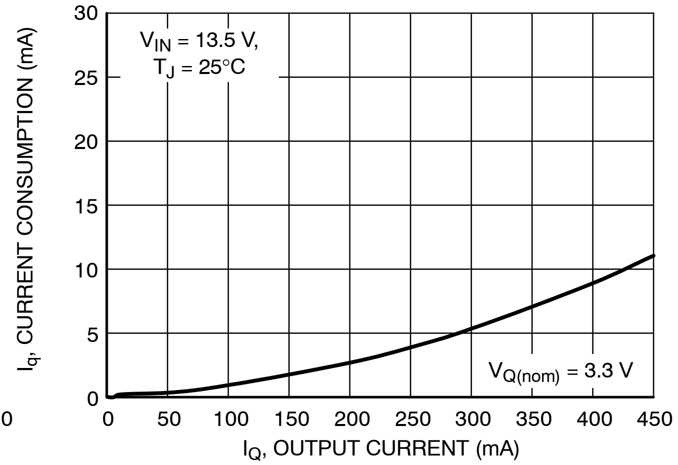


Figure 17. Current Consumption I_q vs. Output Current I_Q

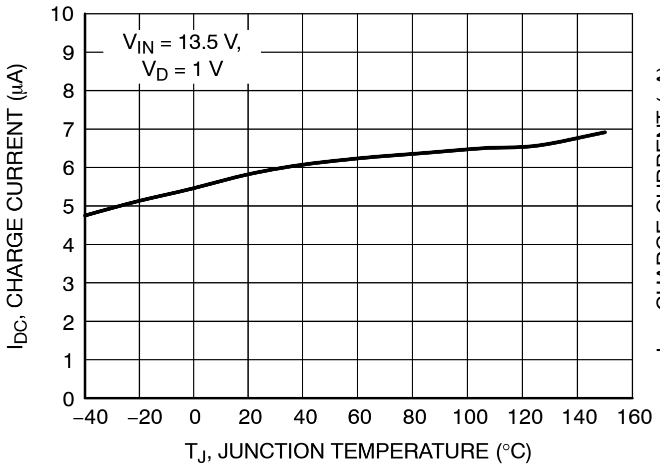


Figure 18. Charge Current $I_{D,C}$ vs. Temperature T_J

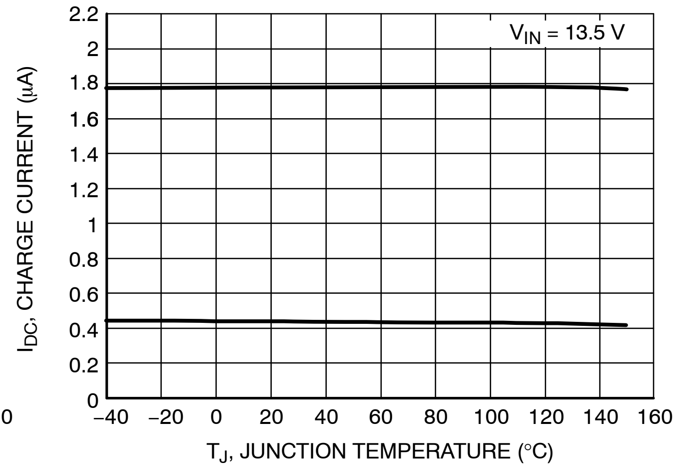


Figure 19. Delay Switching Threshold V_{DU}, V_{DL} vs. Temperature T_J

TYPICAL PERFORMANCE CHARACTERISTICS

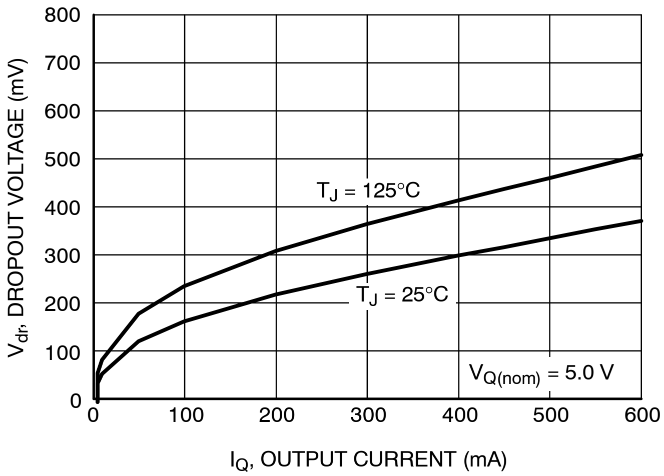


Figure 20. Drop Voltage V_{dr} vs. Output Current I_Q

APPLICATION INFORMATION

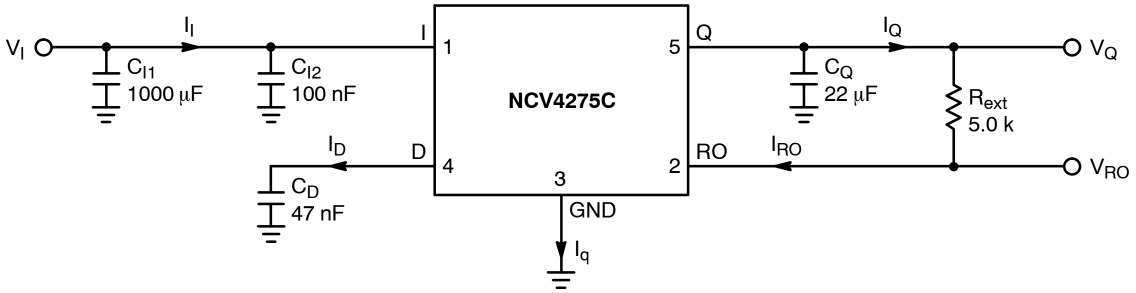


Figure 21. Test Circuit

Circuit Description

The NCV4275C is an integrated low dropout regulator that provides 5.0 V or 3.3 V, 450 mA protected output and a signal for power on reset. The regulation is provided by a PNP pass transistor controlled by an error amplifier with a bandgap reference, which gives it the lowest possible drop out voltage and best possible temperature stability. The output current capability is 450 mA, and the base drive quiescent current is controlled to prevent over saturation when the input voltage is low or when the output is overloaded. The regulator is protected by both current limit and thermal shutdown. Thermal shutdown occurs above 150°C to protect the IC during overloads and extreme ambient temperatures. The delay time for the reset output is adjustable by selection of the timing capacitor. See Figure 21, Test Circuit, for circuit element nomenclature illustration.

Regulator

The error amplifier compares the reference voltage to a sample of the output voltage (V_Q) and drives the base of a PNP series pass transistor by a buffer. The reference is a bandgap design to give it a temperature−stable output. Saturation control of the PNP is a function of the load current and input voltage. Over saturation of the output power device is prevented, and quiescent current in the ground pin is minimized.

Regulator Stability Considerations

The input capacitors (C_{I1} and C_{I2}) are necessary to stabilize the input impedance to avoid voltage line influences. Using a resistor of approximately 1.0 Ω in series with C_{I2} can stop potential oscillations caused by stray inductance and capacitance.

The output capacitor helps determine three main characteristics of a linear regulator: startup delay, load transient response and loop stability. The capacitor value and type should be based on cost, availability, size and temperature constraints. A tantalum, aluminum or ceramic capacitors can be used. The range of stability versus capacitance, load current and capacitive ESR is illustrated in Figures 2 to 5. Minimum ESR for C_Q = 22 μF is native ESR of ceramic capacitors. The aluminum electrolytic capacitor is the least expensive solution, but, if the circuit operates at low temperatures (−25°C to −40°C), both the capacitance and ESR of the capacitor will vary considerably. The capacitor manufacturer's data sheet usually provides this information.

The value for the output capacitor C_Q shown in Figure 21, Test Circuit, should work for most applications; however, it is not necessarily the optimized solution. Stability is guaranteed for $C_Q \geq 22$ μF and an ESR ≤ 4.5 Ω (5.0 V Version), 3.5 Ω (3.3 V Version). ESR characteristics were measured with ceramic capacitors and additional resistors to emulate ESR. Murata ceramic capacitors were used, GRM32ER71A226ME20 (22 μF, 10 V, X7R, 1210), GRM31MR71E105KA01 (1 μF, 25 V, X7R, 1206).

Reset Output

The reset output is used as the power on indicator to the microcontroller. This signal indicates when the output voltage is suitable for reliable operation of the controller. It pulls low when the output is not considered to be ready. RO is pulled up to V_Q by an external resistor, typically 5.0 kΩ in value. The input and output conditions that control the Reset Output and the relative timing are illustrated in Figure 22, Reset Timing.

Output voltage regulation must be maintained for the delay time before the reset output signals a valid condition. The delay for the reset output is defined as the amount of time it takes the timing capacitor on the delay pin to charge from a residual voltage of 0.0 V to the upper timing threshold voltage V_{DU}. The charging current for this is $I_{D,C}$ and D pin voltage in steady state is typically 2.4 V. By using typical IC parameters with a 47 nF capacitor on the D pin, the following time delay for 5.0 V regulator is derived:

$$t_{RD} = C_D V_{DU} / I_{D,C}$$

$$t_{RD} = 47\text{ nF } (1.8\text{ V}) / 5.5\ \mu\text{A} = 15.4\text{ ms}$$

Other time delays can be obtained by changing the capacitor value.

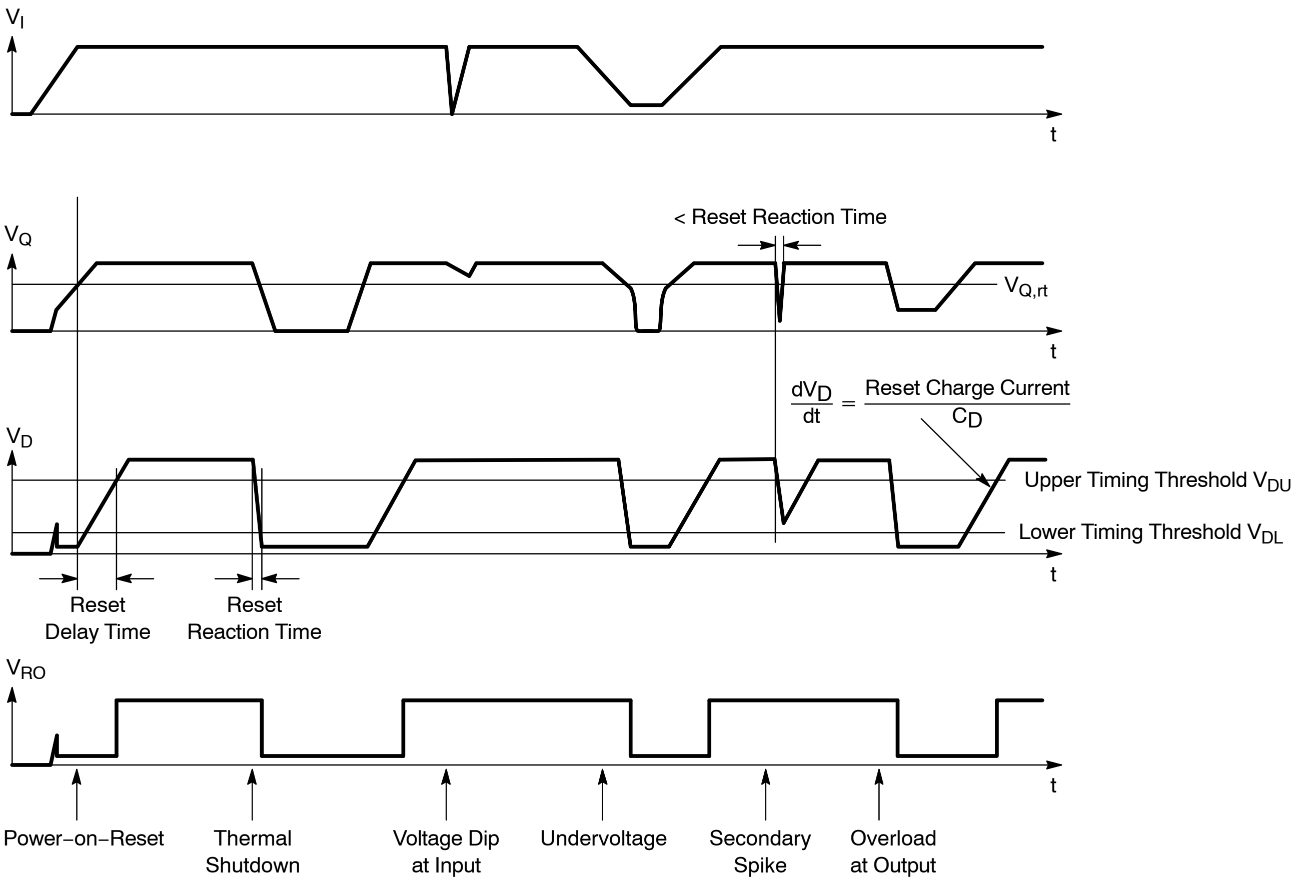


Figure 22. Reset Timing

Calculating Power Dissipation in a Single Output Linear Regulator

The maximum power dissipation for a single output regulator (Figure 23) is:

$$P_{D(max)} = [V_{I(max)} - V_{Q(min)}] I_{Q(max)} + V_{I(max)} I_q \quad (1)$$

where

$V_{I(max)}$ is the maximum input voltage,

$V_{Q(min)}$ is the minimum output voltage,

$I_{Q(max)}$ is the maximum output current for the application,

I_q is the quiescent current the regulator consumes at $I_{Q(max)}$.

Once the value of $P_{D(max)}$ is known, the maximum permissible value of $R_{\theta JA}$ can be calculated:

$$R_{\theta JA} = \frac{150^\circ C - T_A}{P_D} \quad (2)$$

The value of $R_{\theta JA}$ can then be compared with those in the package section of the data sheet. Those packages with $R_{\theta JA}$'s less than the calculated value in Equation 2 will keep the die temperature below 150°C.

In some cases, none of the packages will be sufficient to dissipate the heat generated by the IC, and an external heatsink will be required.

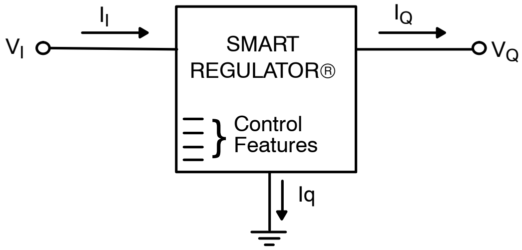


Figure 23. Single Output Regulator with Key Performance Parameters Labeled

Heatsinks

A heatsink effectively increases the surface area of the package to improve the flow of heat away from the IC and into the surrounding air.

Each material in the heat flow path between the IC and the outside environment will have a thermal resistance. Like series electrical resistances, these resistances are summed to determine the value of $R_{\theta JA}$:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CS} + R_{\theta SA} \quad (3)$$

where

$R_{\theta JC}$ is the junction–to–case thermal resistance,

$R_{\theta CS}$ is the case–to–heatsink thermal resistance,

$R_{\theta SA}$ is the heatsink–to–ambient thermal resistance.

$R_{\theta JC}$ appears in the package section of the data sheet. Like $R_{\theta JA}$, it too is a function of package type. $R_{\theta CS}$ and $R_{\theta SA}$ are functions of the package type, heatsink and the interface between them. These values appear in heatsink data sheets of heatsink manufacturers.

Thermal, mounting, and heatsinking considerations are discussed in the ON Semiconductor application note AN1040/D.

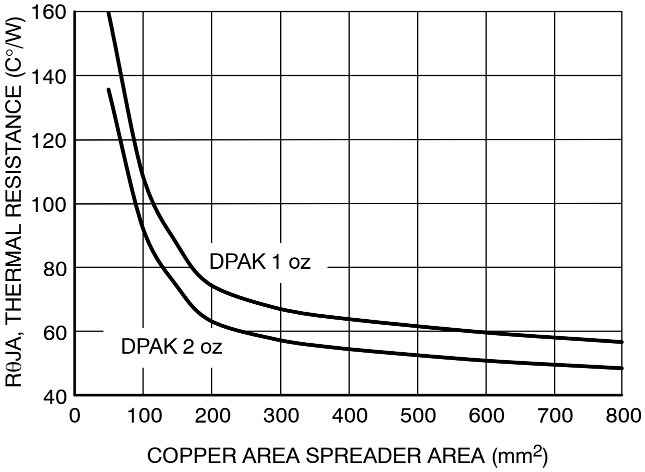


Figure 24. θJA vs. Copper Spreader Area, DPAK 5–Lead

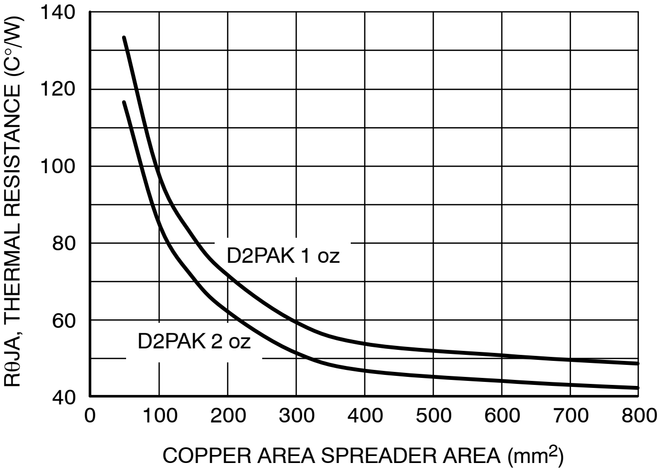


Figure 25. θJA vs. Copper Spreader Area, D^2PAK 5–Lead

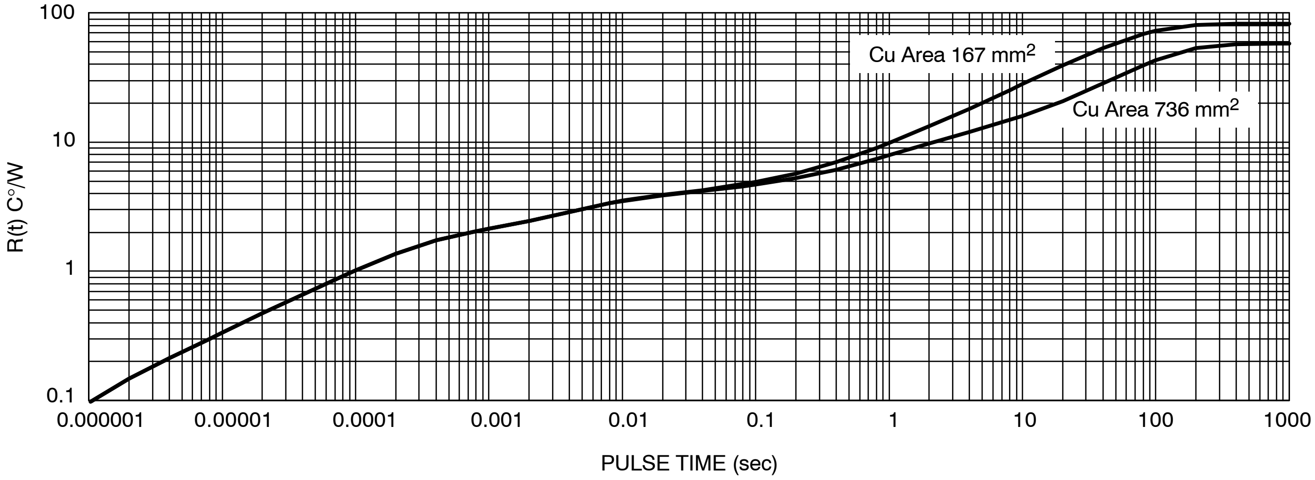


Figure 26. Single−Pulse Heating Curves, DPAK 5−Lead

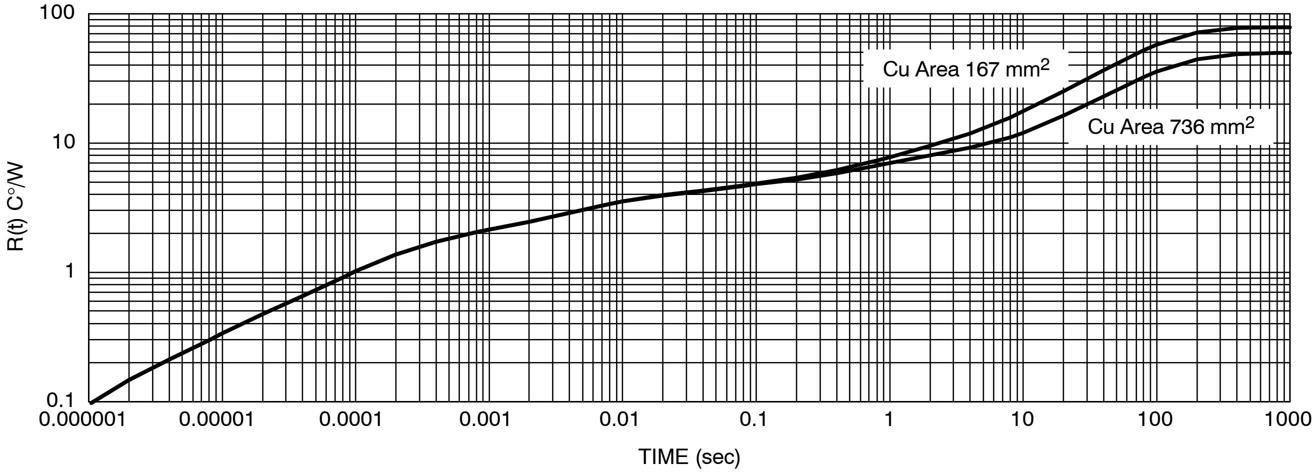


Figure 27. Single−Pulse Heating Curves, D^{2}PAK 5−Lead

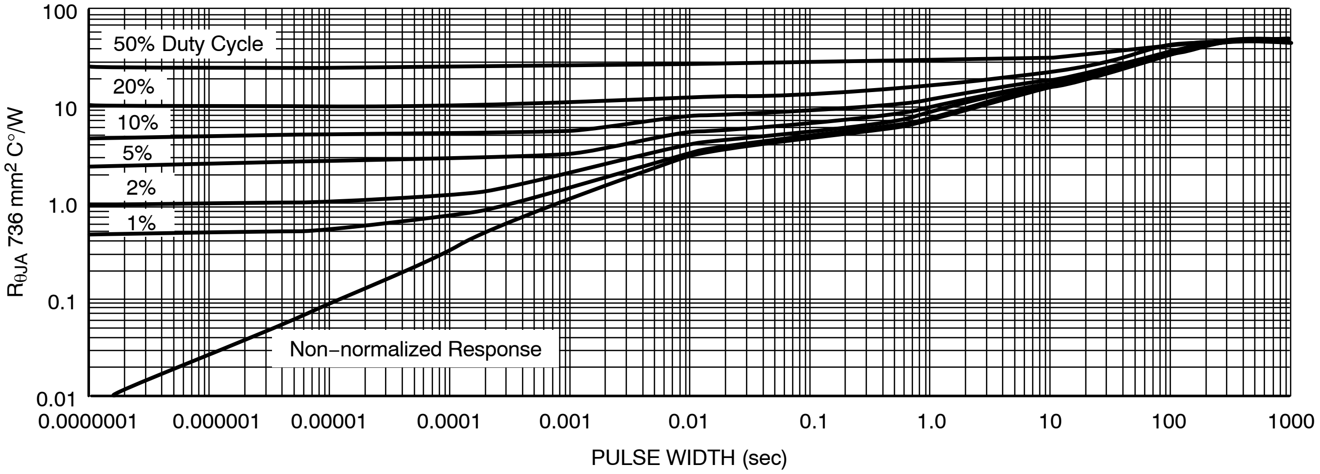


Figure 28. Duty Cycle for 1” Spreader Boards, DPAK 5−Lead

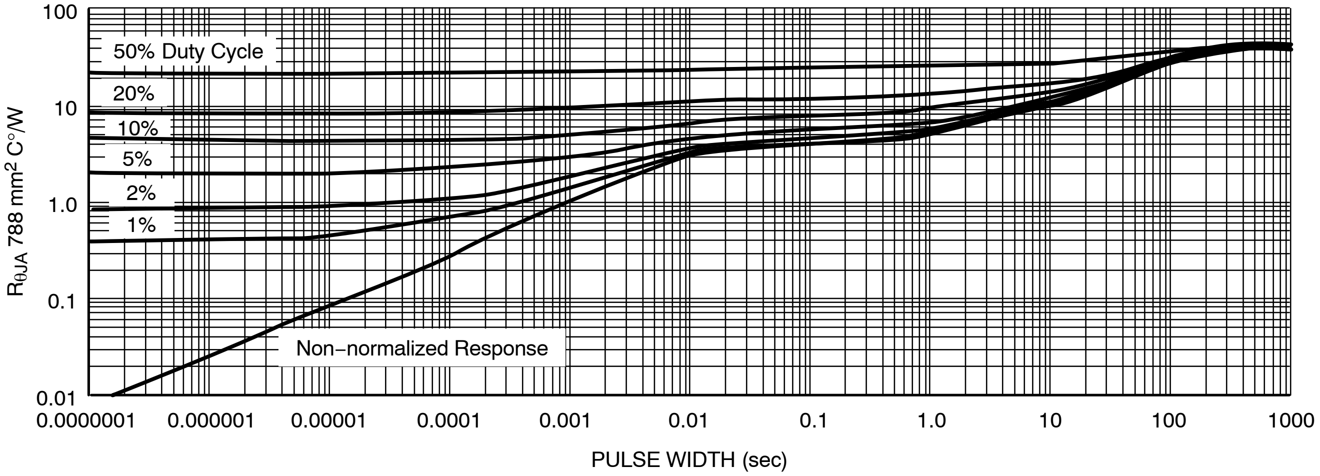
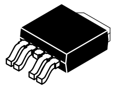


Figure 29. Duty Cycle for 1” Spreader Boards, D^{2}PAK 5−Lead

ORDERING INFORMATION

Device	Output Voltage	Package	Shipping†
NCV4275CDS50R4G	5.0 V	D2PAK (Pb−Free)	800 / Tape & Reel
NCV4275CDT50RKG		DPAK (Pb−Free)	2500 / Tape & Reel
NCV4275CDS33R4G	3.3 V	D2PAK (Pb−Free)	800 / Tape & Reel
NCV4275CDT33RKG		DPAK (Pb−Free)	2500 / Tape & Reel

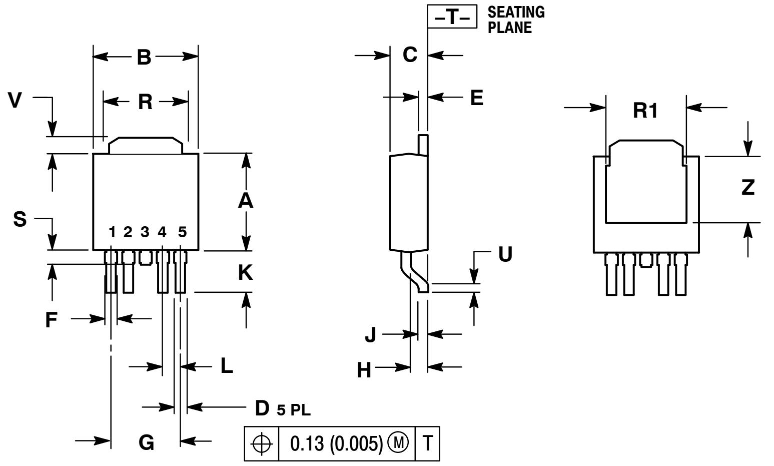
†For information on tape and reel specifications,including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



SCALE 1:1

DPAK−5, CENTER LEAD CROP
CASE 175AA
ISSUE B

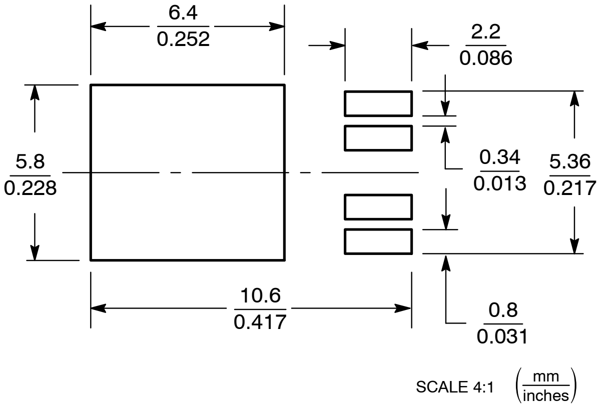
DATE 15 MAY 2014



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

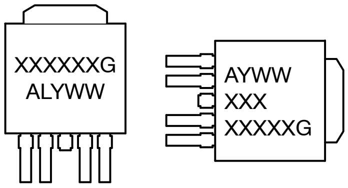
	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.22
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.020	0.028	0.51	0.71
E	0.018	0.023	0.46	0.58
F	0.024	0.032	0.61	0.81
G	0.180 BSC		4.56 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.102	0.114	2.60	2.89
L	0.045 BSC		1.14 BSC	
R	0.170	0.190	4.32	4.83
R1	0.185	0.210	4.70	5.33
S	0.025	0.040	0.63	1.01
U	0.020	−−−	0.51	−−−
V	0.035	0.050	0.89	1.27
Z	0.155	0.170	3.93	4.32

RECOMMENDED SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAMS*



IC **Discrete**

XXXXXX = Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

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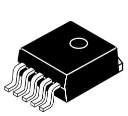
DESCRIPTION:	**DPAK−5 CENTER LEAD CROP**	**PAGE 1 OF 1**

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

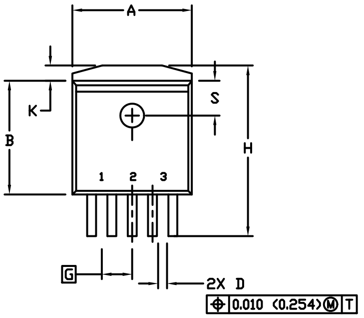
ON Semiconductor®



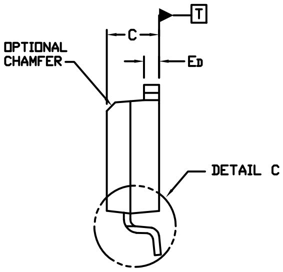
SCALE 1:1

D²PAK 5−LEAD
CASE 936A−02
ISSUE E

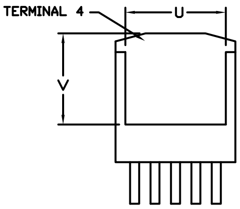
DATE 28 JUL 2021



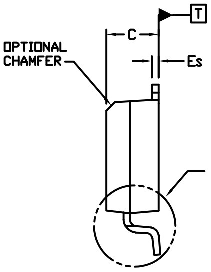
TOP VIEW



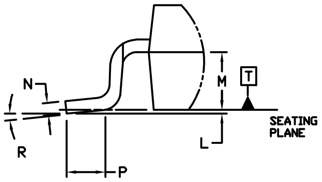
SIDE VIEW
DUAL GUAGE CONSTRUCTION



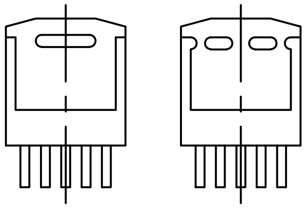
BOTTOM VIEW



SIDE VIEW
SINGLE GUAGE CONSTRUCTION



DETAIL C
TIP LEADFORM
ROTATED 90° CW

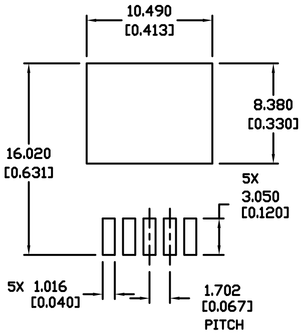


BOTTOM VIEW
OPTIONAL CONSTRUCTIONS

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCHES
3. TAB CONTOUR OPTIONAL WITHIN DIMENSIONS A AND K.
4. DIMENSIONS U AND V ESTABLISH A MINIMUM MOUNTING SURFACE FOR TERMINAL 4.
5. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH OR GATE PROTRUSIONS. MOLD FLASH AND GATE PROTRUSIONS NOT TO EXCEED 0.025 (0.635) MAXIMUM.

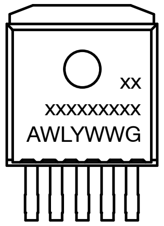
DIM	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.396	0.403	9.804	10.236
B	0.356	0.368	9.042	9.347
C	0.170	0.180	4.318	4.572
D	0.026	0.036	0.660	0.914
ED	0.045	0.055	1.143	1.397
ES	0.018	0.026	0.457	0.660
G	0.067 BSC		1.702 BSC	
H	0.539	0.579	13.691	14.707
K	0.050 REF		1.270 REF	
L	0.000	0.010	0.000	0.254
M	0.088	0.102	2.235	2.591
N	0.018	0.026	0.457	0.660
P	0.058	0.078	1.473	1.981
R	0°	8°	0°	8°
S	0.116 REF		2.946 REF	
U	0.200 MIN		5.080 MIN	
V	0.250 MIN		6.350 MIN	



RECOMMENDED MOUNTING FOOTPRINT *

* For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXXX	= Device Code
A	= Assembly Location
WL	= Wafer Lot
Y	= Year
WW	= Work Week
G	= Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	**D2PAK 5−LEAD**	**PAGE 1 OF 1**

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