

- Suitable for IEEE Standard 488-1978 (GPIB)
- 8-Channel Bidirectional Transceivers
- Designed to Implement Control Bus Interface
- Designed for Single Controller
- High-Speed Advanced Low-Power Schottky Circuitry
- Low Power Dissipation . . . 46 mW Max Per Channel
- Fast Propagation Times . . . 20 ns Max
- High-Impedance pnp Inputs
- Receiver Hysteresis . . . 650 mV Typ
- Bus-Terminating Resistors Provided on Driver Outputs
- No Loading of Bus When Device Is Powered Down ( $V_{CC} = 0$ )
- Power-Up/Power-Down Protection (Glitch Free)

#### description/ordering information

The SN75ALS161 eight-channel general-purpose interface bus transceivers are high-speed, advanced low-power Schottky-process devices designed to provide the bus-management and data-transfer signals between operating units of a single-controller instrumentation system. When combined with the SN75ALS160 octal bus transceivers, this device provides a complete 16-wire interface for the IEEE 488 bus.

The SN75ALS161 device features eight driver-receiver pairs connected in a front-to-back configuration to form input/output (I/O) ports at both the bus and terminal sides. The direction of data through these driver-receiver pairs is determined by the direction-control (DC) and talk-enable (TE) signals.

The driver outputs general-purpose interface bus (GPIB I/O ports) feature active bus-terminating resistor circuits designed to provide a high impedance to the bus when  $V_{CC} = 0$ . The drivers are designed to handle sink-current loads up to 48 mA. Each receiver features pnp transistor inputs for high input impedance and hysteresis of 400 mV on the commercial part, and 250 mV on the military part, minimum, for increased noise immunity. All receivers have 3-state outputs, to present a high impedance to the terminal when disabled.

The SN75ALS161 is characterized for operation from 0°C to 70°C.

#### ORDERING INFORMATION

TA	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	PDIP (N)	Tube of 20	SN75ALS161N	SN75ALS161N
	SOIC (DW)	Tube of 25	SN75ALS161DW	75ALS161
		Reel of 2000	SN75ALS161DWR	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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# SN75ALS161

## OCTAL GENERAL-PURPOSE INTERFACE BUS TRANSCEIVERS

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FUNCTION TABLE  
RECEIVE/TRANSMIT

CONTROLS			BUS-MANAGEMENT CHANNELS					DATA-TRANSFER CHANNELS		
DC	TE	ATN <sup>†</sup>	ATN <sup>†</sup>	SRQ	REN	IFC	EOI	DAV	NDAC	NRFD
H	H	H	R	T	R	R	T	T	R	R
							R			
L	L	H	T	R	T	T	R	R	T	T
							T			
H	L	X	R	T	R	R	R	R	T	T
L	H	X	T	R	T	T	T	T	R	R

H = high level, L = low level, R = receive, T = transmit, X = irrelevant

Direction of data transmission is from the terminal side to the bus side, and the direction of data receiving is from the bus side to the terminal side.

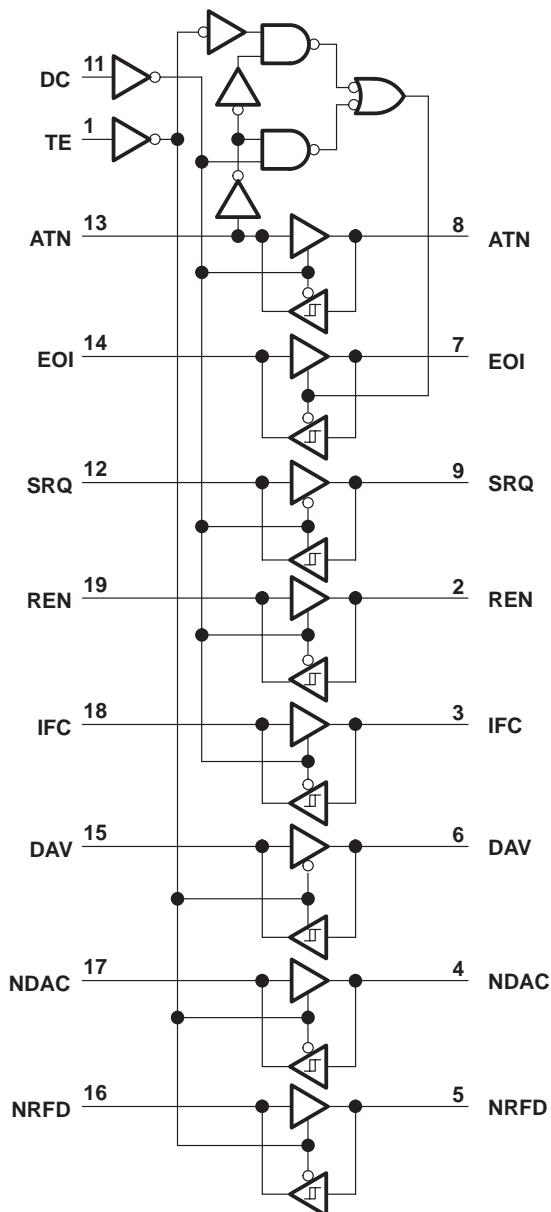
Data transfer is noninverting in both directions.

<sup>†</sup> ATN is a normal transceiver channel that functions additionally as an internal direction control or talk enable for EOI whenever the DC and TE inputs are in the same state. When DC and TE are in opposite states, the ATN channel functions as an independent transceiver only.



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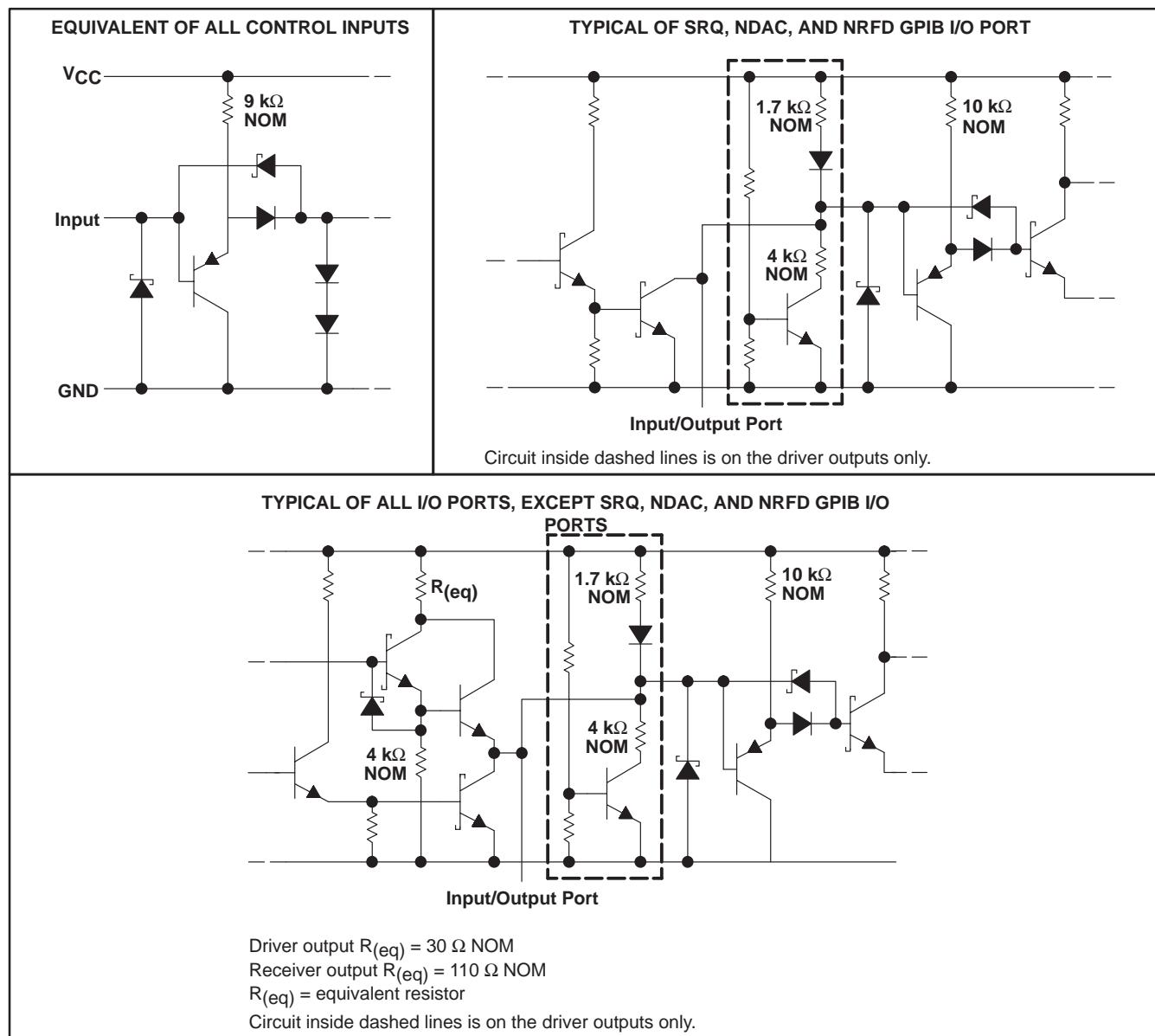
logic diagram (positive logic)



# SN75ALS161 OCTAL GENERAL-PURPOSE INTERFACE BUS TRANSCEIVERS

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## schematics of inputs and outputs



**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

Supply voltage, $V_{CC}$ (see Note 1) .....	7 V
Input voltage, $V_I$ .....	5.5 V
Low-level driver output current, $I_{OL}$ .....	100 mA
Package thermal impedance, $\theta_{JA}$ (see Notes 2 and 3): DW package .....	58°C/W
	N package .....
	69°C/W
Operating virtual junction temperature, $T_J$ .....	150°C
Storage temperature range, $T_{STG}$ .....	–65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to network ground terminal.

2. Maximum power dissipation is a function of  $T_J(\max)$ ,  $\theta_{JA}$ , and  $T_A$ . The maximum allowable power dissipation at any allowable ambient temperature is  $P_D = (T_J(\max) - T_A)/\theta_{JA}$ . Operating at the absolute maximum  $T_J$  of 150°C can affect reliability.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

**recommended operating conditions**

		MIN	NOM	MAX	UNIT
$V_{CC}$	Supply voltage	4.75	5	5.25	V
$V_{IH}$	High-level input voltage	2			V
$V_{IL}$	Low-level input voltage			0.8	V
$I_{OH}$	High-level output current	Bus ports with pullups active		–5.2	mA
		Terminal ports		–800	µA
$I_{OL}$	Low-level output current	Bus ports		48	mA
		Terminal ports		16	
$T_A$	Operating free-air temperature	0	70		°C



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# SN75ALS161

## OCTAL GENERAL-PURPOSE INTERFACE BUS TRANSCEIVERS

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**electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)**

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT	
$V_{IK}$	Input clamp voltage	$I_I = -18 \text{ mA}$		-0.8	-1.5		V	
$V_{hys}$	Hysteresis voltage ( $V_{IT+} - V_{IT-}$ )	Bus		0.4	0.65		V	
$V_{OH}^§$ High-level output voltage	Terminal	$I_{OH} = -800 \mu\text{A}$ , $V_{CC} = \text{MIN}$	$T_A = 25^\circ\text{C}$ and MAX	2.7	3.5		V	
			$T_A = \text{MIN}$	2.7	3.5			
	Bus	$I_{OH} = -5.2 \text{ mA}$ , $V_{CC} = \text{MIN}$	$T_A = 25^\circ\text{C}$ and MAX	2.2				
			$T_A = \text{MIN}$	2.2				
$V_{OL}$	Terminal	$I_{OL} = 16 \text{ mA}$ , $V_{CC} = \text{MIN}$		0.3	0.5		V	
	Bus	$I_{OL} = 48 \text{ mA}$ , $V_{CC} = \text{MIN}$		0.35	0.5			
$I_I$	Input current at maximum input voltage	Terminal	$V_I = 5.5 \text{ V}$ , $V_{CC} = \text{MAX}$	0.2	100		$\mu\text{A}$	
$I_{IH}$	High-level input current	Terminal and control inputs	$V_I = 2.7 \text{ V}$ , $V_{CC} = \text{MAX}$	0.1	20		$\mu\text{A}$	
$V_{I/O}$	Voltage at GPIB I/O port		$I_{I(bus)} = 0$	2.5	3	3.7	V	
			$I_{I(bus)} = 0$	2.5	3	3.7		
			$I_{I(bus)} = -12 \text{ mA}$			-1.5		
$I_{IL}$	Low-level input current	Terminal and control inputs	$V_I = 0.5 \text{ V}$ , $V_{CC} = \text{MAX}$	-10	-100		$\mu\text{A}$	
$I_{I/O}$	Current into GPIB I/O port	Power on	$V_{I(bus)} = -1.5 \text{ V to } 0.4 \text{ V}$	-1.3			mA	
			$V_{I(bus)} = 0.4 \text{ V to } 2.5 \text{ V}$	0	-3.2			
			$V_{I(bus)} = 2.5 \text{ V to } 3.7 \text{ V}$		2.5			
			$V_{I(bus)} = 3.7 \text{ V to } 5 \text{ V}$	0	2.5			
			$V_{I(bus)} = 5 \text{ V to } 5.5 \text{ V}$	0.7	2.5			
	Power off		$V_{CC} = 0$	$V_{I(bus)} = 0 \text{ to } 2.5 \text{ V}$		40	$\mu\text{A}$	
$I_{OS}^§$	Terminal		$V_{CC} = \text{MAX}$		-15	-35	-75	mA
			$V_{CC} = \text{MAX}$		-25	-50	-125	
$I_{CC}$	Supply current	No load, $V_{CC} = \text{MAX}$		55	75		mA	
$C_{I/O}$	GPIB I/O port capacitance	$V_{CC} = 0 \text{ to } 5 \text{ V}$ , $V_{I/O} = 0 \text{ to } 2 \text{ V}$ , $f = 1 \text{ MHz}$		30			pF	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

§  $V_{OH}$  and  $I_{OS}$  apply to 3-state outputs only.



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**switching characteristics over recommended operating free-air temperature range,  $V_{CC} = 5$  V**

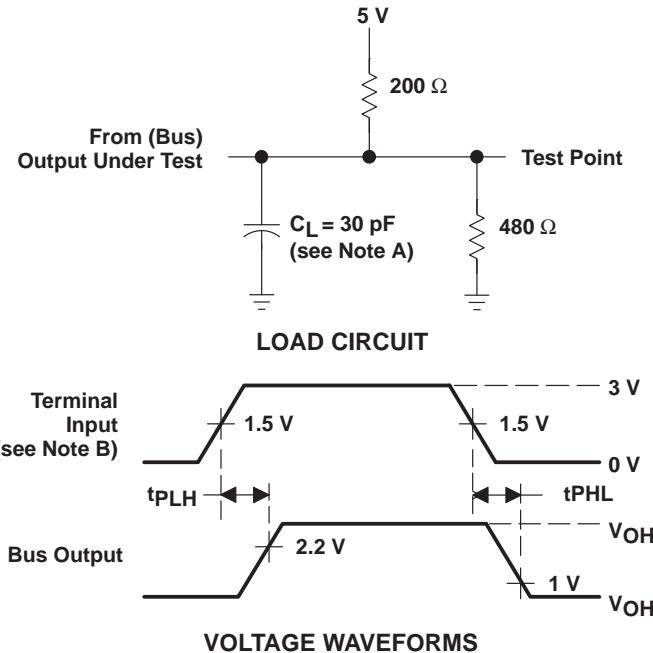
PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
$t_{PLH}$ Propagation delay time, low- to high-level output	Terminal	Bus	$C_L = 30$ pF, See Figure 1		10	20	ns
$t_{PHL}$ Propagation delay time, high- to low-level output					12	20	
$t_{PLH}$ Propagation delay time, low- to high-level output	Bus	Terminal	$C_L = 30$ pF, See Figure 2		5	10	ns
$t_{PHL}$ Propagation delay time, high- to low-level output					7	14	
$t_{PZH}$ Output enable time to high level	TE or DC	Bus (ATN, EOI, REN, IFC, and DAV)	$C_L = 15$ pF, See Figure 3		30		ns
$t_{PHZ}$ Output disable time from high level					20		
$t_{PZL}$ Output enable time to low level					45		
$t_{PLZ}$ Output disable time from low level					20		
$t_{PZH}$ Output enable time to high level	TE or DC	Terminal	$C_L = 15$ pF, See Figure 4		30		ns
$t_{PHZ}$ Output disable time from high level					25		
$t_{PZL}$ Output enable time to low level					30		
$t_{PLZ}$ Output disable time from low level					25		

† All typical values are at  $T_A = 25^\circ\text{C}$ .

# SN75ALS161 OCTAL GENERAL-PURPOSE INTERFACE BUS TRANSCEIVERS

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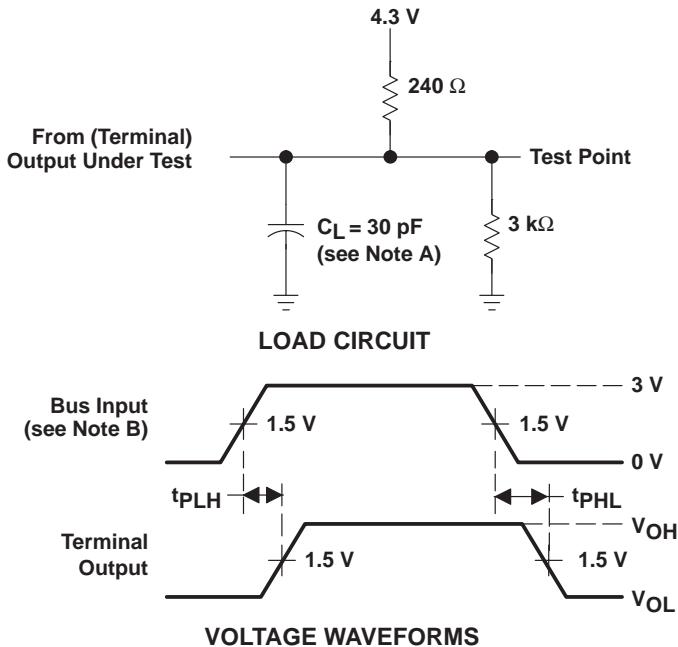
## PARAMETER MEASUREMENT INFORMATION



NOTES: A.  $C_L$  includes probe and jig capacitance.  
B. The input pulse is supplied by a generator having the following characteristics: PRR  $\leq$  1 MHz, 50% duty cycle,  $t_r \leq 6$  ns,  $t_f \leq 6$  ns,  $Z_0 = 50 \Omega$ .

Figure 1. Terminal-to-Bus Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



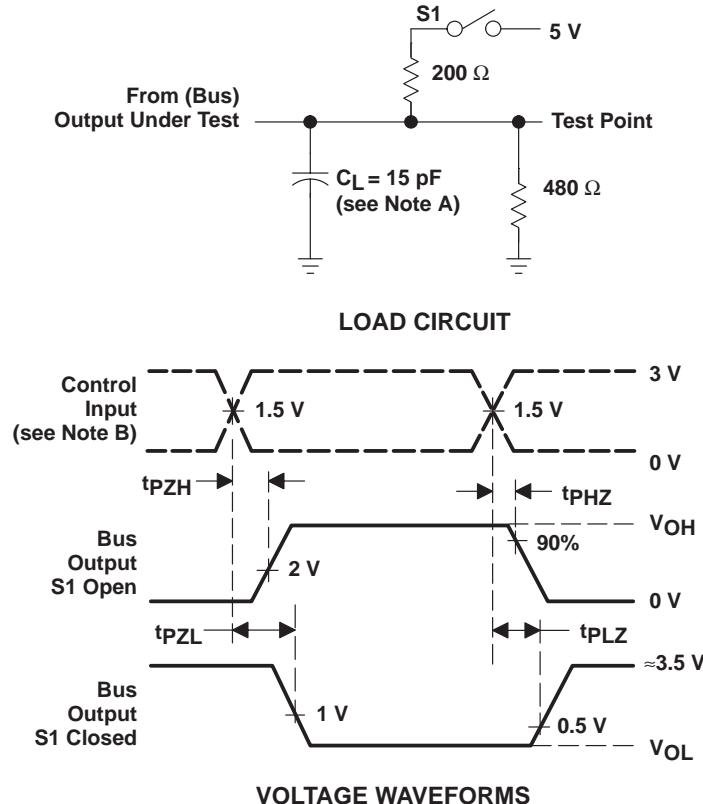
NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. The input pulse is supplied by a generator having the following characteristics: PRR  $\leq$  1 MHz, 50% duty cycle,  $t_r \leq 6$  ns,  $t_f \leq 6$  ns,  $Z_0 = 50 \Omega$ .

Figure 2. Bus-to-Terminal Load Circuit and Voltage Waveforms

# SN75ALS161 OCTAL GENERAL-PURPOSE INTERFACE BUS TRANSCEIVERS

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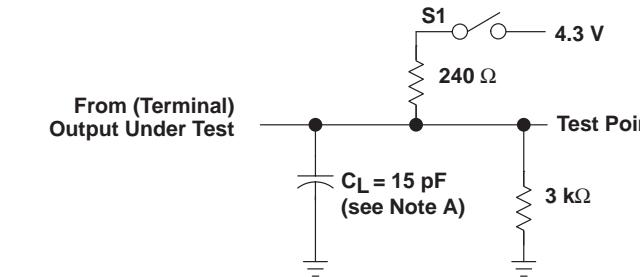
## PARAMETER MEASUREMENT INFORMATION



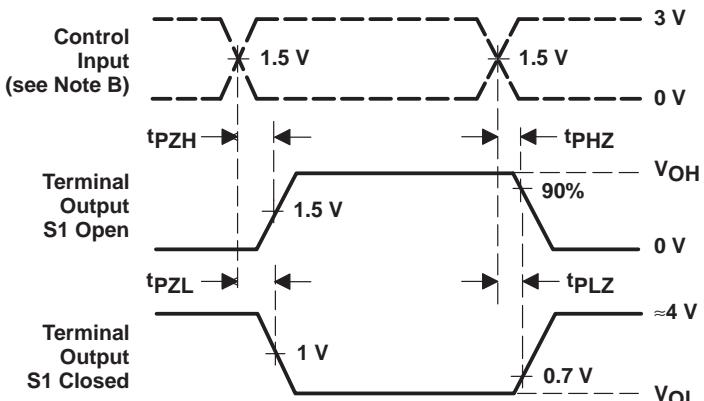
NOTES: A.  $C_L$  includes probe and jig capacitance.  
B. The input pulse is supplied by a generator having the following characteristics: PRR  $\leq 1 \text{ MHz}$ , 50% duty cycle,  $t_r \leq 6 \text{ ns}$ ,  $t_f \leq 6 \text{ ns}$ ,  $Z_O = 50 \Omega$ .

Figure 3. Bus Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A.  $C_L$  includes probe and jig capacitance.

B. The input pulse is supplied by a generator having the following characteristics: PRR  $\leq$  1 MHz, 50% duty cycle,  $t_r \leq 6$  ns,  $t_f \leq 6$  ns,  $Z_0 = 50 \Omega$ .

Figure 4. Terminal Load Circuit and Voltage Waveforms

# SN75ALS161 OCTAL GENERAL-PURPOSE INTERFACE BUS TRANSCEIVERS

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## TYPICAL CHARACTERISTICS<sup>†</sup>

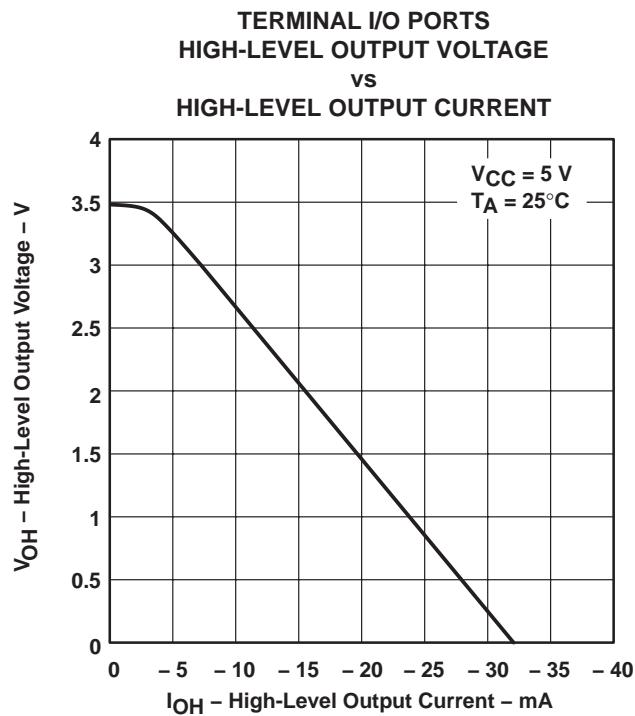


Figure 5

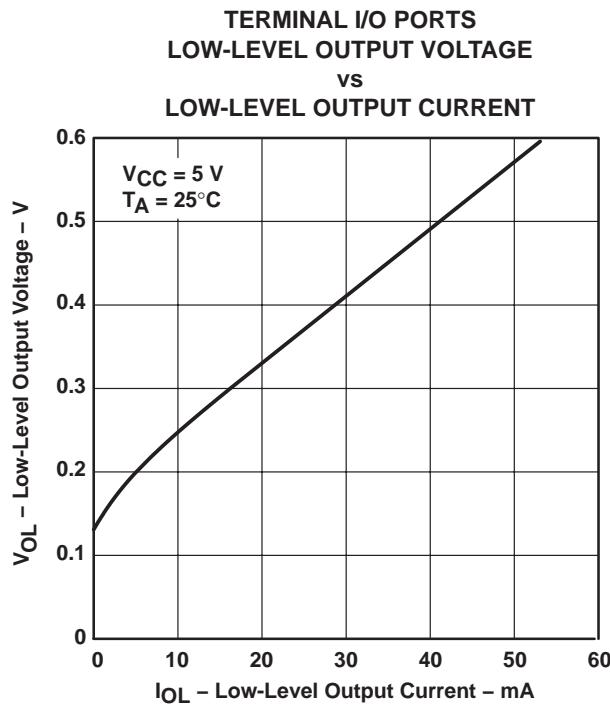


Figure 6

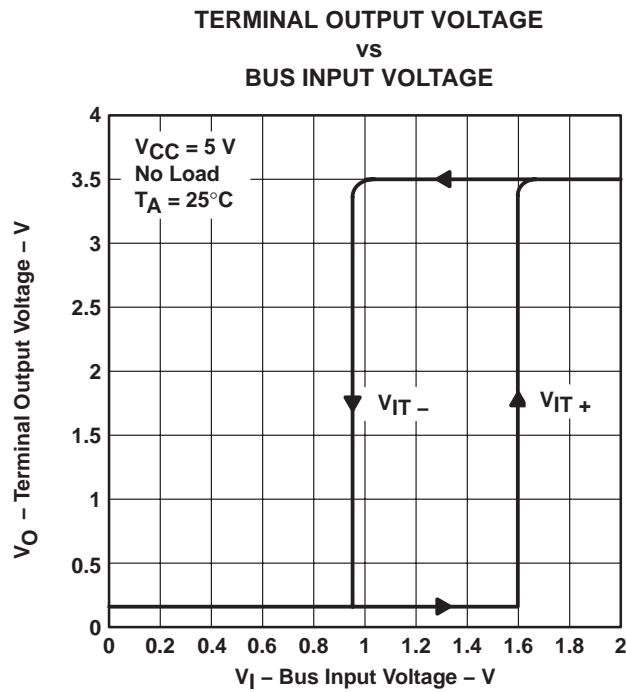


Figure 7

<sup>†</sup> Operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied.

TYPICAL CHARACTERISTICS<sup>†</sup>

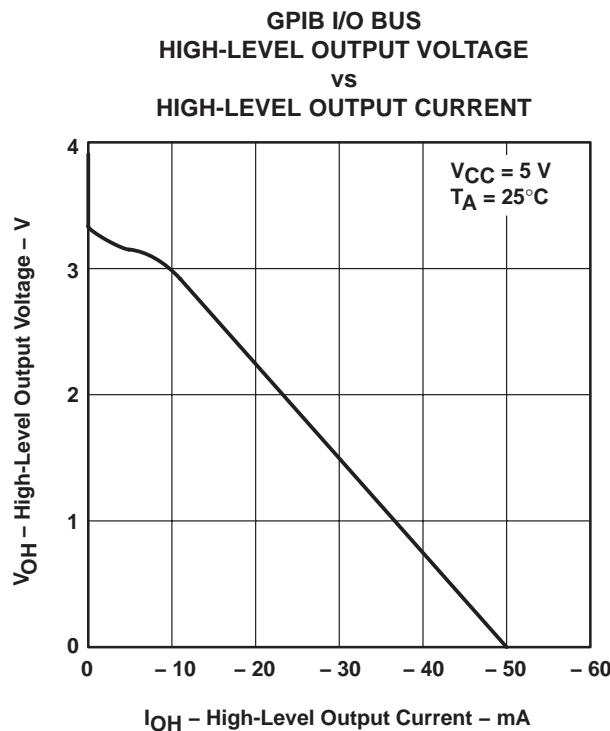


Figure 8

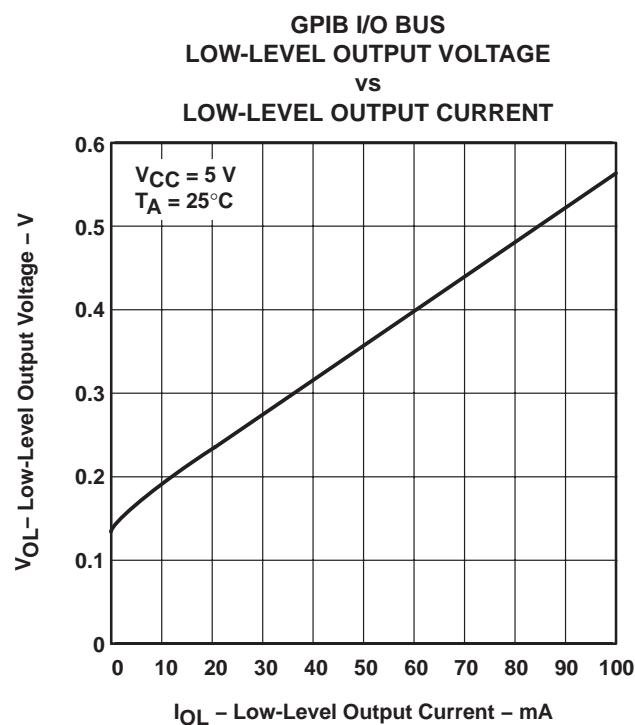


Figure 9

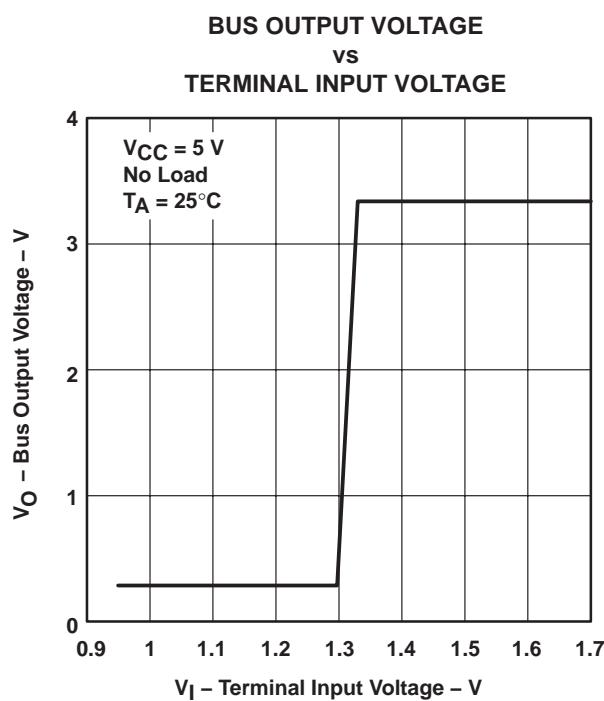


Figure 10

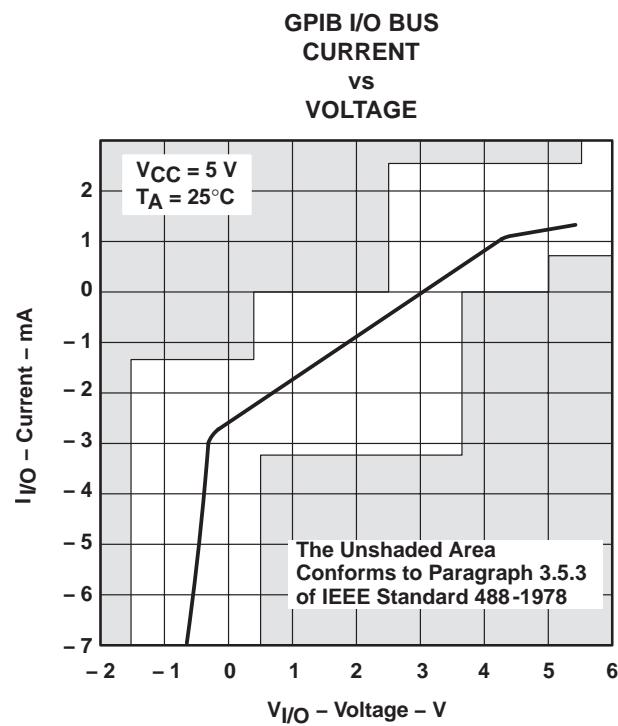


Figure 11

<sup>†</sup> Operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied.

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
SN75ALS161DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75ALS161DWE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75ALS161DWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75ALS161DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75ALS161DWRE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75ALS161DWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75ALS161N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN75ALS161NE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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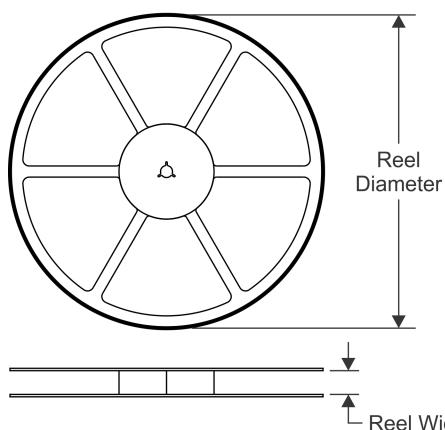
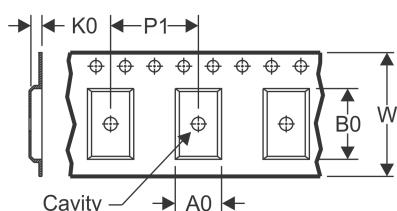
**OTHER QUALIFIED VERSIONS OF SN75ALS161 :**

- Military: [SN55ALS161](#)

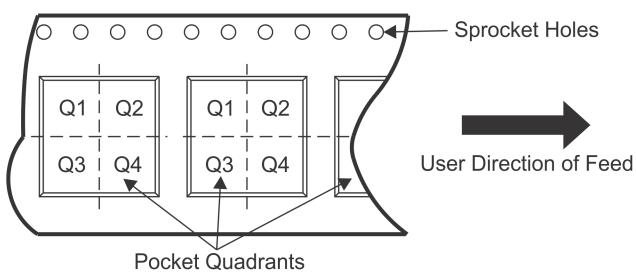
NOTE: Qualified Version Definitions:

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- Military - QML certified for Military and Defense Applications

**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75ALS161DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1

**TAPE AND REEL BOX DIMENSIONS**

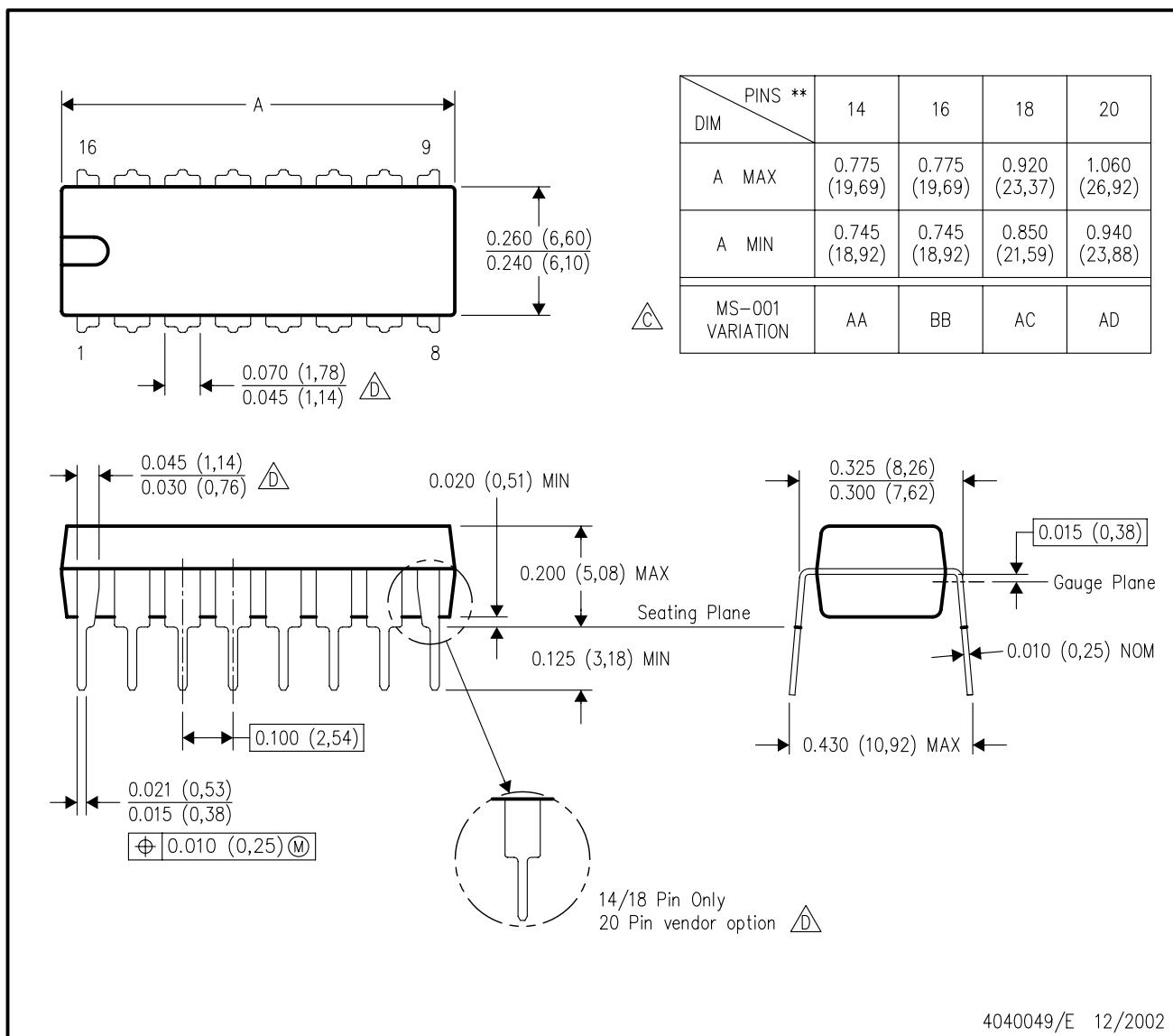
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75ALS161DWR	SOIC	DW	20	2000	367.0	367.0	45.0

## N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



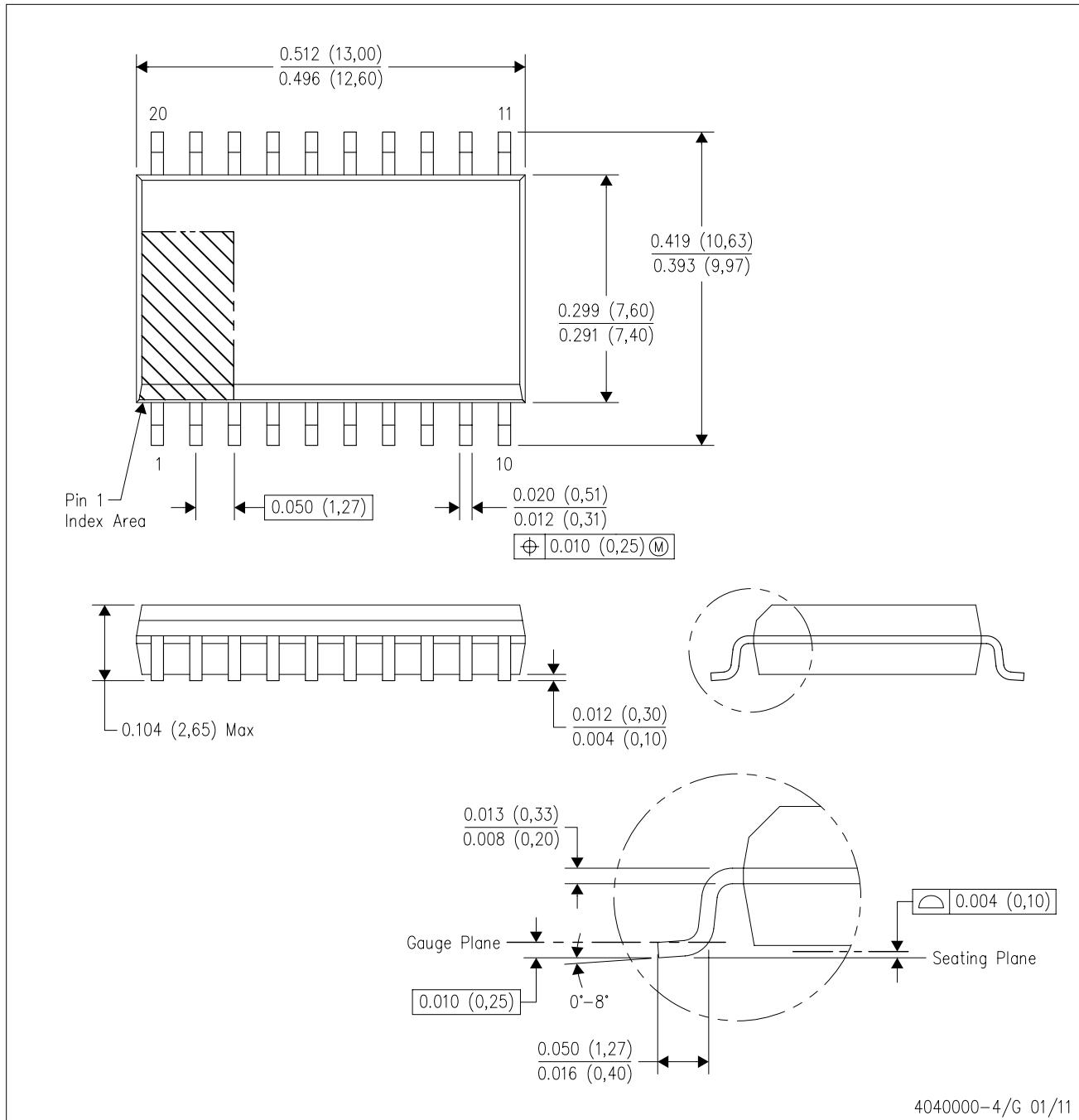
NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.

C. Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).

D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

DW (R-PDSO-G20)

PLASTIC SMALL OUTLINE

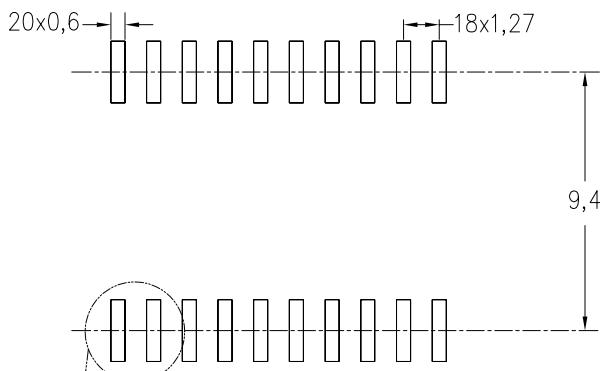
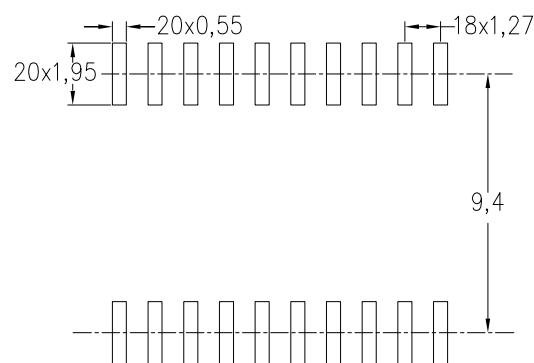


NOTES:

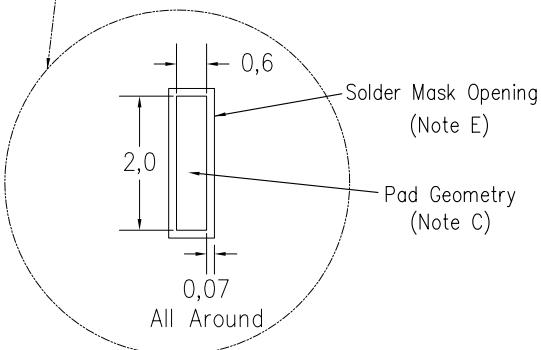
- All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
- This drawing is subject to change without notice.
- Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0.15).
- Falls within JEDEC MS-013 variation AC.

DW (R-PDSO-G20)

PLASTIC SMALL OUTLINE

Example Board Layout  
(Note C)Stencil Openings  
(Note D)

Non Solder Mask Define Pad



4209202-4/E 07/11

NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Refer to IPC7351 for alternate board design.
- Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
- Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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